



## LOW SKEW CLOCK DRIVER/ BUFFER FOR MOBILE PC WITH FOUR SO-DIMMS

**QS5810**

### FEATURES:

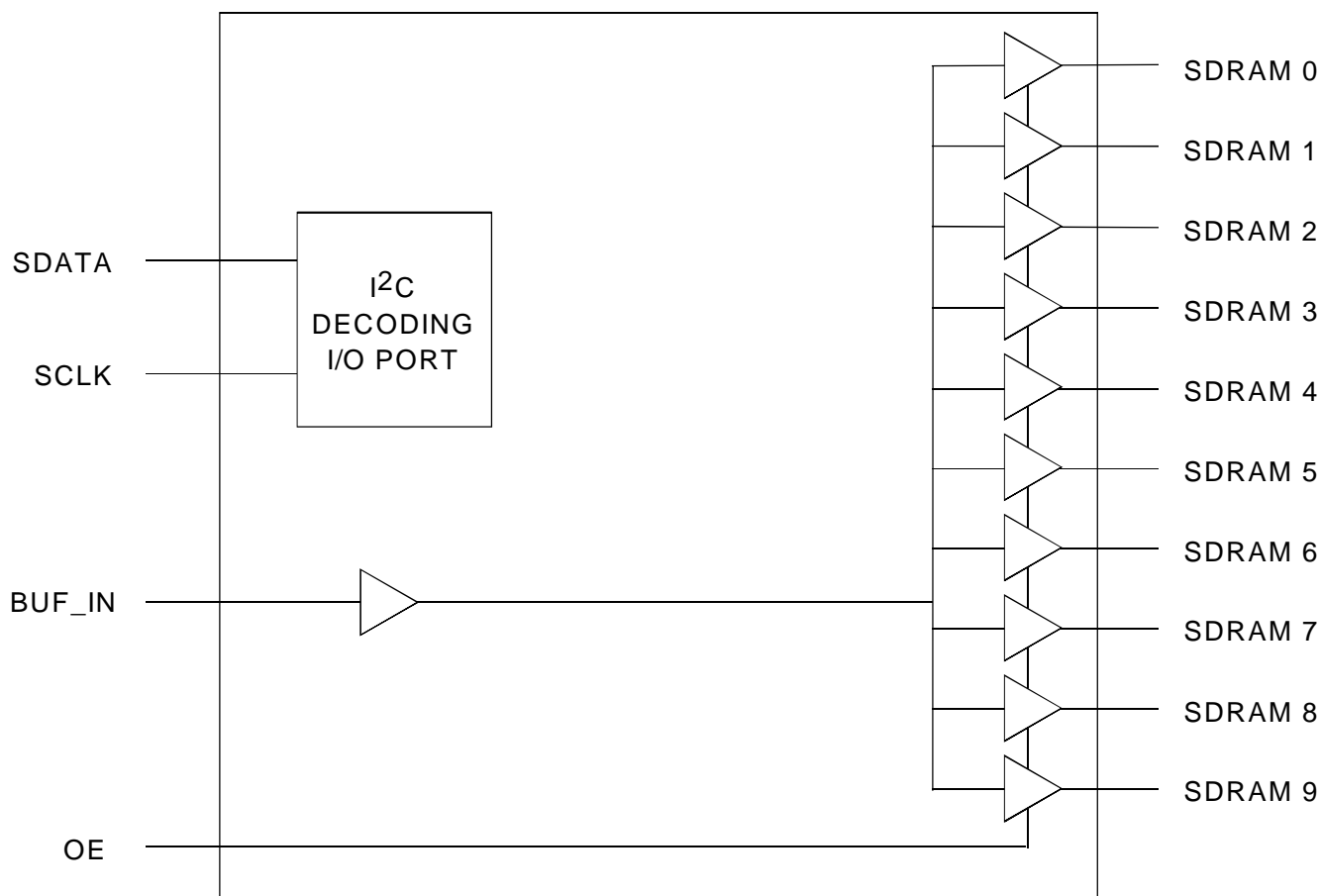
- 1 to 10 output buffer/driver
- Tri-state pin for testing
- I<sup>2</sup>C programming capability
- Power Supply Voltage 3.3V  $\pm$ 5%
- Low Skew Outputs (<200ps)
- Multiple V<sub>DD</sub> and GND for noise reduction
- 28 Pin SSOP package

### DESCRIPTION

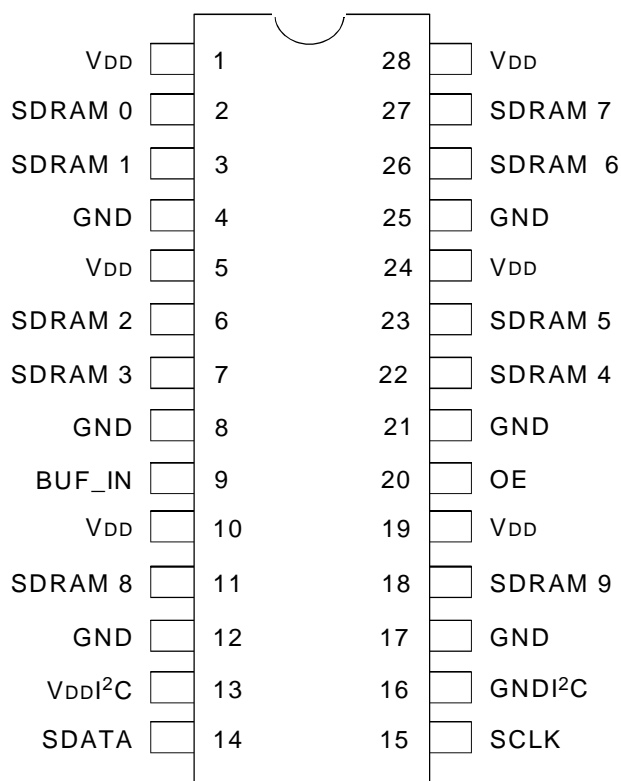
The QS5810 is a high speed, low noise 1-10 non-inverting buffer designed for SDRAM clock buffer applications. Out of the 10 outputs, 8 could be used to drive up to four SDRAM SO-DIMMS, and the remaining can be used for external feedback to a PLL stage for synchronization to master clock.

The QS5810 also includes an I<sup>2</sup>C interface, which can enable or disable each output clock driver. By turning the outputs on and off, I<sup>2</sup>C will aid in reducing the Electro Magnetic Interference (EMI).

### FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION



SSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max.	Unit
	Supply Voltage to Ground	– 0.5 to 4.6V	V
	DC Output Voltage V <sub>OUT</sub>	– 0.5 to + 4.6V	V
	DC Output Voltage V <sub>IN</sub>	– 0.5 to + 4.6	V
	DC Input Diode Current with V <sub>I</sub> < 0	– 20	mA
	Maximum Power Dissipation at T <sub>A</sub> = 85°C	600	mW
	TSTG Storage Temperature	–65 to 150	°C

### NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## PIN DESCRIPTION

Pin Name	Description
SDRAM (0:3)	SDRAM Byte 0 Clock Outputs.
SDRAM (4:7)	SDRAM Byte 1 Clock Outputs.
SDRAM (8:9)	SDRAM Byte 2 Clock Outputs.
BUF_IN	Input for Buffers.
SDATA	I <sup>2</sup> C Data Input. It has 100kΩ internal pull up to VDD.
SCLK	I <sup>2</sup> C Data Input. It has 100kΩ internal pull up to VDD.
OE	Tri-State Output Enable. When asserted LOW, clock outputs are high impedance. It has 100kΩ internal pull up to VDD.
VDD	3.3V power supply for output buffers.
GND	Ground for output buffers.
GNDI <sup>2</sup> C	Ground for I <sup>2</sup> C circuitry.
VDDI <sup>2</sup> C	3.3V Power Supply for I <sup>2</sup> C circuitry.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions	Min.	Typ. <sup>(1)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Voltage Level	For all Inputs	2	—	—	V
$V_{IL}$	Input LOW Voltage Level	For all inputs except I <sup>2</sup> C inputs (SDATA and SCLK)	—	—	0.8	V
		I <sup>2</sup> C Inputs (SDATA and SCLK)	—	—	0.7	
$I_{IH}$	Input High Current	$V_{IN} = V_{DD}$	-5	—	5	$\mu\text{A}$
$I_{IL}$	Input Low Current	$V_{IN} = 0\text{V}$ ; BUF_IN	-5	—	5	$\mu\text{A}$
		$V_{IN} = 0\text{V}$ ; OE, SDATA, SCLK	-100	—	0	
$I_{DD}$	Supply Current	$C_L = 0\text{pF}$ ; $f_{IN}@66.66\text{MHz}^{(1)}$	—	50	70	mA
		$C_L = 0\text{pF}$ ; $f_{IN}@100\text{MHz}^{(1)}$	—	75	105	
		$C_L = 30\text{pF}$ ; $f_{IN}@66.66\text{MHz}^{(1)}$	—	110	130	
		$C_L = 30\text{pF}$ ; $f_{IN}@100\text{MHz}^{(1)}$	—	165	195	
		BUF_IN 0 = GND or $V_{DD}$ , all other inputs to $V_{DD}$	—	—	500	$\mu\text{A}$
$V_{OH}$	Output High Voltage	SDRAM (0:9) $I_{OH} = -36\text{mA}$	2.4	—	—	V
$V_{OL}$	Output Low Voltage	SDRAM (0:9) $I_{OL} = 25\text{mA}$	—	—	0.4	V
$V_{OL}^{I^2C}$	Output Low Voltage	SDATA $I_{OL}^{I^2C} = 3\text{mA}$	—	—	0.4	V

### NOTE:

1. Typical values are at  $V_{CC} = 3.3\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.

## AC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Test Conditions	Min.	Typ. <sup>(1)</sup>	Max.	Unit
$t_R$	Rise Time <sup>(1)</sup>	0.4V to 2.4V; $C_L = 30\text{pF}$	—	—	2.2	ns
$t_F$	Fall Time <sup>(1)</sup>	2.4V to 0.4V; $C_L = 30\text{pF}$	—	—	2.2	ns
$D_t$	Duty Cycle <sup>(1)</sup>	$V_T = 1.5\text{V}$ ; $C_L = 30\text{pF}$ , with 50% Input Clock	45	50	55	%
$T_{SK}$	Skew (output-output) <sup>(1)</sup>	$V_T = 1.5\text{V}$ ; $C_L = 30\text{pF}$ for all outputs	—	—	200	ps
$T_{PHL}$ or $T_{PLH}$	Propagation Delay	$V_T = 1.5\text{V}$	—	—	6	ns
$T_{PZL}$ or $T_{PZH}$	Enable Delay, OE to SDRAM	$V_T = 1.5\text{V}$	—	—	8	ns
$T_{PLZ}$ or $T_{PHZ}$	Disable Delay, OE to SDRAM	$V_T = 1.5\text{V}$	—	—	8	ns

## OPERATING CHARACTERISTICS , $T_A = 25^{\circ}\text{C}$

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{DD}$	Power Supply Voltage	3.135	3.3	3.465	V
$T_A$	Operating Temperature	-40	25	85	$^{\circ}\text{C}$
$C_L$	Load Capacitance	—	—	30	pF
$C_{IN}$	Input Capacitance	—	—	15	pF

## I<sup>2</sup>C SERIAL INTERFACE CONTROL

The I<sup>2</sup>C interface permits individual enable/disable of each clock output: any unused outputs may be disabled to reduce the EMI. The QS5810 is a slave receiver device. It can read back the data stored in the latches for verification.

The data transfer rate supported by the I<sup>2</sup>C interface is 100k bits/sec. Data is transferred in bytes (with the addition of start, stop, acknowledge bits) in sequential order from the lowest to highest byte with the ability to stop after any complete byte has been transferred. The first two bytes transferred must be a Command Code followed by a Byte Count. Both of these bytes are ignored by the device.

The I<sup>2</sup>C address of the QS5810 is:

A7	A6	A5	A4	A3	A2	A1
1	1	0	1	0	0	1

Address A0 is the read/write bit and is set to 0 for writes and 1 for reads. During read back, the first byte read is a Byte Count representing the number of bytes following (fixed at 3).

## SERIAL CONFIGURATION COMMAND BITMAPS

Byte 0: SDRAM Active/Inactive Register  
 (1 = Enable, 0 = Disable), Default = Enable

Bit	Pin #	Description
Bit 7	—	Initialize to 0
Bit 6	—	Initialize to 0
Bit 5	—	Initialize to 0
Bit 4	—	Initialize to 0
Bit 3	7	SDRAM 3 (Active/Inactive)
Bit 2	6	SDRAM 2 (Active/Inactive)
Bit 1	3	SDRAM 1 (Active/Inactive)
Bit 0	2	SDRAM 0 (Active/Inactive)

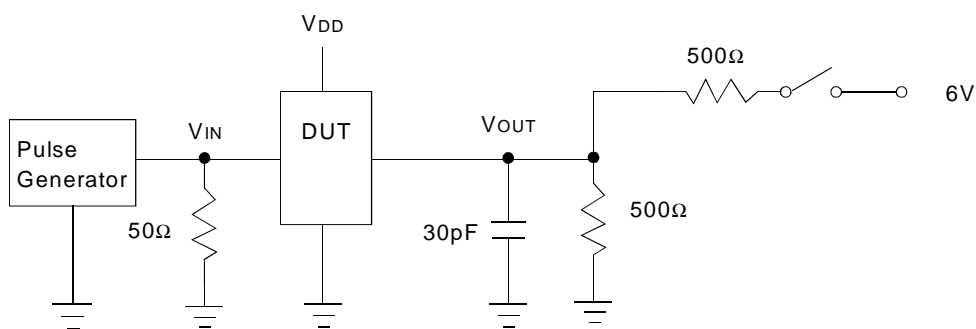
Byte 1: SDRAM Active/Inactive Register  
 (1 = Enable, 0 = Disable), Default = Enable

Bit	Pin #	Description
Bit 7	27	SDRAM 7 (Active/Inactive)
Bit 6	26	SDRAM 6 (Active/Inactive)
Bit 5	23	SDRAM 5 (Active/Inactive)
Bit 4	22	SDRAM 4 (Active/Inactive)
Bit 3	—	Initialize to 0
Bit 2	—	Initialize to 0
Bit 1	—	Initialize to 0
Bit 0	—	Initialize to 0

Byte 2: SDRAM Active/Inactive Register  
 (1 = Enable, 0 = Disable), Default = Enable

Bit	Pin #	Description
Bit 7	18	SDRAM 9 (Active/Inactive)
Bit 6	11	SDRAM 8 (Active/Inactive)
Bit 5	—	Reserved, 1 at power up, set to 0
Bit 4	—	Reserved, 1 at power up, set to 0
Bit 3	—	Reserved, 1 at power up, set to 0
Bit 2	—	Reserved, 1 at power up, set to 0
Bit 1	—	Reserved, 1 at power up, set to 0
Bit 0	—	Reserved, 1 at power up, set to 0

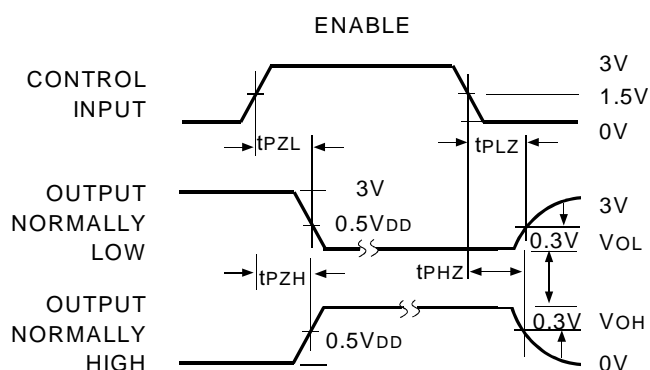
## TEST CIRCUIT



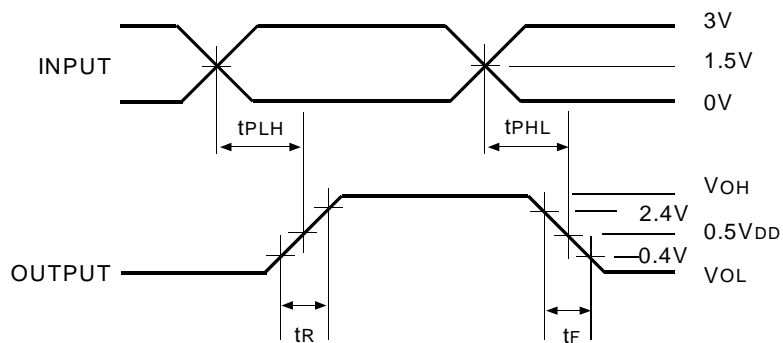
Parameter Tested	Switch Position
tPLZ, tPZL	Closed
All Others	Open

## AC TEST CIRCUIT

### ENABLE AND DISABLE TIMES

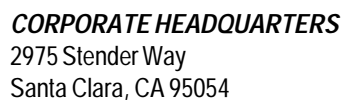


### PROPAGATION DELAY



```

graph LR
    QS[QS] --> Device_Type[Device Type]
    QS --> Package[Package]
    Device_Type --> 5810[5810]
    Device_Type --> PV[PV]
    Package --> PV
    5810 --- 5810_Label[Low Skew Clock Driver]
    PV --- PV_Label[Shrink Small Outline Package (SO28-7)]
  
```



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