

# LOW SKEW CMOS PLL CLOCK DRIVER WITH INTEGRATED LOOP FILTER

QS5917T

### **FEATURES**

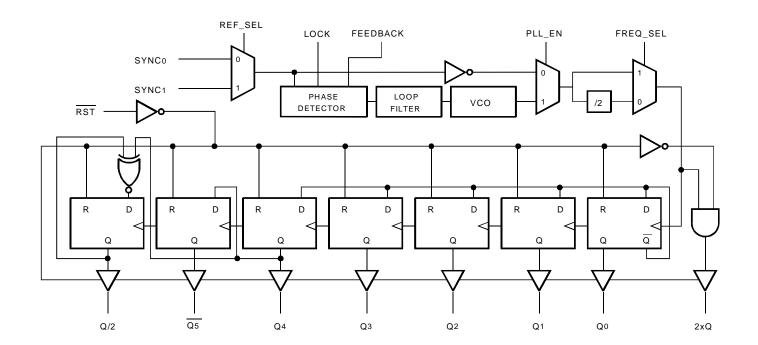
- 5V operation
- 2xQ output, Q/2 output, Q output
- Outputs tri-state while  $\overline{\mathsf{RST}}$  low
- Internal loop filter RC network
- Low noise TTL level outputs
- < 500ps output skew, Q0-Q4</li>
- PLL disable feature for low frequency testing
- Balanced Drive Outputs ± 24mA
- 132MHz maximum frequency (2xQ output)
- Functional equivalent to Motorola MC88915
- ESD > 2000V
- Latch-up > -300mA
- Available in QSOP and PLCC packages

### **DESCRIPTION**

The QS5917T Clock Driver uses an internal phase locked loop (PLL) to lock low skew outputs to one of two reference clock inputs. Eight outputs are available: Qo-Q4, 2xQ, Q/2, Q5. Careful layout and design insures < 500ps skew between the Qo-Q4, and Q/2 outputs. The QS5917T includes an internal RC filter which provides excellent jitter characteristics and eliminates the need for external components. In addition, TTL level outputs reduce clock signal noise. Various combinations of feedback and a divide-by-2 in the VCO path allow applications to be customized for linear VCO operation over a wide range of input SYNC frequencies. The VCO can also be disabled by the PLL\_EN signal to allow low frequency or DC testing. The LOCK output asserts to indicate when phase lock has been achieved. The QS5917T is designed for use in high-performance workstations, multi-board computers, networking hardware, and mainframe systems. Several can be used in parallel or scattered throughout a system for guaranteed low skew, system-wide clock distribution networks.

For more information on PLL clock driver products, see Application Note AN-227.

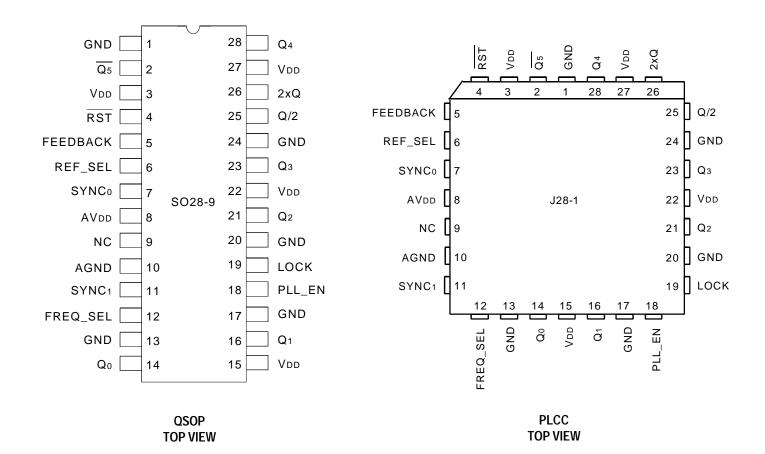
### **FUNCTIONAL BLOCK DIAGRAM**



INDUSTRIAL TEMPERATURE RANGE

**JULY 2000** 

## **PIN CONFIGURATION**



### ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Rating	Max.	Unit
	Supply Voltage to Ground	-0.5 to +7	٧
	DC Input Voltage VIN	-0.5 to +7	V
	AC Input Voltage (pulse width ≤20ns)	-3	V
	Maximum Power Dissipation (TA = 85°C)	1.2	W
Tstg	Storage Temperature Range	-65 to +150	°C

### NOTE:

 Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## **CAPACITANCE** ( $T_A = 25^{\circ} C$ , f = 1MHz, $V_{IN} = 0V$ )

	QSOP		PL		
Parameter	Тур.	Max.	Тур.	Max.	Unit
CIN	3	4	4	6	pF
Соит	7	9	8	10	pF

## **PIN DESCRIPTION**

Pin Name	I/O	Description
SYNC <sub>0</sub>	I	Reference clock input
SYNC1	I	Reference clock input
REF_SEL	I	Reference clock select. When 1, selects SYNC1. When 0, selects SYNC0.
FREQ_SEL	I	VCO frequency select. For choosing optimal VCO operating frequency depending on input frequency.
FEEDBACK	I	PLL feedback input which is connected to a user selected output pin. External feedback provides flexibility for different output frequency relationships. See the Frequency Selection Table for more information.
Q0 -Q4	0	Clock outputs
Q5	0	Clock output. Matched in frequency, but inverted with respect to Q.
2xQ	0	Clock output. Matched in phase, but frequency is double the Q frequency.
Q/2	0	Clock output. Matched in phase, but frequency is half the Q frequency.
LOCK	0	PLL lock indication signal. 1 indicates positive lock. 0 indicates that the PLL is not locked and outputs may not be synchronized to the inputs.
RST	I	Asynchronous reset. Resets all output registers. When 0, all outputs are held in a tri-stated condition. When 1, outputs are enabled (normal operation).
PLL_EN	I	PLL enable. When 1, PLL is enabled (normal operation). When 0, PLL is disabled (for testing purposes).
NC	_	No Connection

## **OUTPUT FREQUENCY SPECIFICATIONS**

Industrial:  $TA = -40^{\circ}C$  to  $+85^{\circ}C$ ,  $AVDD/VDD = 5.0V \pm 5\%$ 

Symbol	Description	- 70	- 100	- 132	Units
F <sub>2</sub> XQ	Max Frequency, 2xQ output	70	100	132	MHz
Fo	Max Frequency, Qo - Q4, $\overline{\text{Q5}}$ outputs	35	50	66	MHz
FQ/2	Max Frequency, Q/2 output	17.5	25	33	MHz

## FREQUENCY SELECTION TABLE

	Output Used for	SYNC (MHz) (allowable range)			Output Frequen	cy Relationships	
FREQ_SEL	Feedback	Min.	Max	Q/2	Q <sub>5</sub>	Q Outputs	2XQ
1	Q/2	14	F2XQ / 4	SYNC	- SYNC X 2	SYNC X 2	SYNC X 4
1	Q0 -Q4	28	F2XQ / 2	SYNC / 2	- SYNC	SYNC	SYNC X 2
1	Q5	28	F2XQ / 2	- SYNC / 2	SYNC	- SYNC	- SYNC X 2
1	2xQ	56	F2XQ <sup>(1)</sup>	SYNC / 4	- SYNC / 2	SYNC/2	SYNC
0	Q/2	7	F2XQ / 8	SYNC	- SYNC X 2	SYNC X 2	SYNC X 4
0	Q0 -Q4	14	F2XQ / 4	SYNC / 2	- SYNC	SYNC	SYNC X 2
0	<u>Q</u> 5	14	F2XQ / 4	- SYNC / 2	SYNC	- SYNC	- SYNC X 2
0	2xQ	28	F2XQ / 2	SYNC / 4	- SYNC / 2	SYNC/2	SYNC

#### NOTF:

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: TA =  $-40^{\circ}$ C to  $+85^{\circ}$ C, AVDD/VDD = 5.0V  $\pm 5\%$ 

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
VIH	Input HIGH Voltage	Guaranteed Logic HIGH Level	2	_	_	V
VIL	Input LOW Voltage	Guaranteed Logic LOW Level	_	_	0.8	V
Vон	Output HIGH Voltage	V <sub>DD</sub> = Min., I <sub>OH</sub> = -24mA <sup>(1)</sup>	2.4	_	_	V
		$V_{DD} = Min., IOH = -100\mu A$	3	_	_	V
Vol	Output LOW Voltage	V <sub>DD</sub> = Min., I <sub>OL</sub> = 24mA <sup>(1)</sup>	_	_	0.55	V
		V <sub>DD</sub> = Min., I <sub>OL</sub> = 100μA	_	_	0.2	V
loz	Output Leakage Current	Vout = Vdd or GND, Vdd = Max.	_	_	±5	μΑ
lin	Input Leakage Current	VIN = AVDD or GND, AVDD = Max.	_	_	±5	μΑ

#### NOTE:

### **POWER SUPPLY CHARACTERISTICS**

Symbol	Parameter	Test Conditions (1)	Тур.	Max.	Unit
$\Delta Icc$	Input Power Supply Current per TTL Input HIGH (2)	VDD = Max., VIN = 3.4V	0.4	1.5	mA
ICCD	Dynamic Power Supply Current	VDD = Max	_	0.4	mA/MHz

#### NOTES:

- 1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
- 2. This specification does not apply to the PLL\_EN input.

<sup>1.</sup> For the -132 speed grade, maximum input frequency is restricted to 100MHz.

<sup>1.</sup> IoL and IoH are 12mA and -12mA, respectively, for the LOCK output.

## **INPUT TIMING REQUIREMENTS**

Symbol	Description	Min.	Max.	Unit
tr, tr	Maximum input rise and fall times, 0.8V to 2V	_	3	ns
Fı	Input Clock Frequency, SYNCo, SYNC1 (1)	14	F2XQ	MHz
tpwc	Input clock pulse, HIGH or LOW	2	_	ns
Dн	Duty cycle, SYNCo, SYNC1	25	75	%

#### NOTE:

## **SWITCHING CHARACTERISTICS OVER OPERATING RANGE**

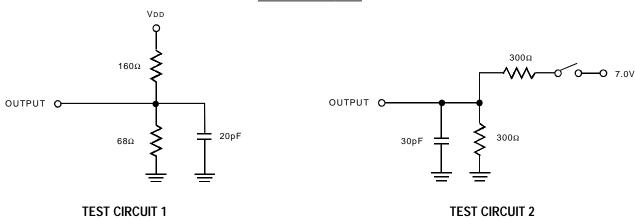
Symbol	Parameter	Min.	Max.	Unit
tskr	Output Skew Between Rising Edges, Qo-Q4 and Q/2 (1)	_	350	ps
tskf	Output Skew Between Falling Edges, Qo-Q4 (1)	_	350	ps
tskall	Output Skew, All Outputs (1)	_	500	ps
tpw	Pulse Width, $\overline{Q_5}$ , 2xQ outputs	Tcy/2 - 0.65	Tcy/2 + 0.65	ns
tpw	Pulse Width, Q <sub>0</sub> -Q <sub>4</sub> , Q/2 outputs (1)	Tcy/2 - 0.5	Tcy/2 + 0.5	ns
tu	Cycle-to-Cycle Jitter, 33MHz (3)	_	0.25	ns
tpD	SYNC Input to Feedback Delay, 28MHz	- 100	400	ps
tpD	SYNC Input to Feedback Delay, 33MHz, $50\Omega$ to $1.5V$	- 100	400	ps
tLOCK	SYNC to Phase Lock	_	10	ms
tpzh tpzl	Output Enable Time, RST LOW to HIGH (2)	0	7	ns
tPHZ tPLZ	Output Disable Time, RST HIGH to LOW (2)	0	6	ns
tr, tr	Output Rise/Fall Times, 0.8V to 2V	0.4	1.5	ns

#### NOTES:

- 1. Skew specifications apply under identical environments (loading, temperature, VDD, device speed grade).
- 2. Measured in open loop mode PLL\_EN = 0.
- 3. Jitter is characterized using an oscilloscope. Measurement is taken one cycle after jitter. Jitter is characterized but not tested. See FREQUENCY SELECTION TABLE for information on proper FREQ\_SEL level for specified input frequencies.

<sup>1.</sup> The FI specification is based on Q output feedback. See the Frequency Selection Table for more detail on allowable SYNC input frequencies for different feedback combinations.

### **TEST LOAD**



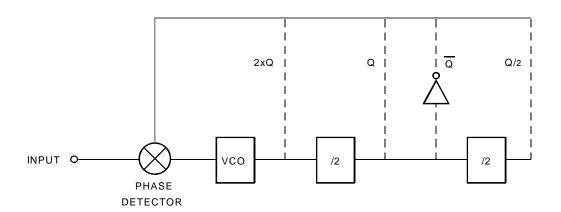
TEST CIRCUIT 2 is used for output enable/disable parameters. TEST CIRCUIT 1 is used for all other timing parameters.

### **PLL OPERATION**

The Phase Locked Loop (PLL) circuit included in the QS5917T provides for replication of incoming SYNC clock signals. Any manipulation of that signal, such as frequency multiplying or inversion is performed by digital logic following the PLL (see the block diagram). The key advantage of the

PLL circuit is to provide an effective zero propagation delay between the output and input signals. In fact, adding delay circuits in the feedback path, 'propagation delay' can even be negative! A simplified schematic of the QS5917T PLL circuit is shown below.

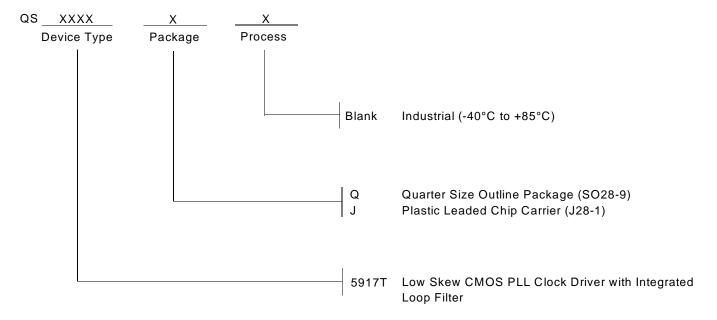
### SIMPLIFIED DIAGRAM OF QS5917T FEEDBACK



The phase difference between the output and the input frequencies feeds the VCO which drives the outputs. Whichever output is fed back, it will stabilize at the same frequency as the input. Hence, this is a true negative feedback closed loop system. In most applications, the output will optimally have zero phase shift with respect to the input. In fact, the internal loop filter on the QS5917T typically provides within 150ps of phase shift between input and output.

If the user wishes to vary the phase difference (typically to compensate for backplane delays), this is most easily accomplished by adding delay circuits to the feedback path. The respective output used for feedback will be advanced by the amount of delay in the feedback path. All other outputs will retain their proper relationships to that output.

### ORDERING INFORMATION





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