CMOS 8-Bit microcomputer

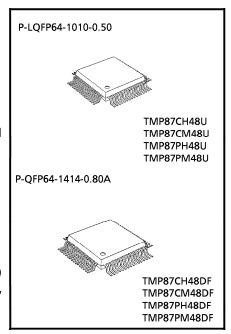
# TMP87CH48U/DF, TMP87CM48U/DF

TMP87CH48/CM48 are a low power, high-speed and high-performance 8-bit single chip microcomputer, including large capacity ROM/RAM, input/output ports, a multiple timer counter, serial interfaces (UART, I<sup>2</sup>C bus, and SIO), four 12-bit PWM outputs, a 10-bit AD converter and two oscillators.

Product No.	ROM	RAM	Package	ОТР
TMP87CH48U	16 Kbytes	E12 human	P-LQFP64-1010-0.50	TMP87PH48U
TMP87CH48DF	10 Kbytes	512 bytes	P-QFP64-1414-0.80A	TMP87PH48DF
TMP87PM48U	32 Kbytes	4 1/2 10 10 10 10	P-LQFP64-1010-0.50	TMP87PM48U
TMP87PM48DF	32 Kbytes	1 Kbytes	P-QFP64-1414-0.80A	TMP87PM48DF

#### **Features**

- 8-bit single chip microcomputer TLCS-870 series
- Minimum instruction execution time: 0.5 μs (at 8 MHz), 122 μs (at 32.768 kHz)
- 412 basic machine instructions: 129 types
- 15 interrupt sources (External: 6, Internal: 9)
  - All sources have independent latches each, and nested interrupt control is available.
  - Edge-selectable external interrupts with noise reject.
  - High-speed task switching by register bank changeover
- ◆ Input/output ports (56 pins)
  - High current output: 8 pins (Typ.20 mA), LED direct drive
- 16-bit timer counters: 2 channels
  - Timer, Event counter, PPG (Programmable Pulse Generator) output, Pulse width measurement, External trigger timer, Window modes



030619FBP2

- The information contained herein is subject to change without notice. The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA for any infringements of patents or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of TOSHIBA or others.
- or patent rights of TOSHIBA or others.

  TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.

  In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the "Handling Guide for Semiconductor Devices," or "TOSHIBA Semiconductor Reliability Handbook" etc..

  The TOSHIBA products listed in this document are intended for usage in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.). These TOSHIBA products are neither intended nor warranted for usage in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury ("Unintended Usage"). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, airplane or spaceship instruments, transportation instr
- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance / Handling Precautions.

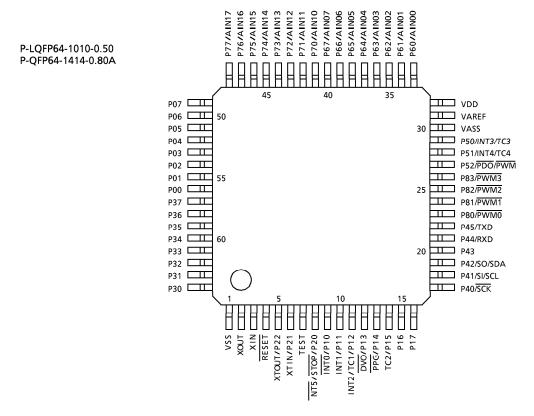


Purchase of TOSHIBA I<sup>2</sup>C components conveys a license under the Philips I<sup>2</sup>C Patent Rights to use these components in an I<sup>2</sup>C system, provided that the system conforms to the I<sup>2</sup>C Standard Specification as defined by Philips.

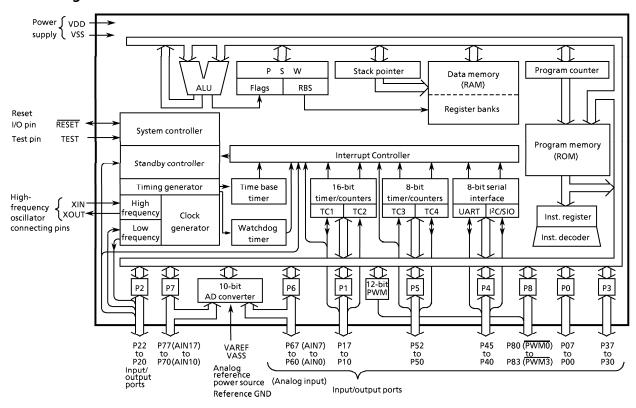
> 87CH48-1 2003-07-09

- ◆ 8-bit timer counters: 2 channels
  - Timer, Event counter, Capture (Pulse width/duty measurement)
     PWM (Changeable pulse width)
     output, PDO (ProgrammableDivider Output)
- ◆ Time base timer (Interrupt frequency: 1 to 16384 Hz)
- ◆ Divider output functions (Frequency: 1 to 8 kHz)
- Watchdog timer
  - Interrupt/reset output (programmable)
- ◆ DA conversion (Changeable pulse width) output
  - 12-bit resolution: 4 channels
- ◆ UART: 1 channel (Parity/framing/overrun error detection)
- ◆ Serial bus interface (SBI-ver. B) 1 channel (I<sup>2</sup>C bus or clock synchronous SIO)
- ◆ 10-bit successive approximation type AD converter
  - Analog input: 16 channels
  - Conversion time: 24.5  $\mu$ s or 98  $\mu$ s (at 8 MHz)
- ◆ Clock oscillation circuit: Two circuits
  - Single/dual clock modes (Initial mode is always set to a single clock mode.)
- ◆ Low consumption power (Five modes)
  - STOP mode: Oscillation stop (Battery/capacitor back-up). Port output hold/high-impedance.
  - SLOW mode: Low consumption power operation by low-frequency clock
  - IDEL1 mode: CPU stops, and only peripheral hardware operates using high-frequency clock. Release by interrupts (CPU restarts).
  - IDEL2 mode: CPU stops, and only peripheral hardware operates using high or low-frequency clock). Release by interrupts.
  - SLEEP mode: CPU stops, and only peripheral hardware operates using low-frequency clock. Release by interrupts.
- ◆ Operation voltage: 2.7 to 5.5 V at 4.2 MHz/32.768 kHz, 4.5 to 5.5 V at 8 MHz/32.768 kHz
- ◆ Emulation pod: BM87CH48/CM48U0A

#### Pin Assignments (Top View)



# **Block Diagram**



# **Pin Function**

Pin Name	Input/Output	Fun	ctions		
P07 to P00	I/O				
P17, P16	I/O	8-bit programmable input/output port (tri-state).			
P15 (TC2)	I/O (Input)	Each bit of these ports can be individually configured as an input or	Timer counter 2 input		
P14 (PPG)	I/O (Output)	an output under software control.	Programmable pulse generator output		
P13 (DVO)		When used as an external interrupt input or a timer counter input, the latch	Divider output		
P12 (INT2/TC1)		must be set to input mode. When used as PPG output or a divider output, the	External interrupt input 2 or Timer counter 1 input		
P11 (INT1)	I/O (Input)	output latch must be set to "1".	External interrupt input 1		
P10 (ĪNTŌ)			External interrupt input 0		
P22 (XTOUT)	I/O (Output)	3-bit input/output port. When used as an input port, an	Low-frequency oscillator connecting pins (32.768 kHz). For inputting external clock,		
P21 (XTIN) P20 (ĪNT5/STOP)	I/O (Input)	oscillator connecting pin, an external interrupt input or STOP mode release input of P20, the output latch must be set to "1".	XTIN is used and XTOUT is opened. External interrupt input 5 or STOP mode release signal input		
P37 to P30	I/O	8-bit input/output port (high current or output latch must be set to "1".	utput). When used as an input port, the		
P45 (TxD)	I/O (Output)		UART serial data output (send)		
P44 (RxD)	I/O (Input)	8-bit input/output port.	UART serial data output (receive)		
P43	1/0	When used as an input port, a serial			
P42 (SO/SDA)	I/O (Output, I/O)	interface pin, the output latch must be set to "1".	SIO serial data output or I <sup>2</sup> C bus data input/output		
P41 (SI/SCL)	I/O (Input, I/O)	sector:	SIO serial data output or I <sup>2</sup> C bus clock input/output		
P40 (SCK)	I/O (I/O)		SIO serial clock input/output		
P52 (PWM/PDO)	I/O (Output)	3-bit input/output port. When used as an input port, PWM output, high-speed PWM output, a	8-bit PWM output or 8-bit programmable divider output		
P51 (INT4/TC4)	I/O (Input)	programmable divider output, an external interrupt input or timer	External interrupt input 4 or Timer counter 4 input		
P50 (INT3/TC3)	i/O (iriput)	counter input, the output latch must be set to "1".	External interrupt input 3 or Timer counter 3 input		
P67 (AIN7) to P60 (AIN0) P77 (AIN17) to P70 (AIN10)	1/0	8-bit programmable input/output port (tri-state). Each bit of these ports can be individually configured as an input or an output under software control. When used as an analog input, the latch must be set to an analog input mode by P6CR and P7CR.)	AD converter analog input		
P83 (PWM3) to P80 (PWM0)	I/O (Output)	4-bit programmable input/output port (tri-state). Each bit of the port can be individually configured as an input or an output under software control. An input or an output is determined by setting P8CR.	DA conversion (PWM) output (PWM3 to PWM0)		
XIN, XOUT	Input, Output	Oscillator connecting pins for high freque For inputting external clock, XIN is used a			
RESET	I/O	Reset signal input or watchdog timer of clock-reset output.	output/address-trap-reset output/system-		
TEST	Input	Test pin for outgoing test. Be externally t	ied to low.		
VDD, VSS	Power Supply	+ 5 V, 0 V (GND)			
VAREF, VASS	Power Supply	AD conversion analog reference voltage,	Reference GND.		

### **Operational Description**

#### 1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, an interrupt controller, and a watchdog timer. This section provides a description of the CPU core, the program memory (ROM), the data memory (RAM), and the reset circuit.

### 1.1 Memory Address Map

The TLCS-870 Series is capable of addressing 64 Kbytes of memory. Figure 1-1 shows the memory address maps of the TMP87CH48/CM48. In the TLCS-870 Series, the memory is organized 4 address spaces (ROM, RAM, SFR, and DBR). It uses a memory mapped I/O system, and all I/O registers are mapped in the SFR/DBR address spaces. There are 16 banks of general-purpose registers. The register banks are also assigned to the first 128 bytes of the RAM address space.

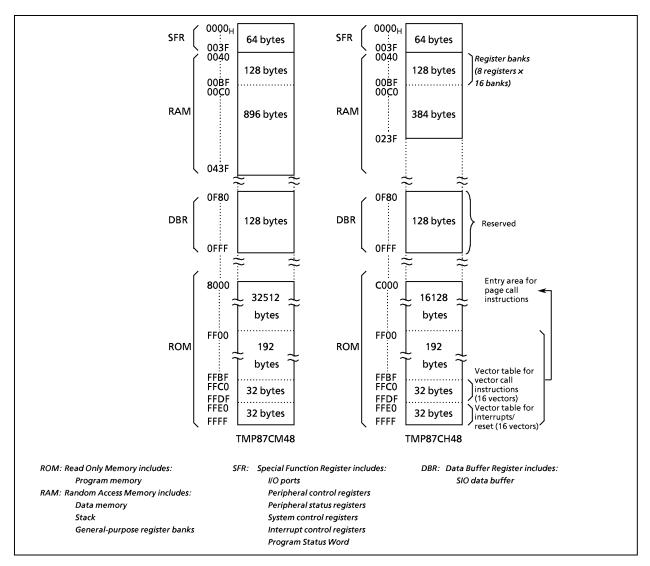


Figure 1-1. Memory Address Maps

2003-07-09

## **Electrical Characteristics**

#### (1) TMP87CH48

Absolute Maximum Ratings

 $(V_{SS} = 0 V)$ 

Parameter	Symbol	Conditions	Ratings	Unit	
Supply voltage	$V_{DD}$		- 0.3 to 6.5	٧	
Input voltage	V <sub>IN</sub>		- 0.3 to V <sub>DD</sub> + 0.3	V	
Output voltage	V <sub>OUT</sub>		- 0.3 to V <sub>DD</sub> + 0.3	V	
Output support (Bandaria)	I <sub>OUT1</sub>	Ports P0, P1, P2, P4, P5, P6, P7, P8	3.2		
Output current (Per 1 pin)	I <sub>OUT2</sub>	Port P3	30	mA	
O to the world (Table I)	Σ I <sub>OUT1</sub>	Ports P0, P1, P2, P4, P5, P6, P7, P8	120	mA	
Output current (Total)	Σ I <sub>OUT2</sub>	Port P3	120		
Power dissipation	PD		350	mW	
Soldering temperature (Time)	Tsld		260 (10 s)	°C	
Storage temperature	Tstg		– 55 to 125	°C	
Operating temperature	Topr		- 40 to 85	°C	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

**Recommended Operating Conditions** 

 $(V_{SS} = 0 \text{ V}, \text{ Topr} = -40 \text{ to } 85^{\circ}\text{C})$ 

Parameter	Symbol	Pins		Conditions	Min	Max	Unit
			fc = 8	NORMAL1/2 modes	4.5		
			MHz	IDLE1/2 modes			
Supply voltage			4.2 MHz	NORMAL1/2 modes			
	$V_{DD}$			IDLE1/2 modes	2.7	5.5	V
				SLOW mode			
				SLEEP mode			
				STOP mode	2.0		
	V <sub>IH1</sub>	Except hysteresis input	$V_{DD} \ge 4.5 \text{ V}$ $V_{DD} < 4.5 \text{ V}$		$V_{DD} \times 0.70$		
Input high voltage	V <sub>IH2</sub>	Hysteresis input			V <sub>DD</sub> × 0.75	$V_{DD}$	٧
	V <sub>IH3</sub>				V <sub>DD</sub> × 0.90		
	V <sub>IL1</sub>	Except hysteresis input				$V_{DD} \times 0.30$	
Input low voltage	V <sub>IL2</sub>	Hysteresis input	] '	7 <sub>DD</sub> ≥ 4.5 V	0	$V_{DD} \times 0.25$	v
	V <sub>IL3</sub>		\	/ <sub>DD</sub> < 4.5 V		V <sub>DD</sub> × 0.10	
		VIN VOUT	V <sub>DD</sub> = 4.5 to 5.5 V		0.4	8.0	MHz
Clock frequency	fc	XIN, XOUT	V <sub>DD</sub> = 2.7 to 5.5 V		0.4	4.2	IVITZ
	fs	XTIN, XTOUT			30.0	34.0	kHz

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (Supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: The condition of clock frequency is in NORMAL1/2 modes and IDLE1/2 modes.

**DC** Characteristics

 $(V_{SS} = 0 \text{ V}, \text{ Topr} = -40 \text{ to } 85^{\circ}\text{C})$ 

Parameter	Symbol	Pins	Conditions	Min	Тур.	Max	Unit
Hysteresis voltage	V <sub>HS</sub>	Hysteresis inputs	VDD = 5.0 V	-	0.9	_	V
	I <sub>IN1</sub>	TEST					
Input current	I <sub>IN2</sub>	Open drain ports, Tri-state ports	VDD = 5.5 V V <sub>IN</sub> = 5.5 V/0 V	-	_	± 2	μΑ
	I <sub>IN3</sub>	RESET, STOP					
Input resistance	R <sub>IN2</sub>	RESET	VDD = 5.0 V	100	220	450	kΩ
Output leakage current		Sink open drain ports	V <sub>DD</sub> = 5.5 V, V <sub>OUT</sub> = 5.5 V	_	-	2	
	I <sub>LO</sub>	Tri-state ports	V <sub>DD</sub> = 5.5 V, V <sub>OUT</sub> = 5.5/0 V	_	_	± 2	$\mu$ A
Output high voltage	V <sub>OH2</sub>	Tri-state ports	$V_{DD} = 4.5 \text{ V}, I_{OH} = -0.7 \text{ mA}$	4.1	-	-	٧
Output low voltage	V <sub>OL</sub>	Except for XOUT and P3	V <sub>DD</sub> = 4.5 V, I <sub>OL</sub> = 1.6 mA	-	_	0.4	mA
Output Low current	I <sub>OL3</sub>	P3	V <sub>DD</sub> = 4.5 V, V <sub>OL</sub> = 1.0 V	-	20	-	mA
Supply current in NORMAL 1, 2 modes			$V_{DD} = 5.5 \text{ V}$ $V_{IN} = 5.3 \text{ V}/0.2 \text{ V}$	_	4.5	5.5	mA
Supply current in IDLE 1, 2 modes			fc = 8 MHz fs = 32.768 kHz	_	2.5	4.0	mA
Supply current in NORMAL 1, 2 modes			$V_{DD} = 3.0 \text{ V}, V_{IN} = 2.8 \text{ V}/0.2 \text{V}$ $V_{IN} = 4.19 \text{ MHz}$	_	1.75	3.0	mA
Supply current in IDLE 1, 2 modes	] ,		fs = 32.768 kHz	_	1.25	2.0	mA
Supply current in SLOW mode	l <sub>DD</sub>		$V_{DD} = 3.0 \text{ V}$ $V_{IN} = 2.8 \text{ V}/0.2 \text{ V}$	_	20	30	μΑ
Supply current in SLEEP mode			fs = 32.768 kHz	-	10	20	μΑ
Supply current in STOP mode			V <sub>DD</sub> = 5.5 V V <sub>IN</sub> = 5.3 V/0.2 V	-	0.5	10	μΑ

Note 1: Typical values show those at Topr =  $25^{\circ}$ C

Note 2: Input Current  $I_{IN1}$ ,  $I_{IN3}$ ; The current through resistor is not included, when the input resistor (pull-up or pull-down) is contained.

Note 3: IDD except for I<sub>REF</sub>.

**AD Conversion Characteristics** 

 $(V_{SS} = 0 \text{ V}, V_{DD} = 2.7 \text{ to } 5.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$ 

				Тур.		Max		
Parameter	Symbol	Conditions	Min		ADCDR1 ADC		DR2	Unit
					ADCDICT	ACK = 0	ACK = 1	
A	$V_{AREF}$	V > 2.5.V	2.7	-		$V_{DD}$		V
Analog reference voltage	V <sub>ASS</sub>	$V_{AREF} - V_{ASS} \ge 2.5 V$	V <sub>SS</sub>	_	1.5			\ \ \ \ \ \
Analog input voltage	V <sub>AIN</sub>		V <sub>ASS</sub>	_		$V_{AREF}$		٧
Analog supply current	I <sub>REF</sub>	V <sub>AREF</sub> = 5.5 V, V <sub>ASS</sub> = 0.0 V	_	0.5		1.2		mA
Nonlinearity error		V <sub>DD</sub> = 5.0, V <sub>SS</sub> = 0.0 V V <sub>AREF</sub> = 5.000 V	_	_	± 1	± 3	± 2	
Zero point error		V <sub>ASS</sub> = 0.000 V	_	_	± 1	± 3	± 2	
Full scale error		$V_{DD} = 2.7, V_{SS} = 0.0 \text{ V}$	_	_	± 1	± 3	± 2	LSB
Total error		V <sub>AREF</sub> = 2.700 V V <sub>ASS</sub> = 0.000 V	_	_	± 2	± 6	± 4	

Note 1:  $\triangle V_{AREF} = V_{AREF} - V_{ASS}$ ADCDR1: 8 bits - AD conversion result (1LSB =  $\triangle V_{AREF}$ /256) ADCDR2: 10 bits - AD conversion result (1LSB =  $\triangle V_{AREF}$ /1024)

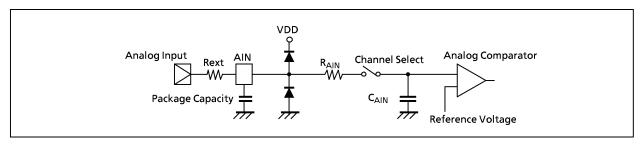
Note 2: Quantizing error is not contained in those errors.

## **AD Input Characteristics**

(Topr =  $-40 \text{ to } 85^{\circ}\text{C}$ )

Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
Input impedance (Resistance)	В	VDD = 5.0 V, Conversion time 23 $\mu$ s (fc = 8 MHz)	-	5	_	kΩ
	R <sub>AIN</sub>	$V_{DD} = 2.7 \text{ V}$ , Conversion time 43.8 $\mu$ s (fc = 4.2 MHz)	20	_	K77	
	C <sub>AIN</sub>	$V_{DD} = 5.0 \text{ V}$ , Conversion time 23 $\mu$ s (fc = 8 MHz)		7	_	
Input impedance (Capacity)		$V_{DD} = 2.7 \text{ V}$ , Conversion time 43.8 $\mu$ s (fc = 4.2 MHz)	-	7	-	pF
Source impedance	Rext	$V_{DD} = 5.0 \text{ V}$ , Conversion time 23 $\mu$ s (fc = 8 MHz)	-	_	5	
		$V_{DD} = 2.7 \text{ V}$ , Conversion time 43.8 $\mu$ s (fc = 4.2MHz)	-	_	5	kΩ

Note: Input current (Output leak current) error (Max  $\pm 2 \mu$ A) and quantizing error (Max  $\pm 4$ LSB) for AD are contained.



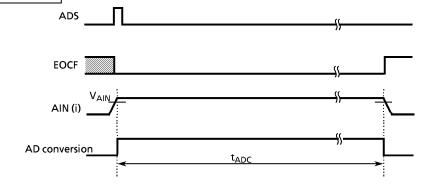
AD Pin Mode

## **AC Characteristics**

(Vac	_	٥٧	Tonr	_	- 40 to	85°C\
(VSS	=	υν,	TOP	=	- 40 to	65 C)

Parameter	Symbol	Conditions	V <sub>DD</sub>	Min	Тур.	Max	Unit
		In NORMAL 1, 2 mode	4.5 to	0.5		40	
Machina avelatima		In IDLE 1, 2 mode	5.5 V	0.5	ı	10	
Machine cycle time	t <sub>cy</sub>	In SLOW mode	2.7 to	447.6		133.3	$\mu$ S
		In SLEEP mode	5.5 V	117.6	_		
High level clock pulse width	t <sub>WCH</sub>	For external clock operation	4.5 to	62.5		_	
Low level clock pulse width	t <sub>WCL</sub>	(XIN input), fc = 8 MHz	5.5 V	62.5	-		ns
High level clock pulse width	t <sub>WSH</sub>	For external clock operation	2.7 to	44.7			
Low level clock pulse width	t <sub>WSL</sub>	(XTIN input), fs = 32.768 kHz	5.5 V	14.7	_	_	$\mu$ S
AD conversion time	1.	ADCCR bit 4; ACK = 0	-	-	49 tcy	-	
	t <sub>ADC</sub>	ADCCR bit 4; ACK = 1	-	-	196 tcy	-	ns

# Timing of AD Conversion



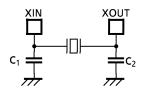
Note 1: During AD conversion, make the level of  $V_{AIN}$  stable.

Note 2: i = 17 to 10, 07 to 00

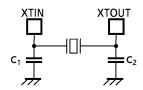
**Recommended Oscillating Conditions** 

 $(V_{SS} = 0 \text{ V}, \text{ Topr} = -40 \text{ to } 85^{\circ}\text{C})$ 

	0 111 1	Oscillation		_		Recommended Constant		
Parameter	Oscillator	Frequency	VDD	Recommend	ded Oscillator	C <sub>1</sub>	C <sub>2</sub>	
	Ceramic	8 MHz	4.5 to 5.5 V	KYOCERA	KBR8.0M			
	resonator		2.7 to 5.5 V	KYOCERA	KBR4.0MS	30 pF	30 pF	
oscillation		4 MHz		MURATA	CSA4.00MG			
		8 MHz	4.5 to 5.5 V	точосом	210B 8.0000			
	Crystal oscillator	4 MHz	2.7 to 5.5 V	тоуосом	204B 4.0000	20 pF	20 pF	
Low-frequency oscillation	Crystal oscillator	32.768 kHz	2.7 to 5.5 V	NDK	MX-38T	15 pF	15 pF	



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

- Note 1: When it is used in high electrical field, an electrical shield of the package is recommended to retain normal operations.
- Note 2: TOYAMA MURATA MFG. CO., LTD (JAPAN)

The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change.

For up-to-date information, please refer to the following URL;

http://www.murata.co.jp/search/index.html

## **Electrical Characteristics**

#### (2) TMP87CM48

Absolute Maximum Ratings

 $(V_{SS} = 0 V)$ 

Parameter	Symbol	Conditions	Ratings	Unit	
Supply voltage	$V_{DD}$		- 0.3 to 6.5	V	
Input voltage	$V_{IN}$		$-0.3$ to $V_{DD} + 0.3$	V	
Output voltage	V <sub>OUT</sub>		- 0.3 to V <sub>DD</sub> + 0.3	V	
Output support (Bandaria)	I <sub>OUT1</sub>	Ports P0, P1, P2, P4, P5, P6, P7, P8	3.2	mA	
Output current (Per 1 pin)	I <sub>OUT2</sub>	Port P3	30		
O to the world (Table I)	Σ l <sub>OUT1</sub>	Ports P0, P1, P2, P4, P5, P6, P7, P8	120		
Output current (Total)	Σ I <sub>OUT2</sub>	Port P3	120	mA	
Power dissipation	PD		350	mW	
Soldering temperature (Time)	Tsld		260 (10 s)	°C	
Storage temperature	Tstg		– 55 to 125	°C	
Operating temperature	Topr		- 40 to 85	°C	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

**Recommended Operating Conditions** 

$$(V_{SS} = 0 \text{ V}, \text{ Topr} = -40 \text{ to } 85^{\circ}\text{C})$$

Parameter	Symbol	Pins		Conditions	Min	Max	Unit
			fc = 8	NORMAL1/2 modes	4.5		
			MHz	IDLE1/2 modes	-1.3		
Supply voltage			fc =	NORMAL1/2 modes		5.5	
	$V_{DD}$		4.2 MHz	IDLE1/2 modes	2.7		V
			fs =	SLOW mode	2.,		
			32.768 kHz	SLEEP mode			
				STOP mode	2.0		
	V <sub>IH1</sub>	Except hysteresis input	$V_{DD} \ge 4.5 \text{ V}$ $V_{DD} < 4.5 \text{ V}$		$V_{DD} \times 0.70$		
Input high voltage	V <sub>IH2</sub>	Hysteresis input			$V_{DD} \times 0.75$	$V_{DD}$	V
	V <sub>IH3</sub>				V <sub>DD</sub> × 0.90		
	V <sub>IL1</sub>	Except hysteresis input		, > A E V		$V_{DD} \times 0.30$	
Input low voltage	$V_{IL2}$	Hysteresis input	]	$V_{\rm DD} \ge 4.5  \rm V$	0	$V_{DD} \times 0.25$	V
	V <sub>IL3</sub>		\	/ <sub>DD</sub> < 4.5 V		$V_{DD} \times 0.10$	
	٠,	VIN VOLIT	V <sub>DD</sub> = 4.5 to 5.5 V			8.0	MHz
Clock frequency	fc	XIN, XOUT	V <sub>DD</sub>	= 2.7 to 5.5 V	0.4	4.2	IVITIZ
	fs	XTIN, XTOUT		•	30.0	34.0	kHz

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: The condition of clock frequency is in NORMAL1/2 modes and IDLE1/2 modes.

**DC** Characteristics

 $(V_{SS} = 0 \text{ V}, \text{ Topr} = -40 \text{ to } 85^{\circ}\text{C})$ 

Parameter	Symbol	Pins	Conditions	Min	Тур.	Max	Unit
Hysteresis voltage	V <sub>HS</sub>	Hysteresis inputs	VDD = 5.0 V	-	0.9	_	٧
	I <sub>IN1</sub>	TEST					
Input current	I <sub>IN2</sub>	Open drain ports, Tri-state ports	VDD = 5.5 V V <sub>IN</sub> = 5.5 V/0 V	-	_		μΑ
	I <sub>IN3</sub>	RESET, STOP					
Input resistance	R <sub>IN2</sub>	RESET	VDD = 5.0 V	100	220	450	kΩ
Output leakage		Sink open drain ports	V <sub>DD</sub> = 5.5 V, V <sub>OUT</sub> = 5.5 V	_	-	2	
current	I <sub>LO</sub>	Tri-state ports	V <sub>DD</sub> = 5.5 V, V <sub>OUT</sub> = 5.5/0 V	_	_	± 2	$\mu$ A
Output high voltage	V <sub>OH2</sub>	Tri-state ports	$V_{DD} = 4.5 \text{ V}, I_{OH} = -0.7 \text{ mA}$	4.1	-	-	٧
Output low voltage	V <sub>OL</sub>	Except for XOUT and P3	V <sub>DD</sub> = 4.5 V, I <sub>OL</sub> = 1.6 mA	_	_	0.4	mA
Output low current	I <sub>OL3</sub>	P3	V <sub>DD</sub> = 4.5 V, V <sub>OL</sub> = 1.0 V	_	20	_	mA
Supply current in NORMAL 1, 2 modes			$V_{DD} = 5.5 \text{ V}$ $V_{IN} = 5.3 \text{ V}/0.2 \text{ V}$	_	4.75	6.4	mA
Supply current in IDLE 1, 2 modes			fc = 8 MHz fs = 32.768 kHz	_	3.25	4.65	mA
Supply current in NORMAL 1, 2 modes			$V_{DD} = 3.0 \text{ V}, V_{IN} = 2.8 \text{ V}/0.2 \text{V}$ $V_{IN} = 4.19 \text{ MHz}$	_	1.85	3.2	mA
Supply current in IDLE 1, 2 modes	] ,		fs = 32.768 kHz	-	1.35	2.2	mA
Supply current in SLOW mode	l <sub>DD</sub>		$V_{DD} = 3.0 \text{ V}$ $V_{IN} = 2.8 \text{ V}/0.2 \text{ V}$	_	20	30	μΑ
Supply current in SLEEP mode			fs = 32.768 kHz	_	10	20	μΑ
Supply current in STOP mode			V <sub>DD</sub> = 5.5 V V <sub>IN</sub> = 5.3 V/0.2 V	-	0.5	10	μΑ

Note 1: Typical values show those at Topr =  $25^{\circ}$ C

Note 2: Input Current  $I_{IN1}$ ,  $I_{IN3}$ : The current through resistor is not included, when the input resistor (pull-up or pull-down) is contained.

Note 3: IDD except for I<sub>REF</sub>.

**AD Conversion Characteristics** 

 $(V_{SS} = 0 \text{ V}, V_{DD} = 2.7 \text{ to } 5.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$ 

					Max			
Parameter	Symbol	Conditions	Min	Тур.	ADCDR1	ADC		Unit
						ACK = 0	ACK = 1	
A mala a mafananaa walta na	$V_{AREF}$	V > 25V	2.7	_	V <sub>DD</sub>			V
Analog reference voltage	V <sub>ASS</sub>	$V_{AREF} - V_{ASS} \ge 2.5 V$	V <sub>SS</sub>	-	1.5			
Analog input voltage	$V_{AIN}$		V <sub>ASS</sub>	-		$V_{AREF}$		٧
Analog supply current	I <sub>REF</sub>	V <sub>AREF</sub> = 5.5 V, V <sub>ASS</sub> = 0.0 V	_	0.5		1.2		mA
Nonlinearity error		V <sub>DD</sub> = 5.0, V <sub>SS</sub> = 0.0 V V <sub>AREF</sub> = 5.000 V	_	_	± 1	± 3	± 2	
Zero point error		VAREF = 3.000 V VASS = 0.000 V	_	_	± 1	± 3	± 2	LCD
Full scale error		V <sub>DD</sub> = 2.7, V <sub>SS</sub> = 0.0 V V <sub>AREF</sub> = 2.700 V	_	_	± 1	± 3	± 2	LSB
Total error		$V_{ASS} = 0.000 \text{ V}$	_	_	± 2	± 6	± 4	

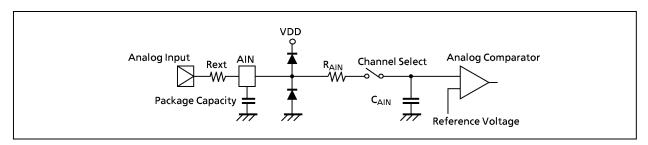
Note 1:  $\triangle V_{AREF} = V_{AREF} - V_{ASS}$ ADCDR1: 8 bits - AD conversion result (1LSB =  $\triangle V_{AREF}$ /256) ADCDR2: 10 bits - AD conversion result (1LSB =  $\triangle V_{AREF}$ /1024)

Note 2: Quantizing error is not contained in those errors.

AD Input Characteristics	$(Topr = -40 \text{ to } 85^{\circ}C)$
--------------------------	--

Parameter	Symbol	Conditions		Тур.	Max	Unit
Input impedance (Resistance)	ь	VDD = 5.0 V, Conversion time 23 $\mu$ s (fc = 8 MHz)	-	5	-	kO
Input impedance (Resistance)	R <sub>AIN</sub>	$V_{DD} = 2.7 \text{ V}$ , Conversion time 43.8 $\mu$ s (fc = 4.2 MHz)	-	20	-	kΩ
		$V_{DD} = 5.0 \text{ V}$ , Conversion time 23 $\mu$ s (fc = 8 MHz)	-	7	_	
Input impedance (Capacity)	C <sub>AIN</sub>	$V_{DD} = 2.7 \text{ V}$ , Conversion time 43.8 $\mu$ s (fc = 4.2 MHz)	-	7	_	pF
Commentered	Davet	$V_{DD} = 5.0 \text{ V}$ , Conversion time 23 $\mu$ s (fc = 8 MHz) –	-	-	5	
Source impedance	Rext	$V_{DD} = 2.7 \text{ V}$ , Conversion time 43.8 $\mu$ s (fc = 4.2 MHz)	_	-	5	kΩ

Note: Input current (output leak current) error (Max  $\pm 2 \mu$ A) and quantizing error (Max  $\pm 4$ LSB) for AD are contained.



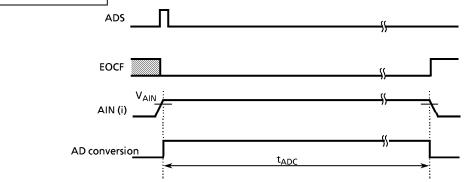
AD Pin Mode

AC Characteristics	(Vs
AC Characteristics	( \ \ \ \ \ \

$(V_{SS} = 0 V,$	Topr =	- 40 to 85°C)
------------------	--------	---------------

Parameter	Symbol	Conditions	V <sub>DD</sub>	Min	Тур.	Max	Unit
		In NORMAL 1, 2 mode	4.5 to			4.0	
Machina avala tima		In IDLE 1, 2 mode	5.5 V	5.5 V 0.5 -		10	
Machine cycle time	t <sub>cy</sub>	In SLOW mode	2.7 to	117.6			$\mu$ S
		In SLEEP mode	5.5 V 117.6	-	133.3		
High level clock pulse width	t <sub>WCH</sub>	For external clock operation	4.5 to	62.5		-	
Low level clock pulse width	t <sub>WCL</sub>	(XIN input), fc = 8 MHz	5.5 V	62.5	-		ns
High level clock pulse width	t <sub>WSH</sub>	For external clock operation	2.7 to				
Low level clock pulse width	t <sub>WSL</sub>	(XTIN input), fs = 32.768 kHz	5.5 V	14.7	-	_	$\mu$ S
			49 tcy	-			
AD conversion time	t <sub>ADC</sub>	ADCCR bit 4; ACK = 1	-	-	196 tcy	-	ns

# Timing of AD Conversion



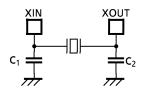
Note 1: During AD conversion, make the level of  $V_{AIN}$  stable.

Note 2: i = 17 to 10, 07 to 00

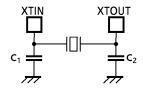
**Recommended Oscillating Conditions** 

 $(V_{SS} = 0 \text{ V}, \text{ Topr} = -40 \text{ to } 85^{\circ}\text{C})$ 

Danis at an Oasi Hatan		Oscillation	VDD	Recommended Oscillator		Recommended Constant		
Parameter	Parameter Oscillator					C <sub>1</sub>	C <sub>2</sub>	
High-frequency Oscillation	Ceramic	8 MHz	4.5 to 5.5 V	KYOCERA	KBR8.0M			
	Resonator	4 MHz	2.7 to 5.5 V	KYOCERA	KBR4.0MS	30 pF	30 pF	
				MURATA	CSA4.00MG			
	Crystal Oscillator	8 MHz	4.5 to 5.5 V	тоуосом	210B 8.0000			
		4 MHz	2.7 to 5.5 V	тоуосом	204B 4.0000	20 pF	20 pF	
Low-frequency Oscillation	Crystal Oscillator	32.768 kHz	2.7 to 5.5 V	NDK	MX-38T	15 pF	15 pF	



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

- Note 1: When it is used in high electrical field, an electrical shield of the package is recommended to retain normal operations.
- Note 2: TOYAMA MURATA MFG. CO., LTD (JAPAN)

The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change.

For up-to-date information, please refer to the following URL;

http://www.murata.co.jp/search/index.html