TOSHIBA RISC PROCESSOR **TENTATIVE**

TMPR3907F
32-Bit TX System RISC

1. GENERAL DESCRIPTION

The TMPR3907F (TX3907) is a TX39 family microprocessor incorporating a 32-bit TX39/H core developed by Toshiba. Designed for use in OA equipment, the TX3907 also incorporates such peripheral circuits as a memory controller, a PCI controller, and timers.

2. FEATURES

TX39/H core

- An original Toshiba core based on the R3000A architecture of MIPS Technologies, Inc. of the United States.
- Instruction cache: 4 KB; data cache: 1 KB

DRAM controller

- Two banks x three channels
- Supports Fast Page and Hyper Page (EDO) modes.

ROM controller

- One bank x five channels (in Half-Speed Bus mode: three channels)
- Supports mask ROM, Page mode ROM, EPROM, E^2PROM, flash ROM, and SRAM.

PCI controller

- Compliance with PCI Local Bus Specification Revision 2.1.
- Initiator/target/arbiter

Interrupt controller

- Five internal interrupts; three external interrupts

Timers

- 24-bit up-counter: three channels (one channel usable as a watchdog timer)

Serial I/O

- UART: one channel

Bus interface

- DRAM address/ROM address/data separate bus
- 16-bit Data Bus and Half-Speed Bus modes (1/2 bus frequency) selectable
- 5 V tolerant input (data bus)

Power supply: 3.3 V

Maximum operating frequency: 66 MHz (PCI: 33 MHz)

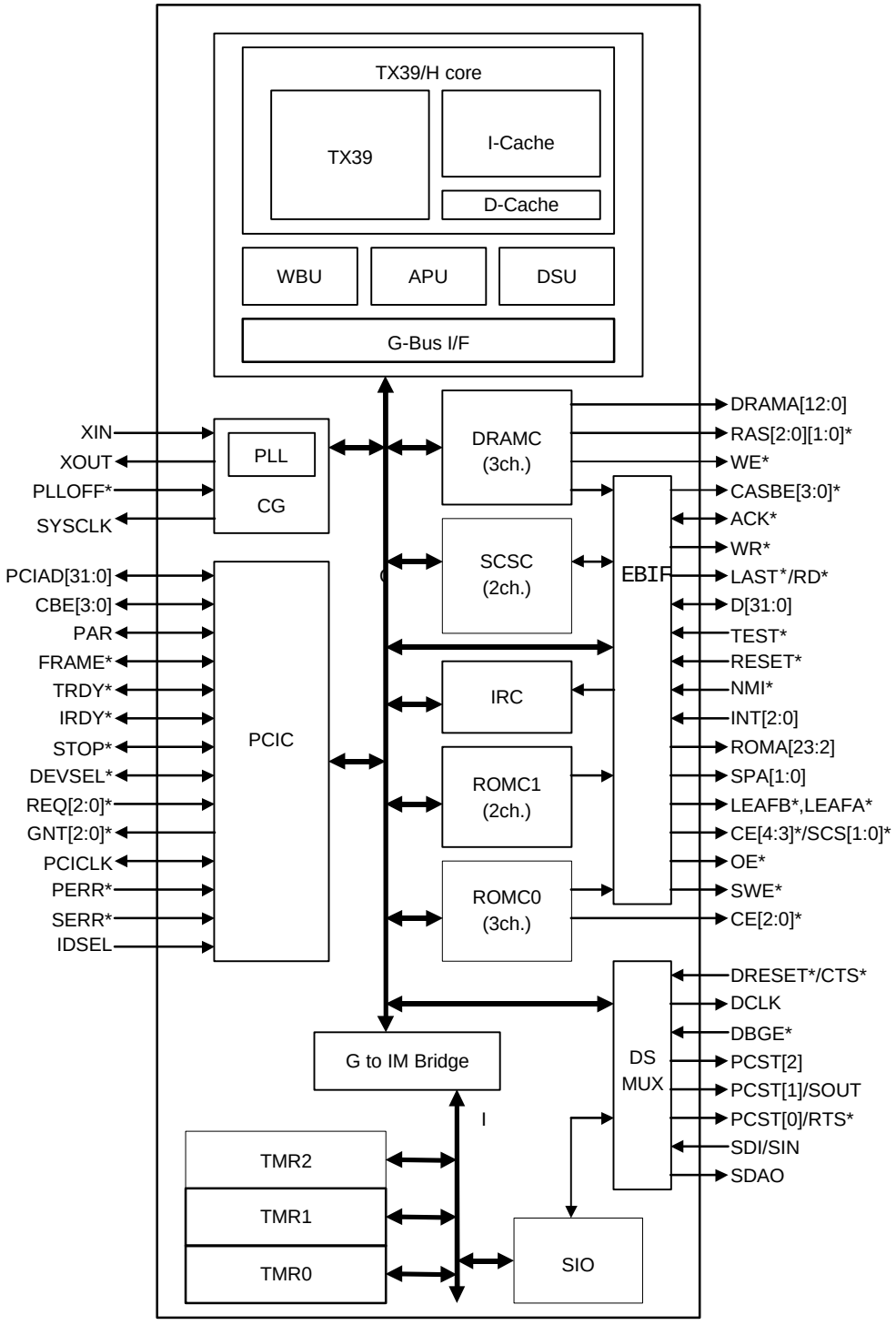
Power dissipation: 800 mW (typ.)

Package: 208-pin plastic QFP

* R3000A is the trademark of MIPS Technologies, Inc.

3. SYSTEM CONFIGURATION

3.1 TX3907 BLOCK DIAGRAM



4. PIN DESCRIPTION

4.1 PIN ASSIGNMENT

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	INT[1]	31	ROMA[9]	61	VDD	91	DRAMA[12]
2	INT[0]	32	OE*	62	VSS	92	RAS0[0]*
3	GNT[2]*	33	SYSCLK	63	D[26]	93	RAS0[1]*
4	GNT[1]*	34	ACK*	64	D[19]	94	RAS1[0]*
5	GNT[0]*	35	LAST*/RD*	65	D[27]	95	RAS1[1]*
6	ROMA[23]	36	VDD	66	DRAMA[0]	96	VSS
7	ROMA[22]	37	VSS	67	DRAMA[1]	97	VDD
8	CE[4]*/SCS[1]*	38	VSS	68	DRAMA[2]	98	RAS2[0]*
9	VDD	39	ROMA[10]	69	DRAMA[3]	99	RAS2[1]*
10	VDD	40	ROMA[11]	70	DRAMA[4]	100	CASBE[0]*
11	VSS	41	ROMA[12]	71	DRAMA[5]	101	CASBE[1]*
12	CE[3]*/SCS[0]*	42	ROMA[13]	72	VSS	102	CASBE[3]*
13	CE[2]*	43	VDD	73	VSS	103	CASBE[2]*
14	CE[1]*	44	ROMA[14]	74	VDD	104	WE*
15	VSS	45	ROMA[15]	75	DRAMA[6]	105	D[0]
16	CE[0]*	46	ROMA[16]	76	DRAMA[10]	106	D[8]
17	SWE*	47	ROMA[17]	77	D[20]	107	PLLOFF*
18	WR*	48	ROMA[18]	78	D[28]	108	PLL_VSS
19	SPA[0]	49	ROMA[19]	79	D[21]	109	VSS
20	SPA[1]	50	VSS	80	D[29]	110	XIN
21	ROMA[2]	51	ROMA[20]	81	D[22]	111	XOUT
22	ROMA[3]	52	ROMA[21]	82	D[30]	112	VDD
23	ROMA[4]	53	LEAFA*	83	D[23]	113	PLL_VDD
24	ROMA[5]	54	LEAFB*	84	D[31]	114	VDD
25	VDD	55	D[16]	85	VDD	115	D[1]
26	VSS	56	D[24]	86	VSS	116	D[9]
27	VSS	57	D[17]	87	DRAMA[7]	117	D[2]
28	ROMA[6]	58	D[25]	88	DRAMA[11]	118	D[10]
29	ROMA[7]	59	D[18]	89	DRAMA[8]	119	VSS
30	ROMA[8]	60	VSS	90	DRAMA[9]	120	D[3]

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
121	D[11]	143	DCLK	165	VDD	187	PCIAD[20]
122	D[4]	144	PCICLK	166	PCIAD[14]	188	PCIAD[21]
123	D[12]	145	PCIAD[0]	167	PCIAD[15]	189	PCIAD[22]
124	D[13]	146	PCIAD[1]	168	CBE[1]	190	PCIAD[23]
125	D[5]	147	VDD	169	PAR	191	IDSEL
126	D[14]	148	PCIAD[2]	170	SERR*	192	VSS
127	D[6]	149	PCIAD[3]	171	PERR*	193	CBE[3]
128	D[15]	150	PCIAD[4]	172	STOP*	194	PCIAD[24]
129	D[7]	151	PCIAD[5]	173	VSS	195	PCIAD[25]
130	VSS	152	PCIAD[6]	174	DEVSEL*	196	PCIAD[26]
131	VSS	153	PCIAD[7]	175	TRDY*	197	PCIAD[27]
132	RESET*	154	VDD	176	IRDY*	198	PCIAD[28]
133	TEST*	155	VSS	177	FRAME*	199	PCIAD[29]
134	NMI*	156	VSS	178	CBE[2]	200	VSS
135	SDAO	157	CBE[0]	179	PCIAD[16]	201	VDD
136	DRESET*/CTS*	158	PCIAD[8]	180	PCIAD[17]	202	VSS
137	SDI/SIN	159	PCIAD[9]	181	VDD	203	PCIAD[30]
138	DBGE*	160	PCIAD[10]	182	VSS	204	PCIAD[31]
139	PCST[2]	161	PCIAD[11]	183	VSS	205	REQ[2]*
140	PCST[1]/SOUT	162	PCIAD[12]	184	VDD	206	REQ[1]*
141	PCST[0]/RTS*	163	PCIAD[13]	185	PCIAD[18]	207	REQ[0]*
142	VSS	164	VSS	186	PCIAD[19]	208	INT[2]

The asterisk(*) after the signal name indicates active law.

4.2 PIN FUNCTIONS

Signal Name	I/O	Function
System interface signals		
SYSCLK	O	System clock Outputs the same clock as that of the TX39/H core (Full-Speed Bus mode) or half the clock of the TX39/H core (Half-Speed Bus mode). Output can be halted using the ROMA[20] pin at a reset.
CASBE[3:0]*	O	CAS / Byte Enable Indicates the position of the valid data on the data bus D[31:0]. Operates as a CAS* signal at DRAM access (including refresh cycle). In 16-bit Bus mode, CASBE[1:0]* only is used. The following shows the correspondence between CASBE[3:0] and the data bus. CASBE[3]* D[31:24] CASBE[2]* D[23:16] CASBE[1]* D[15:8] CASBE[0]* D[7:0]
D[31:0]	I/O	Data Data bus. In 16-bit Bus mode, D[15:0] is used.
LAST*/RD*	O	Last/Read In Full-Speed Bus mode, functions as the LAST* signal, which indicates the end of bus operation. In Half-Speed Bus mode, functions as the RD* signal, which indicates that the bus operation in progress is a read.
WR*	O	Write Indicates that the bus operation in progress is a write.
ACK*	I/O	Acknowledge In Full-Speed Bus mode, functions as an output signal which indicates the completion of the bus operation. In Half-Speed mode, operates as an input signal which completes the SCS operation.
RESET*	I	Reset Holding this signal low for at least 60 system clocks initializes the TX3907. The TX3907 is initialized in accordance with the ROMA[23:9] setting at a RESET* signal rising edge.

Clock signals		
XIN	I	Crystal input Connect a crystal oscillator to this pin. The TX39/H core operates at eight times the crystal oscillator.
XOUT	O	Crystal output Connect a crystal oscillator to this pin.
PLLOFF*	I	PLL off Used to halt oscillation of the PLL of the TX3907 built-in clock generator.
Interrupt signals		
NMI*	I	Non-maskable interrupt The non-maskable interrupt signal.
INT[2:0]	I	Interrupt request External interrupt request signal.
Memory interface signals		
DRAMA[12:0]	O	DRAM address DRAM address signal.
RAS2[1:0]* RAS1[1:0]* RAS0[1:0]*	O	RAS DRAM RAS signal.
WE*	O	Write enable DRAM write enable signal.
ROMA[23:9]	I/O	ROM address ROM and SCS addresses. ROMA[23:9] is loaded to the TX3907 on the RESET* signal rising edge and is used for the TX3907 initial settings.
ROMA[8:2]	O	
SPA [1:0]	O	Special address Signal for the ROM lower address. Used in 16-bit Bus mode and for interleaving.
CE[4:3]*/ SCS[1:0]*	O	Chip enable/system chip select In Full-Speed Bus mode, functions as the chip select signal for ROM channels 3 and 4. In Half-Speed Bus mode, functions as the chip select signal for SCS channels 0 and 1.
CE[2:0]*	O	Chip enable Chip select signal for ROM channels 0, 1, and 2.
OE*	O	Output enable ROM output enable signal.
SWE*	O	SRAM write enable SRAM/flash ROM write enable signal.
LEAFA* LEAFB*	O	LEAF Used to switch the data bus between odd and even when ROM is in Interleave mode.

PCI interface signals		
PCIAD[31:0]	I/O	PCI address and data Address and data multiplex bus.
CBE[3:0]*	I/O	Bus command and byte enable Command and byte enable signal.
PAR	I/O	Parity Parity signal for PCIAD[31:0] and CBE[3:0].
FRAME*	I/O	Cycle frame Indicates that a bus operation is in progress.
IRDY*	I/O	Initiator ready Indicates that the initiator is ready to complete the data transfer.
TRDY*	I/O	Target ready Indicates that the target is ready to complete the data transfer.
STOP*	I/O	Stop Used by the target to request the initiator to halt the data transfer.
IDSEL	I	Initialization device select Chip select signal used at configuration access.
DEVSEL*	I/O	Device select Response signal used by the target to assert access from the initiator.
REQ[2:0]*	I	Request Signal used by the master to request bus mastership.
GNT[2:0]*	O	Grant Indicates that bus mastership is granted to the master.
PERR*	I	Parity Error Indicates that data parity error occurred in a bus cycle other than a special cycle.
SERR*	I	System Error Indicates data parity error in a special cycle, address parity error, or a fatal error.
PCICLK	I/O	PCI Clock PCI bus clock. Two modes are supported: output from the TX3907 PCI controller or input to the TX3907 PCI controller from an external source. The mode is determined by the ROMA[21] signal state on the RESET* signal rising edge.

Debugging interface Four of the eight debugging interface pins are also used as SIO pins. When ROMA[16:12] is set to 11111 on the RESET* signal rising edge, these pins are used for an external real-time debug system. When ROMA[16:12] is set to 11110 on the RESET* signal rising edge, these pins operate as SIO pins. Do not set ROMA[16:12] other than as above. The ROMA[16:12] is pulled up internally.		
DRESET*/CTS*	I	Debug reset/clear to send Functions as the DRESET* signal for an external real-time debug system or as the SIO CTS* signal.
DCLK	O	Debug clock DCLK signal for an external real-time debug system.
DBGE*	I	Debugger enable DBGE* signal for an external real-time debug system.
PCST[2]	O	PC Trace Status [2] PCST[2] signal for an external real-time debug system.
PCST[1]/SOUT	O	PC trace status [2] Functions as the PCST[1] signal for an external real-time debug system or as the SIO data output signal.
PCST[0]/RTS*	O	PC trace status [0]/Request to send Functions as the PCST[0] signal for an external real-time debug system or as the SIO RTS* signal.
SDI/SIN	I	Serial data input/Serial input Functions as the SDI signal for an external real-time debug system or as the SIO data input signal.
SDAO	O	Serial data and address output SDAO signal for an external real-time debug system.
Other signals		
TEST*	I	Test Test pin. Leave fixed to high.

TX3907 initial setting signals

These initial setting input signals use same pins as those for ROMA signals. The signals are loaded to the TX3907 on the RESET* signal rising edge and are used for the TX3907 initial settings. The signals are all pulled up internally.

Initial Setting Signals	ROMA	Function
BOOT16*	ROMA[23]	Boot 16 bits Sets the boot ROM (channel 0) bus width. High: 32 bits Low: 16 bits
BOOTIL*	ROMA[22]	Boot interleave Sets the boot ROM (channel 0) mode. High: Non interleave Low: Interleave
PCICLKIN*	ROMA[21]	PCICLK input Sets the PCI clock input/output. High: Sets the PCI clock as an output signal. Low: Sets the PCI clock as an input signal.
SYSCLKEN	ROMA[20]	SYSCLK enable Sets the SYSCLK output. High: Outputs SYSCLK. Low: Does not output SYSCLK (set to Hi-Z).
ENDIAN	ROMA[19]	Endian Sets the endian. Used fixed to big endian. High: Big endian Low: Reserved
BOOTPG*	ROMA[18]	Boot page Sets the type of boot ROM (channel 0). High: Non-Page mode ROM Low: Page mode ROM
HALF*	ROMA[17]	Half Sets the bus speed. High: Full-Speed Bus mode Low: Half-Speed Bus mode
DPM[4:0]	ROMA[16:12]	Debug Port mode Sets how the eight debugging port pin signals are used. 11111: Real-time debug system signal 11110: SIO signal 11101 to 00000: Reserved

PCI3	ROMA[11]	PCI clock divisor Sets the PCI clock frequency. It is valid when PCICLKIN* is High. High: Sets PCICLK to one third of the TX39/H core frequency. Low: Sets PCICLK to half the TX39/H core frequency.
CGRESET*	ROMA[10]	CGRESET Resets the built-in clock generator. While the RESET* signal is low, functions as the CGRESET* signal.
D0BASE	ROMA[9]	DRAMC channel 0 base address Sets the initial value of the DRAMC channel 0 base address. High: Sets the base address initial value to 0x2000_0000. Low: Sets the base address initial value to 0x0000_0000.

5. ELECTRICAL CHARACTERISTICS

5.1 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{DD}	–0.3 to 5.0	V
Input Voltage D[31:0], DRESET*/CTS*, SDI/SIN	V_{IN1}	–0.3 to 5.3V	V
Other than above	V_{IN2}	–0.3 to V_{DD}_+_0.3V	V
Storage Temperature	T_{STG}	–40 to 125	°C
Maximum Power Dissipation	P_D	TBD	W

Note: Exceeding the absolute maximum ratings when using this LSI may permanently damage the device. In normal operation, use the LSI under the recommended operating conditions. Exceeding these conditions can affect the reliability of the LSI

5.2 RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	MIN	MAX	Unit
Supply Voltage	V_{DD}		3.0	3.6	V
Operating Temperature	T_a		0	70	°C

Note: This product is designed principally for OA equipment applications. If using for other applications, please contact Toshiba engineering staff.

5.3 DC CHARACTERISTICS

5.3.1 DC Characteristics of Pins Other Than PCI Interface Pins

(T_a = 0 to 70°C, V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V)

Parameter	Symbol	Conditions	MIN	MAX	Unit
Low-level input voltage	V_{IL1}	XIN, ACK*, RESET*, PLLOFF*, NMI*, INT[2:0], DRESET*/CTS*, SDI/SIN		V_{DD} × 0.2	V
	V_{IL2}	Other than above		0.8	
High-level input voltage	V_{IH1}	XIN, ACK*, RESET*, PLLOFF*, NMI*, INT[2:0], DRESET*/CTS*, SDI/SIN	V_{DD} × 0.8		V
	V_{IH2}	Other than above	20		
Low-level output current	I_{OL1}	DRAMA[12:0], LEAFA*, LEAFB* V_{OL} = 0.4V		16	mA
	I_{OL2}	Other than above V_{OL} = 0.4V		8	mA
High-level output current	I_{OH1}	DRAMA[12:0], LEAFA*, LEAFB* V_{OH} = 2.4V	−16		mA
	I_{OH2}	Other than above V_{OH} = 2.4V	−8		mA
Operating current	I_{DD}			TBD	
Input leakage current	I_{IH}		−10	10	µA
	I_{IL}		−10	10	µA

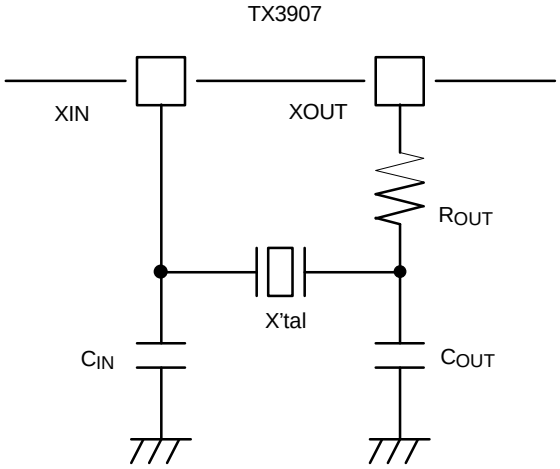
5.3.2 DC Characteristics of PCI Interface pins

(T_a = 0 to 70°C, V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V)

Parameter	Symbol	Conditions	MIN	MAX	Unit
Low-level input voltage	V_{ILP}		−0.5	V_{DD} × 0.3	V
High-level input voltage	V_{IHP}		V_{DD} × 0.5	V_{DD} + 0.5	V
Low-level output voltage	V_{OL}	I_{OUT} = 1500μA		V_{DD} × 0.1	V
High-level output voltage	V_{OH}	I_{OUT} = −500μA	V_{DD} × 0.9		V
Input leakage current	I_{IH}	0 < V_{IN} < V_{DD}	−10	10	μA
	I_{IL}		−10	10	μA

5.4 CRYSTAL OSILLATOR CHARACTERISTICS

5.4.1 Recommended Oscillator Conditions



Parameter	Symbol	Recommended Value	Unit
Crystal oscillator Frequency	f_{IN}	6.25 to 8.25	MHz
Output resistance	R_{OUT}	T.B.D.	kΩ
External Capacitor	C_{IN}, C_{OUT}	T.B.D.	pF
Crystal oscillator Rising time	t_r	5(1)	ns
Crystal oscillator Falling time	t_f	5(1)	ns

(1) Reference values. Refer to the latest data provided by the manufacturer of the crystal oscillator.

5.4.2 Electrical Characteristics

(T_a = 0 to 70°C, V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V)

Parameter	Symbol	Conditions	MIN	TYP.	MAX	Unit
Oscillation start time	t_{STA}	f = 6.25 to 8.25MHz	–	500	T.B.D.	μS

5.5 AC CHARACTERISTICS (OTHER THAN PCI INTERFACE PINS)

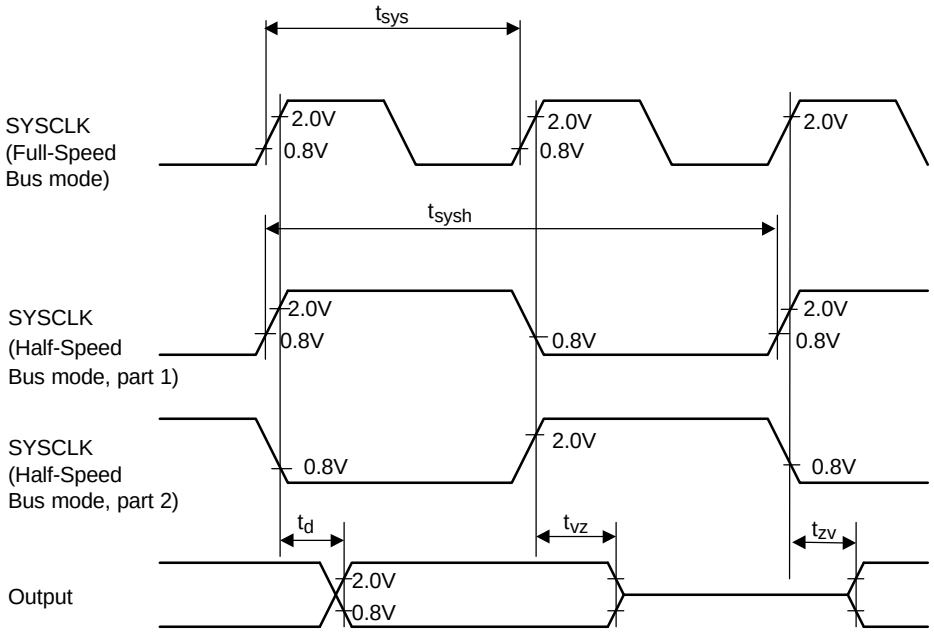
5.5.1 Table of AC Characteristics

(Unless otherwise specified, T_a = 0 to 70°C, V_{DD} = 3.3V ± 0.3V, V_{SS} = 0 V, C_L = 50pF)

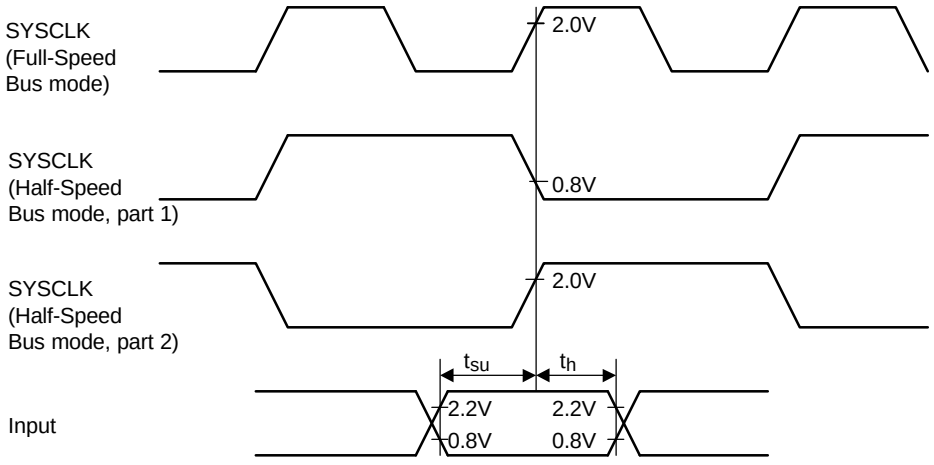
Parameter	Symbol	Decipation	MIN	MAX	Unit
t_{sys}	SYSCLK	Full speed bus mode	15	–	ns
t_{sysh}	SYSCLK	Half speed bus mode	30	–	ns
t_1	ROMA[23:2]	Output delay	–	10	ns
t_2	SPA[1:0]	Output delay	–	10	ns
t_3	CASBE[3:0]*	Output delay	–	10	ns
t_4	D[31:0]	Output delay	–	10	ns
t_5	D[31:0]	HI-Z → _Active delay	–	10	ns
t_6	D[31:0]	Active → Hi-Z Output delay	–	10	ns
t_9	LAST*/RD*	Output delay	–	10	ns
t_{10}	WR*	Output delay	–	10	ns
t_{11}	ACK*	Output delay	–	10	ns
t_{12}	DRAMA[12:0]	Output delay	–	10	ns
t_{15}	RAS[2:0][1:0]	Output delay	–	10	ns
t_{16}	WE*	Output delay	–	10	ns
t_{17}	SCS[1:0]*	Output delay	–	10	ns
t_{18}	CE[4:0]*	Output delay	–	10	ns
t_{19}	OE*	Output delay	–	10	ns
t_{20}	SWE*	Output delay	–	10	ns
t_{21}	LEAFA*, LEAFB*	Output delay	–	10	ns
t_{41}	D[31:0]	Input setup	8	–	ns
t_{42}	D[31:0]	Input hold	0	–	ns
t_{45}	NMI*	Input setup	10	–	ns
t_{46}	NMI*	Input hold	0	–	ns
t_{47}	INT[2:0]	Input setup	8	–	ns
t_{48}	INT[2:0]	Input hold	0	–	ns
t_{49}	ACK*	Input setup	8	–	ns
t_{50}	ACK*	Input hold	0	–	ns
t_{91}	RESET*	Reset period	60	–	t_{sys}
t_{92}	RESET*	Input hold	T.B.D.	–	ns
t_{STA}	ROMA[10]	Oscillation start time	–	T.B.D.	ns

5.5.2 Definition of AC Characteristics

- In Full-Speed Bus mode, all signals operate on the SYSCLK rising edge.
- In Half-Speed Bus mode, only the SCS access signals operate on the SYSCLK rising edge. Other access signals operate on the SYSCLK rising or falling edge.



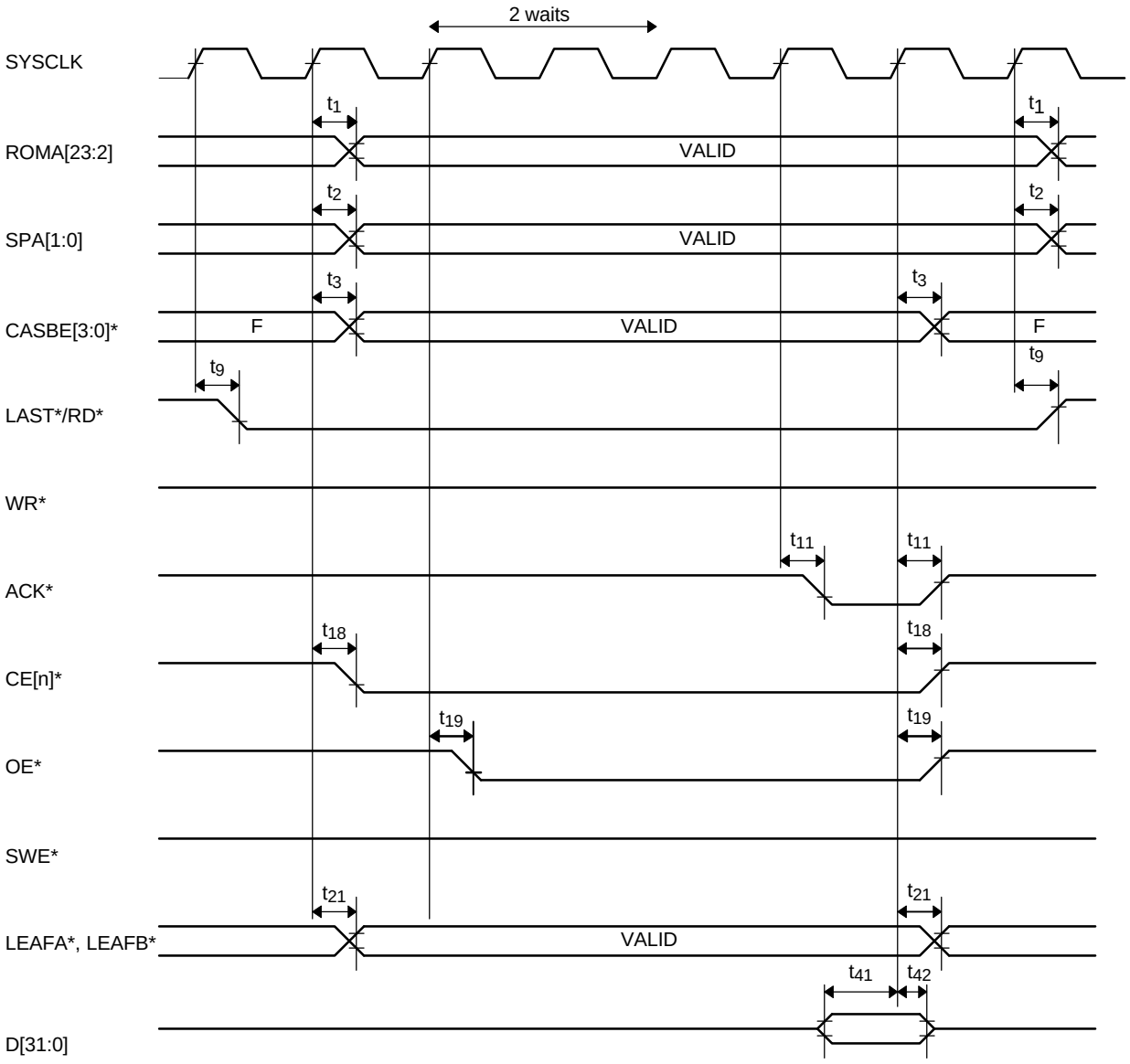
t_d: Output delay t_{vz}: Active → Hi-Z delay t_{zv}: Hi-Z → active delay



t_{su}: Input setup t_h: Input hold

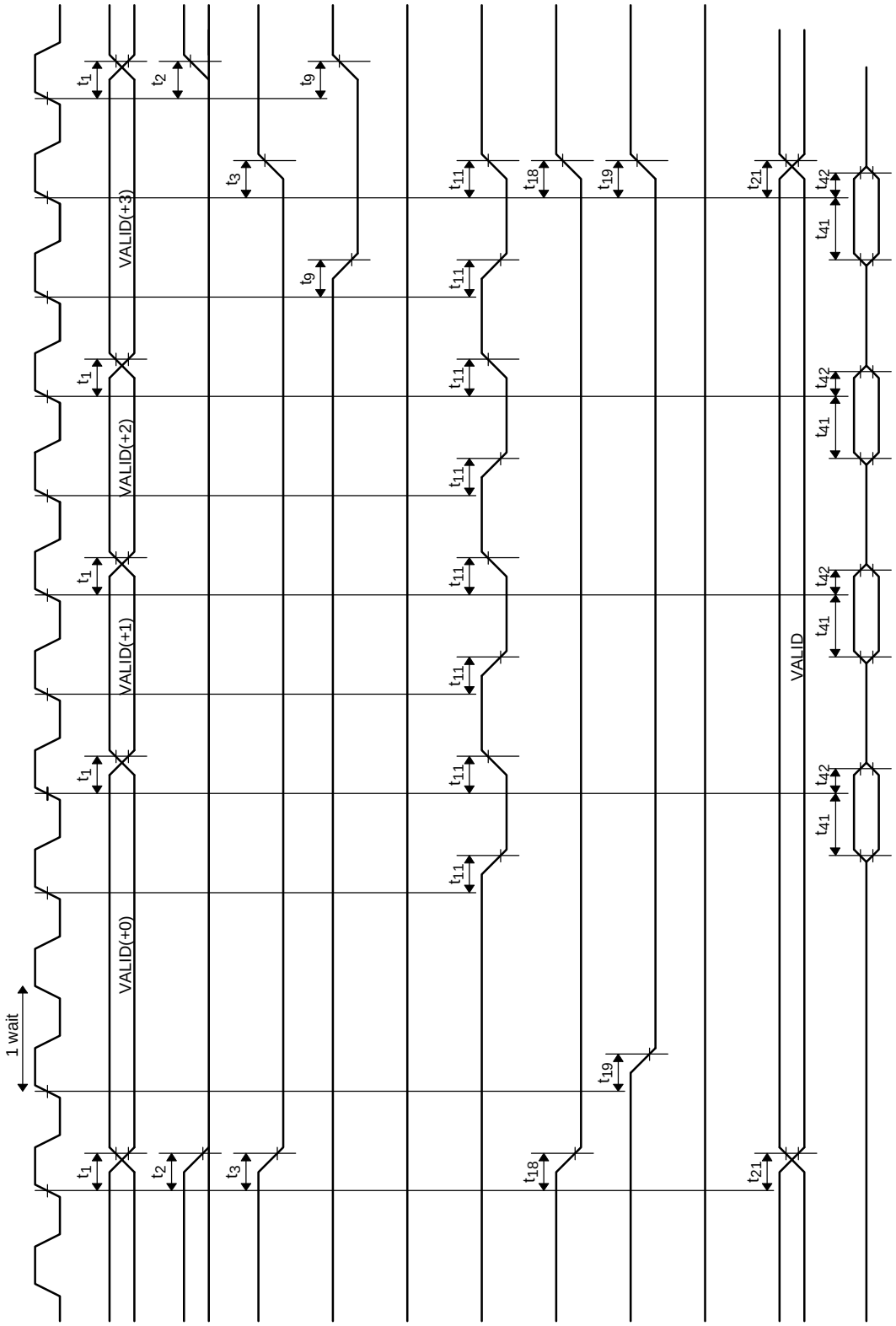
5.5.3 Timing Diagram

- ROM read (Full-Speed Bus mode, single read, 2 waits)

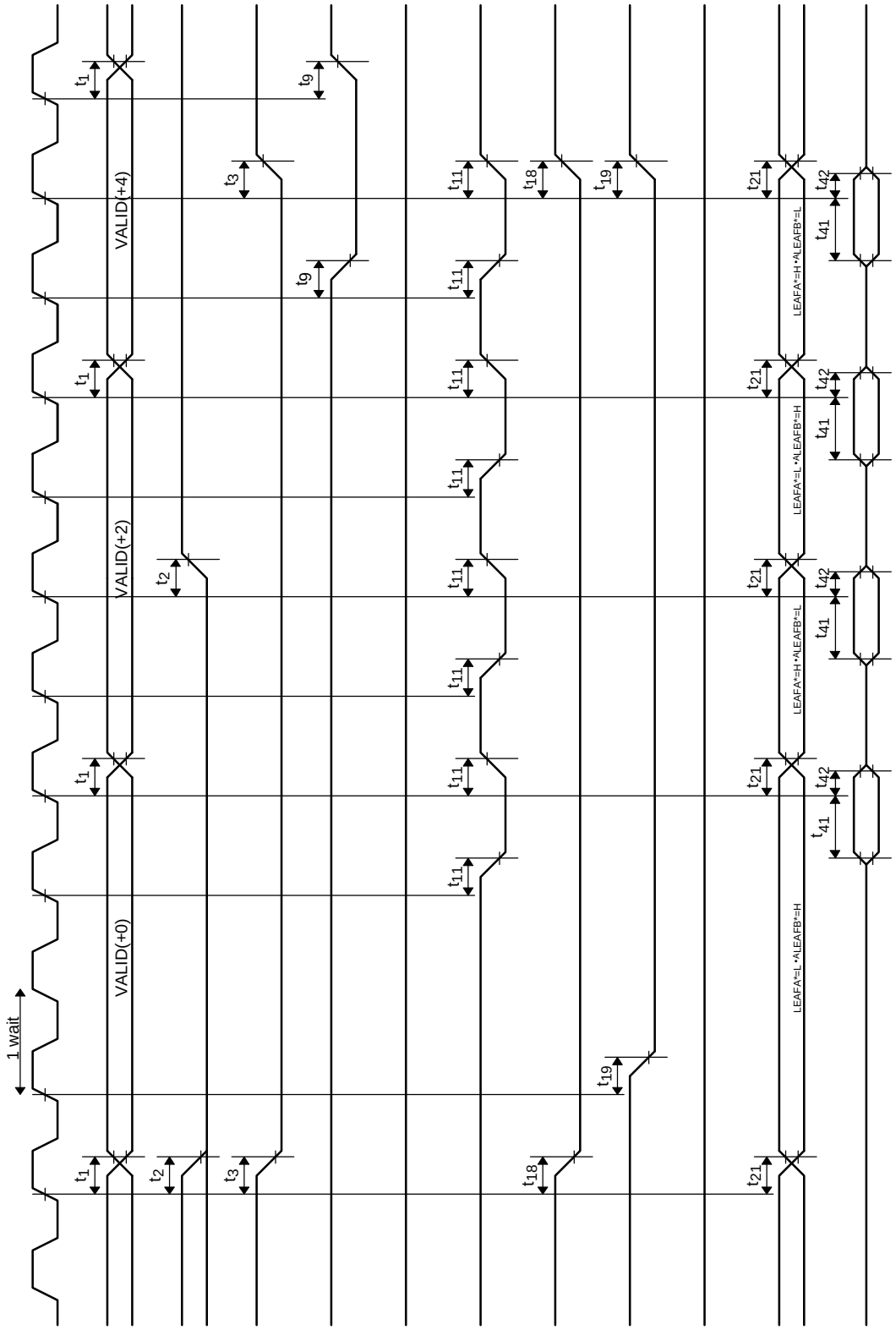


TENTATIVE

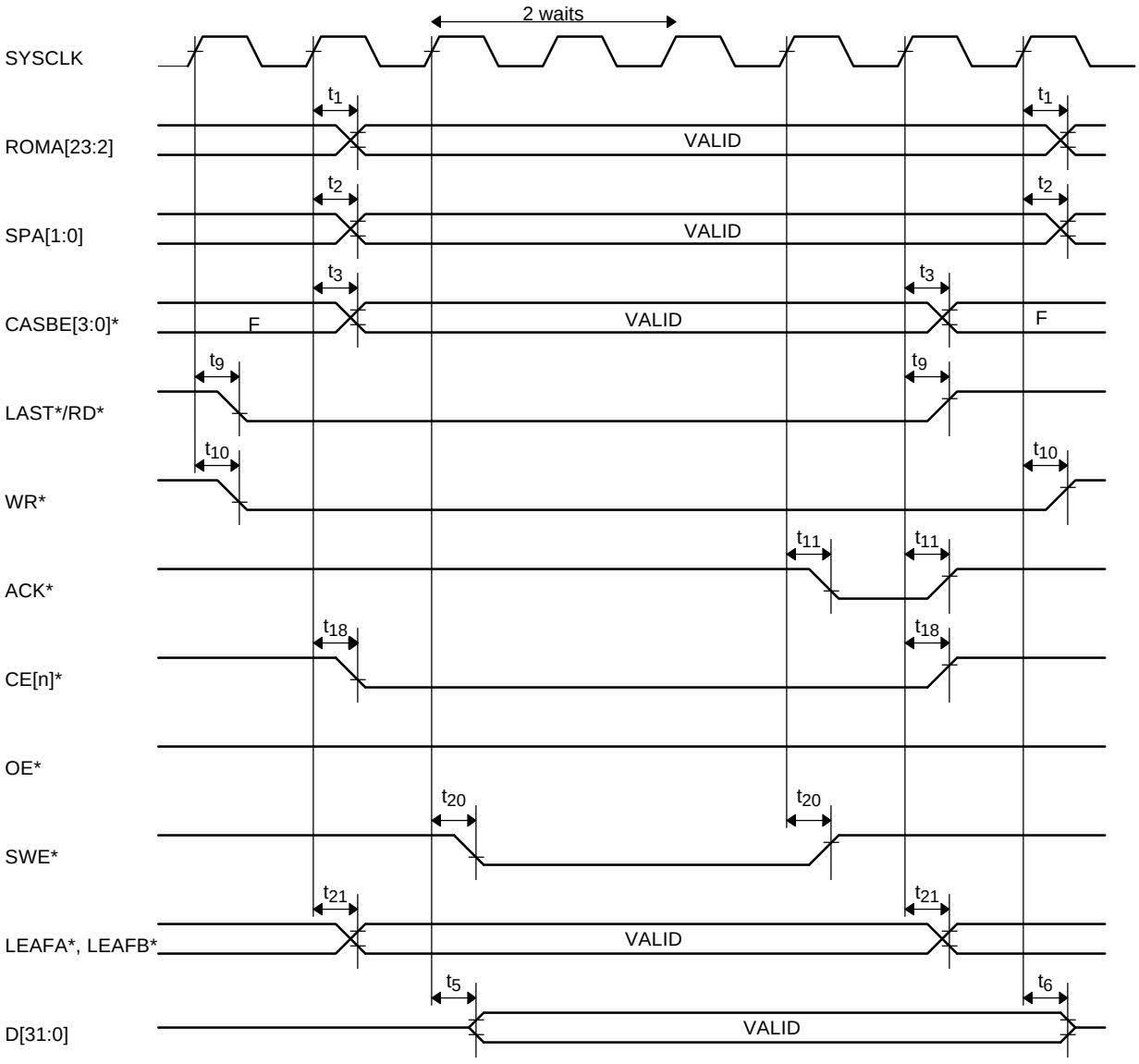
- ROM read (Full-Speed Bus mode, page ROM, burst read, 1-0 waits)



- ROM read (Full-Speed Bus mode, page ROM, burst read, interleave, 1-0 waits)

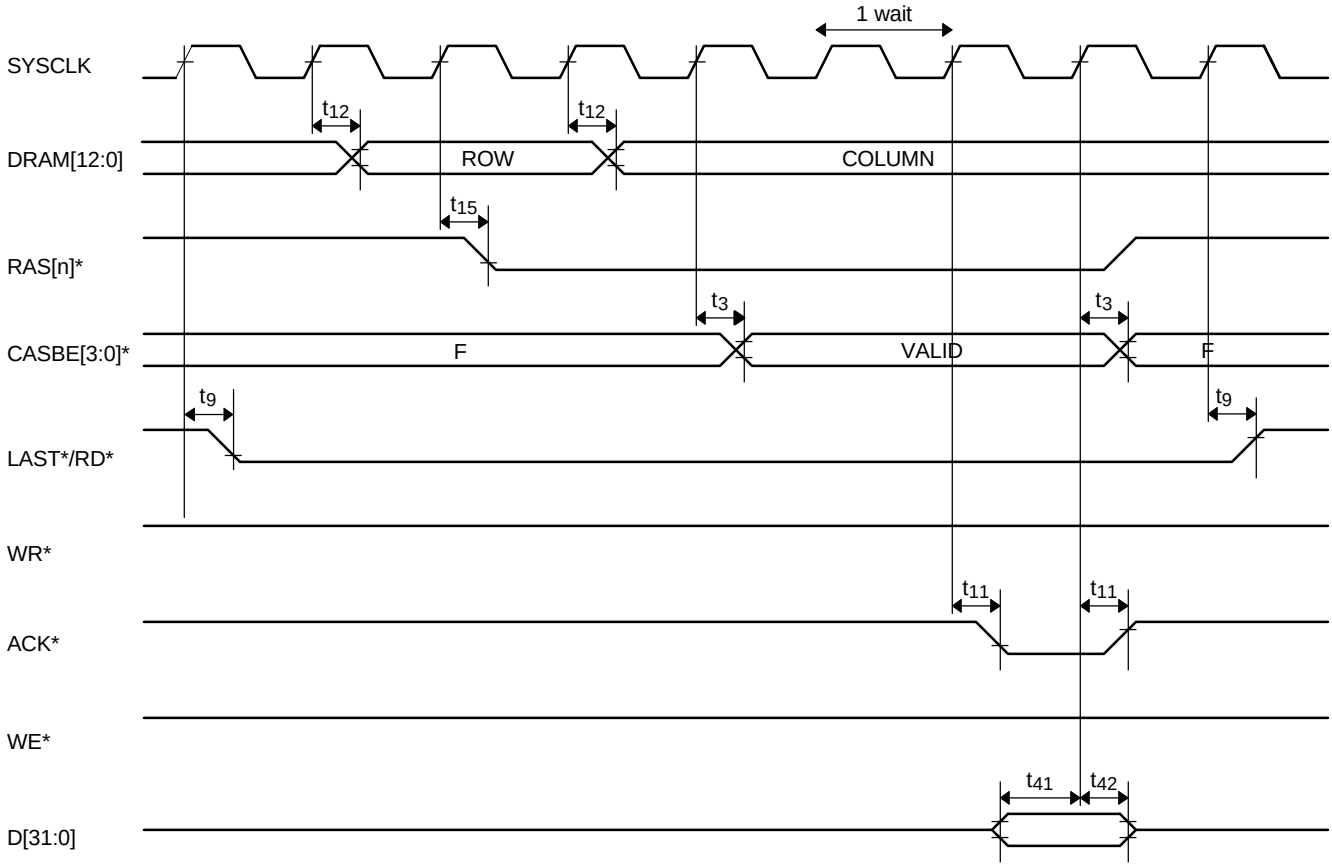


- SRAM write (Full-Speed Bus mode, single write, 2 waits)

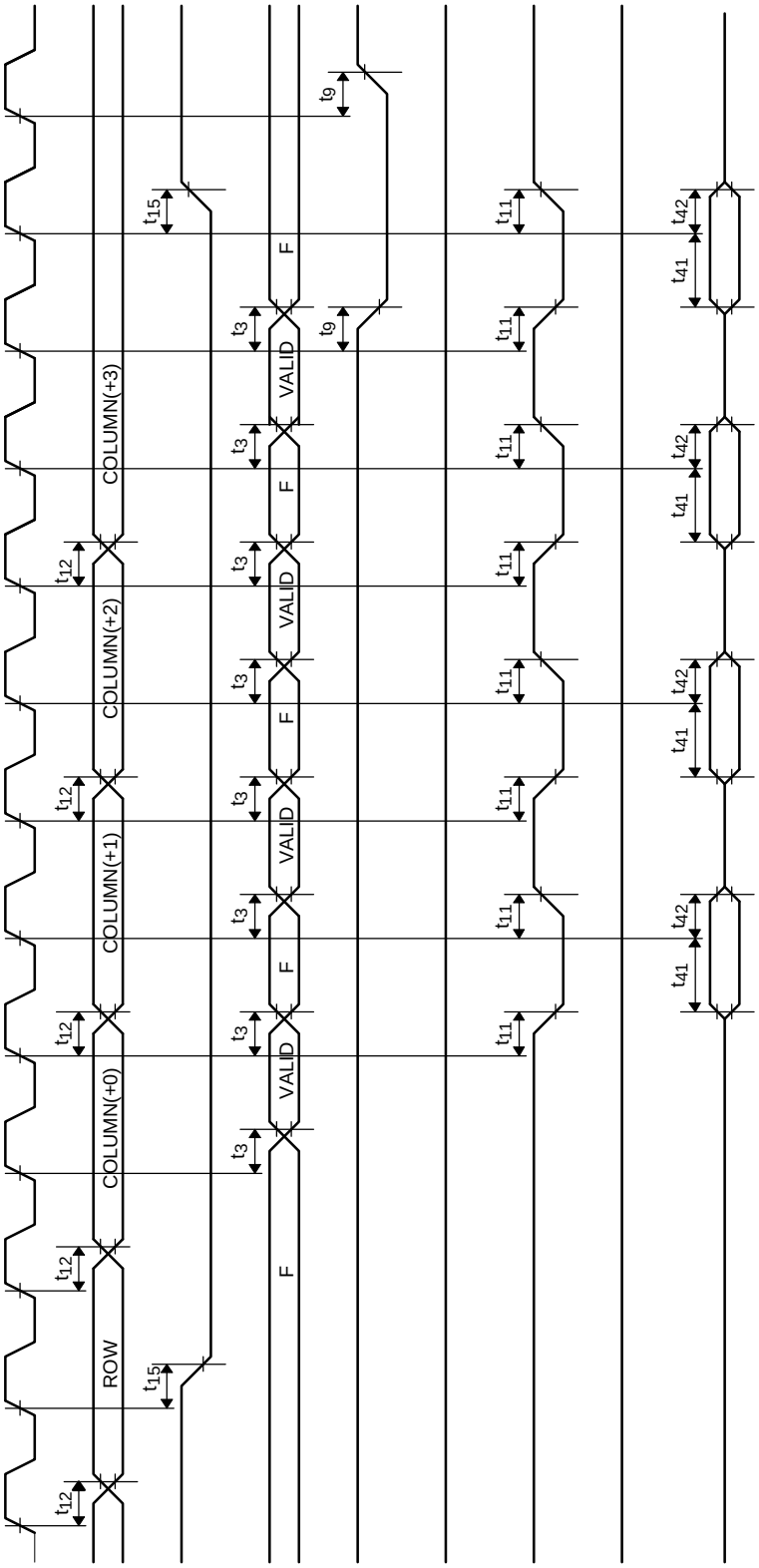


TENTATIVE

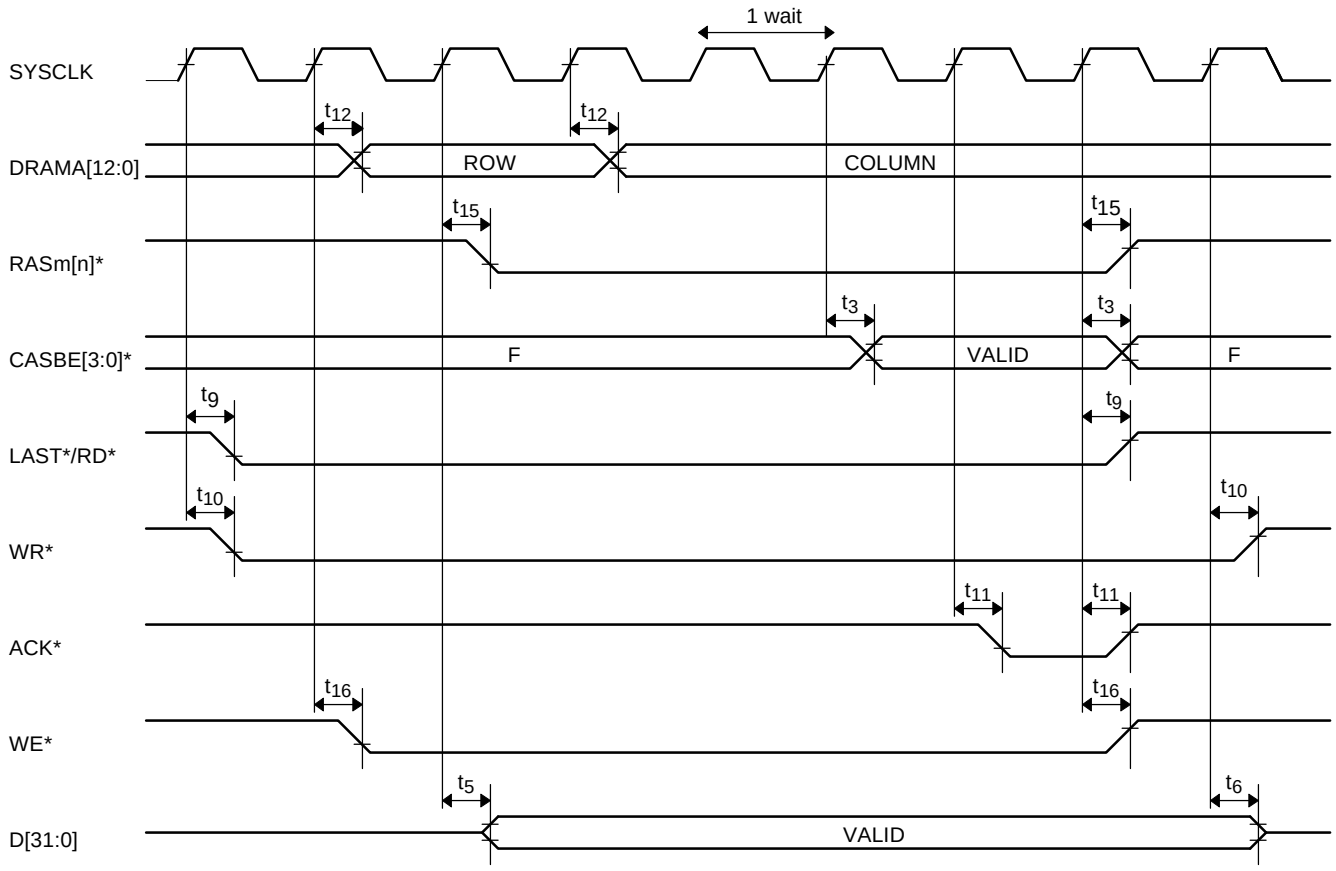
- DRAM read (Full-Speed Bus mode, single read, 1 wait)



- DRAM read (Full-Speed Bus mode, EDO burst, 0-0 wait)

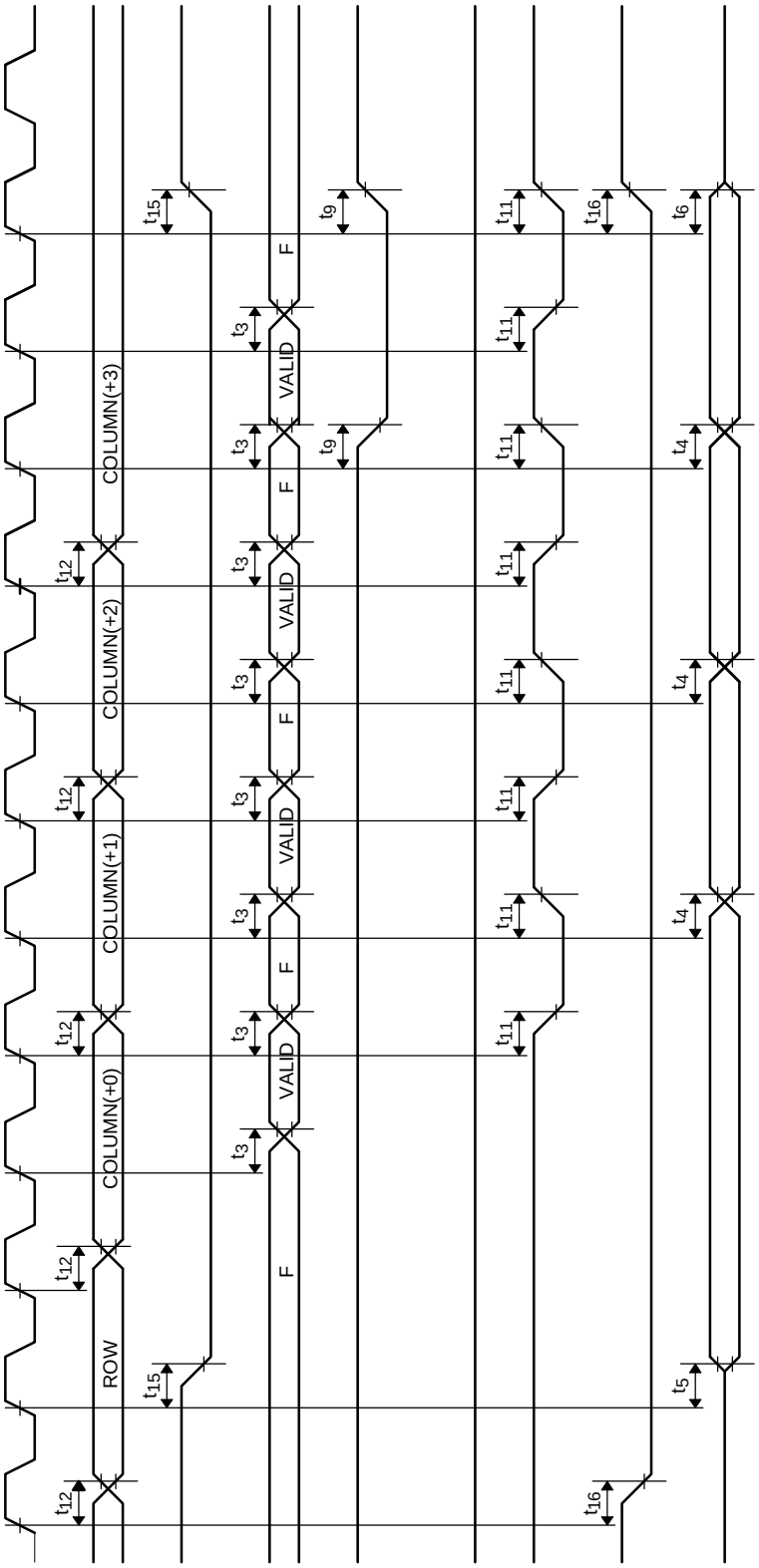


- DRAM write (Full-Speed Bus mode, single write, 1 wait)

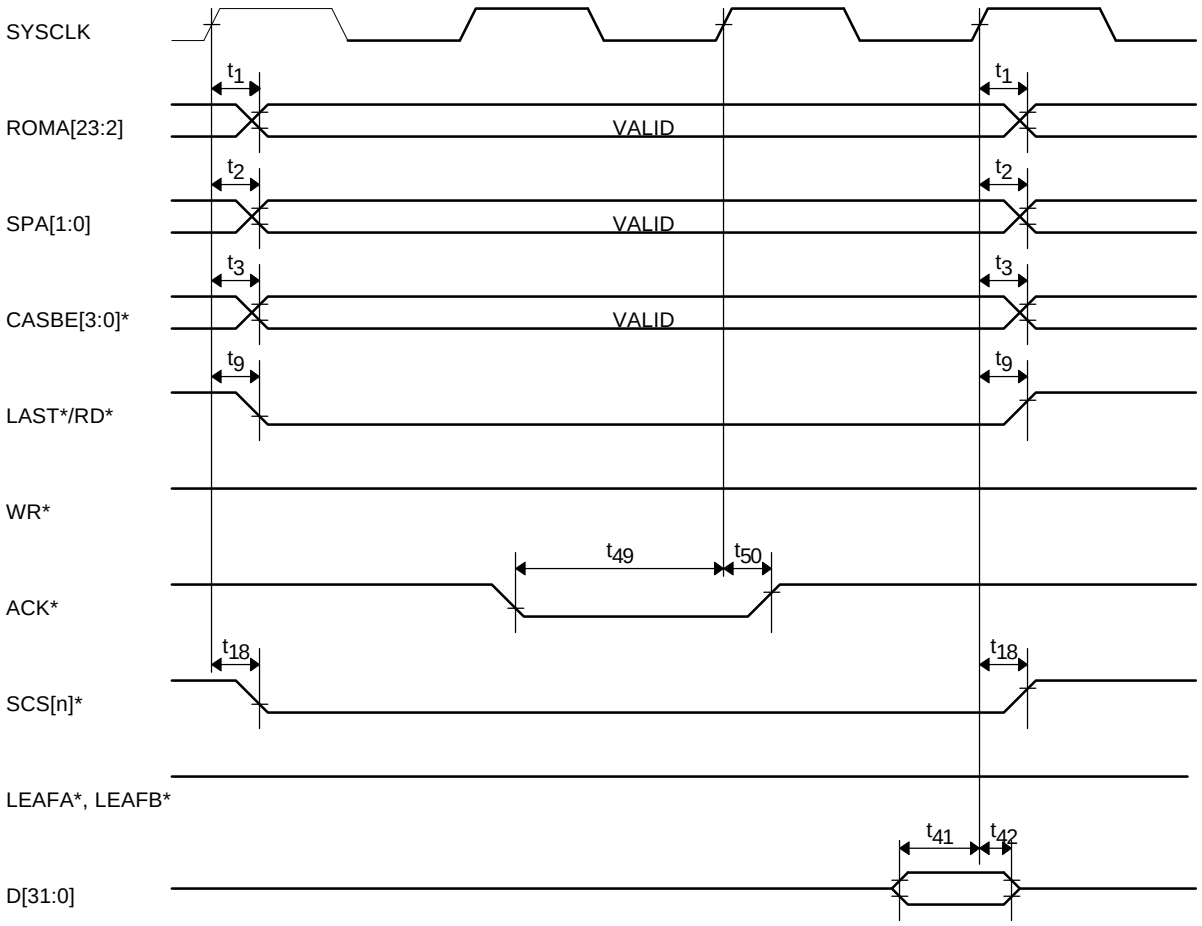


TENTATIVE

- DRAM write (Full-Speed Bus mode, EDO burst, 0-0 wait)

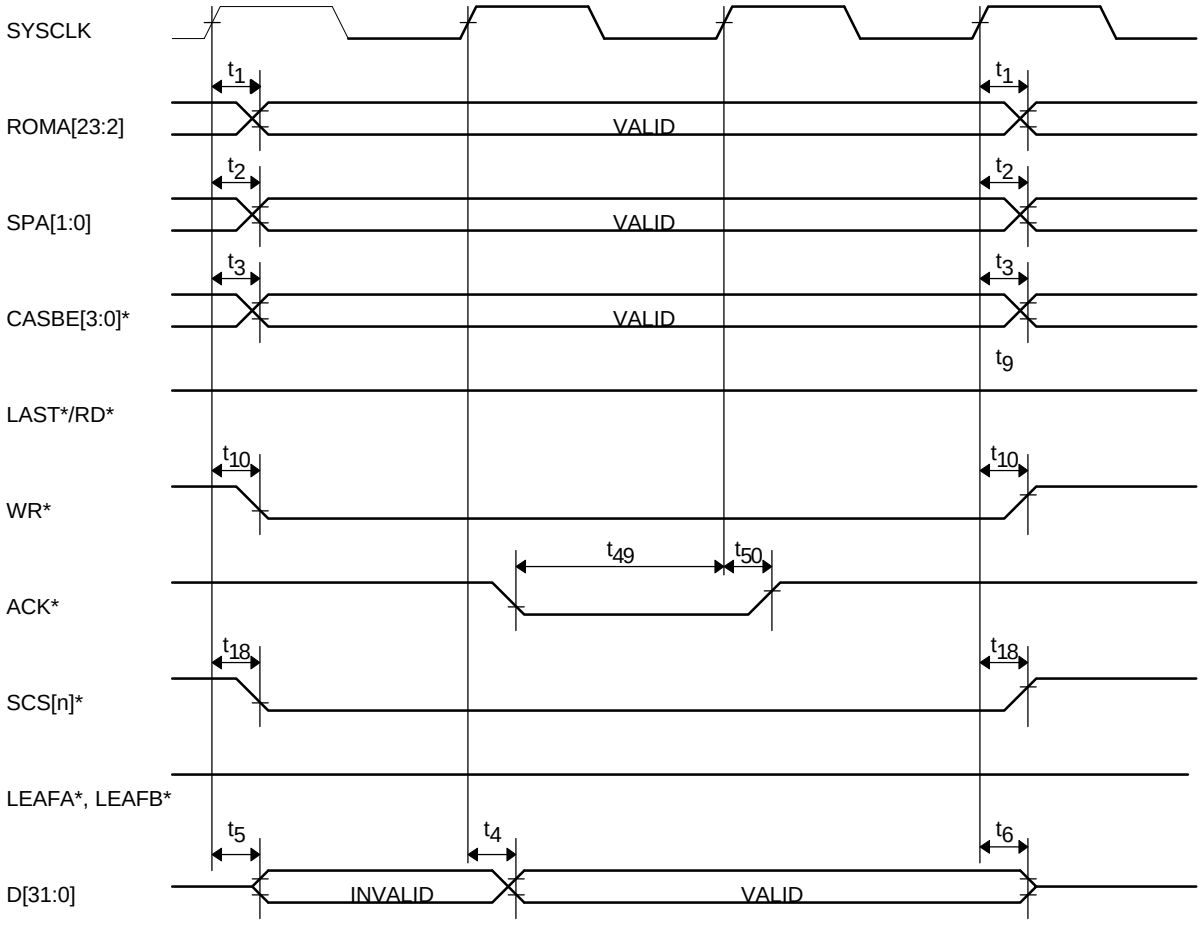


- SCS read (Half-Speed Bus Mode, single read, external ACK*)

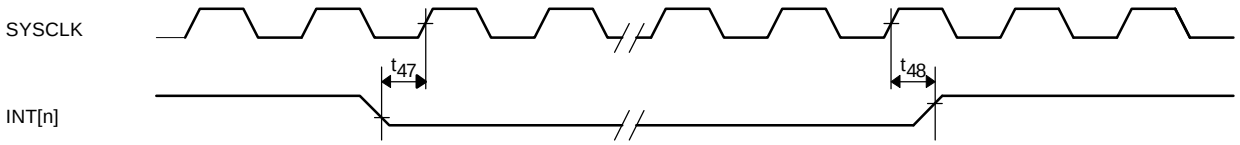


TENTATIVE

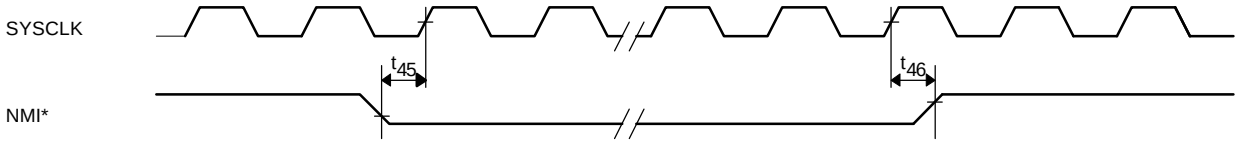
- SCS write (Half-Speed Bus Mode, single write, external ACK*)



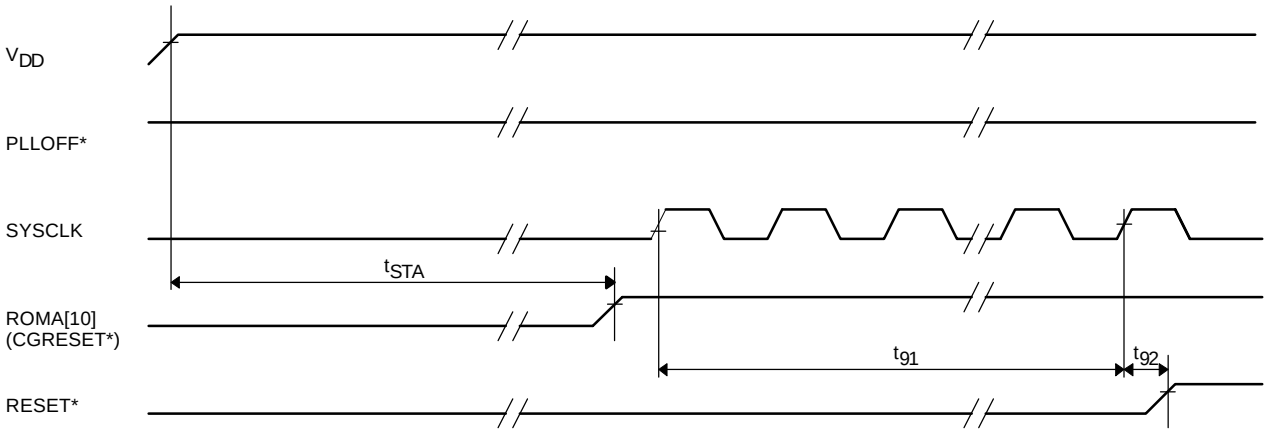
- Interrupt



- NMI*



- Power-on reset



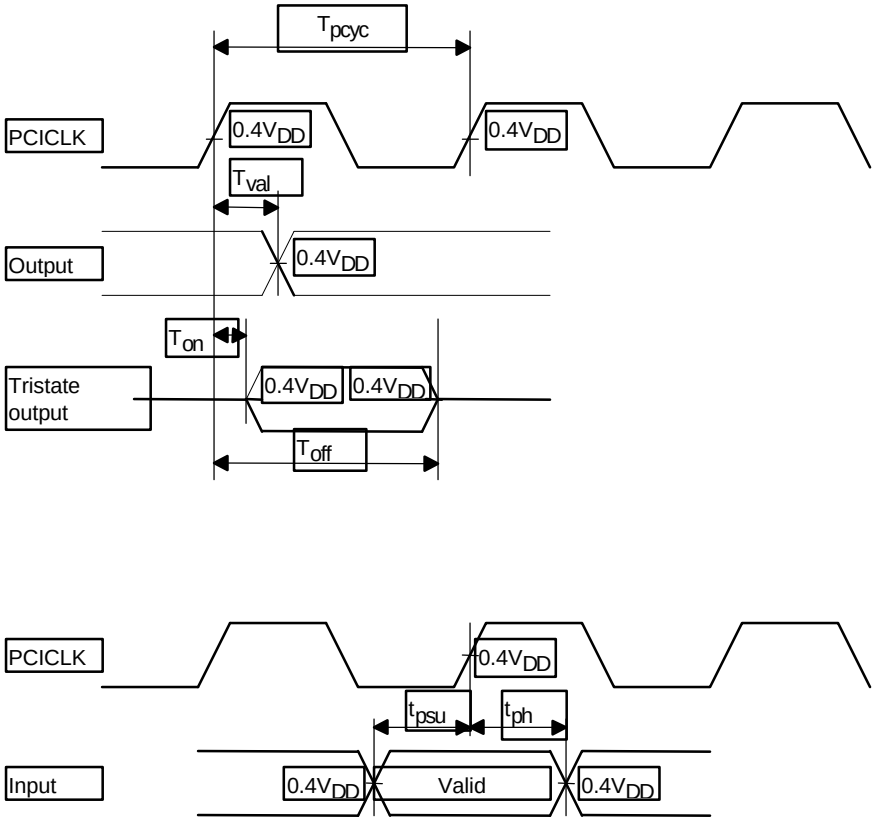
5.6 AC CHARACTERISTICS (PCI INTERFACE PIN)

5.6.1 AC Characteristics Table

(Unless otherwise specified, T_a = 0 to 70 (C, V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V, C_L = 10 pF)

Parameter	Description	MIN	MAX	Unit
t_{pcyc}	PCICLK cycle time	30	–	ns
t_{val}	Valid output delay from PCICLK (bus connection)	2	11	ns
t_{val}(ptp)	Valid output delay from PCICLK (p-p connection)	2	12	ns
t_{on}	Hi-Z → active delay	2	–	ns
t_{off}	Active → Hi-Z delay	–	28	ns
t_{psu}	Input setup for PCICLK (bus connection)	7	–	ns
t_{psu}(REQ*)	Input setup for PCICLK (REQ*)	12	–	ns
t_{ph}	Hold for PCICLK	0	–	ns

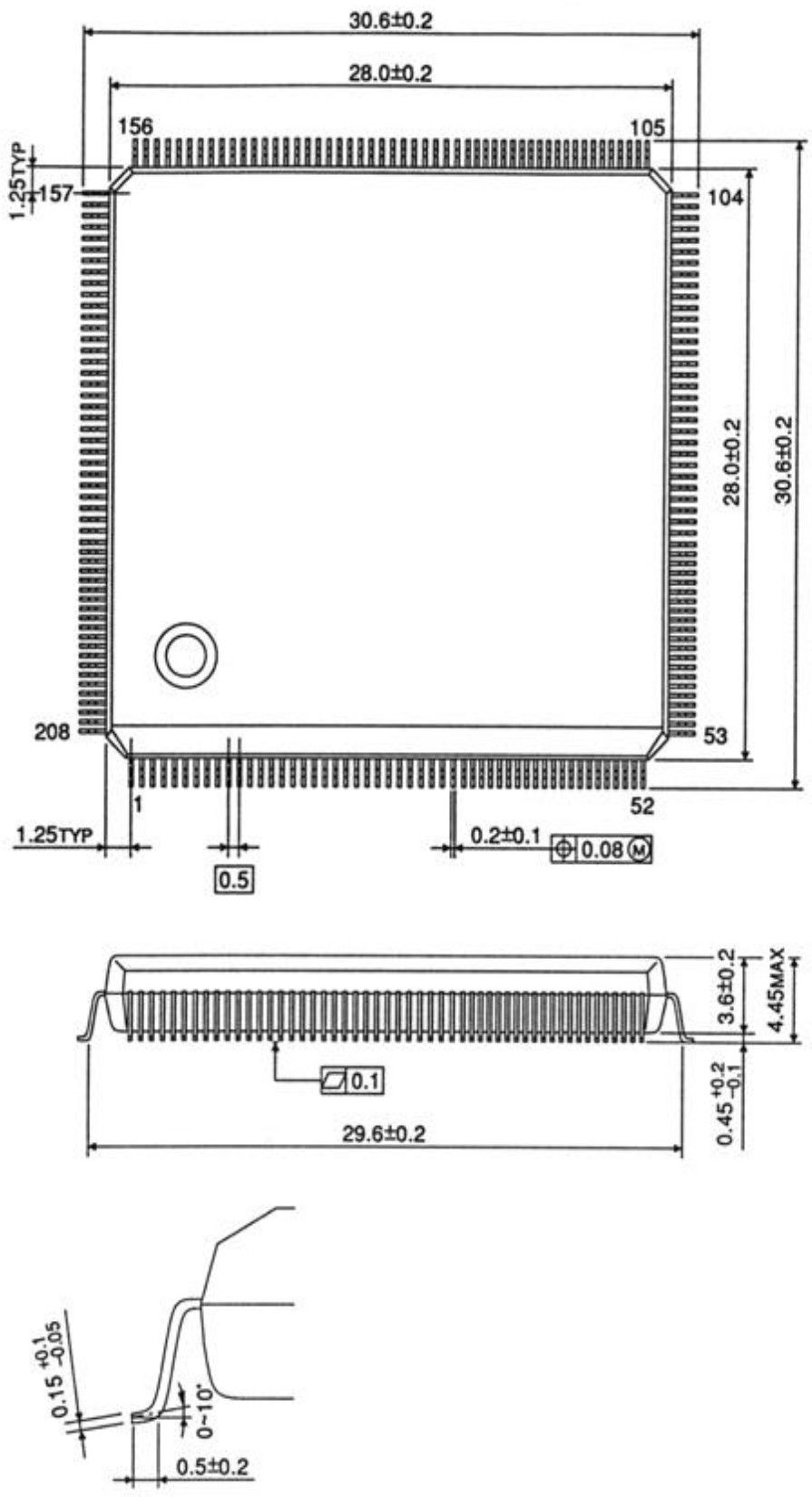
5.6.2 Definition of AC Characteristics



TENTATIVE

6. PACKAGE DIMENSIONS

QFP208-P-2828-0.50 Unit: mm



TENTATIVE