

8834750 TAG SEMICONDUCTORS LTD

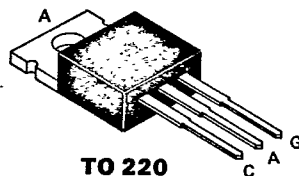
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TAG SEMICONDUCTORS LTD

**S0805BH -
S0805NH SCR'S****8.0 A 200-800 V <5 mA**

The S0805 series silicon controlled rectifiers are high performance glass passivated PNP devices. These parts are intended for general purpose high voltage applications where moderate gate sensitivity is required.

**Absolute Maximum Ratings** $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Part Nr.	Symbol	Min.	Max.	Unit	Test Conditions
Repetitive Peak Off State Voltage	S0805BH	V_{DRM} V_{RRM}	200		V	$T_j = -40^\circ\text{C}$ to 125°C $R_{GK} = 1\text{K}\Omega$
	S0805DH		400		V	
	S0805MH		600		V	
	S0805NH		800		V	
On-State Current		$I_T(RMS)$	8.0		A	All Conduction Angles $T_C = 85^\circ\text{C}$
Average On-State Current		$I_T(AV)$	5.1		A	Half Cycle, $\Theta = 180^\circ$, $T_C = 85^\circ\text{C}$
Nonrept. On-State Current		I_{TSM}	88		A	Half Cycle, 60 Hz
Nonrept. On-State Current		I_{TSM}	80		A	Half Cycle, 50 Hz
Fusing Current		I^2t	32		A^2s	$t = 10\text{ ms}$, Half Cycle
Peak Gate Current		I_{GM}	2		A	$10\mu\text{s}$ max.
Peak Gate Dissipation		P_{GM}	5		W	$10\mu\text{s}$ max.
Gate Dissipation		$P_{G(AV)}$	0.5		W	20 ms max.
Operating Temperature		T_j	-40	125	$^\circ\text{C}$	
Storage Temperature		T_{stg}	-40	125	$^\circ\text{C}$	
Soldering Temperature		T_{sld}		250	$^\circ\text{C}$	1.6 mm from case, 10 s max.

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Min.	Max.	Unit	Test Conditions
Off-State Leakage Current	I_{DRM}/I_{RRM}	0.5		mA	@ $V_{DRM} + V_{RRM}$, $R_{GK} = 1\text{K}\Omega$, $T_j = 125^\circ\text{C}$
Off-State Leakage Current	I_{DRM}/I_{RRM}	5		μA	@ $V_{DRM} + V_{RRM}$, $R_{GK} = 1\text{K}\Omega$, $T_j = 25^\circ\text{C}$
On-State Voltage	V_T	1.95		V	at $I_T = 16\text{ A}$, $T_j = 25^\circ\text{C}$
On-State Threshold Voltage	$V_{T(TO)}$	1.05		V	$T_j = 125^\circ\text{C}$
On-State Slope Resistance	r_T	65		m Ω	$T_j = 125^\circ\text{C}$
Gate Trigger Current	I_{GT}	5		mA	$V_D = 7\text{ V}$
Gate Trigger Voltage	V_{GT}	2.0		V	$V_D = 7\text{ V}$
Holding Current	I_H	25		mA	$R_{GK} = 1\text{K}\Omega$
Latching Current	I_L	50		mA	$R_{GK} = 1\text{K}\Omega$
Critical Rate of Voltage Rise	dv/dt	50		V/ μs	$V_D = .67 \times V_{DRM}$, $R_{GK} = 1\text{K}\Omega$, $T_j = 125^\circ\text{C}$
Critical Rate of Current Rise	di/dt	100		A/ μs	$I_G = 25\text{ mA}$, $di_G/dt = 0.25\text{ A}/\mu\text{s}$, $T_j = 125^\circ\text{C}$
Gate Controlled Delay Time	t_{gd}	500		ns	$I_G = 25\text{ mA}$, $di_G/dt = 0.25\text{ A}/\mu\text{s}$
Commutated Turn-Off Time	t_q	50		μs	$T_C = 85^\circ\text{C}$, $V_D = .67 \times V_{DRM}$, $V_R = 35\text{ V}$, $I_T = I_T(AV)$
Thermal Resistance junc. to case	$R_{\theta jc}$	4		K/W	
Thermal Resistance junc. to amb.	$R_{\theta ja}$	60		K/W	

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