CMOS 8-Bit Microcontroller

TMP88CP76F, TMP88CS76F

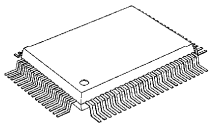
The TMP88CP76 and TMP88CS76 are the high speed and high performance 8-bit single chip microcomputers. These MCU contain VFT (Vacuum Fluorescent Tube) driver, serial interface, 8-bit AD converter and multi-function timer/counter on a chip.

Part No.	ROM	RAM	Package	OTP version
TMP88CP76F	48K × 8bit + 256 × 8bit	1K × 8-bit	P-QFP80-1420-0.80B	TMP88PS76F
TMP88CS76F	64K × 8bit + 256 × 8bit	2K × 8-bit		

Features

- ◆ 8-bit single-chip microcomputer TLCS-870/X series microcomputer
- ◆ interrupt sources: 16 (3 external, 13 internal)
- ◆ I/O ports: 68 pins
- ◆ Three 16-bit Timer/Counters
  - TC1: Timer
  - TC2: Timer, Event counter, Window modes
  - ETC1: Timer, Event counter, Window mode
    Minimum resolution: 500 μs at 8 MHz
    Two capture inputs (edge-selectable)
    One compare outputs
    (High/Low/Toggle/Steady output modes)
- ◆ 8-bit Timer/Counter
  - TC4: Timer, Event counter, PWM output,
    Programmable divider output modes
- ◆ Time Base Timer (Interrupt frequency: 1 Hz to 16384 Hz)
- ◆ Divider output function (frequency: 1 kHz to 8 kHz)

P-QFP80-1420-0.80B



TMP88CP76
TMP88CS76
TMP88PS76

000707EBA1

◆ Watchdog Timer
- Interrupt source/reset output (programmable)

◆ 8-bit Serial Interfaces
- With 8bytes transmits/receive data buffer
- Internal/external serial clock, and 4/8-bit mode

◆ Serial bus Interface
- I^2C bus, 8-Bit SIO Modes

◆ 8-bit successive approximate type AD converter with sample and hold
- 12 analog inputs
- Conversion time: 23 μs at 8 MHz

◆ Vacuum Fluorescent Tube Driver (automatic display)
- Programmable grid scan
- High breakdown voltage ports (max.40 V × 40 bits)

◆ Dual clock operation
- Single/Dual-clock mode

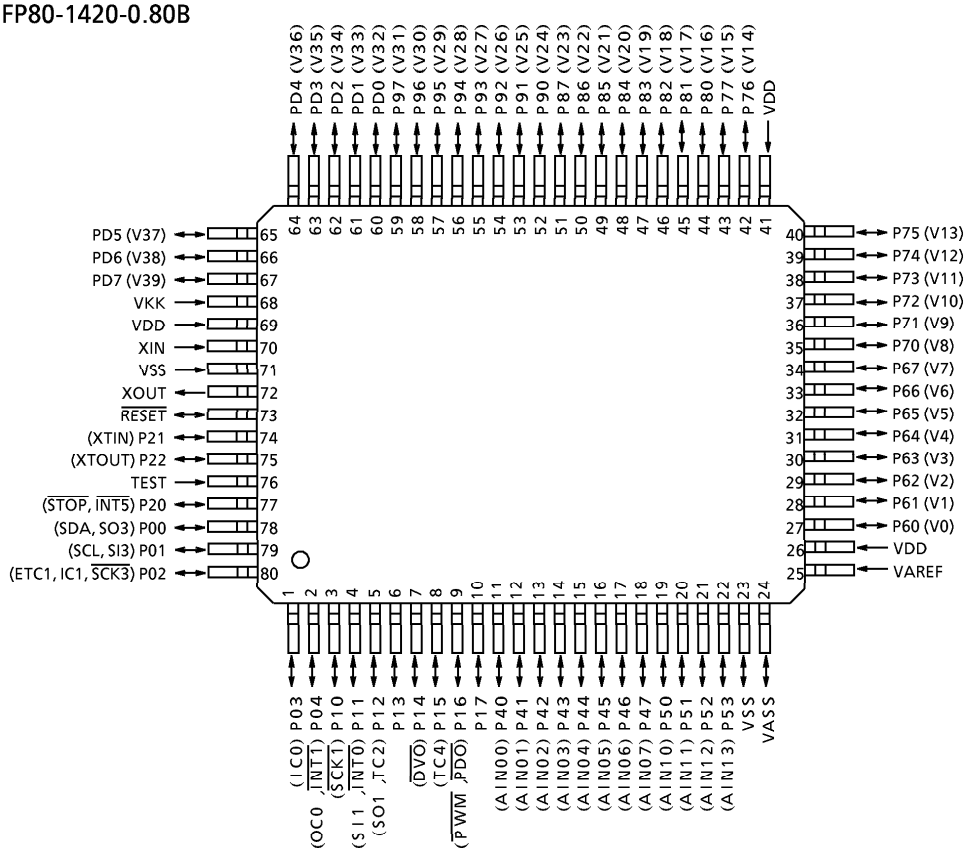
◆ Five Power saving operating modes
- STOP mode: Oscillation stops. Battery/Capacitor back-up.Port output hold/High-impedance.
- SLOW mode: Low power consumption operation using low-frequency clock (32.768 kHz)
- IDLE1 mode: CPU stops, and Peripherals operate using high-frequency clock. Release by interrupts.
- IDLE2 mode: CPU stops, and Peripherals operate using high-and low-frequency clock. Release by interruput.
- SLEEP mode: CPU stops, and Peripherals operate using low-frequency clock. Release by interrupts.

◆ Wide operating voltage: 4.5 to 5.5 V at 12.5 MHz / 32.768 kHz, 2.7 to 5.5 V at 32.768 kHz

◆ Emulation Pod: BM87CP77F0A

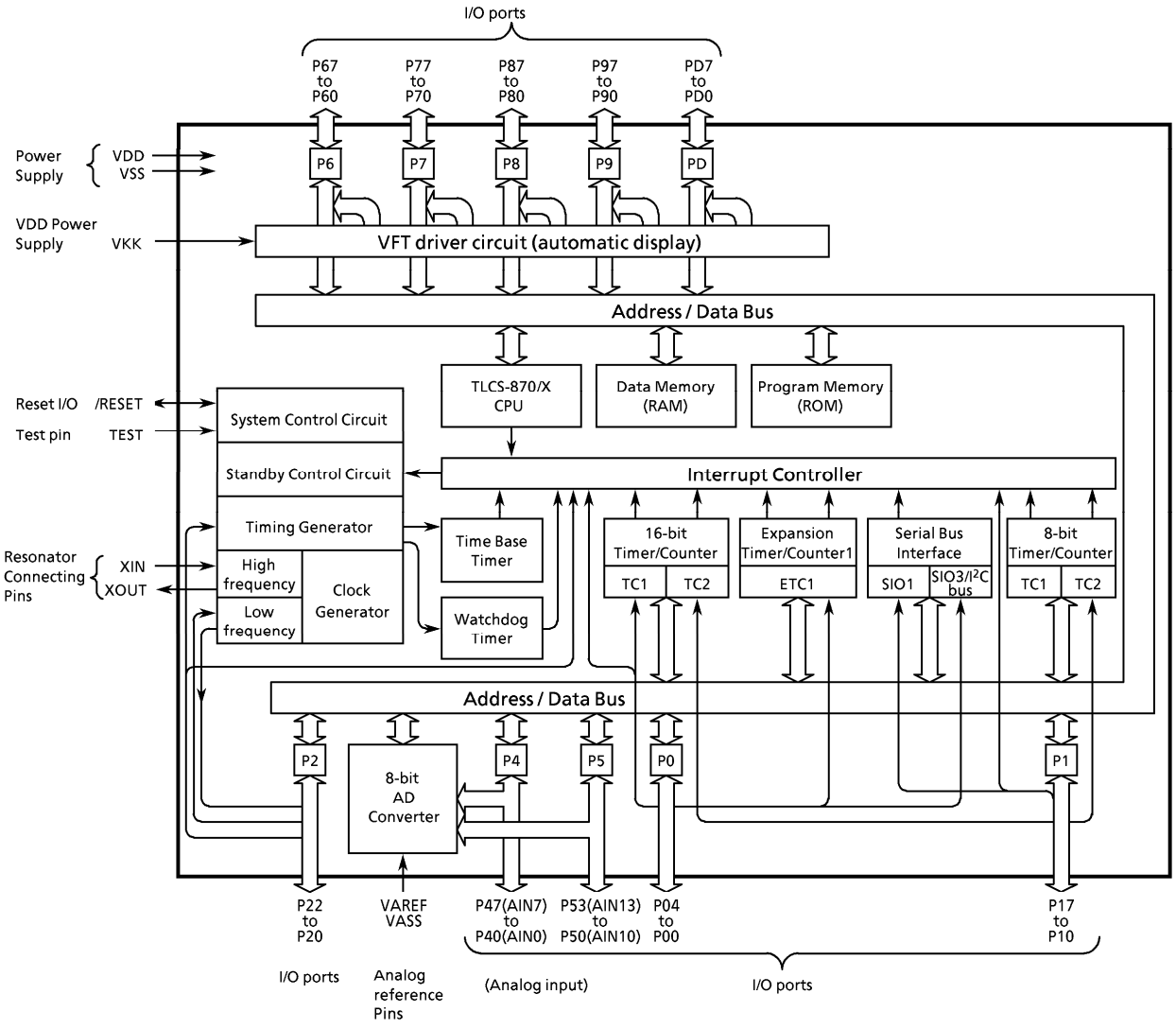
Pin Assignments (Top View)

P-QFP80-1420-0.80B



Note: All VDDs should be connected externally for keeping the same voltage level.

Block Diagram



Pin Function

Pin Name	I/O	Function	
P04 (OC0,INT1)	I/O (I/O)	5-bit input / output port with latch. When used as input port, multi function timer/counter, external interrupt input, serial bus interface, the latch must be set to "1".	Expansion Timer/Counter compare output 0 or External interrupt input 1
P03 (IC0)	I/O (input)		Expansion Timer/Counter capture input 0
P02 (IC1,ETC1,$\overline{SCK3}$)	I/O (I/O)		Expansion Timer/Counter capture input 1 or Expansion Timer/Counter 1 input or SIO 3 serial clock input/output
P01(SCL,SI3)	I/O (I/O)		I^2C bus serial clock input/output or SIO3 serial data input
P00(SDA,SO3)	I/O (I/O)		I^2C bus serial data input/output or SIO3 serial data output
P17	I/O	8-bit programmable input/output ports (tris-tate). Each bit of this port can be individually configured as an input or an output under software control. When used as serial interface, external interrupt input, timer/ counter input, the input mode is configured. When used as divider output, timer/ counter output, serial data output, the latch must be set to "1" and the output mode is configured.	
P16 ($\overline{PWM}$,$\overline{PDO}$)	I/O (output)		8-bit PWM output or 8-bit programmable divider output
P15 (TC4)	I/O (input)		Timer/Counter 4 input
P14 ($\overline{DVO}$)	I/O (output)		Divider output
P13	I/O		
P12 (SO1, TC2)	I/O (I/O)		SIO1 serial data output or Timer/Counter 2 input
P11 (SI1, $\overline{INT0}$)	I/O (input)		SIO1 serial data input or External interrupt 0 input
P10 ($\overline{SCK1}$)	I/O (I/O)		SIO1 serial clock input/output
P22 (XTOUT)	I/O (I/O)	3-bit input/output port with latch. When used as input port, external interrupt input, STOP mode release signal input, the input mode is configured.	Resonator connectiong pins (32.768kHz). For inputting external clock, XTIN is used and XOUT is opened.
P21 (XTIN)	I/O (input)		
P20 ($\overline{INT5}$, $\overline{STOP}$)	I/O (input)		External interrupt input 5 or STOP mode release signal input
P47 (AIN07) to P40 (AIN00)	I/O (input)	8-bit programmable input/output ports (tri-state). Each bit of this port can be individually configured as an input or an output under software control. When used as analog input, the input mode is configured.	AD converter analog inputs
P53 (AIN13) to P50 (AIN10)	I/O (input)	4-bit programmable input/output ports (tri-state). Each bit of this port can be individually configured as an input or an output under software control. When used as analog input, the input mode is configured.	AD converter analog inputs
P67 (V7) to P60 (V0)	I/O (output)	Six 8-bit high breakdown voltage output ports with the latch. When used as a VFT driver output, the latch must be cleared to "0".	VFT driver output
P77 (V15) to P70 (V8)	I/O (output)		
P87 (V23) to P80 (V16)	I/O (output)		
P97 (V31) to P90 (V24)	I/O (output)		
PD7 (V39) to PD0 (V31)	I/O (output)		
XIN,XOUT	Input, output	Resonator connecting pins for high-frequency clock. For inputting external clock, XIN is used and XOUT is opened.	
RESET	I/O	Reset signal input or watchdog timer output/address-trap-reset output /sistem-clock-reset outputed.	
TEST	Input	Test pin for out-going test.Be tied to low.	
VDD,VSS (Note)	Power Suppry	+ 5 V, 0 V (GND)	
VKK		VFT driver power supply	
VAREF,VASS		Analog reference voltae inputs (High, Low)	

Note: All VDDs should be connected externally for keeping the same voltage level.

Operational Description

1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, an interrupt controller, and a watchdog timer. This section provides a description of the CPU core, the program memory (ROM), the data memory (RAM), and the reset circuit.

1.1 Memory Address Map

TLCS-870/X Series, the memory is organized 4 address spaces (ROM, RAM, SFR, and DBR). Figure 1-1 shows the memory address maps of the TMP88CP76/S76. It uses a memory mapped I/O system, and all I/O registers are mapped in the SFR/DBR address spaces. There are 16 banks of general-purpose registers.

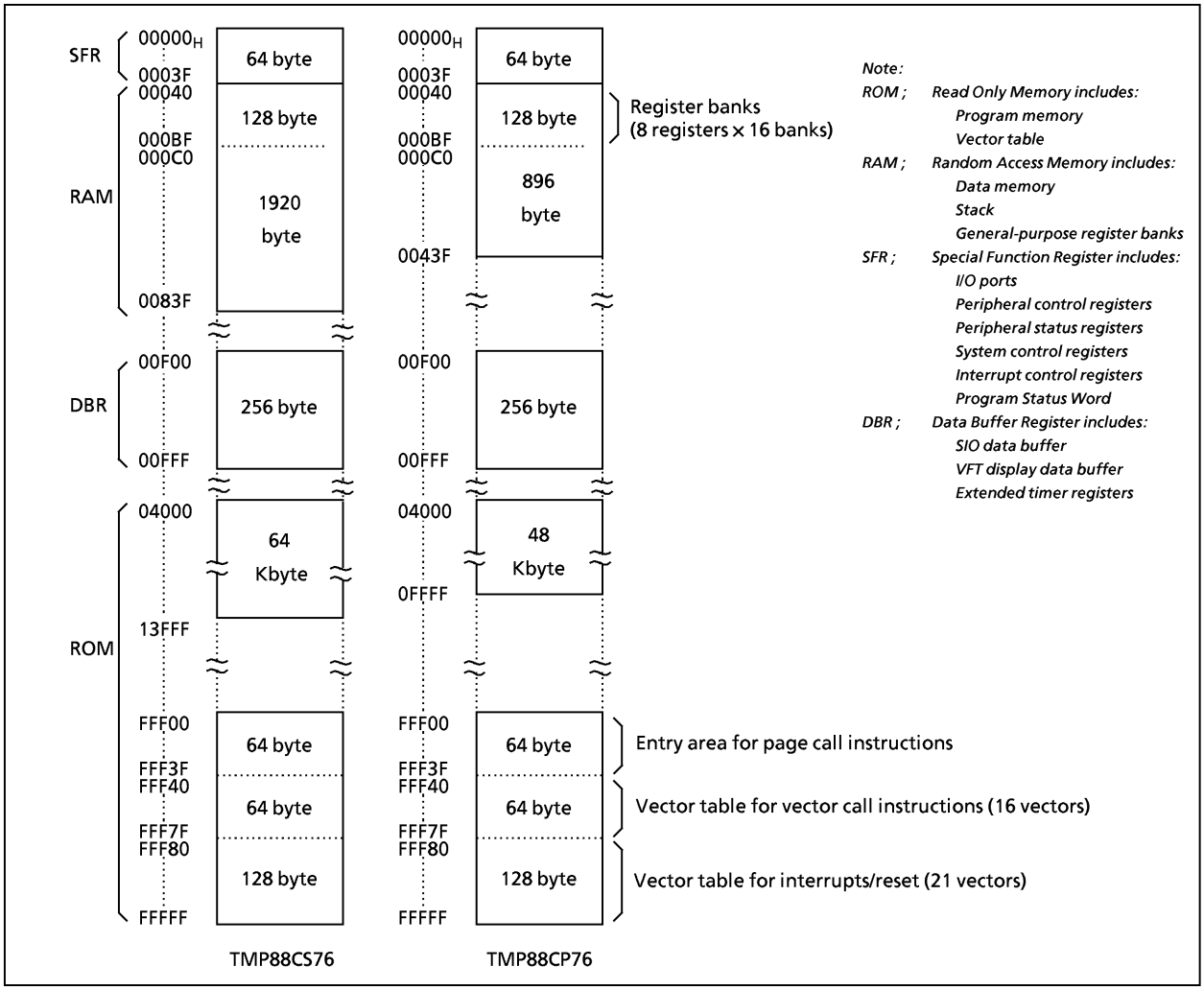


Figure 1-1. Memory Address Maps

1.2 Program Memory (ROM)

The TMP88CP76 has a 48 Kbytes (addresses 04000_H to $0FFFF_H$) and 256 bytes (addresses $FFF00_H$ to $FFFFF_H$), the TMP88CS76 has a 64 Kbytes (address 04000_H to $13FFF_H$) and 256 bytes (addresses $FFF00_H$ to $FFFFF_H$) of program memory (mask programmed ROM). Figure1-1 shown in Memory address maps.
Addresses $FFF00_H$ to $FFFFF_H$ in the program memory can also be used for special purposes.

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Pins	Ratings	Unit
Supply Voltage	V_{DD}		– 0.3 to 6.5	V
Input Voltage	V_{IN1}	P1, P2, P4, P5, XOUT, $\overline{RESET}$	– 0.3 to V_{DD} + 0.3	V
	V_{IN2}	P0 port	– 0.3 to 5.5 V	
Output Voltage	V_{OUT1}	P1, P2, P4, P5, XOUT, $\overline{RESET}$	– 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	P0 port	– 0.3 to 5.5 V	
	V_{OUT3}	Source open drain ports	V_{DD} – 40 to V_{DD} + 0.3	
Output Current (Per 1 pin)	I_{OUT1}	P0, P1, P2, P4, P5 ports	3.2	mA
	I_{OUT2}	P6, P7, P80, 81 Ports	– 25	
	I_{OUT3}	P82 to P87, P9, PD ports	– 12	
Output Current (Total)	ΣI_{OUT1}	P1, P4, P5 ports	– 40	mA
	ΣI_{OUT2}	P0, P1, P2, P4, P5 ports	60	
	ΣI_{OUT3}	P6, P7, P8, P9, PD ports	– 120	
Power Dissipation [Topr = 25°C]	PD Note2		1200	mW
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to + 125	°C
Operating Temperature	Topr		– 30 to + 70	°C

Note 1: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Note 2: Power Dissipation (PD) ; For PD, it is necessary to decrease -14.3 mw/°C.

Note 3: All VDDs should be connected externally for keeping the same voltage level.

Recommended Operating Conditions (V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions		Min	Max	Unit
Supply Voltage	V_{DD}		fc = 12.5 MHz	NORMAL 1, 2 modes	4.5	5.5	V
				IDLE1, 2 modes			
			fs = 32.768 kHz	SLOW mode			
				SLEEP mode			
				STOP mode	2.0		
Input High Voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		$V_{DD} \times 0.70$	V_{DD}	V
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.90$		
Input Low Voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V			$V_{DD} \times 0.30$	V
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V			$V_{DD} \times 0.10$	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 4.5 V to 5.5 V		1.0	12.5	MHz
	fs	XTIN, XTOUT	V_{DD} = 2.7 V to 5.5 V		30.0	34.0	kHz

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

How to calculate power consumption.

With the TMP88CP76/S76, a pull-down resistor (Rk = 80 kΩ typ.) can be built into a VFT driver using mask option (port by port). The share of VFT driver loss (VFT driver output loss + pull-down resistor (Rk) loss) in power consumption Pmax is high. When using a fluorescent display tube with a large number of segments, the maximum power consumption Pd must not be exceeded.

power consumption Pmax = operating power consumption + normal output port loss + VFT driver loss

Where,
operating power consumption: VDD x IDD
normal power consumption: Σ Iout2 x 0.4
VFT driver loss: VFT driver output loss + pull-down resistor (Rk) loss

Example:
When Ta = 10 to 50°C and a fluorescent display tube with segment output = 3 mA, digit output = 15 mA, Vxx = -25 V is used.
Operating conditions: VDD = 5 V ± 10%, fc = 8 MHz, VFT dimmer time (DIM) = (14/16) x tseg:

Power consumption Pmax = (1) + (2) + (3)
Where, segments pin = X grid pin = Y, Y = 2
(1) Operating power consumption: $V_{DD} \times I_{DD}$ = 5.5 V × 22 mA = 121 mW
(2) Normal output port loss: Σ Iout2 x 0.4 V = 60 mA × 0.4 V = 24 mW
(3) VFT driver loss: segment pin = 3 mA x 2 V x number of segments X = 6 mW x X
digit pin = 15 mA x 2 V x 14/16 (DIM) x number of grids Y
= 52.5 mW
Rk loss = (5.5 + 25 V)² / 50 kΩ x (number of segments X + number of digits Y) = 18.605 mW x (X + 2)

Therefore, Pmax = 121 mW + 24 mW + 6 mW × X + 52.5 mW + 18.605 mWx (X + 2) = 234.71 + 24.605X

Maximum power consumption Pd when Ta = 50°C is determined by the following equation:
PD = 1200 mW-(14.3 x 25) = 842.5 mW
The number of segments X which can be lit is:
PD > Pmax
842.5 mW > 234.71 mW + 24.605 X
24.7 > X

Thus, a fluorescent display tube with less than 24 segments can be used. If a fluorescent display tube with 24 segments or more is used, either a pull-down resistor must be attached externally , or the number of segments to be lit must be kept to less than 24 by software.

D.C. Characteristics

(V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions	Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis input		–	0.9	–	V
Input Current	I_{IN1}	TEST	V_{DD} = 5.5 V V_{IN} = 5.5 V / 0 V	–	–	± 2	μA
	I_{IN2}	Open drain ports, Tri-state ports					
	I_{IN3}	$\overline{RESET}$, $\overline{STOP}$					
Input Resistance	R_{IN2}	RESET		100	220	450	kΩ
Pull-down Resistance	R_K	Source open drain ports	V_{DD} = 5.5 V, V_{KK} = – 30 V	50	80	110	
Output Leakage Current	I_{LO1}	Sink open drain ports	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	–	–	2	μA
	I_{LO2}	Source open drain ports	V_{DD} = 5.5 V, V_{OUT} = – 32 V	–	–	– 2	
	I_{LO3}	Tri-state ports	V_{DD} = 5.5 V, V_{OUT} = 5.5 V / 0 V	–	–	2	
Output High Voltage	V_{OH2}	Tri-state ports	V_{DD} = 4.5 V, I_{OH} = – 0.7 mA	4.1	–	–	V
Output Low Voltage	V_{OL}	Except XOUT	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	–	–	0.4	V
Output High current	I_{OH1}	P6, P7, P80, P81 ports	V_{DD} = 4.5 V, V_{OH} = 2.4 V	–	– 30	–	mA
	I_{OH2}	P82 to P87, P9, PD ports		–	– 15	–	
Supply Current in NORMAL 1, 2 modes	I_{DD}		V_{DD} = 5.5 V V_{IN} = 5.3 V / 0.2 V fc = 12.5 MHz fs = 32.768 kHz	–	15	22	mA
Supply Current in IDLE 1, 2 modes				–	6	12	
Supply Current in SLOW mode			V_{DD} = 3.0 V V_{IN} = 2.8 V / 0.2 V fs = 32.768 kHz	–	30	60	μA
Supply Current in SLEEP mode				–	15	30	
Supply Current in STOP mode			V_{DD} = 5.5 V V_{IN} = 5.3 V / 0.2 V	–	0.5	10	

Note 1: Typical values show those at Topr = 25°C , V_{DD} = 5.0 V.

Note 2: Input Current I_{IN1},I_{IN3} ; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

AD Conversion Characteristics

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}		4.5	–	V_{DD}	V
	V_{ASS}		V_{SS}			
Analog Input Voltage	V_{AIN}		V_{ASS}	–	V_{AREF}	V
Analog Supply Current	I_{REF}	V_{AREF} = 5.5 V, V_{ASS} = 0.0 V	–	0.5	1.0	mA
Nonlinearity Error		V_{DD} = 5.0 V, V_{SS} = 0.0 V V_{AREF} = 5.000 V V_{ASS} = 0.000 V	–	–	± 1	LSB
Zero Point Error			–	–	± 1	
Full Scale Error			–	–	± 1	
Total Error			–	–	± 2	

Note: Total errors includes all errors, except quantization error.

A.C. Characteristics

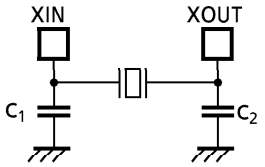
(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine Cycle Time	tcy	In NORMAL1, 2 modes	0.32	–	10	μs
		In IDLE 1, 2 modes				
		In SLOW mode	117.6	–	133.3	
		In SLEEP mode				
High Level Clock Pulse Width	t_{WCH}	For external clock operation (XIN input), fc = 12.5 MHz	32	–	–	ns
Low Level Clock Pulse Width	t_{WCL}					
High Level Clock Pulse Width	t_{WSH}	For external clock operation (XTIN input), fs = 32.768 kHz	15.2	–	–	μs
Low Level Clock Pulse Width	t_{WSL}					

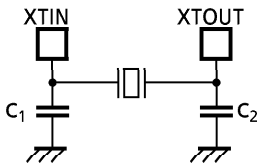
Recommended Oscillating Conditions

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Oscillator	Oscillation Frequency	Recommended Oscillator		Recommended Constant C_1	Recommended Constant C_2
High-frequency Oscillation	Ceramic Resonator	12.5 MHz	Murata	CSA12.5MTZ	30 pF	30 pF
		8 MHz	Murata	CSA8.00MTZ	30 pF	30 pF
	Crystal Oscillator	12.5 MHz	NDK	AT-51	10 pF	10 pF
Low-frequency Oscillation	Crystal Oscillator	32.768 kHz	NDK	MX-38T	15 pF	15 pF



(1) High-frequency Oscillation



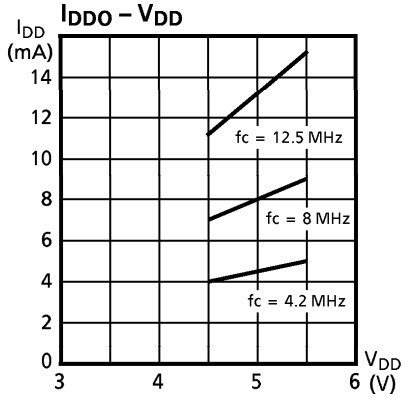
(2) Low-frequency Oscillation

Note: An electrical shield by metal shield plate on the surface of IC package should be recommendable in order to prevent the device from the high electric fieldstress applied from CRT (Cathode Ray Tube) for continuous reliable operation.

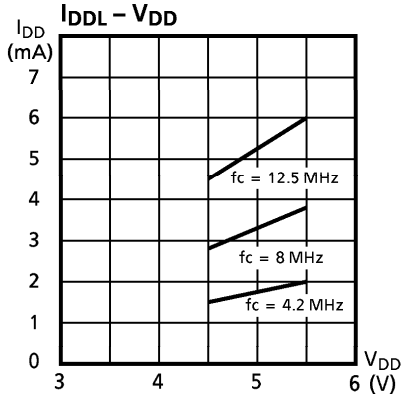
Typical Characteristics

(Ta = 25°C)

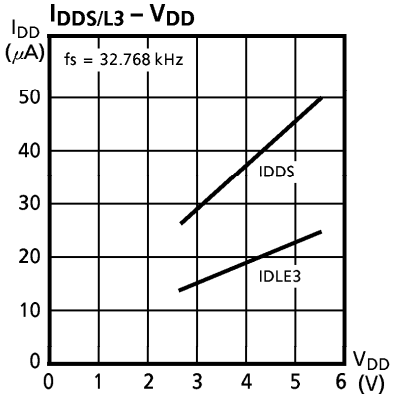
$I_{DDO} - V_{DD}$



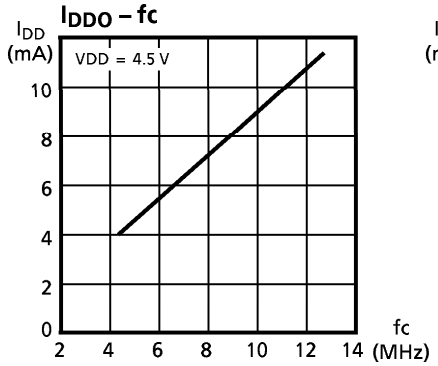
$I_{DDL} - V_{DD}$



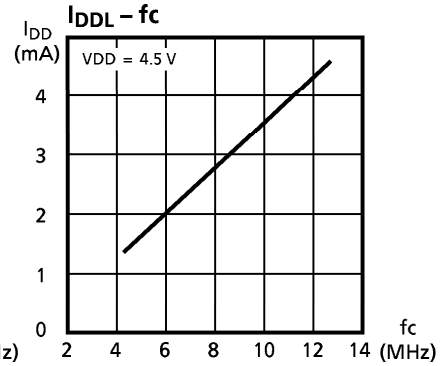
$I_{DDS/L3} - V_{DD}$



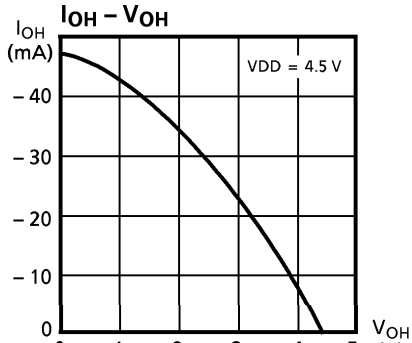
$I_{DDO} - fc$



$I_{DDL} - fc$

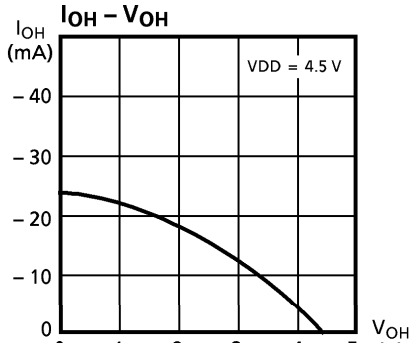


$I_{OH} - V_{OH}$



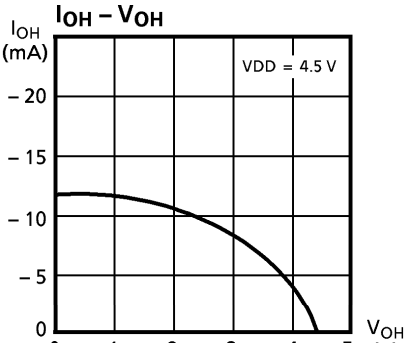
P6, P7, P80, P81 ports

$I_{OH} - V_{OH}$



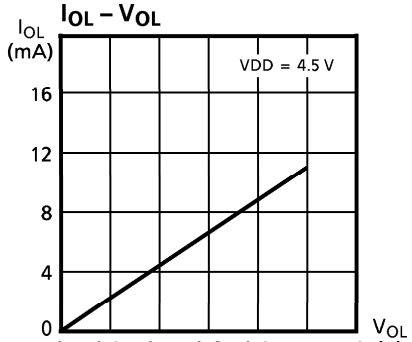
P82 to P87, P9, PD ports

$I_{OH} - V_{OH}$



P1, P3, P4, P5 ports

$I_{OL} - V_{OL}$



P0, P1, P2, P3, P4, P5 ports