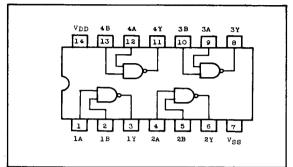
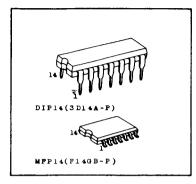
C2MOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC40H000P/F

TC40H000 QUAD 2-INPUT NAND GATE

PIN CONNECTION





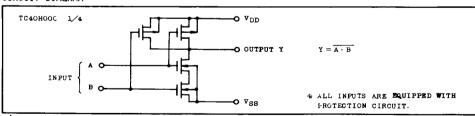
MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{DD}	V _{SS-0.5} ~ V _{SS+10}	V
Input Voltage	VIN	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	VOUT	V _{SS} -0.5 ~ V _{DD+0.5}	v
Input Current	IIN	±10	mA
Power Dissipation	PD	300(DIP)/130(MFP)	mW
Storage Temperature	Tstg	-65 ∿ 150	°C
Lead Temp./Time	Tsol	260°C · 10 sec	

TRUTH TABLE

INF	UT	CUTPUT
A	ь	Y
L	L	Н
H	L	н
L	Н	н
Н	Н	L

CIRCUIT DIAGRAM



RECOMMENDED OPERATING CONDITIONS (VSS=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN:	TYP.	MAX.	UNIT
Supply Voltage	v _{DD}	_	2.0	-	8.0	V
Input Voltage	VIN	-	0	-	V _{DD}	v
Operating Temperature	Topr	-	-40		85	°c

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ELECTRICAL CHARACTERISTICS(VSS=0.0V)

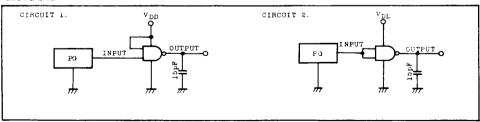
CHARACTERISTIC	CYMBOL TEST CONDI	TEST CONDITION	v _{DD}	-40°C		25°C			85°C		UNIT
CHARACTERISTIC	SIMBUL	TEST CONDITION	(V)	MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	UNIT
High Level Output Voltage	v _{он}	$ I_{OUT} < I_{\mu}A$ $v_{IN} = v_{SS}, v_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	v
Low Level Output Voltage	v _{OL}	I _{OUT} <1μ A V _{IN} =V _{DD}	5	-	0.05	-	0.0	0.05		0.05	V
High Level Output Current	IOH	V _{OH} =4.6V V _{IN} =V _{SS} , V _{DD}	5	-0.52	-	-0.44		-	-0.36	-	mA
Low Level Output Current	I _{OL}	V _{OL} =0.4V V _{IN} =V _{DD}	5	1.4	-	1.1		-	0.8	-	urs.
Input "H"	VIH	I _{OUT} <1µA	5	4.0	-	4.0		-	4.0	-	
Voltage "L" Level	VIL	VOUT=0.5V VOUT=4.5V	5	-	1.0	-		1.0	-	1.0	V
Input "H" Level	IIH	V _{IH} =8.0V	8	-	0.3	-	10-5	0.3	-	1.0	μА
Current "L" Level	IIL	v _{IL} =0.0v	8	-	-0.3	-	-10 ⁻⁵	-0.3	-	-1.0	""
Quiescent Supply	- 00	*V _{IN} =V _{SS} , V _{DD}	5	-	2.0	-	10-3	2.0	-	10.0	μА

* All valid input combinations.

SWITCHING CHARACTERISTICS (Ta=25°C, Vss=0.0V, Ct=15pF)

CHARACTERISTIC (SYMBOL	TEST CONDITION	$v_{DD(V)}$	MIN.	TYP.	MAX.	UNIT
Output Rise Time		tor	Circuit 1	5		26	40	
Output Fall Time		tof	Circuit 1	5	-	16	30	ns
Propagation Delay Time	(Low-High)	tpLH		5	-	18	27	
	(High-Low)	tpHL	Circuit 1	5	-	14	21	ns
1 1 1 1 1 1	(Low-High)	tpLH		5	-	13	20	i
	(High-Low)	tpHL	Circuit 2	5	_	15	23	ns
Input Capacitance		CIN		+	-	5	-	pF

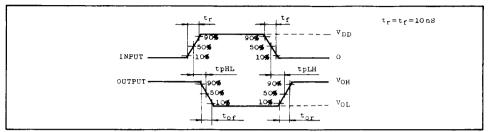
SWITCHING TIME TEST CIRCUIT



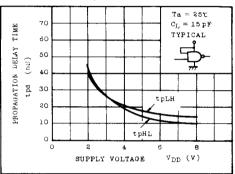
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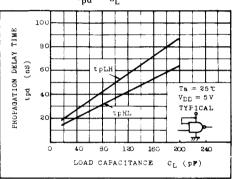
SWITCHING TIME TEST WAVEFORM



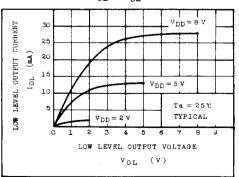
 $t_{pd} - v_{DD}$



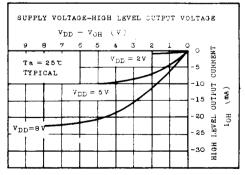
 $t_{pd} - c_L$



IOL - VOL



IOH - (VDD - VOH)



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