

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

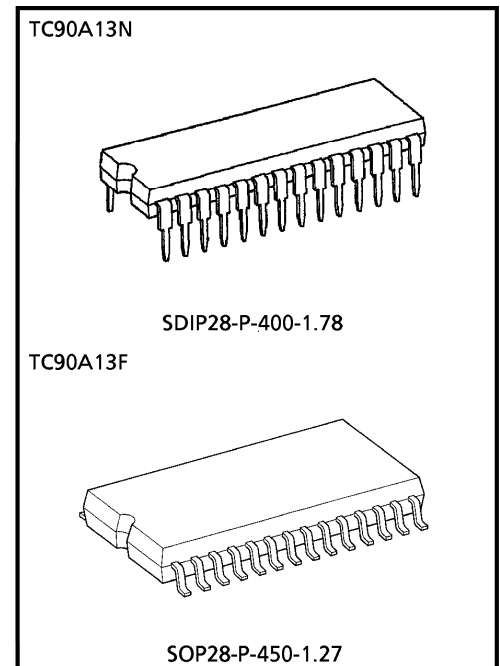
TC90A13N, TC90A13F

3 LINE DIGITAL Y / C SEPARATION IC

The TC90A13N and TC90A13F separate luminance (Y) and chrominance (C) signals from an NTSC composite video signal. It employs the Toshiba original logical comb filter to realize high performance Y/C separation at low cost.

FEATURES

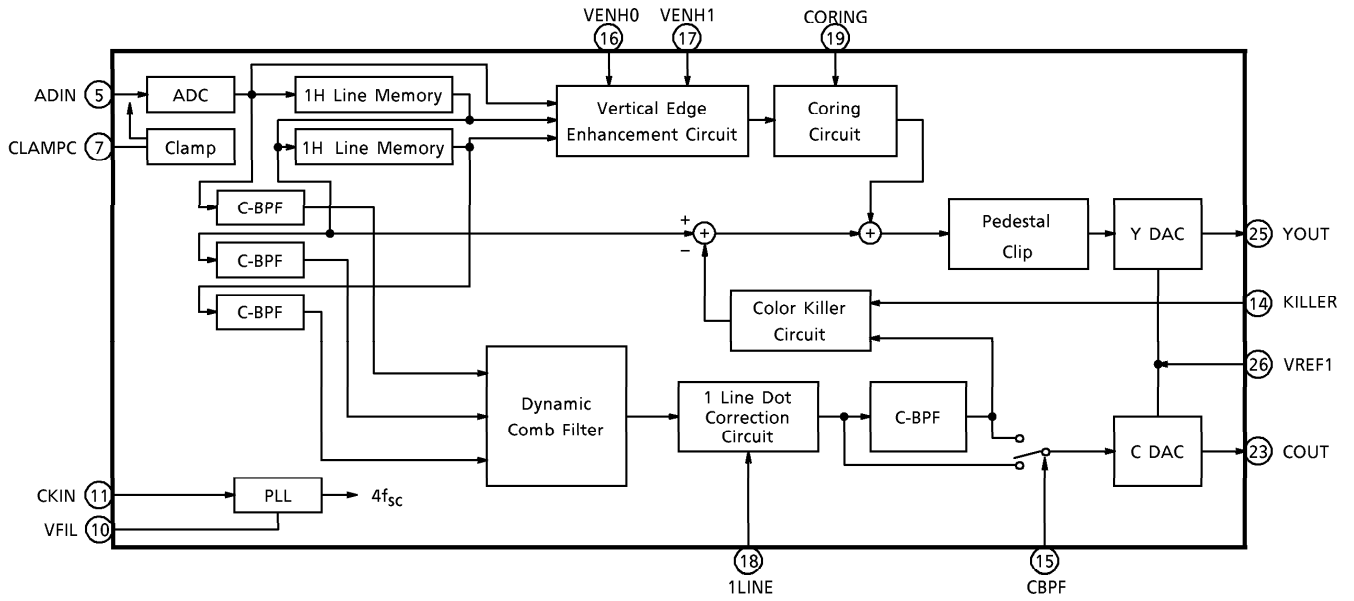
- NTSC system
- PLL 4X multiplication circuit
- Sync. tip clamping circuit
- 8bit A/D converter
- 8bit D/A converters (2ch)
- 2H line memory
- Dynamic comb filter
- 1 line dot correction circuit
- Vertical enhancer
- Color killer mode (Y/C separation OFF)
- Chrominance wide band output mode
- SDIP28/SOP28 package
- 5V single power supply



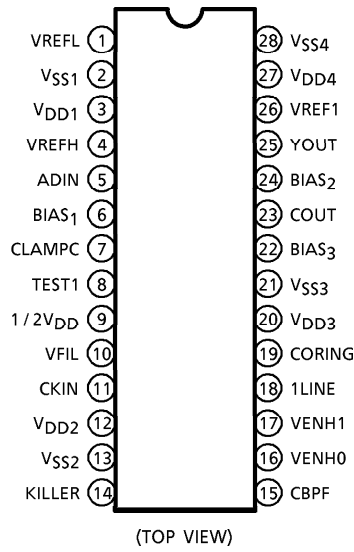
Weight

SDIP28-P-400-1.78 : 1.7g (Typ.)
SOP28-P-450-1.27 : 0.8g (Typ.)

BLOCK DIAGRAM



TERMINAL CONNECTION DIAGRAM



TERMINAL FUNCTION

| PIN No. | NAME | FUNCTION | PIN No. | NAME | FUNCTION |
|---------|--------|-------------------------|---------|--------|--|
| 1 | VREFL | Bias for ADC | 15 | CBPF | L : C-BPF = WIDE, H : NARROW |
| 2 | VSS1 | GND for ADC | 16 | VENH0 | Vertical edge enhanced level (VENH0, VENH1) = (L, L) = OFF (H, L) = Low (L, H) = MID, (H, H) = High |
| 3 | VDD1 | VDD for ADC | 17 | VENH1 | |
| 4 | VREFH | Bias for ADC | 18 | 1LINE | L : 1 line color ON H : 1 line color OFF |
| 5 | ADIN | Video input | 19 | CORING | L : Coring ON H : Coring OFF |
| 6 | BIAS1 | Bias for ADC | 20 | VDD3 | VDD for digital |
| 7 | CLAMPC | Clamp filter | 21 | VSS3 | GND for digital |
| 8 | TEST1 | Test terminal | 22 | BIAS3 | Bias for DAC |
| 9 | 1/2VDD | Bias for line memory | 23 | COUT | C output |
| 10 | VFIL | VCO filter | 24 | BIAS2 | Bias for DAC |
| 11 | CKIN | Clock input | 25 | YOUT | Y output |
| 12 | VDD2 | VDD for PLL | 26 | VREF1 | Bias for DAC |
| 13 | VSS2 | GND for PLL | 27 | VDD4 | VDD for DAC |
| 14 | KILLER | L : Color, H : B/W mode | 28 | VSS4 | GND for DAC |

(Note) Pin 9 and Pin 26 require external bias

FUNCTION BLOCK DESCRIPTIONS**1. Input clamp (CLAMP)**

This block performs sync tip clamping of the composite video signal. It provides a feedback signal for clamping A/D-converted minimum data at Y/C separation to the internal DC bias level.

2. A/D converter (ADC)

This block comprises a high-speed series-parallel 8bit A/D converter that accepts an input video signal of $1.5V_{p-p}$ (from sync level to 100% white level).

3. 1H memory

This block consists of DRAM resident line memory for 1H delay. The 3-line comb filter is configured from two pairs of line memory.

4. Vertical edge enhancement circuit (VENH)

This block enhances the uncorrelated components among the three lines of the luminance signal following coring. There are three enhancement level selections of HIGH (1.9dB), MID (1.0dB) and LOW (0.5dB). The luminance signal, obtained by subtracting the chrominance signal from the composite video signal, is added to the vertical edge enhancement component and output through the D/A converter. However, this output signal is limited to the pedestal level (fixed internally) by the pedestal clipping circuit (except for the sync tip level).

5. Horizontal band-pass filter (BPF)

In this block, with fsc as the center frequency of the BPF, the chrominance signal is extracted from the 0H, 1H and 2H delayed composite video signal. Since the BPF for the chrominance signal output can be controlled (ON or OFF), the chrominance output can therefore be switched between a narrow band width and a wide band width.

6. Vertical dynamic comb filter (DCF)

This block comprises a band-pass filter that extracts the vertical component of the chrominance signal. Using Toshiba original logic, a correlation of the three lines is sought for. The absence of correlation is taken as an indication of a luminance signal, at which time chrominance signal output is suppressed.

7. 1-line dot correction circuit

Previously, a 1-line-only chrominance signal was processed as a luminance signal resulting in dot crawl. This circuit prevents this problem by extracting the 1-line dot component and adding it to the dynamic comb filter output. This circuit block can be set ON or OFF.

8. Clock and memory timing generator (RTIM)

This block supplies a 4 fsc (PLL 4X multiplied) buffered signal to the other circuit blocks, and also generates a timing signal for the memory.

9. D/A converter (DAC)

This block comprises a high-speed 8bit D/A converter. It provides Y output at approximately $1.5V_{p-p}$ and burst-level C output at approximately $572mV_{p-p}$.

MODE TABLE

| PIN 14 KILLER | PIN 15 CBPF | PIN 16 VENH0 | PIN 17 VENH1 | PIN 18 1 LINE | PIN 19 CORING | MODE | ACTION |
|------------------|----------------|-----------------|-----------------|------------------|------------------|---|--|
| L | — | — | — | — | — | Y/C separation ON | Color mode |
| H | — | — | — | — | — | Y/C separation OFF | B/W mode (Killer) |
| — | L | — | — | — | — | Chrominance signal horizontal band width WIDE | Passes through BPF for chrominance signal output |
| — | H | — | — | — | — | Chrominance signal horizontal band width NARROW | Does not pass through BPF for chrominance signal output |
| — | — | L | L | — | — | Vertical enhance OFF | No vertical enhancement |
| — | — | H | L | — | — | Vertical enhance level MID | Vertical enhancement level 0.5dB |
| — | — | L | H | — | — | Vertical enhance level LOW | Vertical enhancement level 1.0dB |
| — | — | H | H | — | — | Vertical enhance level HIGH | Vertical enhancement level 1.9dB |
| — | — | — | — | L | — | 1 line color ON | 1 line dot correction circuit ON |
| — | — | — | — | H | — | 1 line color OFF | 1 line dot correction circuit OFF |
| — | — | — | — | — | L | Coring ON | Coring circuit ON |
| — | — | — | — | — | H | Coring OFF | Coring circuit OFF |

RATINGS AND CHARACTERISTICS

The following specifications were obtained in part from the test circuit shown on page 8.

MAXIMUM RATINGS (Ta = 25°C)

| CHARACTERISTIC | SYMBOL | RATING | UNIT | |
|----------------------|----------------------|--|------|----|
| Power Supply Voltage | V _{DD} | V _{SS} ~V _{SS} + 6.0 | V | |
| Input Voltage | V _{IN} | - 0.3~V _{DD} + 0.3 | V | |
| Power Dissipation | TC90A13N TC90A13F | P _D (Note) | 900 | mW |
| | | | 600 | |
| Storage Temperature | T _{stg} | - 55~125 | °C | |

(Note) Ta = 75°C

RECOMMENDED OPERATING CONDITIONS

| CHARACTERISTIC | SYMBOL | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|-----------------------|------------------|----------------|------|------|-----------------|------|
| Power Supply Voltage | V _{DD} | — | 4.75 | 5.0 | 5.25 | V |
| Input Voltage | V _{IN} | — | 0 | — | V _{DD} | V |
| Operating Temperature | T _{opr} | — | - 10 | — | 75 | °C |

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (Ta = 25°C, VDD = 5V)

| CHARACTERISTIC | | SYMBOL | TEST CIR-CUIT | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|----------------------------|------------|--------|---------------|---|------|------|------|------|
| Power Supply Voltage | | VDD | 1 | CLOCK = 3.579545MHz 500mVp-p VREF1 = 3.0V 1/2VDD = 2.5V VIN = No input (Note 2) | 4.75 | 5.0 | 5.25 | V |
| Supply Current | | IDD | 1 | | 40 | 60 | 80 | mA |
| Output Voltage Level | | YOUT | 1 | | 3.0 | 3.15 | 3.3 | V |
| | | COUT | | | 3.9 | 4.0 | 4.1 | |
| Pin Voltage Level | | VREFL | 1 | | 1.4 | 1.5 | 1.6 | V |
| | | VREFH | | | 3.4 | 3.5 | 3.6 | |
| | | ADIN | | | 1.5 | 1.6 | 1.8 | |
| | | BIAS1 | | | 0.8 | 1.4 | 2.4 | |
| | | BIAS2 | | | 0.8 | 1.6 | 2.6 | |
| | | BIAS3 | | | 2.4 | 3.4 | 4.4 | |
| | | CLAMPC | | | 2.0 | 3.0 | 4.0 | |
| | | VFIL | | | 0.9 | 1.9 | 2.9 | |
| | | CKIN | | | 1.5 | 2.2 | 3.0 | |
| Input Voltage | High Level | VIH | 1 | | 4 | — | — | V |
| | Low Level | VIL | 1 | — | — | 1 | | |
| ADIN Pin Input Capacitance | | CIN | 1 | — | 50 | — | pF | |
| Pull Down Resistance | | RPD | 1 | 25 | 50 | 100 | kΩ | |

(Note 1) External bias must be applied at Pin 9 and Pin 26.

(Note 2) IDD is VIN = modulated lamp wave.

AC CHARACTERISTICS

Y output (Ta = 25°C, VDD = 5V, Clock frequency 3.579545MHz, 0.5Vp-p, S1 = 2, VREF1 = 3.0V)

| CHARACTERISTIC | SYMBOL | TEST CIRCUIT | TEST CONDITION | MIN. | TYP. | MAX. | UNIT | |
|---|-----------------|--------------|---|---------|------|------|-------------------|----|
| Input Level | V _{IN} | 1 | 0~140IRE | — | 1.5 | 1.6 | V _{p-p} | |
| Low Frequency Gain | GV | 1 | S2 = 2, S3 = 2, S4 = 1, S5 = 2 V _{IN} = 15.734kHz, 1.5V _{p-p} V _{dc} = 2.5V | -0.5 | 0.0 | 0.5 | dB | |
| Frequency Response | MTF1 | 1 | S2 = 2, S3 = 2, S4 = 1, S5 = 2 V _{IN} = 1.5V _{p-p} V _{dc} = 2.5V | f2 / f1 | -2.0 | -1.2 | -0.5 | dB |
| | MTF2 | 1 | V _{IN} = 1.5V _{p-p} V _{dc} = 2.5V | f4 / f1 | -3.0 | -2.0 | -1.5 | |
| Comb Characteristics | Comb | 1 | S2 = 2, S3 = 2, S4 = 1, S5 = 2 V _{IN} = 1.5V _{p-p} V _{dc} = 2.5V | f2 / f3 | 40 | 45 | — | dB |
| Linearity (Fig.1) | L _s | 1 | S2 = 1, S3 = 1, S4 = 1, S5 = 2 | Y1 / Y2 | 35 | 40 | 43 | % |
| | L _y | 1 | V _{IN} = 5 step signal, 1.5V _{p-p} (Fig.2) | S / Y2 | 57 | 60 | 63 | |
| Output Impedance | Z _O | 1 | S2 = 1, S3 = 1, S5 = 2 V _{IN} = 15.734kHz, 1.5V _{p-p} V _{dc} = 2.5V $Z_O = \frac{V1 - V2}{V2} \times 400$ V1 : S4 = 1, V2 : S4 = 2 | 250 | 400 | 700 | Ω | |
| Clock Leakage (4f _{sc} Components) | L _{ck} | 1 | S2 = 2, S3 = 2, S4 = 1, S5 = 1 V _{IN} = No input | — | 5.0 | 20 | mV _{rms} | |
| Fundamental Clock Leakage (f _{sc} Components) | L _{sc} | 1 | S2 = 2, S3 = 2, S4 = 1, S5 = 1 V _{IN} = No input | — | 1.0 | 2.0 | mV _{rms} | |

C output (Ta = 25°C, V_{DD} = 5V, Clock frequency 3.579545MHz, 0.5V_{p-p}, S1 = 1, VREF1 = 3.0V)

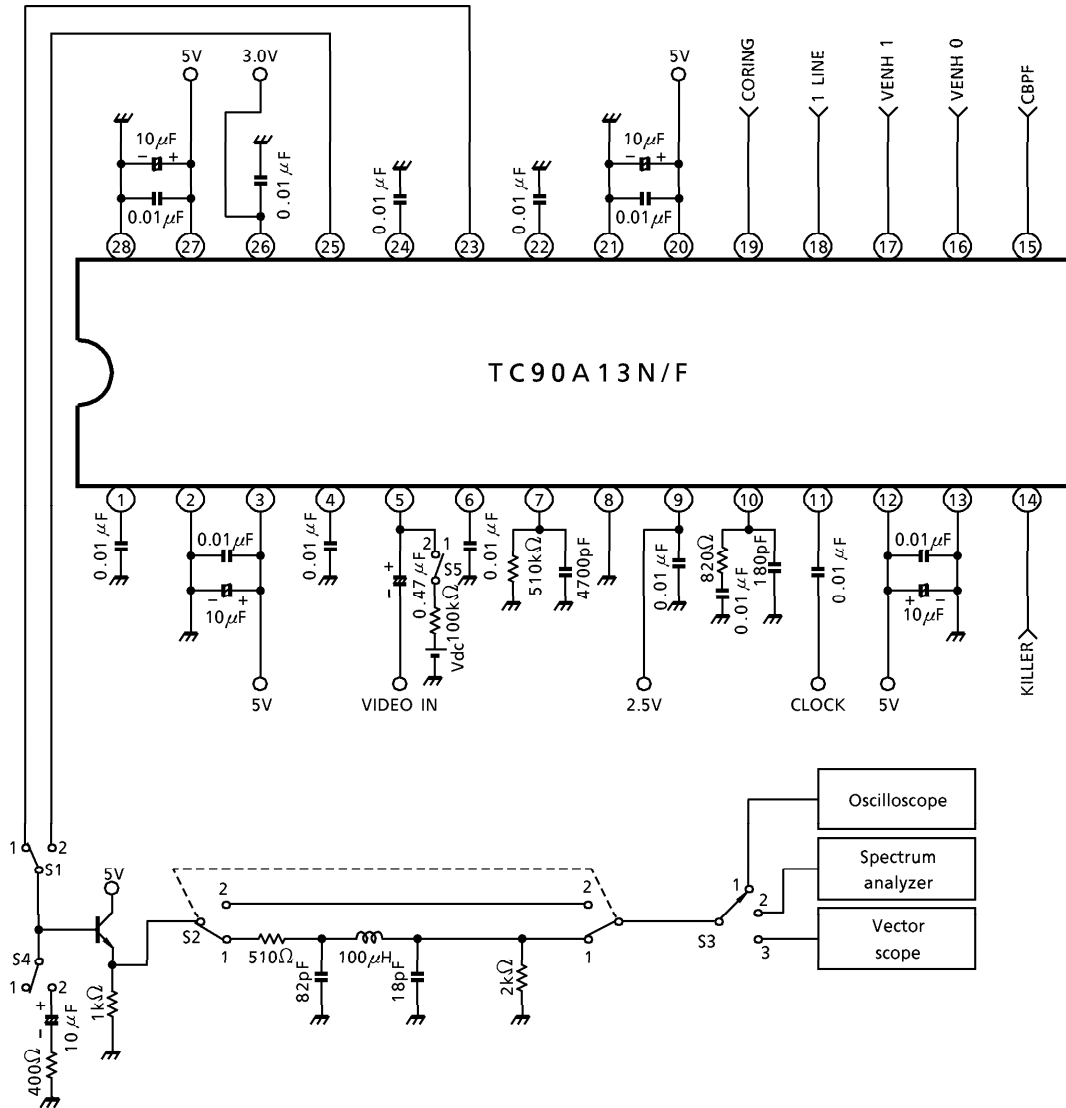
| CHARACTERISTIC | | SYMBOL | TEST CIR-CUIT | TEST CONDITION | MIN. | TYP. | MAX. | UNIT | |
|---|--------|-----------------|---------------|--|---------|------|------|-------------------|----|
| BPF Characteristics | WIDE | BWCW | 1 | S2 = 2, S3 = 2, S4 = 1, S5 = 2 Difference of amplitude between 1f _{SC} and 1f _{SC} - 503496Hz V _{IN} = 1.5V _{p-p} , V _{dc} = 2.5V | -0.5 | -0.2 | — | dB | |
| | NARROW | BWCN | 1 | S2 = 2, S3 = 2, S4 = 1, S5 = 2 Difference of amplitude between 1f _{SC} and 1f _{SC} - 503496Hz V _{IN} = 1.5V _{p-p} , V _{dc} = 2.5V | -1.0 | -0.5 | — | | |
| Gain | | CV | 1 | S2 = 2, S3 = 2, S4 = 1, S5 = 1 V _{IN} = f _{SC} , 430mV _{p-p} | -2.0 | -0.9 | -0.6 | dB | |
| Comb Characteristics | | Comb | 1 | S2 = 2, S3 = 2, S4 = 1, S5 = 2 V _{IN} = 430mV _{p-p} , V _{dc} = 2.5V | f3 / f2 | 30 | 35 | — | dB |
| Differential Gain | | DG | 1 | S2 = 2, S3 = 3, S4 = 1, S5 = 1 V _{IN} = 5 step signal, Y = 140IRE = 1.5V _{p-p} C = 40IRE (Fig.2) | 0 | 2 | 5 | % | |
| Differential Phase | | DP | 1 | DG = (Comax - Comin) / Comax (Fig.3) | 0 | 2 | 5 | ° | |
| Output Impedance | | Z _O | 1 | S2 = 2, S3 = 2, S5 = 2 V _{IN} = 15.734kHz, 1.5V _{p-p} V _{dc} = 2.5V $Z_O = \frac{V1 - V2}{V2} \times 400$ V1 : S4 = 1, V2 : S4 = 2 | 250 | 400 | 700 | Ω | |
| Clock Leak (4f _{SC} Components) | | L _{ck} | 1 | S2 = 2, S3 = 2, S4 = 1, S5 = 1 V _{IN} = No input | — | 5.0 | 20 | mV _{rms} | |
| Fundamental Clock Leak (f _{SC} Components) | | L _{sc} | 1 | S2 = 2, S3 = 2, S4 = 1, S5 = 1 V _{IN} = No input | — | 0.3 | 1.0 | mV _{rms} | |

f1 = 15.734kHz, f2 = 3.587412MHz, f3 = 3.595279MHz, f4 = 4.783216MHz

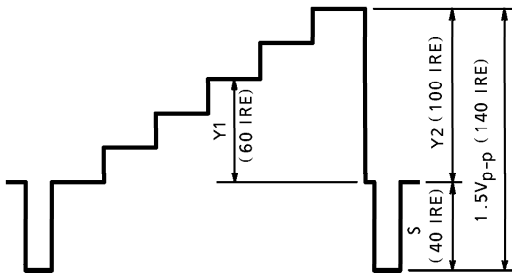
PLL CIRCUIT CHARACTERISTICS

| CHARACTERISTIC | SYMBOL | TEST CIR-CUIT | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|--|-----------------|---------------|----------------|------|------|------|------------------|
| Pull-in Frequency Range | f _{ck} | 1 | — | 3.57 | 3.58 | 3.59 | MHz |
| Input Amplitude (f _{SC} Components) | V _{ck} | 1 | — | 0.4 | 0.5 | — | V _{p-p} |

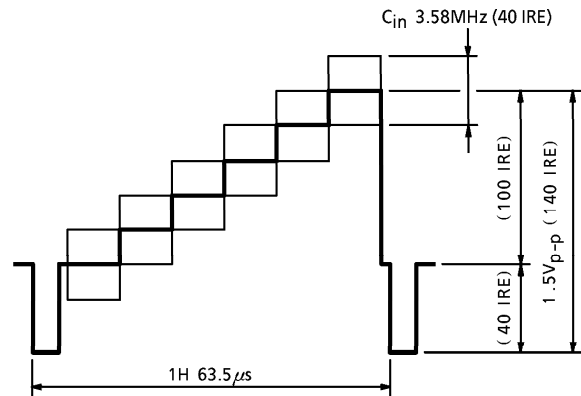
TEST CIRCUIT 1



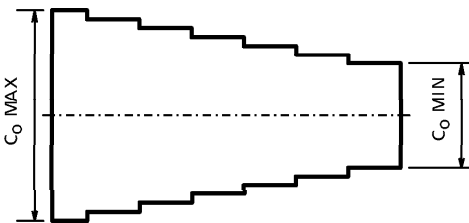
Linearity test (Fig.1)



5 Step signal (Fig.2)

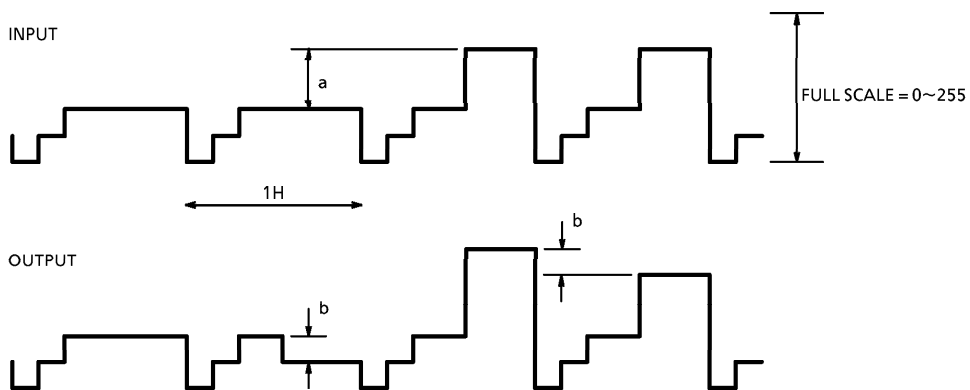


Chroma differential gain (Fig.3)



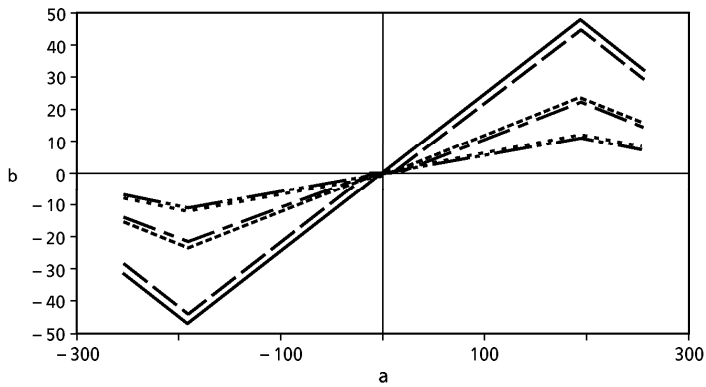
REFERENCE DATA

(Fig.4-a) Definition of vertical edge enhancement

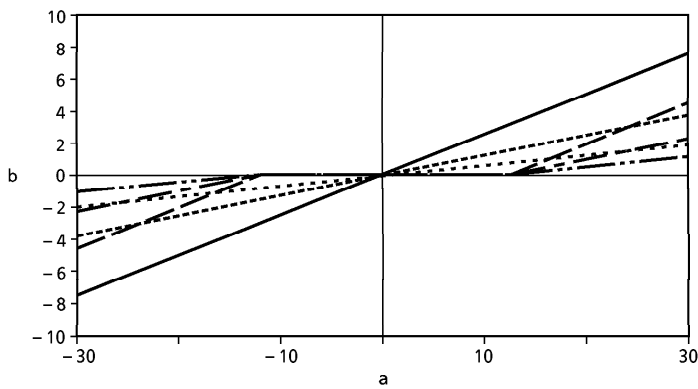


(Note) The output signal, to which the vertical edge enhancement component is added, is limited to pedestal level by the pedestal clip circuit.

(Fig.4-b) Vertical edge enhancement characteristic



(Fig.4-c) Vertical edge enhancement characteristic (detail)



The relation between a and b. (refer to Fig.4-a)

a : The difference in luminance level is in the enhanced part of the edge.

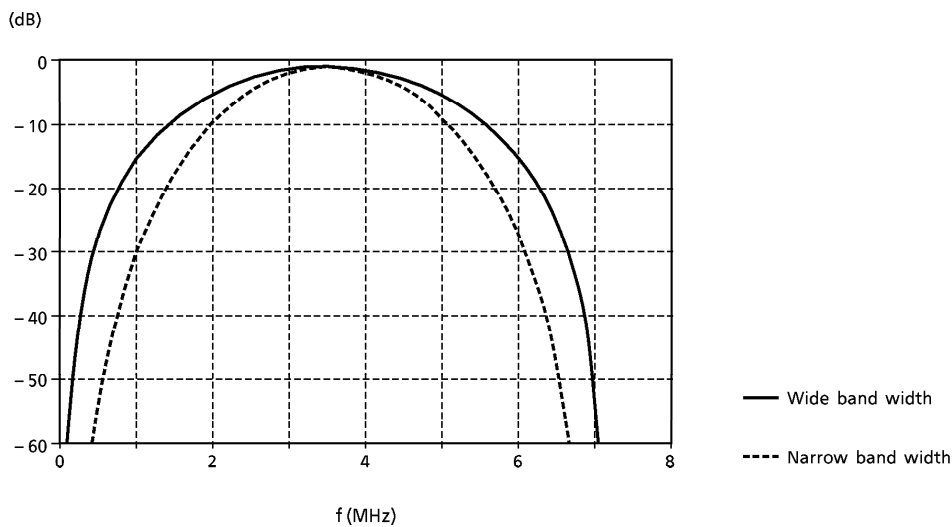
b : The component of vertical edge enhancement that is added to the luminance signal.

Both are expressed as digital values.

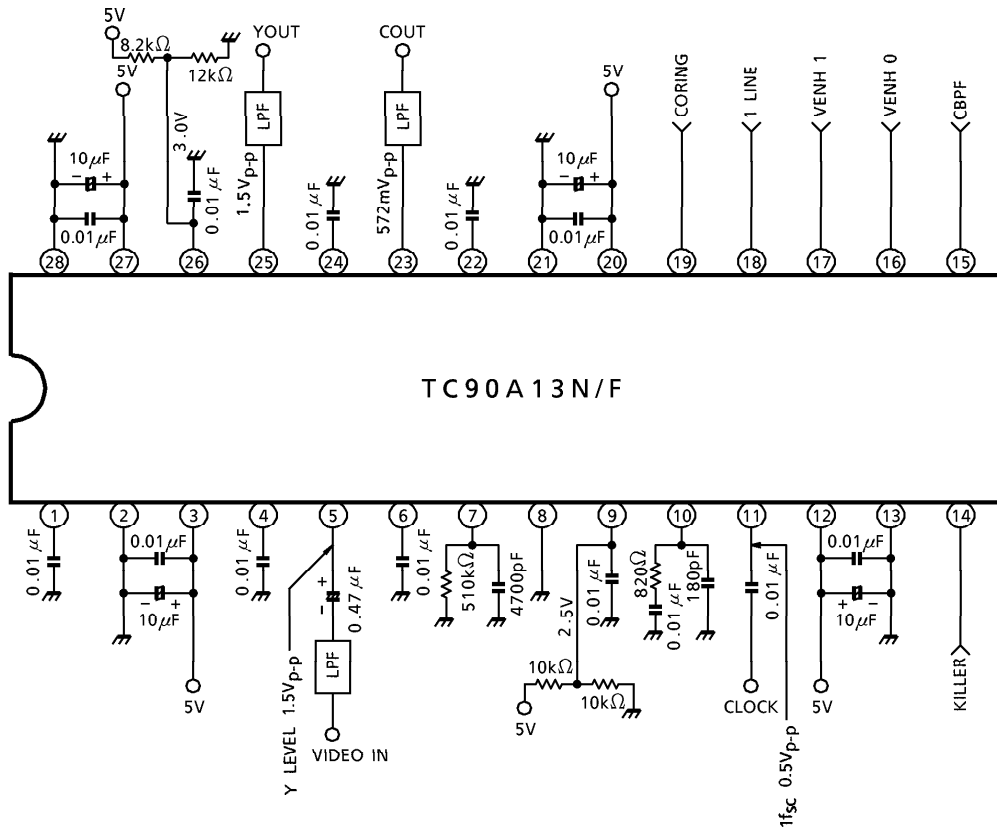
— (A) Enhance Value HIGH - - - - (B) MID ····· (C) LOW
 - - - (D) Enhance value HIGH — — — (E) MID — ··· (F) LOW

A, B, C : Coring=OFF D, E, F : Coring=ON

(Fig.5) Frequency characteristics of chroma output

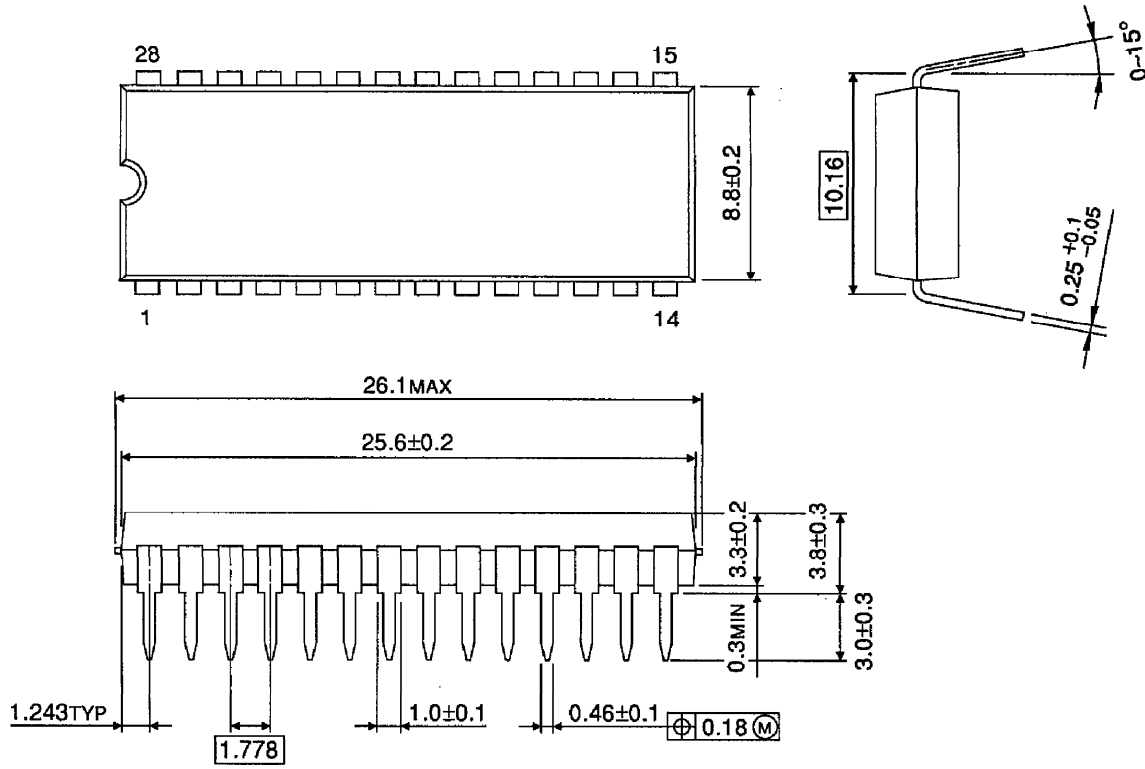


APPLICATION CIRCUIT



PACKAGE DIMENSIONS
SDIP28-P-400-1.78

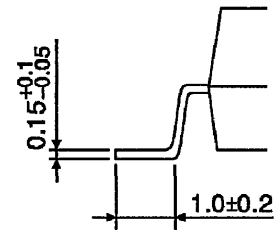
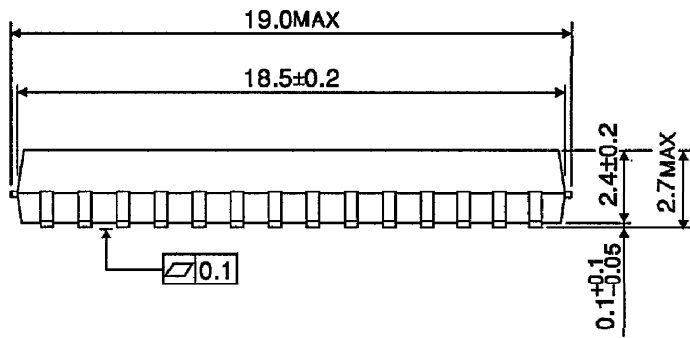
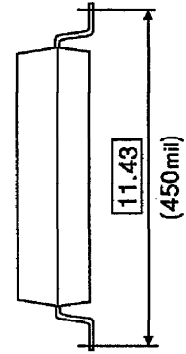
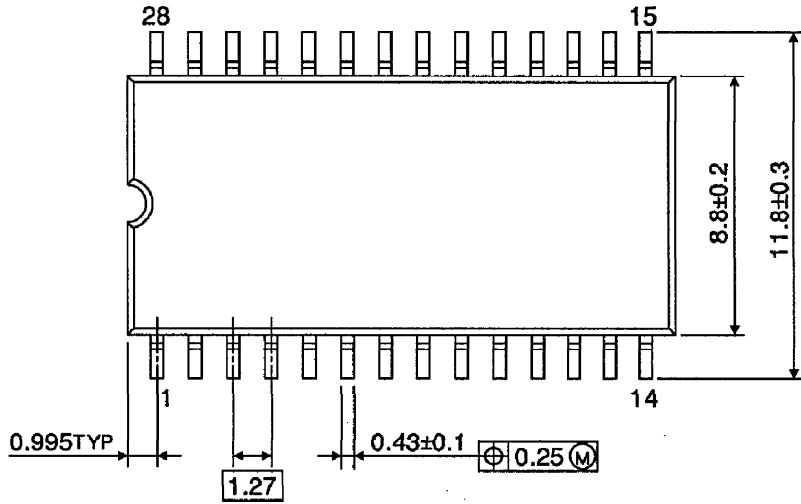
Unit : mm



Weight : 1.7g (Typ.)

PACKAGE DIMENSIONS
SOP28-P-450-1.27

Unit : mm



Weight : 0.8g (Typ.)

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000707EBA

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