TOSHIBA RISC PROCESSOR

TMPR3912AU

(32 bit RISC Microprocessor)

1. GENERAL DESCRIPTION

The TMPR3912AU is a single-chip integrated digital ASSP for PDA(Personal Digital Assistants). The TMPR3912AU consists of PDA system support logic, integrated with the TX39 processor Core designed by Toshiba.

2. FEATURES

- R3000A-based TX39 Processor Core
  - RISC architecture developed by MIPS Technologies, Inc.
  - Toshiba has added its own multiply-add and branch-likely instructions.
  - A single-cycle multiply/accumulate module to allow integrated DSP functions, such as a software modem for high-performance standard data and fax protocols
  - Instruction cache: 4K bytes; data cache : 1K bytes
  - On-chip Translation Lookaside Buffer (TLB) with 32x64-bit wide entries, each of which maps 4KByte page
  - Max 75MHz operation
- Built-in peripheral circuit
  - Clock generator with built-in eightfold-frequency phase-locked loop (PLL)
  - Four-stage write buffer
  - A high performance and flexible Bus Interface Unit
  - Multiple DMA channels
  - Memory controller for DRAM, HDRAM, SDRAM, SRAM, ROM, Flash Memory and PCMCIA
  - Power management unit
  - Big / Little endian
- Low power dissipation
  - 3.3V operation
  - Standby Current 10μA(typ)
  - CPU clock stop mode
  - Power down modes for individual internal peripheral modules
- Plastic LQFP 208-pin package

R3000A is a trademark of MIPS Technologies, Inc.

3. SYSTEM CONFIGURATION

3.1 SYSTEM BLOCK DIAGRAM

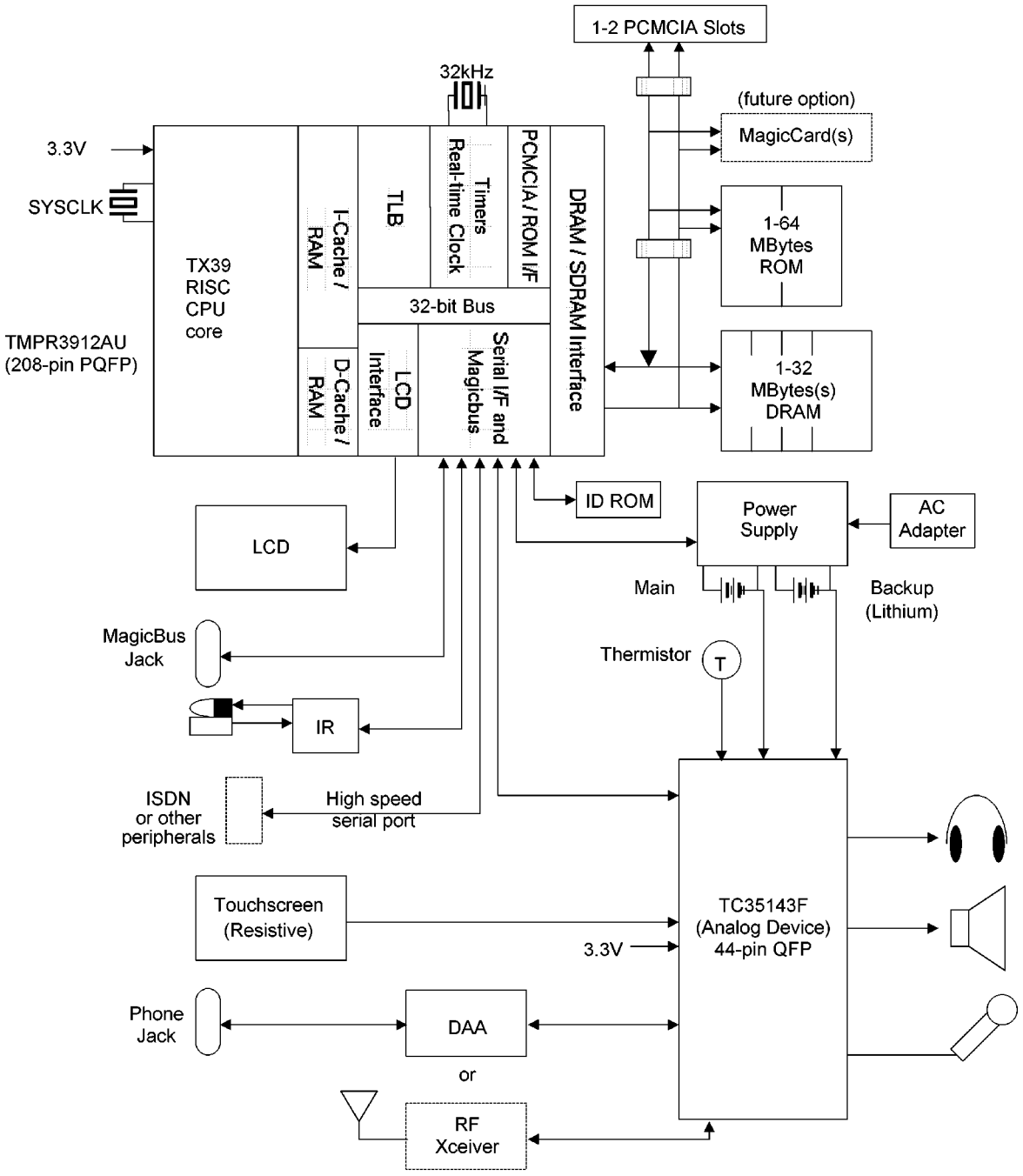


FIG. 3.1 SYSTEM BLOCK DIAGRAM

3.2 TMPR3912AU DIAGRAM

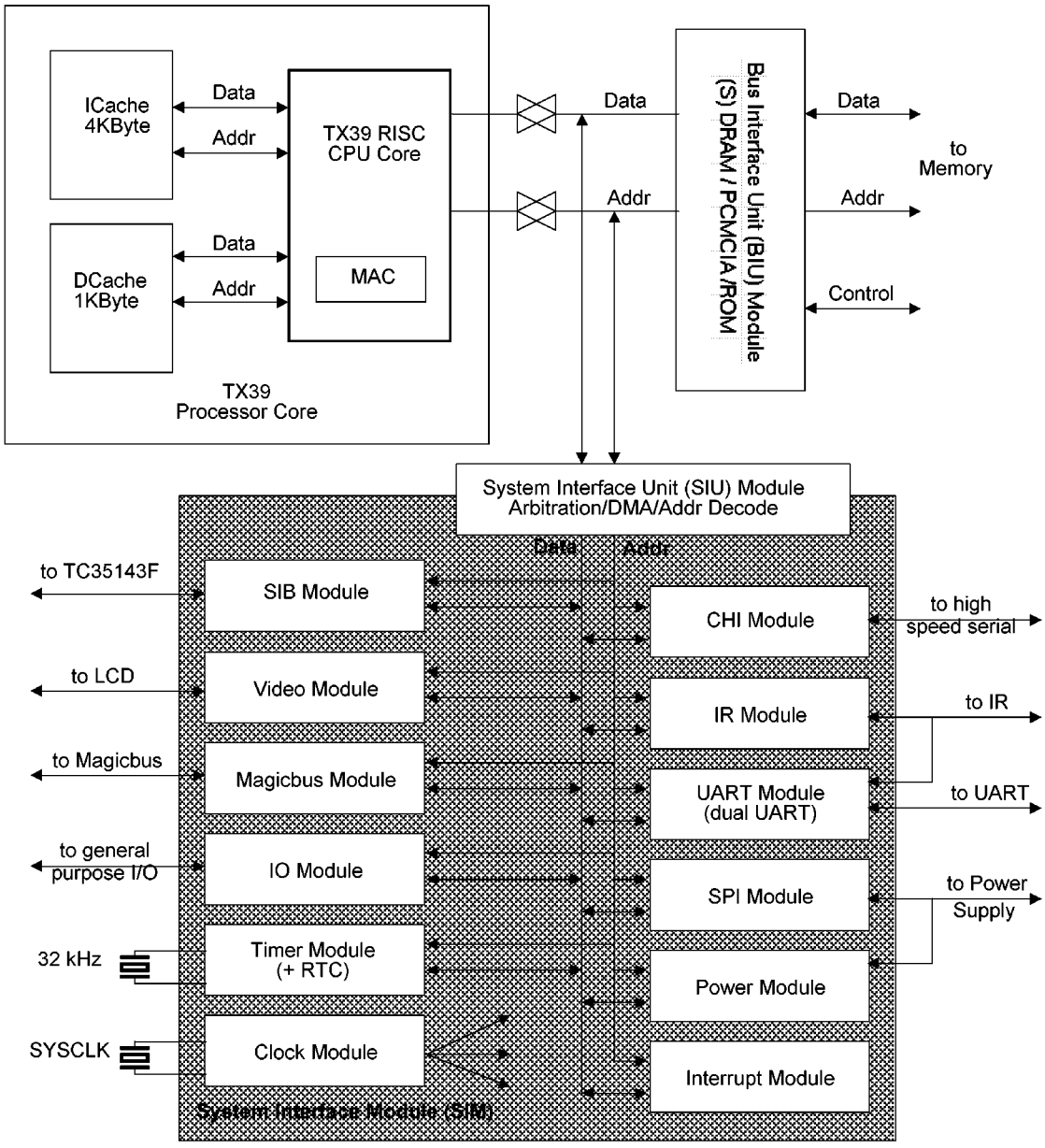


FIG. 3.2 TMPR3912AU BLOCK DIAGRAM

3.3 MEMORY CONNECTIONS

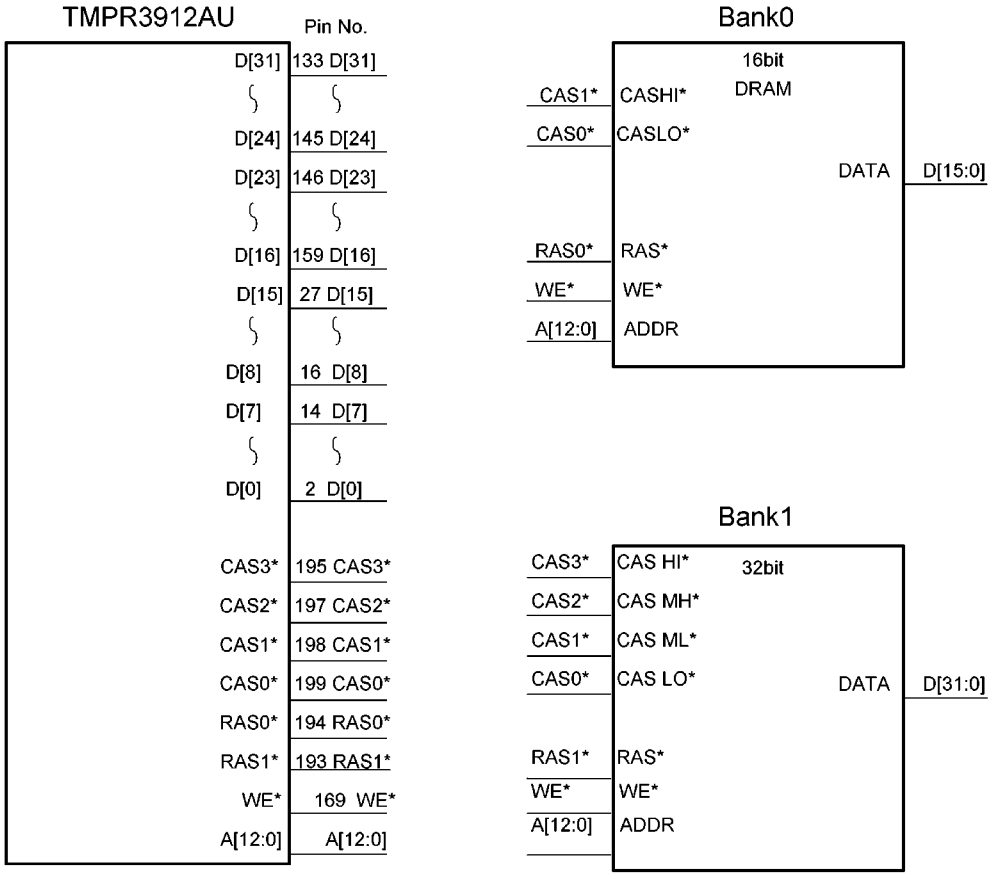
D [31:0] Data Bus and Cas* signals change the name of the pins in the Little Endian mode as follows.

D [31:24]	becomes	D[7:0]
D [23:16]	becomes	D[15:8]
D [15:8]	becomes	D[23:16]
D [7:0]	becomes	D[31:24]
CAS3*	becomes	CAS0*
CAS2*	becomes	CAS1*
CAS1*	becomes	CAS2*
CAS0*	becomes	CAS3*
DQMH	becomes	DQML
DQML	becomes	DQMH

<Note>

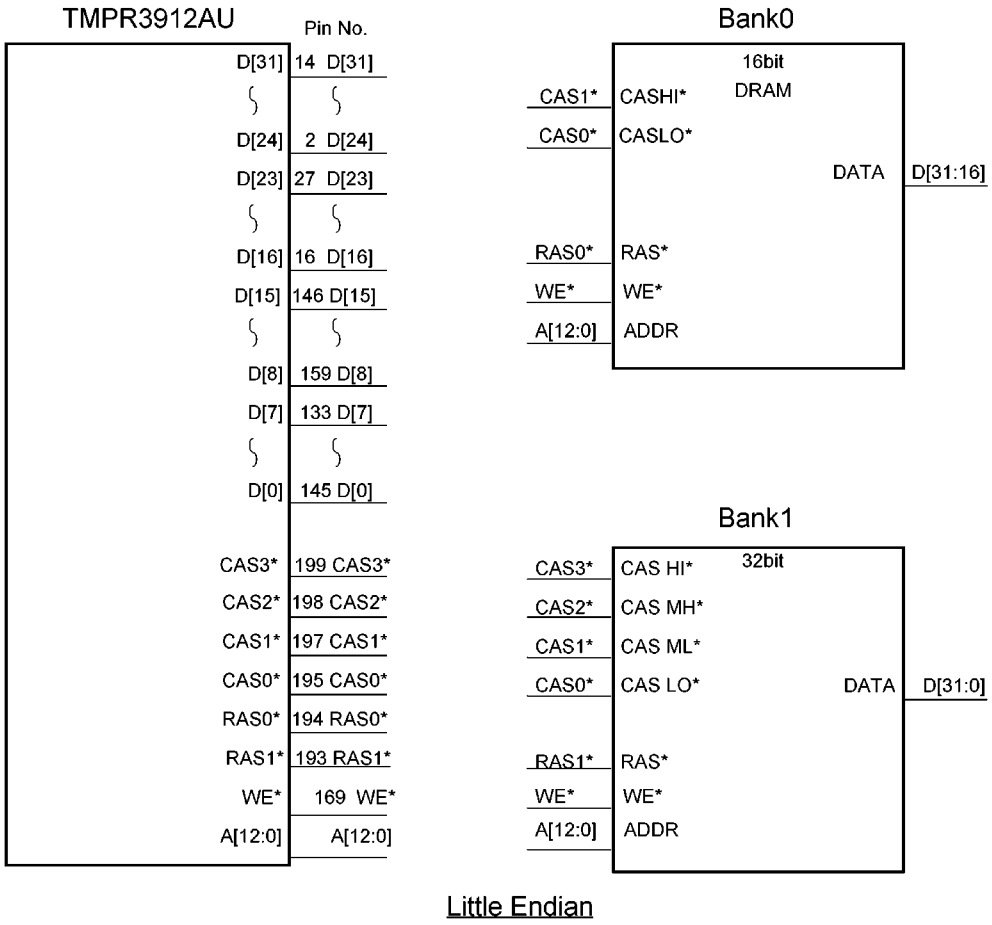
The connection between the TMPR3912AU and Memory depends on the endianess.

3.3.1 MEMORY CONNECTIONS (Big Endian)



Big Endian

3.3.2 MEMORY CONNECTIONS (Little Endian)



Little Endian

4. PINS

4.1 PIN ASSIGNMENT

NO.	I/O	SIGNAL NAME	NO.	I/O	SIGNAL NAME	NO.	I/O	SIGNAL NAME
1	–	VDD	41	I	SIBDIN	81	–	VSS
2	I/O	D[0] (D [24])	42	O	SIBDOUT	82	O	PWRCS
3	–	VSS	43	–	VDD	83	I	PWRINT
4	I/O	D[1] (D [25])	44	I	SIBIRQ	84	I	PWROK
5	I/O	D[2] (D [26])	45	I/O	MIOX[0]	85	–	NC
6	–	VDD	46	I/O	IO[6]	86	I	ONBUTN
7	I/O	D[3] (D [27])	47	I/O	IO[5]	87	I	PON*
8	–	VSS	48	–	VSS	88	I	CPURES*
9	I/O	D[4] (D [28])	49	I/O	CHICLK	89	–	VDD
10	–	VDD	50	I/O	CHIFS	90	O	DISPON
11	I/O	D[5] (D [29])	51	I	CHIDIN	91	O	FRAME
12	I/O	D[6] (D [30])	52	O	CHIDOUT	92	–	VSS
13	–	VSS	53	–	VDD	93	O	DF
14	I/O	D[7] (D [31])	54	I	RXD	94	O	LOAD
15	–	VSS	55	O	TXD	95	O	CP
16	I/O	D[8] (D [16])	56	I/O	IO[4]	96	–	VSS
17	–	VDD	57	–	NC	97	–	VDD
18	I/O	D[9] (D [17])	58	I	IRIN	98	O	VDAT[0]
19	I/O	D[10] (D [18])	59	O	IROUT	99	O	VDAT[1]
20	–	VSS	60	–	VSS	100	O	VDAT[2]
21	I/O	D[11] (D [19])	61	–	VDD	101	O	VDAT[3]
22	–	VDD	62	I	CARDET	102	–	VSS
23	I/O	D[12] (D [20])	63	O	RXPWR	103	I/O	IO[1]
24	I/O	D[13] (D [21])	64	I/O	IO[3]	104	–	VDD
25	–	VSS	65	I/O	IO[2]	105	I	CARD2WAIT*
26	I/O	D[14] (D [22])	66	–	VSS	106	O	CARD2CSH*
27	I/O	D[15] (D [23])	67	O	SPICLK	107	O	CARD2CSL*
28	–	VDD	68	I	SPIIN	108	I/O	IO[0]
29	I	ENDIAN	69	O	SPIOUT	109	–	VSS (PLL)
30	I/O	MIOX[1]	70	–	VDD	110	O	CARDIORD*
31	I	MBUSINT	71	I	TESTCPU	111	O	CARDIOWR*
32	I/O	MBUSDATA	72	I	TESTIN	112	O	CARDREG*
33	–	VSS	73	O	VIDDONE	113	I	CARD1WAIT*
34	I/O	MBUSCLK	74	I	TESTAIU	114	–	VDD (PLL)
35	–	VDD	75	–	VSS	115	O	CARDDIR*
36	–	VDD	76	I	VCC3	116	–	VDD
37	O	SIBMCLK	77	O	BC32K	117	O	CARD1CSL*
38	–	VSS	78	–	VDD	118	O	CARD1CSH*
39	O	SIBSCLK	79	I	C32KIN	119	–	VSS
40	O	SIBSYNC	80	O	C32KOUT	120	O	MCS3*

*Active-low signal

NO.	I/O	SIGNAL NAME	NO.	I/O	SIGNAL NAME	NO.	I/O	SIGNAL NAME
121	O	MCS2*	161	–	NC	201	–	VDD
122	O	MCS1*	162	O	CS0*	202	O	DCKE
123	O	MCS0*	163	O	RD*	203	–	VSS
124	O	CS3*	164	–	VSS	204	I	DCLKIN
125	O	CS2*	165	–	VDD	205	O	DCLKOUT
126	O	CS1*	166	O	DGRNT*	206	–	VDD
127	–	VDD	167	I	DREQ*	207	O	DQMH (DQML)
128	I	SYSCLKIN	168	O	ALE	208	O	DQML (DQMH)
129	O	SYSCLKOUT	169	O	WE*			
130	–	VSS	170	–	VDD			
131	–	VSS	171	I/O	A[12]			
132	–	VDD	172	I/O	A[11]			
133	I/O	D[31] (D [7])	173	–	VSS			
134	I/O	D[30] (D [6])	174	I/O	A[10]			
135	–	VSS	175	I/O	A[9]			
136	I/O	D[29] (D [5])	176	–	VDD			
137	–	VDD	177	I/O	A[8]			
138	I/O	D[28] (D [4])	178	I/O	A[7]			
139	I/O	D[27] (D [3])	179	–	VSS			
140	–	VSS	180	I/O	A[6]			
141	I/O	D[26] (D [2])	181	I/O	A[5]			
142	–	VSS	182	–	VDD			
143	I/O	D[25] (D [1])	183	I/O	A[4]			
144	–	VDD	184	–	VSS			
145	I/O	D[24] (D [0])	185	I/O	A[3]			
146	I/O	D[23] (D [15])	186	I/O	A[2]			
147	–	VDD	187	–	VDD			
148	I/O	D[22] (D [14])	188	I/O	A[1]			
149	–	VSS	189	I/O	A[0]			
150	I/O	D[21] (D [13])	190	–	VSS			
151	–	VDD	191	–	VSS			
152	I/O	D[20] (D [12])	192	O	DCS0*			
153	I/O	D[19] (D [11])	193	O	RAS1*			
154	–	VSS	194	O	RAS0*			
155	I/O	D[18] (D [10])	195	O	CAS3* (CAS0*)			
156	–	VDD	196	–	VDD			
157	I/O	D[17] (D [9])	197	O	CAS2* (CAS1*)			
158	–	VSS	198	O	CAS1* (CAS2*)			
159	I/O	D[16] (D [8])	199	O	CAS0* (CAS3*)			
160	–	VDD	200	–	VSS			

*Active-low signal

( ) indicates the signal name in the Little endian mode

4.2 PIN FUNCTIONS

- Memory Pins

NAME	I/O	DESCRIPTION
D[31:0]	I/O	These pins are the data bus for the system. 8-bit SDRAMs should be connected to bits 7:0 and 16-bit SDRAMs and DRAMs should be connected to bits 15:0. All other 16-bit ports should be connected to bits 31:16. Of course, 32-bit ports should be connected to be bits 31:0. These pins are normally outputs and only become inputs during reads, thus no resistors are required since the bus will only float for a short period of time during bus turn-around.
A[12:0]	O	These pins are the address bus for the system. The address lines are multiplexed and can be connected directly to SDRAM and DRAM devices. To generate the full 26-bit address for static devices, an external latch must be used to latch the signals using the ALE signal. For static devices, address bits 25:13 are provided by the external latch and address bits 12:0 (directly connected from the TMPR3912AU's address bus) are held afterward by the TMPR3912AU for the remainder of the address bus cycle.
ALE	O	This pin is used as the address latch enable to latch A[12:0] using an external latch, for generating the upper address bits 25:13.
RD*	O	This pin is used as the read signal for static devices. This signal is asserted for reads from MC3*-0*, CS3*-0*, CARD2CS* and CARD1CS* for memory and attribute space.
WE*	O	This pin is used as the write signal for system. This signal is asserted for writes to MC3*-0*, CS3*-0*, CARD2CS* and CARD1CS* for memory and attribute space, and for writes to DRAM and SDRAM.
CAS0*(WE0*)	O	This pin is used as the CAS signal for SDRAMs, the CAS signal for D[7:0] for DRAMs, and the write enable signal for D[7:0] for static devices.
CAS1*(WE1*)	O	This pin is used as the CAS signal for D[15:8] for DRAMs, and the write enable signal for D[15:8] for static devices.
CAS2*(WE2*)	O	This pin is used as the CAS signal for D[23:16] for DRAMs, and the write enable signal for D[23:16] for static devices.
CAS3*(WE3*)	O	This pin is used as the CAS signal for D[31:24] for DRAMs, and the write enable signal for D[31:24] for static devices.
RAS0*	O	This pin is used as the RAS signal for SDRAMs and the RAS signal for Bank0 DRAMs.
RAS1*(DCS1*)	O	This pin is used as the chip select signal for Bank1 SDRAMs and the RAS signal for Bank1 DRAMs.

*Active-low signal

NAME	I/O	DESCRIPTION
DCS0*	O	This pin is used as the chip select signal for Bank0 SDRAMs.
DCKE	O	This pin is used as the clock enable for SDRAMs.
DCLKIN	I	This pin must be tied externally to the DCLKOUT signal and is used to match skew for the data input when reading from SDRAM and DRAM devices.
DCLKOUT	O	This pin is the (nominal) 73.728MHz clock for the SDRAMs.
DQMH	O	This pin is the upper data mask for a 16-bit SDRAM configuration.
DQML	O	This pin is the lower data mask for a 16-bit SDRAM or an 8-bit SDRAM configuration.
CS3-0*	O	These pins are the Chip Select 3 through 0 signals. They can be configured to support either 32-bit or 16-bit ports.
MCS3-0*	O	These pins are the MagicCard Chip Select 3 through 0 signals. They only support 16-bit ports.
CARD2CSH*, L*	O	These pins are the Chip Select signals for PCMCIA card slot 2.
CARD1CSH*, L*	O	These pins are the Chip Select signals for PCMCIA card slot 1.
CARDREG*	O	This pin is the REG* signal for the PCMCIA cards.
CARDIORD*	O	This pin is the IORD* signal for the PCMCIA IO cards.
CARDIOWR*	O	This pin is the IOWR* signal for the PCMCIA IO cards.
CARDDIR*	O	This pin is used to provide the direction control for bi-directional data buffers used for the PCMCIA slot(s). This signal will assert whenever CARD2CSH* or CARD2CSL* or CARD1CSH* or CARD1CSL* is asserted and a read transaction is taking place.
CARD2WAIT*	I	This pin is the card wait signal from PCMCIA card slot 2.
CARD1WAIT*	I	This pin is the card wait signal from PCMCIA card slot 1.

*Active-low signal

- Bus Arbitration Pins

NAME	I/O	DESCRIPTION
DREQ*	I	This pin is used to request external arbitration. If the TESTAIU signal is high and the TESTAIU function has been enabled, then once DGRNT* is asserted, external logic can initiate reads or writes to the TMPR3912AU registers by driving the appropriate input signals. If the TESTAIU signal is low or the TESTAIU function has not been enabled, then the TMPR3912AU memory transactions are halted and certain memory signals will be tri-stated when DGRNT* is asserted in order to allow an external master to access memory.
DGRNT*	O	This pin is asserted in response to DREQ* to inform the external test logic or bus master that it can now begin to drive signals.

*Active-low signal

- Clock Pins

NAME	I/O	DESCRIPTION
SYSCLKIN	I	This pin should be connected along with SYSCLKOUT to an external crystal which is the main TMPR3912AU clock source.
SYSCLKOUT	O	This pin should be connected along with SYSCLKIN to an external crystal which is the main TMPR3912AU clock source.
C32KIN	I	This pin along with C32KOUT should be connected to a 32.768 kHz crystal.
C32KOUT	O	This pin along with C32KIN should be connected to a 32.768 kHz crystal.
BC32K	O	This pin is a buffered output of the 32.768 kHz clock.

- CHI Pins

NAME	I/O	DESCRIPTION
CHIFS	I/O	This pin is the CHI frame synchronization signal. This pin is available for use in one of two modes. As an output, this pin allows the TMPR3912AU to be the master CHI sync source. As an input, this pin allows an external peripheral to be the master CHI sync source and the TMPR3912AU CHI module will slave to this external sync.
CHICLK	I/O	This pin is the CHI clock signal. This pin is available for use in one of two modes. As an output, this pin allows the TMPR3912AU to be the master CHI clock source. As an input, this pin allows an external peripheral to be the master CHI clock source and the TMPR3912AU CHI module will slave to this external clock.
CHIDOUT	O	This pin is the CHI serial data output signal.
CHIDIN	I	This pin is the CHI serial data inaut signal.

- IO Pins

NAME	I/O	DESCRIPTION
IO[6:0]	I/O	These pins are general purpose input/output ports. Each port can be independently programmed as an input or output port. Each port can generate a separate positive and negative edge interrupt. Each port can also be independently programmed to use a 16 to 24ms debouncer.
MIOX[1:0]	I/O	These pins are multi-function input/output ports. Each port can be independently programmed as an input or output port, or can be programmed for multi-function use to support test signals (for debugging purposes only). Each port can generate a separate positive and negative edge interrupt. Note that 30 other multi-function pins are available for usage as multi-function input/output ports. These pins are named after their respective standard/normal function and are not listed here.

- Magicbus Pins

NAME	I/O	DESCRIPTION
MBUSCLK	I/O	This pin is the bi-directional Magicbus clock signal. MBUSCLK is an input signal whenever the TMPR3912AU is in the slave mode and is an output signal whenever the TMPR3912AU is in the master mode.
MBUSDATA	I/O	This pin is the bi-directional Magicbus data signal. MBUSDATA is an input signal whenever the TMPR3912AU is in the slave mode and is an output signal whenever the TMPR3912AU is in the master mode.
MBUSINT	I	This pin is the Magicbus interrupt signal. This signal is used to interrupt the TMPR3912AU whenever a peripheral has been attached to or detached from the bus, or whenever a periaheral has initiated an interrupt event.

- Reset Pins

NAME	I/O	DESCRIPTION
CPURES*	I	This pin is used to reset the CPU core. This pin should be connected to a switch for initiating a reset in the event that a software problem might hang the CPU core. The pin should also be pulled up to VSTANDBY† through an external pull-up resistor.
PON*	I	This pin serves as the Power On Reset signal for the TMPR3912AU. This signal must remain low when VSTANDBY is asserted until VSTANDBY is stable. Once VSTANDBY† is asserted, this signal should never go low unless all power is lost in the system.

† VSTANDBY : This signal provides power for the TMPR3912AU and other components in the system that must never lose power. This signal should always be asserted if there is either a good Main Backup Battery, or if a Battery Charger is plugged in.

- Power Supply Pins

NAME	I/O	DESCRIPTION
ONBUTN	I	This pin is used as the On Button for the system. Asserting this signal will cause PWRCS to set to indicate to the System Power Supply to turn power on to the system. PWRCS will not assert if the PWROK signal is low.
PWRCS	O	This pin is used as the chip select for the System Power Supply. When the system is off, the assertion of this signal will cause the System Power Supply to turn VCCDRAM†† and VCC3 on to power up the system. The Power Supply will latch SPI commands on the falling edge of PWRCS.
PWROK	I	This pin provides a status from the System Power Supply that there is a good source of power in the system. This signal typically will be asserted if there is a Battery Charger supplying current or if the Main Battery is good and the Battery Door is closed. If PWROK is low when the system is powered off, PWRCS will not assert as a result of the user pressing the ONBUTN or an interrupt attempting to wake up the system. If the device is on when the PWROK signal goes low, the software will immediately shut down the system since power is about to be lost. When PWROK goes low, there must be ample warning so that the software can shut down the system before power is actually lost.
PWRINT	I	This pin is used by the System Power Supply to alert the software that some status has changed in the System Power Supply and the software should read the status from the System Power Supply to find out what has changed. These will be low priority events, unlike the PWROK status, which is a high priority emergency case.
VCC3	I	This pin provides the status of the power supply for the ROM, TC35143F, system buffers, and other transient components in the system. This signal will be asserted by the System Power Supply when PWRCS is asserted, and will always be turned off when the system is powered down.

†† VCCDRAM : This signal provides power for the DRAM and/or SDRAM. This supply must be off when VSTANDBY is first asserted, and remain off until the system is powered up by the assertion of PWRCS. When the software subsequently powers down the system it may choose to keep this supply on to preserve the contents of memory.

- SIB Pins

NAME	I/O	DESCRIPTION
SIBDIN	I	This pin contains the input data shifted from TC35143F and/or external codec device.
SIBDOUT	O	This pin contains the output data shifted to TC35143F and/or external codec device.
SIBSCLK	O	This pin is the serial clock sent to TC35143F and/or external codec device. The programmable SIBSCLK rate is derived by dividing down from SIBMCLK.
SIBSYNC	O	This pin is the frame synchronization signal sent to TC35143F and/or external codec device. This frame sync is asserted for one clock cycle immediately before each frame starts and all devices connected to the SIB monitor SIBSYNC to determine when they should transmit or receive data.
SIBIRQ	I	This pin is a general purpose input port used for the SIB interrupt source from TC35143F. This interrupt source can be configured to generate an interrupt on either a positive and/or negative edge.
SIBMCLK	I/O	This pin is the master clock source for the SIB logic. This pin is available for use in one of two modes. First, SIBMCLK can be configured as a high-rate output master clock source required by certain external codec devices. In this mode all SIB clocks are synchronously slaved to the main TMPR3912AU system clock CLK2X. Conversely, SIBMCLK can be configured as an input slave clock source. In this mode, all SIB clocks are derived from an external SIBMCLK oscillator source, which is asynchronous with respect to CLK2X. Also, for this mode, SIBMCLK can still be optionally used as a high-rate master clock source required by certain external codec devices.

- SPI Pins

NAME	I/O	DESCRIPTION
SPICLK	O	This pin is used to clock data in and out of the SPI slave device.
SPIOUT	O	This pin contains the data that is shifted into the SPI slave device .
SPIIN	I	This pin contains the data that is shifted out of the SPI slave device.

- UART and IR Pins

NAME	I/O	DESCRIPTION
TXD	O	This pin is the UART transmit signal from the UARTA module.
RXD	I	This pin is the UART receive signal to the UARTA module.
IROUT	O	This pin is the UART transmit signal from the UARTB module or the Consumer IR output signal if Consumer IR mode is enabled.
IRIN	I	This pin is the UART receive signal to the UARTB module.
RXPWR	O	This pin is the receiver power output control signal to the external communication IR analog circuitry.
CARDET	I	This pin is the carrier detect input signal from the external communication IR analog circuitry.

- Video Pins

NAME	I/O	DESCRIPTION
FRAME	O	This pin is the frame synchronization pulse signal between the Video Module and the LCD, and is used by the LCD to return its pointers to the top of the display. The Video Module asserts FRAME after all the lines of the LCD have been shifted and transferred, producing a full frame of display.
DF	O	This pin is the AC signal for the LCD. Since LCD plasma tends to deteriorate whenever subjected to a DC voltage, the DF signal is used by the LCD to alternate the polarity of the row and column voltages used to turn the pixels on and off. The DF signal can be configured to toggle on every frame or can be configured to toggle every programmable number of LOAD signals.
LOAD	O	This pin is the line synchronization pulse signal between the Video Module and the LCD, and is used by the LCD to transfer the contents of its horizontal line shift register to the LCD panel for display. The Video Module asserts LOAD after an entire horizontal line of data has been shifted into the LCD.
CP	O	This pin is the clock signal for the LCD. Data is pushed by the Video Module on the rising edge of CP and sampled by the LCD on the falling edge of CP.
VDAT[3:0]	O	These pins are the data for the LCD. These signals are directly connected to the LCD for 4-bit non-split displays. For 4-bit split and 8-bit non-split displays, an external register is required to demultiplex the 4-bit data into the desired 8 parallel data lines needed for the LCD.
DISPON	O	This pin is the display-on enable signal for the LCD.
VIDDONE	O	This pin is used to externally synchronize events to periods when the video is not shifting.

- Endianess Pins

NAME	I/O	DESCRIPTION
ENDIAN	I	This pin is used to select the endianess of the TMPR3912AU. The "1" level input sets the endianess to the big endian, while the "0" level input to the little endian.

- Test Pins

NAME	I/O	DESCRIPTION
TESTAIU	I	This pin is used to define if the Boot ROM is 16 or 32 bits wide. If the TESTAIU pin is asserted during reset, the BIU will assume a 32-bit Boot ROM. The TESTAIU pin should remain static (either high or low).
TESTCPU	I	This pin is used for debugging purposes only. Then the TESTCPU should not be asserted.
TESTIN	I	This pin is used for debugging purposes only. Then the TESTIN should not be asserted.

- Spare Pins

NAME	I/O	DESCRIPTION
NC	NC	These pins are reserved for future use and should be left unconnected.

- Power Supply Pins

NAME	I/O	DESCRIPTION
VDD (34 pins)	V	These pins are the power pins for the TMPR3912AU.
VSS (34 pins)	G	These pins are the ground pins for the TMPR3912AU.
VDD (for PLL)	V	This pin is the analog power pin for the TMPR3912AU. Keep away from other VDD.
VSS (for PLL)	G	This pin is the analog ground pin for the TMPR3912AU. Keep away from other VSS.

4.3 PIN USAGE INFORMATION

This section contains tables summarizing various aspects of the pin usage for the TMPR3912AU. TABLE 4.3a lists the standard versus multi-function usage for each TMPR3912AU pin, if applicable. Those signal names shown in parentheses are test signals for debugging purposes only. The column showing the multi-function select signal and reset state indicates the internal control signal used to select the multi-function mode, as well as the default configuration of each multi-function pin during reset. The "Bus Arb State" column shows which pins are tri-stated whenever the DGRNT* signal is asserted in response to a DREQ*(external bus arbitration request).

TABLE 4.3a TMPR3912AU STANDARD and MULTI-FUNCTION PIN USAGE

TMPR3912AU pin	Standard Function (I = input, O = output)	Multi-function	Multi-function select (Reset State: 1 = multi-function mode selected; 0 = standard function & mode selected)	Bus Arb State
D[31:0]	D[31:0] (I/O)			Hi-Z
A[12:0]	A[12:0] (I/O)			
ALE	ALE (O)			Hi-Z
RD*	RD* (O)			Hi-Z
WE*	WE* (O)			Hi-Z
CAS0* (WE0*)	CAS0* (O)			Hi-Z
CAS1* (WE1*)	CAS1* (O)			Hi-Z
CAS2* (WE2*)	CAS2* (O)			Hi-Z
CAS3* (WE3*)	CAS3* (O)			Hi-Z
RAS0*	RAS0* (O)			Hi-Z
RAS1* (DCS1*)	RAS1* (O)			Hi-Z
DCS0*	DCS0* (O)			Hi-Z
DCKE	DCKE (O)			Hi-Z
DCLKIN	DCLKIN (I)			
DCLKOUT	DCLKOUT (O)			Hi-Z
DQMH	DQMH (O)			Hi-Z
DQML	DQML (O)			Hi-Z
DREQ*	DREQ* (I)	MIO[27]	MIOSEL[27] (0)	
DGRNT*	DGRNT* (O)	MIO[26]	MIOSEL[26] (0)	
SYSCLKIN	SYSCLKIN (I)			
SYSCLKOUT	SYSCLKOUT (O)			
C32KIN	C32KIN (I)			
C32KOUT	C32KOUT (O)			
BC32K	BC32K(O)	MIO[25]	MIOSEL[25] (1)	
VDAT[3]	VDAT[3] (O)	(BERR)	IRQTEST (0)	
VDAT[2]	VDAT[2] (O)			
VDAT[1]	VDAT[1] (O)	(IRQHIGH)	IRQTEST (0)	
VDAT[0]	VDAT[0] (O)	(IRQLOW)	IRQTEST (0)	
CP	CP (O)			
LOAD	LOAD (O)			
DF	DF (O)			
FRAME	FRAME (O)			

TMPR3912AU pin	Standard Function (I = input, O = output)	Multi-function	Multi-function select (reset state: 1 = Multi-function Mode selected; 0 = Standard function & mode selected)	Bus Arb State
DISPON	DISPON (O)			
PWRCS	PWRCS (O)			
PWRINT	PWRINT (I)			
PWROK	PWROK (I)			
ONBUTN	ONBUTN (I)			
CPURES*	CPURES* (I)			
PON*	PON* (I)			
MBUSCLK	MBUSCLK (I/O)			
MBUSDATA	MBUSDATA (I/O)			
MBUSINT	MBUSINT (I)			
TXD	TXD (O)	MIO[24]	MIOSEL[24] (0)	
RXD	RXD (I)	MIO[23]	MIOSEL[23] (0)	
CS0*	CS0* (O)			Hi-Z
CS1*	CS1* (O)	MIO[22]	MIOSEL[22] (0)	
CS2*	CS2* (O)	MIO[21]	MIOSEL[21] (0)	
CS3*	CS3* (O)	MIO[20]	MIOSEL[20] (0)	
MCS0*	MCS0* (O)	MIO[19]	MIOSEL[19] (1)	
MCS1*	MCS1* (O)	MIO[18]	MIOSEL[18] (1)	
MCS2*	MCS2* (O)	MIO[17]	MIOSEL[17] (1)	
MCS3*	MCS3* (O)	MIO[16]	MIOSEL[16] (1)	
CHIFS	CHIFS (I/O)	MIO[31]	MIOSEL[31] (1)	
CHICLK	CHICLK (I/O)	MIO[30]	MIOSEL[30] (1)	
CHIDOUT	CHIDOUT (O)	MIO[29]	MIOSEL[29] (1)	
CHIDIN	CHIDIN (I)	MIO[28]	MIOSEL[28] (1)	
VCC3	VCC3 (I)			
IO6	IO6 (I/O)			
IO5	IO5 (I/O)			
IO4	IO4 (I/O)			
IO3	IO3 (I/O)			
IO2	IO2 (I/O)			
IO1	IO1 (I/O)			
IO0	IO0 (I/O)			
SPICLK	SPICLK (O)	MIO[15]	MIOSEL[15] (0)	
SPIOUT	SPIOUT (O)	MIO[14]	MIOSEL[14] (0)	
SPIIN	SPIIN (I)	MIO[13]	MIOSEL[13] (0)	
SIBSYNC	SIBSYNC (O)			
SIBDOUT	SIBDOUT (O)			
SIBDIN	SIBDIN (I)			
SIBMCLK	SIBMCLK (I/O)	MIO[12]	MIOSEL[12] (0)	
SIBSCLK	SIBSCLK (O)			

TMPR3912AU pin	standard function (I = input, O = output)	multi-function	multi-function select (reset state: 1 = multi-functzon mode selected; 0 = standard function & mode selected)	Bus Arb State
SIBIRQ	SIBIRQ (I)			
RXPWR	RXPWR (O)			
CARDET	CARDET (I)			
IROUT	IROUT (O)			
IRIN	IRIN (I)			
TESTAIU	TESTAIU (I)			
TESTCPU	TESTCPU (I)			
TESTIN	TESTIN (I)			
VIDDONE	VIDDONE (O)			
CARDREG*	CARDREG*(O) (SHOWDINO / CS*)	MIO[11]	MIOSEL[11] (1)	
CARDIOWR*	CARDIOWR* (O)	MIO[10]	MIOSEL[10] (1)	
CARDIORD*	CARDIORD* (O)	MIO[9]	MIOSEL[9] (1)	
CARD1CSL*	CARD1CSL* (O)	MIO[8]	MIOSEL[8] (1)	
CARD1SCH*	CARD1CSH* (O)	MIO[7]	MIOSEL[7] (1)	
CARD2CSL*	CARD2CSL* (O)	MIO[6]	MIOSEL[6] (1)	
CARD2CSH*	CARD2CSH* (O)	MIO[5]	MIOSEL[5] (1)	
CARD1WAIT*	CARD1WAIT* (I)	MIO[4]	MIOSEL[4] (1)	
CARD2WAIT*	CARD2WAIT* (I)	MIO[3]	MIOSEL[3] (1)	
CARDDIR*	CARDDIR* (O)	MIOX[2]	MIOSEL[2] (1)	
MIOX[1]	(MASTER)	MIOX[1]	MIOSEL[1] (1)	
MIOX[0]	(INSFETCH*)	MIOX[0]	MIOSEL[0] (1)	
ENDIAN	ENDIAN (I)			
NC	SPARE			
VDD-34 pins	+ 3.3 V			
VSS-34 pins	GND			

TABLE 4.3b lists various power-down states and conditions for each TMPR3912AU pin. The "Power-Down Control" column shows the conditions which trigger a power-down for each respective pin. This column also shows the reset state for each of these conditions.

The "PON* state" column defines the state of each pin at power-on reset (PON*). This condition is defined as initial power up of the TMPR3912AU, whereby the TMPR3912AU is initialized and the TMPR3912AU pins are reset to the state shown in the table. This state is entered after power is applied for the very first time (VSTANDBY is turned on but VCC3 is still turned off).

The "1st-time power-up state" column defines the state of each pin after power-up mode (RUNNING STATE) is executed for the first time. This mode is defined as VCC3 applied to the entire system and is initiated by the user pressing the ONBUTN while in the power-on reset (PON*) state. Note that the defined state of various pins for 1st-time power-up may depend on the configuration of external devices attached to these pins. After 1st-time power-up, the software could change the state of various pins to be different from those shown in the table. Thereafter, subsequent transitions from SLEEP STATE to RUNNING STATE might result in different states for these pins.

The "power-down state" column defines the state of each pin during power-down mode (SLEEP STATE). This mode is defined as VCC3 turned off to the entire system, except for the TMPR3912AU (RTC and interrupts alive) and any persistent memory.

TABLE 4.3b TMPR3912AU POWER-DOWN PIN USAGE

TMPR3912AU pin	Power-Down Control powerdown = (vccon & vcc3)* (reset state)	PON* state	1st time power-up state	power-down state
D[31:0]	MEMPOWERDOWN	LOW	LOW	LOW
A[12:0]	MEMPOWERDOWN	LOW	LOW	LOW
ALE		LOW	LOW	LOW
RD*	POWERDOWN	LOW	HI	LOW
WE*	MEMPOWERDOWN	LOW	LOW	LOW
CAS0* (WE0*)	MEMPOWERDOWN	LOW	LOW	LOW
CAS1* (WE1*)	MEMPOWERDOWN	LOW	LOW	LOW
CAS2* (WE2*)	MEMPOWERDOWN	LOW	LOW	LOW
CAS3* (WE3*)	MEMPOWERDOWN	LOW	LOW	LOW
RAS0*	MEMPOWERDOWN	LOW	LOW	LOW
RAS1* (DCS1*)	MEMPOWERDOWN	LOW	LOW	LOW
DCS0*	MEMPOWERDOWN	LOW	LOW	LOW
DCKE	MEMPOWERDOWN	LOW	LOW	LOW
DCLKIN				
DCLKOUT	MEMPOWERDOWN	LOW	LOW	LOW
DQMH	MEMPOWERDOWN	LOW	LOW	LOW
DQML	MEMPOWERDOWN	LOW	LOW	LOW
DREQ*	POWERDOWN & MIOPD[27] (1)	PULL-DOWN	IN	SELECTABLE
DGRNT*	POWERDOWN & MIOPD[26] (0)	LOW	HI	SELECTABLE
SYSCLKIN	POWERDOWN	OSC OFF	OSC ON	OSC OFF
SYSCLKOUT	POWERDOWN	OSC OFF	OSC ON	OSC OFF

TMPR3912AU pin	Power-Down Control powerdown = (vccon & vcc3)* (reset state)	PON* state	1st time power-up state	power-down state
C32KIN		OSC ON	OSC ON	OSC ON
C32KOUT		OSC ON	OSC ON	OSC ON
BC32K	POWERDOWN & MIOPD[25] (1)	PULL-DOWN	IN	SELECTABLE
VDAT[3]	MODULE DISABLE	LOW	LOW	LOW
VDAT[2]	MODULE DISABLE	LOW	LOW	LOW
VDAT[1]	MODULE DISABLE	LOW	LOW	LOW
VDAT[0]	MODULE DISABLE	LOW	LOW	LOW
CP	MODULE DISABLE	LOW	LOW	LOW
LOAD	MODULE DISABLE	LOW	LOW	LOW
DF	MODULE DISABLE	LOW	LOW	LOW
FRAME	MODULE DISABLE	LOW	LOW	LOW
DISPON	MODULE DISABLE	LOW	LOW	LOW
PWRCS		LOW	HI	LOW
PWRINT				
PWROK				
ONBUTN				
CPURES*				
PON*				
MBUSCLK	MODULE DISABLE	OUT LOW	OUT LOW	OUT LOW
MBUSDATA	MODULE DISABLE	OUT LOW	OUT LOW	OUT LOW
MBUSINT				
TXD	POWERDOWN & MIOPD[24] (0)	LOW	LOW	SELECTABLE
RXD	POWERDOWN & MIOPD[23] (1)	PULL-DOWN	IN	SELECTABLE
CS0*	POWERDOWN	PULL-DOWN	HI	PULL-DOWN
CS1*	POWERDOWN & MIOPD[22] (1)	PULL-DOWN	HI	SELECTABLE
CS2*	POWERDOWN & MIOPD[21] (1)	PULL-DOWN	HI	SELECTABLE
CS3*	POWERDOWN & MIOPD[20] (1)	PULL-DOWN	HI	SELECTABLE
MCS0*	POWERDOWN & MIOPD[19] (0)	IN	IN	SELECTABLE
MCS1*	POWERDOWN & MIOPD[18] (0)	IN	IN	SELECTABLE
MCS2*	POWERDOWN & MIOPD[17] (0)	IN	IN	SELECTABLE
MCS3*	POWERDOWN & MIOPD[16] (0)	IN	IN	SELECTABLE
CHIFS	POWERDOWN & MIOPD[31] (1)	PULL-DOWN	IN	SELECTABLE
CHICLK	POWERDOWN & MIOPD[30] (1)	PULL-DOWN	IN	SELECTABLE
CHIDOUT	POWERDOWN & MIOPD[29] (1)	PULL-DOWN	IN	SELECTABLE
CHIDIN	POWERDOWN & MIOPD[28] (1)	PULL-DOWN	IN	SELECTABLE
VCC3	POWERDOWN	PULL-DOWN		PULL-DOWN
IO6	POWERDOWN & IOPD[6] (1)	PULL-DOWN	IN	SELECTABLE
IO5	POWERDOWN & IOPD[5] (1)	PULL-DOWN	IN	SELECTABLE
IO4	POWERDOWN & IOPD[4] (1)	PULL-DOWN	IN	SELECTABLE
IO3	POWERDOWN & IOPD[3] (1)	PULL-DOWN	IN	SELECTABLE
IO2	POWERDOWN & IOPD[2] (1)	PULL-DOWN	IN	SELECTABLE
IO1	POWERDOWN & IOPD[1] (1)	PULL-DOWN	IN	SELECTABLE
IO0	POWERDOWN & IOPD[0] (1)	PULL-DOWN	IN	SELECTABLE

TMPR3912AU pin	Power-Down Control powerdown = (vccon & vcc3)* (reset state)	PON* state	1st time power-up state	power-down state
SPICLK	POWERDOWN & MIOPD[15] (0)	LOW	LOW	SELECTABLE
SPIOUT	POWERDOWN & MIOPD[14] (0)	LOW	LOW	SELECTABLE
SPIIN	POWERDOWN & MIOPD[13] (1)	PULL-DOWN		SELECTABLE
SIBSYNC	POWERDOWN	LOW	LOW	LOW
SIBDOUT	POWERDOWN	LOW	LOW	LOW
SIBDIN	POWERDOWN	PULL-DOWN		PULL-DOWN
SIBMCLK	POWERDOWN & MIOPD[12] (1)	PULL-DOWN	IN	SELECTABLE
SIBSCLK	POWERDOWN	LOW	LOW	LOW
SIBIRQ	POWERDOWN	PULL-DOWN		PULL-DOWN
RXPWR	POWERDOWN	LOW	LOW	LOW
CARDET	POWERDOWN	PULL-DOWN		PULL-DOWN
IROUT	POWERDOWN	LOW	LOW	LOW
IRIN	POWERDOWN	PULL-DOWN		PULL-DOWN
TESTAIU				
TESTCPU				
TESTIN				
VIDDONE	MODULE DISABLE	LOW	LOW	LOW
CARDREG*	POWERDOWN & MIOPD[11] (1)	PULL-DOWN	IN	SELECTABLE
CARDIOWR*	POWERDOWN & MIOPD[10] (1)	PULL-DOWN	IN	SELECTABLE
CARDIORD*	POWERDOWN & MIOPD[9] (1)	PULL-DOWN	IN	SELECTABLE
CARD1CSL*	POWERDOWN & MIOPD[8] (1)	PULL-DOWN	IN	SELECTABLE
CARD1CSH*	POWERDOWN & MIOPD[7] (1)	PULL-DOWN	IN	SELECTABLE
CARD2CSL*	POWERDOWN & MIOPD[6] (1)	PULL-DOWN	IN	SELECTABLE
CARD2CSH*	POWERDOWN & MIOPD[5] (1)	PULL-DOWN	IN	SELECTABLE
CARD1WAIT*	POWERDOWN & MIOPD[4] (1)	PULL-DOWN	IN	SELECTABLE
CARD2WAIT*	POWERDOWN & MIOPD[3] (1)	PULL-DOWN	IN	SELECTABLE
CARDDIR*	POWERDOWN & MIOPD[2] (1)	PULL-DOWN	IN	SELECTABLE
MIOX[1]	POWERDOWN & MIOPD[1] (0)	IN	IN	SELECTABLE
MIOX[0]	POWERDOWN & MIOPD[0] (0)	IN	IN	SELECTABLE
ENDIAN				
NC				
VDD-34 EACH				
VSS-34 EACH				

5. FUNCTION SPECIFICATIONS

5.1 OUTLINE

The TMPR3912AU consists of PDA system support logic, integrated with the TX39 Processor Core designed by Toshiba. For details of the system support logic and the TX39 processor Core, refer to the User's manual and TX39 family user's manual, respectively.

5.2 TX39 PROCESSOR CORE

The TX39 is a Toshiba-developed microprocessor core based on the R3000A RISC architecture developed by MIPS Technologies, Inc. of the United States.

5.2.1 INSTRUCTIONS

All TX39 Processor Core instructions are 32-bit instructions. Apart from some coprocessor instructions, the instructions are upwardly compatible with the R3000A. The TX39 Processor Core instructions can be classified into six types.

- Load and store instructions

  Transfer data between memory and general-purpose registers.
- Computational instructions

  These include arithmetic, logical, shift, multiply, divide, and multiply-add instructions. The multiply-add instructions are extensions to the R3000A. The multiply instructions can also be used as three-operand instructions.
- Special instructions

  Used for system call or break point.
- Jump and branch instructions

  Change the control flow of a program. The Branch-Likely instruction is provided as an extension to the R3000A.
- Coprocessor instructions

  Perform operations for coprocessors. The R3000A LWCz and SWCz instructions are reserved instructions in the TX39 Processor Core. Attempting execution generates a reserved instruction exception. Note that the COPz, CTCz and MTCz instructions are no-operation instructions, the CFCz and MFCz instructions load undefined data to general purpose registers (rt) in the TMPR3912AU.
- System control coprocessor instructions

  Perform operations on the CP0 registers to manipulate the memory management and exception handling functions of the processor.

5.2.2 REGISTERS

The TX39 Processor Core has following registers.

- 32 general purpose registers (32-bit)
- HI/LO registers

  Hold the result of multiply and divide operation.
- PC (Program Counter)
- Cause register

  Indicates the nature of the most recent exception.
- EPC (Exception Program Counter) register

  Holds the program counter at the time the exception occurred, indicating the address where processing is to resume after the exception processing is completed.
- Status register

  Holds the operating mode status (user mode or kernel mode), interrupt masking status, diagnosis status and other such information.
- BadVAddr (Bad Virtual Address) register

  Holds the most recent virtual address for which a virtual address translation error occurred.
- PRId register

  Shows the revision number of the TX39 Processor Core.
- Cache register

  Controls the instruction cache (reserved) and the data cache auto-lock bits.
- Debug register

  Control software debug exception.
- DEPC

  Program counter for software debug exception.

5.2.3 MEMORY MANAGEMENT

The TX39 Processor Core has a 4G-byte memory address space. The 4G-byte memory space consists of a 2G-byte user area and a 2G-byte kernel area. The kernel area contains a cache area and an uncache area.The TX39 Processor Core provides a full-featured memory management unit (MMU) utilizing an on-chip Translation Lookaside Buffer (TLB). The on-chip TLB major characteristics are :

- 32×64-bit wide entries
- fully associative
- 2 entry micro TLB for instruction address translation
- instruction address translation accesses full TLB after micro-TLB miss
- data address translation accesses full TLB

5.2.4 PIPELINE

The TX39 Processor Core pipeline consists of five stages. The pipeline configuration enables the TX39 Processor Core to execute nearly all instructions in one clock.

5.2.5 CACHE

The TMPR3912AU incorporates a 4K-byte instruction cache and a 1K-byte data cache. The instruction cache is direct-mapped with a block size of 16 bytes. The data cache uses two-way set-associative mapping with a block size of four bytes. The data cache has a lock function that locks data in one direction. The write-through method is used to write data back to memory.

5.2.6 DSP FUNCTION

The TX39 Processor Core has a high-speed multiplier/accumulator and supports 32-bit × 32-bit multiplier operations, with 64-bit accumulator in one cycle.

5.3 PERIPHERAL FUNCTIONS

5.3.1 CLOCK GENERATOR

The TMPR3912AU uses an internal PLL and an external crystal oscillator to generate a clock with eight times the input clock frequency. The PLL oscillation can be halted externally to reduce power dissipation.

5.3.2 WRITE BUFFER

The TMPR3912AU incorporates a four-stage write buffer.

5.3.3 BUS INTERFACE UNIT (BIU) MODULE

The TMPR3912AU has a Bus Interface Unit with the following features.

- supports 2 Banks of SDRAM and/or DRAM / HDRAM
  - 8-bit or 16-bit SDRAM configuration
  - 16-bit or 32-bit DRAM configuration
  - 16-bit or 32-bit HDRAM configuration
  - 4 Mbit, 16 Mbit and 64 Mbit parts supported
  - page mode reads and writes supported
  - independent refresh counters for each bank
  - self refreshing parts supported to retain memory when system is powered down

- 4 general purpose chip selects (CS3*-CS0*)
  - 16-bit or 32-bit ports
  - programmable wait states
  - read page mode
- 4 general purpose chip selects (MCS3*- MCS0*)
  - 16-bit ports
  - programmable wait states
  - read page mode
- 2 full PCMCIA slots
  - 16-bit ports
  - IORD and IOWR provided to support I/O cards
  - WAIT signal supported

5.3.4 SYSTEM INTERFACE UNIT (SIU) MODULE

The TMPR3912AU has a System Interface Unit with the following features.

- multi-channel 32-bit DMA controller
- independent DMA controller for video, Magicbus, SIB to/from TC35143F audio/telecom codecs, high-speed serial port, IR, UART, and general purpose UART
- address decoding for the internal registers

5.3.5 CLOCK MODULE

The TMPR3912AU has a Clock module with the following features.

- The TMPR3912AU supports system-wide single crystal configuration, besides the 32 kHz RTC XTAL (reduces cost, power, and board space)
- common crystal rate divided to generate clock for CPU, video, sound, telecom, UARTs, etc.
- independent enabling or disabling of individual clocks under software control, for power management

5.3.6 CONCENTRATION HIGHWAY INTERFACE (CHI) MODULE

The TMPR3912AU has a CHI module with the following features.

- high-speed serial Concentration Highway Interface (CHI) contains logic for interfacing to external full-duplex serial time-division-multiplexed (TDM) communication peripherals
- supports ISDN line interface chips and other PCM/TDM serial devices
- CHI interface is programmable (number of channels, frame rate, bit rate, etc.) to provide support for a variety of formats
- supports data rates up to 4.096 Mbps
- independent DMA support for CHI receive and transmit

5.3.7 INTERRUPT MODULE

The TMPR3912AU has an Interrupt module with the following features.

- contains logic for individually enabling, reading, and clearing all TMPR3912AU interrupt sources
- interrupts generated from internal TMPR3912AU modules or from edge transitions on external signal pins

5.3.8 IO MODULE

The TMPR3912AU has an IO module with the following features.

- contains support for reading and writing the 7 bi-directional general purpose IO pins and the 32 bi-directional multi-function IO pins
- each IO port can generate a separate positive and negative edge interrupt
- independently configurable IO ports allow the TMPR3912AU to support a flexible and wide range of system applications and configurations

5.3.9 IR MODULE

The TMPR3912AU has an IR module with the following features.

- IR consumer mode
  - allows control of consumer electronic devices such as stereos, TVs, VCRs, etc.
  - programmable pulse parameters
  - external analog LED circuitry
- IRDA communication mode
  - not compatible with Gen-I Magic Cap Devices
  - allows communication with other IRDA devices such as FAX machines, copiers, printers, etc.
  - supported by the UART module within the TMPR3912AU
  - external analog receiver preamp and LED circuitry
  - data rate = up to 115 kbps at 1 meter
- IR FSK communication mode
  - compatible with Gen-I Magic Cap Devices
  - supported by the UART module within the TMPR3912AU
  - external analog IR chip(s) perform frequency modulation to generate the desired IR communication mode protocol
  - data rate = up to 36000 bps at 3 meters
- carrier detect state machine
  - periodically enables IR receiver to check if a valid carrier is present

5.3.10 MAGICBUS MODULE

The TMPR3912AU has a Magicbus module with the following features.

- GMI-proprietary serial protocol to communicate with daisy-chainable peripherals and docks
- synchronous, serial 2-wire (clock and data), half-duplex communications protocol
- supports low-cost, low-power peripherals
- compatible with Gen-I Magic Cap Devices
- supports maximum data rate of 14.75 Mbps
- DMA support for Magicbus receive and transmit

5.3.11 POWER MODULE

The TMPR3912AU has a Power module with the following features.

- power-down modes for individual internal peripheral modules
- serial (SPI port) power supply control interface supported
- power management state machine has 3 states: RUNNING, DOZING and SLEEP

5.3.12 SERIAL INTERCONNECT BUS (SIB) MODULE

The TMPR3912AU has a SIB module with the following features.

- The TMPR3912AU contains holding and shift registers to support the serial interface to the TC35413F and/or other optional codec devices
- interface compatible with slave mode 3 of the Crystal CS4216 codec
- synchronous, frame-based protocol
- The TMPR3912AU always master source of clock and frame frequency and phase; programmable clock frequency
- each SIB frame consists of 128 clock cycles, further divided into 2 subframes or words of 64 bits each (supports up to 2 devices simultaneously)
- independent DMA support for audio receive and transmit, telecom receive and transmit
- supports 8-bit or 16-bit mono telecom formats
- supports 8-bit or 16-bit mono or stereo audio formats
- independently programmable audio and telecom sample rates
- CPU read/write registers for subframe control and status

5.3.13 SERIAL PERIPHERAL INTERFACE (SPI) MODULE

The TMPR3912AU has an SPI module with the following features.

- provides interface to SPI peripherals and devices
- full-duplex, synchronous serial data transfers (data in, data out, and clock signals)
- The TMPR3912AU supplies dedicated chip select and interrupt for an SPI interface serial power supply
- 8-bit or 16-bit data word lengths for the SPI interface
- programmable SPI baud rate

5.3.14 TIMER MODULE

The TMPR3912AU has a Timer module with the following features.

- Real Time Clock (RTC) and Timer
- 40-bit counter (30.517 μs granularity); maximum uninterrupted time = 388.36 days
- 40-bit alarm register (30.517 μs granularity)
- 16-bit periodic timer (0.868 μs granularity); maximum timeout = 56.8 ms
- interrupts on alarm, timer, and prior to RTC roll-over

5.3.15 UART MODULE

The TMPR3912AU has a UART module with the following features.

- 2 independent full-duplex UARTs
- programmable baud rate generator
- UARTB port used for serial control interface to external IR module
- UARTA port used for general purpose serial control interface
- UARTA and UARTB DMA support for receive and transmit

5.3.16 VIDEO MODULE

The TMPR3912AU has a Video module with the following features.

- bit-mapped graphics
- supports monochrome, grey scale, or color modes
- time-based dithering algorithm for gray scale and color modes
- supports multiple screen sizes
- supports split and non-split displays
- variable size and relocatable video buffer
- DMA support for fetching image data from video buffer

6. ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATINGS

V_{SS} = 0 V (GND)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	V_{SS}-0.5 to 4.5	V
Input voltage	V_{IN}	V_{SS} - 0.5 to V_{DD} + 0.5	V
Storage temperature	T_{STG}	- 55 to 125	°C
Maximum dissipation (Ta = 70°C)	P_D	1	W

Note: Using an LSI at specifications higher than the maximum ratings can cause permanent damage to the LSI. For normal operation, use under the recommended operating conditions. Exceeding the recommended operating conditions may affect the reliability of the LSI.

6.2 RECOMMENDED OPERATING CONDITIONS

V_{SS} = 0 V (GND)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Power Supply voltage	V_{DD}		3.0	3.3	3.6	V
Operating temperature	T_{OPR}		0	–	70	°C

6.3 DC CHARACTERISTICS

(T_a = 0°C~70°C, V_{DD} = 3.3V±0.3V)

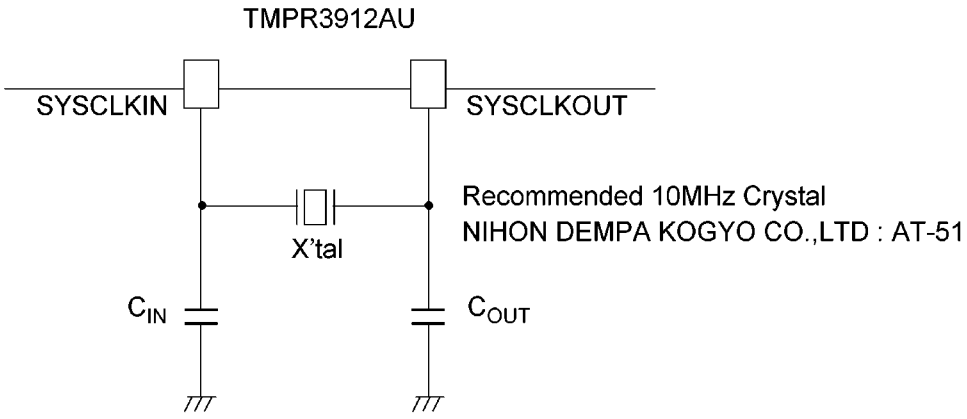
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operating current	I_{DD}	V_{IN} = V_{DD} or V_{SS} V_{DD} = MAX I_{OH} = I_{OL} = 0 mA fin(7)= 10MHz	–	110	130	mA
Static current	$I_{DDS}1$	V_{IN} = V_{DD} or V_{SS} V_{DD} = MAX I_{OH} = I_{OL} = 0 mA SLEEP mode & RTC stop mode	–	10	100	μA
	$I_{DDS}2$	V_{IN} = V_{DD} or V_{SS} V_{DD} = MAX I_{OH} = I_{OL} = 0 mA SLEEP mode & RTC Running mode	–	20	120	μA
Input Leakage current	I_{IN}	V_{IN} = V_{DD} or V_{SS}	-10	–	10	μA
Input voltage (1)	V_{IH1}	V_{DD} = 3.6V	V_{DD}×0.8	–	V_{DD}+0.3	V
	V_{IL1}	V_{DD} = 3.0V	-0.3	–	V_{DD}×0.2	V
Input voltage (2)	V_{IH2}	V_{DD} = 3.6V	2.4	–	V_{DD}+0.3	V
	V_{IL2}	V_{DD} = 3.0V	-0.3	–	0.6	V
Output voltage (3)	V_{OH1}	V_{DD} = 3.0V, I_{OH} = -4mA	V_{DD}-0.6	–	–	V
	V_{OL1}	V_{DD} = 3.0V, I_{OL} = 4mA	–	–	V_{DD}+0.4	V
Output voltage (4)	V_{OH2}	V_{DD} = 3.0V, I_{OH} = -8mA	V_{DD}-0.6	–	–	V
	V_{OL2}	V_{DD} = 3.0V, I_{OL} = 8mA	–	–	V_{DD}+0.4	V
Output voltage (5)	V_{OH3}	V_{DD} = 3.0V, I_{OH} = -16mA	V_{DD}-0.6	–	–	V
	V_{OL3}	V_{DD} = 3.0V, I_{OL} = 16mA	–	–	V_{DD}+0.4	V
Output voltage (6)	V_{OH4}	V_{DD} = 3.0V, I_{OH} = -24mA	V_{DD}-0.6	–	–	V
	V_{OL4}	V_{DD} = 3.0V, I_{OL} = 24mA	–	–	V_{DD}+0.4	V
Input current (Pull-down resister)	I_{IHP}	V_{DD} = MAX VIN = V_{DD}	20	–	120	μA

(1) SYSCLKIN , DCLKIN
(2) Other inputs
(3) D[31;0], RAS0*, RAS1*, DCS0*, DCKE*, DQMH, DQML, DREQ*, DGRNT*, BC32K, VDAT[3:0], CP, LOAD, DF, FRAME, DISPON, VIDDONE, PWRCS, TXD, RXD, CS3-O*, CHIFS, CHICLK, CHIDOUT, CHIDIN, IO[6;0], SPICLK, SPIOUT, SPIIN, SIBSYNC, SIBDOUT, SIBMCLK, SIBCLK, RXPWR, IROUT, CARD1WAIT*, CARD2WAIT*, MIOX[2:0]
(4) A[12:0], ALE, RD*, WE*, CAS3-O*, CARDREG*, CARDIOWR*, CARD1CSL*, CARD1CSH*, CARD2CSL*, CARD2CSH*
(5) DCLKOUT
(6) MBUSCLK, MBUSDATA
(7) fin is the frequency of the clock input from pins SYSCLKIN and SYSCLKOUT

6.4 CRYSTAL OSCILLATOR CHARACTERISTICS

6.4.1 CRYSTAL OSCILLATOR CONDITIONS

(1) 10MHz CRYSTAL



Parameter	Symbol	Recommended value		Unit
		MIN.	MAX.	
Crystal Oscillator frequency	f_{IN}	8.25	9.216	MHz
External capacitors	C_{IN},C_{OUT}	10	33	pF

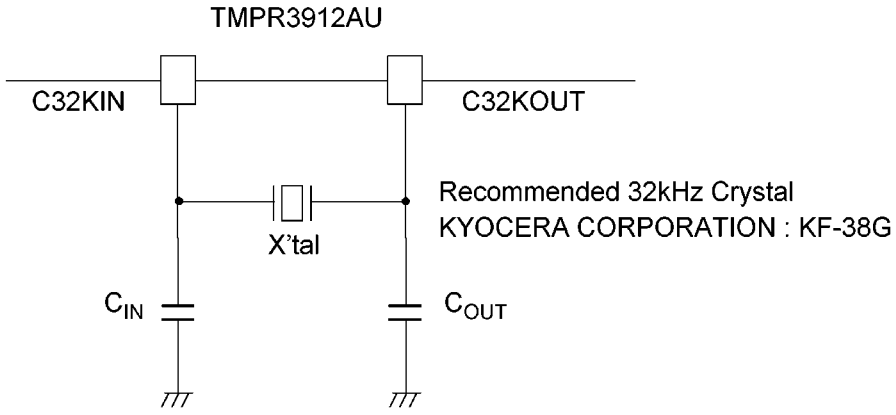
Please note that there are some consideration on the location of the external crystal as follows.

1.Please place the crystal as close to the TMPR3912AU as possible.

2.Please place the crystal as far from data bus lines as possible.

3.Plase surround the crystal area with GND.

(2) 32kHz CRYSTAL



Parameter	Symbol	Recommended value		Unit
		MIN.	MAX.	
External capacitors	C_{IN},C_{OUT}	10	33	pF

Please note that there are some consideration on the location of the external crystal as follows.

1.Please place the crystal as close to the TMPR3912AU as possible.

2.Please place the crystal as far from data bus lines as possible.

3.Plase surround the crystal area with GND.

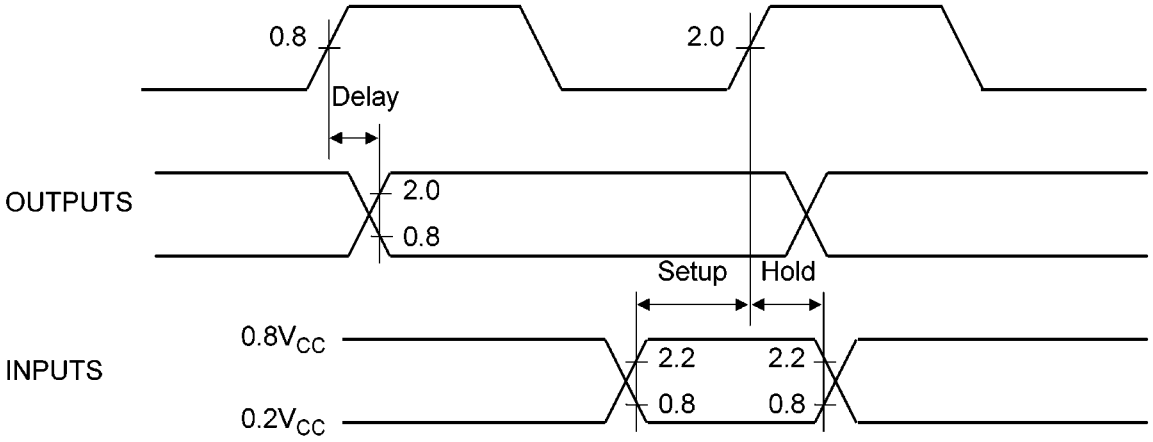
6.4.2 ELECTRICAL SPECIFICATIONS

(V_{SS} = 0V, V_{DD} = 3.3V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Crystal stabilization time 10MHz	$T_{STA-10M}$	f = 8.25MHz~9.216MHz X'tal : AT-51 Cin = Cout = 10pF~33pF	–	–	10	ms
Crystal stabilization time 32kHz	$T_{STA-32k}$	f = 32kHz X'tal : KF-38G Cin = Cout = 10pF~33pF	–	–	2	s

6.5 TMPR3912AU TIMING

6.5.1 DEFINITION OF AC SPECIFICATION



6.6 AC CHARACTERISTICS

The following operating conditions apply to all values specified in this section.

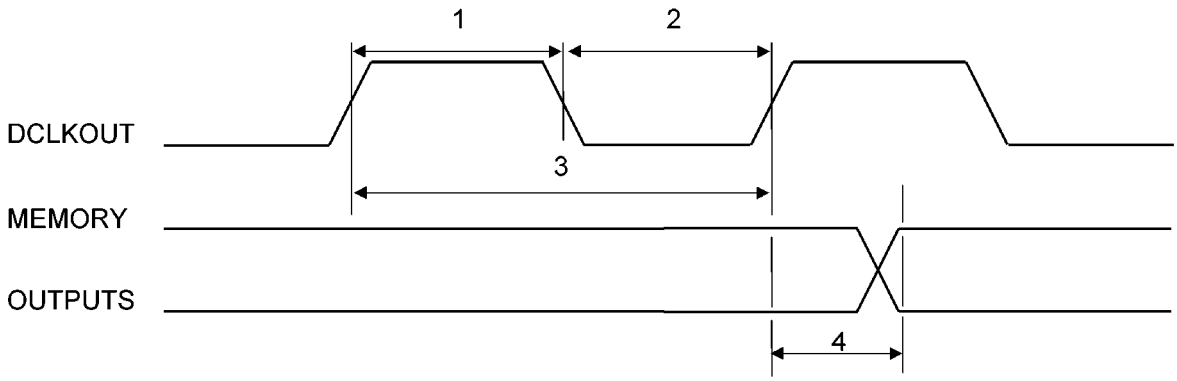
T_a = 0~70 °C, V_{DD} = 3.3±0.3V, External Capacitance = 40pF

<Memory Interface>

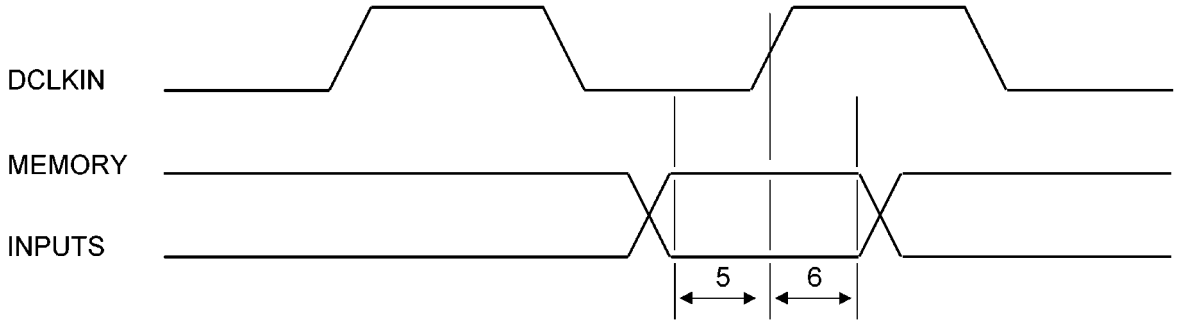
Item	Parameter	Rising / Falling	MIN.	MAX.	Unit
1	DCLKOUT high time	–	5.4	–	ns
2	DCLKOUT low time	–	5.4	–	ns
3	DCLKOUT period	–	13.5	–	ns
4	Delay DCLKOUT to ALE	Rising	–	5	ns
4	Delay DCLKOUT to ALE	Falling	–	3	ns

<Memory Interface>

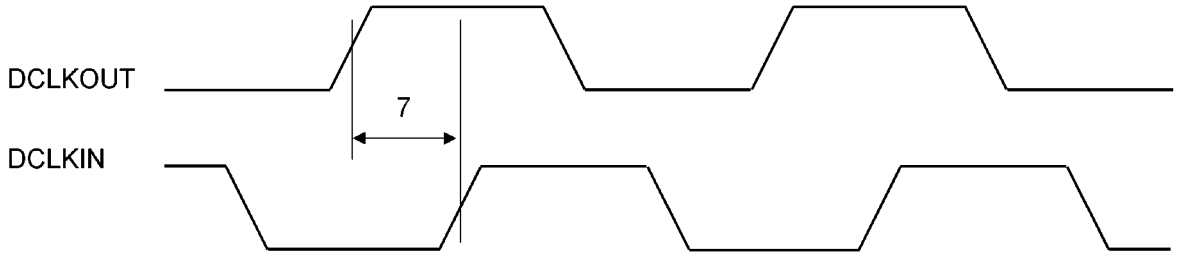
Item	Parameter	Rising / Falling	MIN.	MAX.	Unit
4	Delay DCLKOUT to A[12:0]	–	–	8	ns
4	Delay DCLKOUT to D[31:16]	–	–	8	ns
4	Delay DCLKOUT to D[15:0]	–	1.5	8	ns
4	Delay DCLKOUT to CS3-0*	Rising	–	10	ns
4	Delay DCLKOUT to CS3-0*	Falling	–	10	ns
4	Delay DCLKOUT to RD*	Rising	–	8	ns
4	Delay DCLKOUT to RD*	Falling	–	7	ns
4	Delay DCLKOUT to WE*	Rising	–	5	ns
4	Delay DCLKOUT to WE*	Falling	–	4	ns
4	Delay DCLKOUT to CAS3-0*	Rising	–	2.5	ns
4	Delay DCLKOUT to CAS3-0*	Falling	–	2.5	ns
4	Delay DCLKOUT to CARDxCSx*	Rising	–	9	ns
4	Delay DCLKOUT to CARDxCSx*	Falling	–	8	ns
4	Delay DCLKOUT to CARDDIR*	Rising	–	12	ns
4	Delay DCLKOUT to CARDDIR*	Falling	–	11	ns
4	Delay DCLKOUT to CARDREG*	Rising	–	9	ns
4	Delay DCLKOUT to CARDREG*	Falling	–	10	ns
4	Delay DCLKOUT to CARDIORD*	Rising	–	10	ns
4	Delay DCLKOUT to CARDIORD*	Falling	–	9	ns
4	Delay DCLKOUT to CARDIOWR*	Rising	–	9	ns
4	Delay DCLKOUT to CARDIOWR*	Falling	–	9	ns
4	Delay DCLKOUT to RAS0*	Rising	–	6	ns
4	Delay DCLKOUT to RAS0*	Falling	–	6	ns
4	Delay DCLKOUT to RAS1*	Rising	1.0	8	ns
4	Delay DCLKOUT to RAS1*	Falling	1.0	9	ns
4	Delay DCLKOUT to DQMH/L	Rising	1.0	8	ns
4	Delay DCLKOUT to DQMH/L	Falling	1.0	9	ns
4	Delay DCLKOUT to DCS0*	Rising	1.0	7	ns
4	Delay DCLKOUT to DCS0*	Falling	1.0	6	ns
4	Delay DCLKOUT to DCKE	Rising	1.0	8	ns
4	Delay DCLKOUT to DCKE	Falling	1.0	8	ns
4	Delay DCLKOUT to MCS3-0*	Rising	–	10	ns
4	Delay DCLKOUT to MCS3-0*	Falling	–	10	ns
5	D[31 : 16] to DCLKIN Setup time	–	1	–	ns
6	D[31 : 16] to DCLKIN Hold time	–	2	–	ns
5	D[15:0] to DCLKIN Setup time	–	0	–	ns
6	D[15:0] to DCLKIN Hold time	–	2.5	–	ns
7	DCLKOUT to DCLKIN Board Delay time	–	0	3	ns



Memory Output and Clock Timing



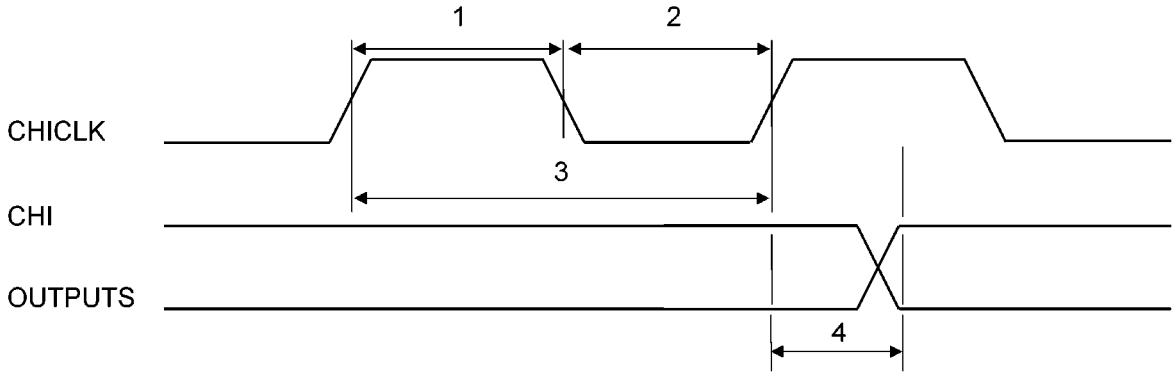
Memory Input Timing



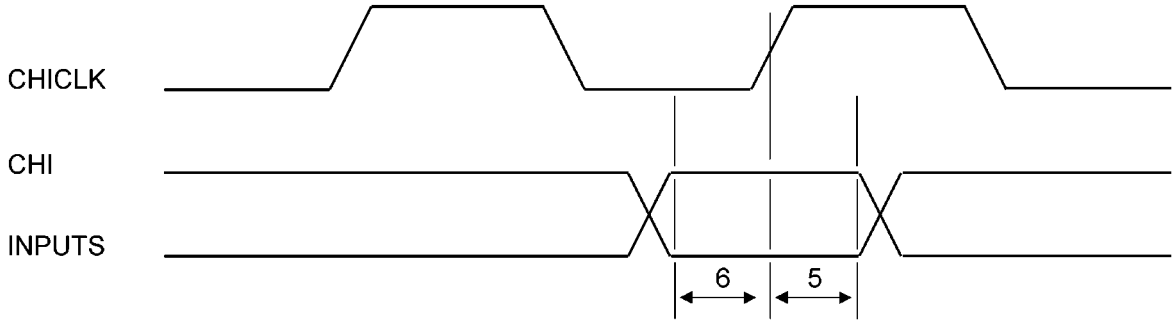
DCLKOUT to DCLKIN

<CHI>

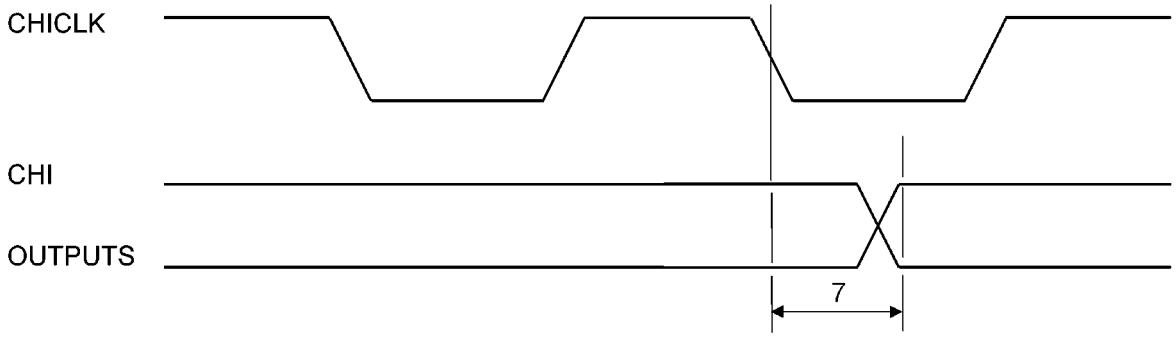
Item	Parameter	Rising / Falling	MIN.	MAX.	Unit
1	CHICLK high time	–	100	–	ns
2	CHICLK low time	–	100	–	ns
3	CHICLK period	–	225	–	ns
4	Delay CHICLK Rising to CHIDOUT(Master)	Rising	–	5	ns
4	Delay CHICLK Rising to CHIDOUT(Master)	Falling	–	5	ns
7	Delay CHICLK Falling to CHIDOUT(Master)	Rising	–	5	ns
7	Delay CHICLK Falling to CHIDOUT(Master)	Falling	–	5	ns
4	Delay CHICLK Rising to CHIFS(Master)	Rising	–	5	ns
4	Delay CHICLK Rising to CHIFS(Master)	Falling	–	5	ns
7	Delay CHICLK Falling to CHIFS(Master)	Rising	–	5	ns
7	Delay CHICLK Falling to CHIFS(Master)	Falling	–	5	ns
4	Delay CHICLK Rising to CHIDOUT(Slave)	Rising	–	15	ns
4	Delay CHICLK Rising to CHIDOUT(Slave)	Falling	–	15	ns
7	Delay CHICLK Falling to CHIDOUT(Slave)	Rising	–	15	ns
7	Delay CHICLK Falling to CHIDOUT(Slave)	Falling	–	15	ns
4	Delay CHICLK Rising to CHIFS(Slave)	Rising	–	15	ns
4	Delay CHICLK Rising to CHIFS(Slave)	Falling	–	15	ns
7	Delay CHICLK Falling to CHIFS(Slave)	Rising	–	15	ns
7	Delay CHICLK Falling to CHIFS(Slave)	Falling	–	15	ns
5	CHIDIN to CHICLK Rising Setup time(Master)	–	20	–	ns
6	CHIDIN to CHICLK Rising Hold time(Master)	–	20	–	ns
8	CHIDIN to CHICLK Falling Setup time(Master)	–	20	–	ns
9	CHIDIN to CHICLK Falling Hold time(Master)	–	20	–	ns
5	CHIFS to CHICLK Rising Setup time(Slave)	–	20	–	ns
6	CHIFS to CHICLK Rising Hold time(Slave)	–	20	–	ns
8	CHIFS to CHICLK Falling Setup time(Slave)	–	20	–	ns
9	CHIFS to CHICLK Falling Hold time(Slave)	–	20	–	ns
5	CHIDIN to CHICLK Rising Setup time(Slave)	–	20	–	ns
6	CHIDIN to CHICLK Rising Hold time(Slave)	–	20	–	ns
8	CHIDIN to CHICLK Falling Setup time(Slave)	–	20	–	ns
9	CHIDIN to CHICLK Falling Hold time(Slave)	–	20	–	ns



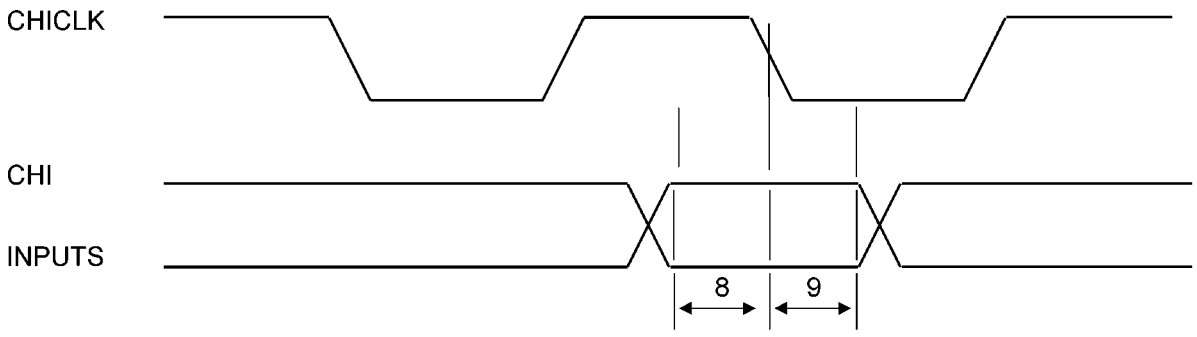
CHI Output and Clock Timing (CHITXEDGE=1)



CHI Input Timing (CHIRXEDGE=1)



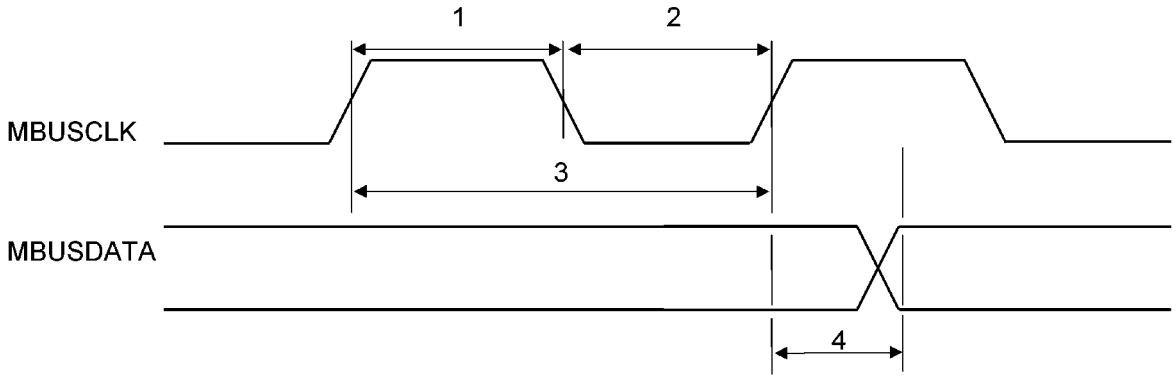
CHI Output and Clock Timing (CHITXEDGE=0)



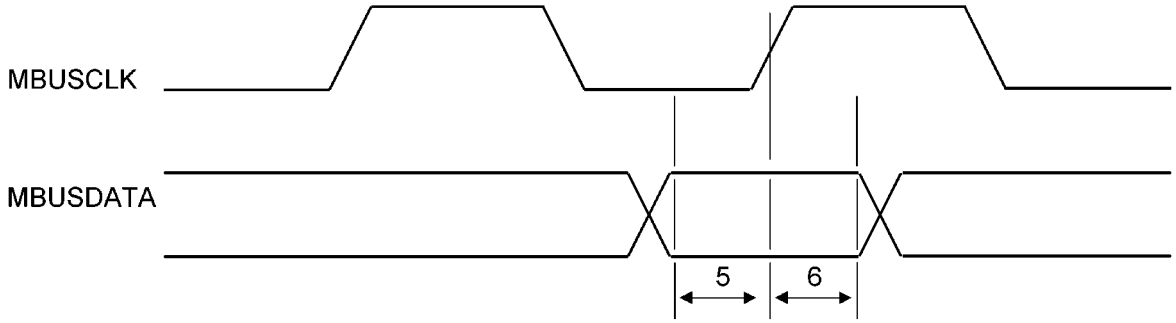
CHI Input Timing (CHIRXEDGE=0)

<Magic Bus>

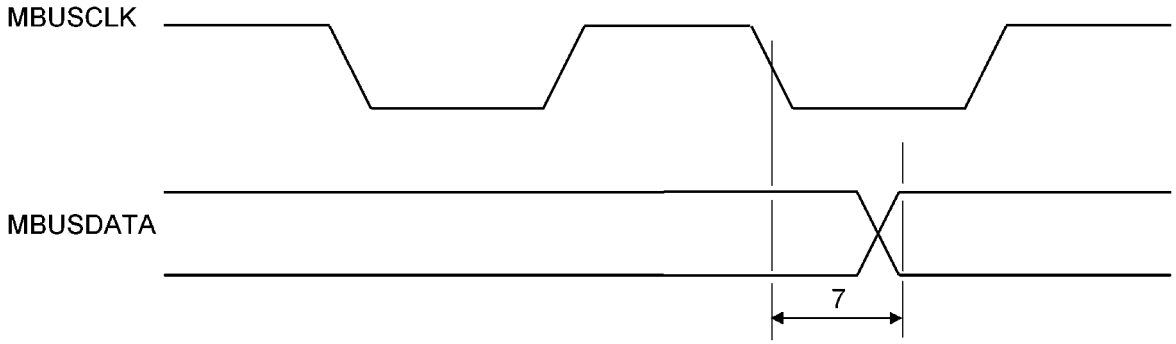
Item	Parameter	Rising / Falling	MIN.	MAX.	Unit
1	MBUSCLK high time	–	10	–	ns
2	MBUSCLK low time	–	10	–	ns
3	MBUSCLK period	–	25	–	ns
4	Delay MBUSCLK Rising to MBUSDATA(Master)	Rising	–	2	ns
4	Delay MBUSCLK Rising to MBUSDATA(Master)	Falling	–	2	ns
7	Delay MBUSCLK Falling to MBUSDATA(Master)	Rising	–	2	ns
7	Delay MBUSCLK Falling to MBUSDATA(Master)	Falling	–	2	ns
5	MBUSDATA to MBUSCLK Rising Setup time(Slave)	–	4	–	ns
6	MBUSDATA to MBUSCLK Rising Hold time(Slave)	–	5	–	ns
8	MBUSDATA to MBUSCLK Falling Setup time(Slave)	–	4	–	ns
9	MBUSDATA to MBUSCLK Falling Hold time	–	5	–	ns



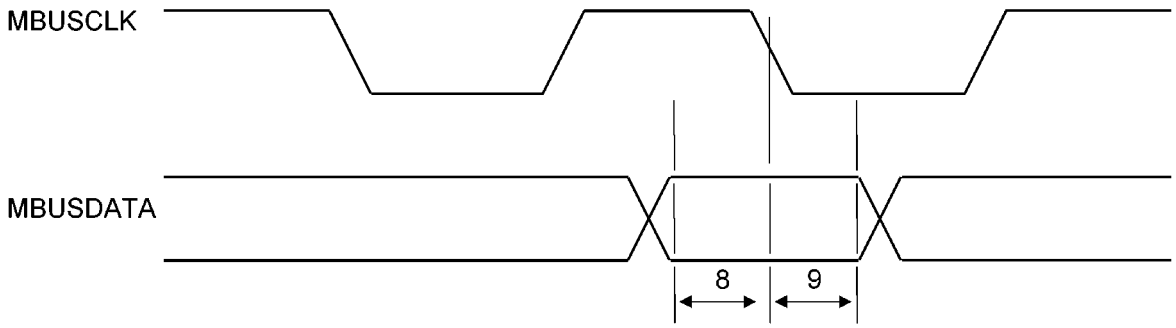
Magic Bus Output and Clock Timing (Master, PHAPOL=1)



Magic Bus Input Timing (Slave, RCVPHAPOL=0)



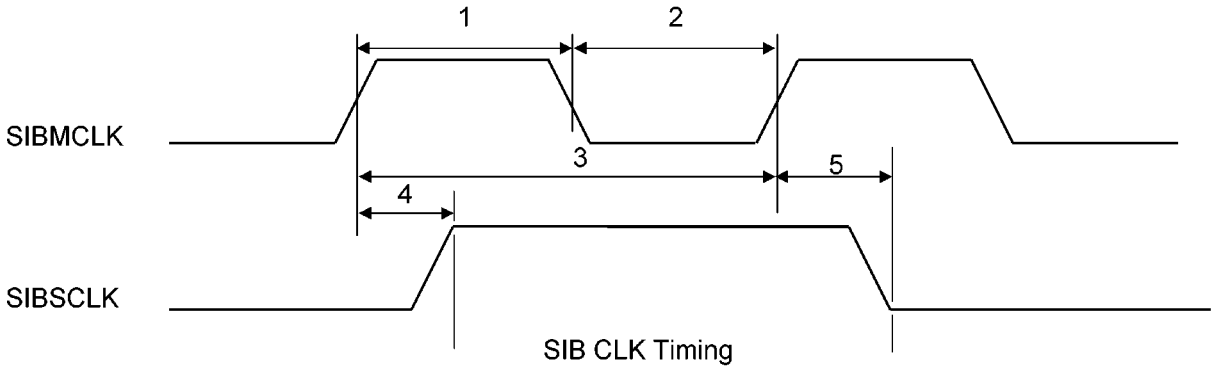
Magic Bus Output and Clock Timing (Master, PHAPOL=0)



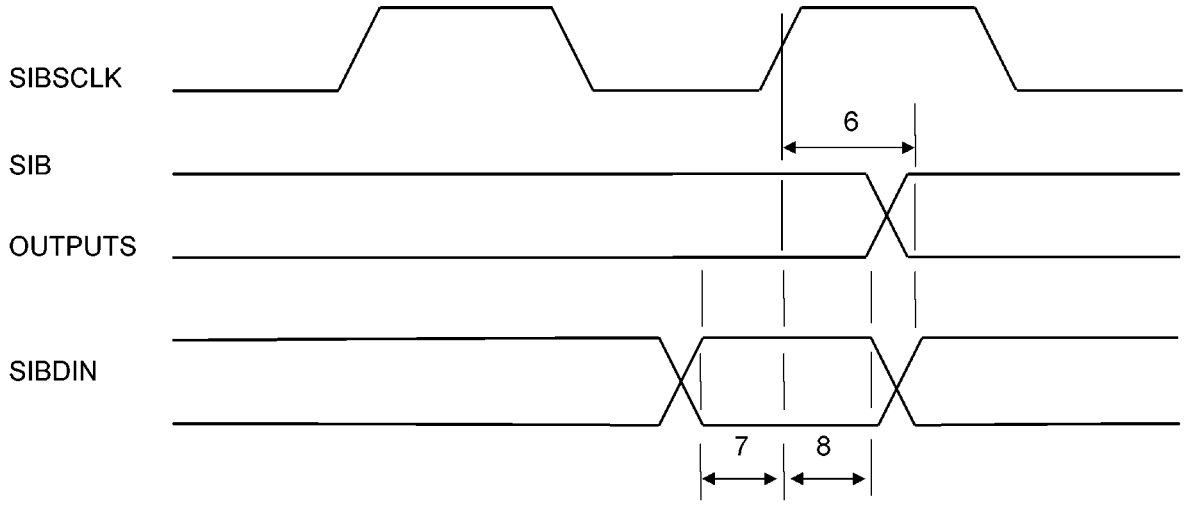
Magic Bus Input Timing (Slave, RCVPHAPOL=1)

<SIB>

Item	Parameter	Rising / Falling	MIN.	MAX.	Unit
1	SIBMCLK high time	–	20	–	ns
2	SIBMCLK low time	–	20	–	ns
3	SIBMCLK period	–	50	–	ns
4	Delay SIBMCLK (Master) to SIBSCLK	Rising	–	5	ns
5	Delay SIBMCLK (Master) to SIBSCLK	Falling	–	5	ns
6	Delay SIBSCLK Rising to SIBSYNC	Rising	–	2	ns
6	Delay SIBSCLK Rising to SIBSYNC	Falling	–	2	ns
6	Delay SIBSCLK Rising to SIBDOUT	Rising	–	2	ns
6	Delay SIBSCLK Rising to SIBDOUT	Falling	–	2	ns
7	SIBDIN to SIBSCLK Rising Setup time	–	20	–	ns
8	SIBDIN to SIBSCLK Rising Hold time	–	0	–	ns



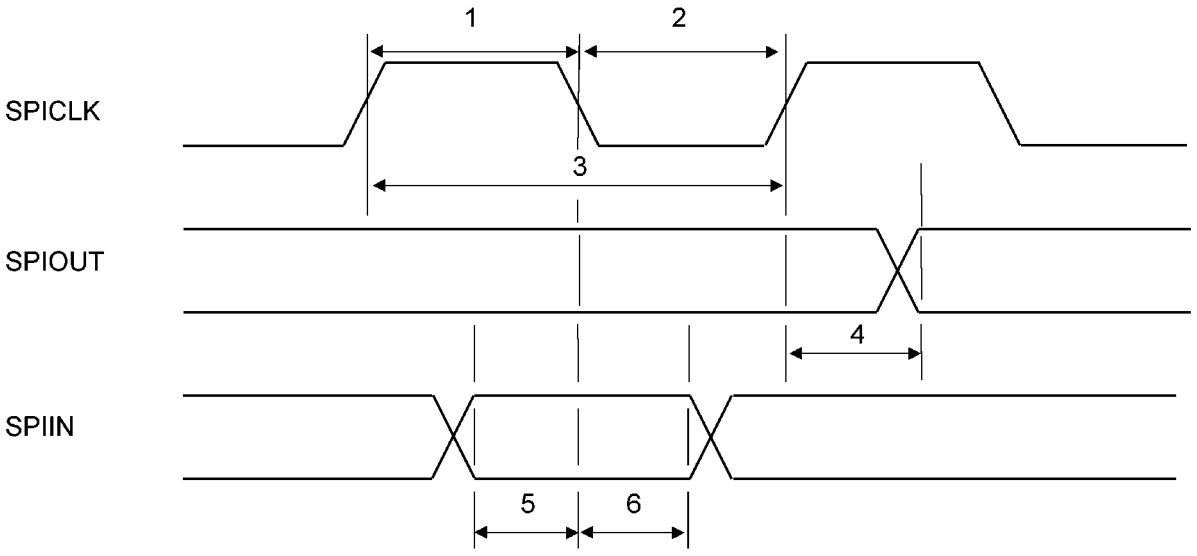
SIB CLK Timing



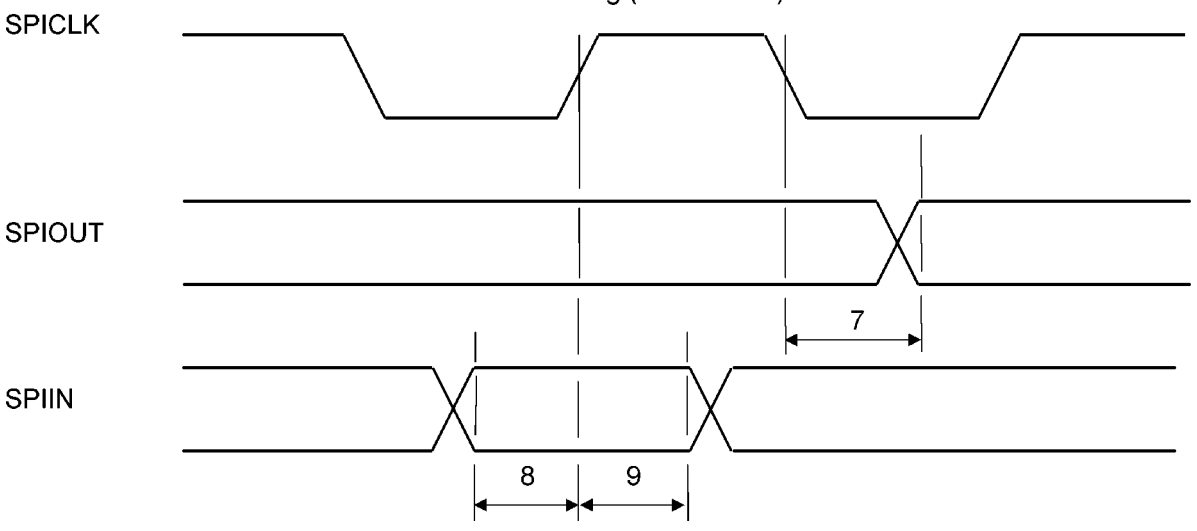
SIB Timing

<SPI>

Item	Parameter	Rising / Falling	MIN.	MAX.	Unit
1	SPICLK high time	–	120	–	ns
2	SPICLK low time	–	120	–	ns
3	SPICLK period	–	250	–	ns
4	Delay SPICLK Rising to SPIOUT	Rising	–	5	ns
4	Delay SPICLK Rising to SPIOUT	Falling	–	5	ns
7	Delay SPICLK Falling to SPIOUT	Rising	–	5	ns
7	Delay SPICLK Falling to SPIOUT	Falling	–	5	ns
5	SPIIN to SPICLK Rising Setup time	–	15	–	ns
6	SPIIN to SPICLK Rising Hold time	–	15	–	ns
8	SPIIN to SPICLK Falling Setup time	–	15	–	ns
9	SPIIN to SPICLK Falling Hold time	–	15	–	ns



SPI Timing (PHAPOL=1)

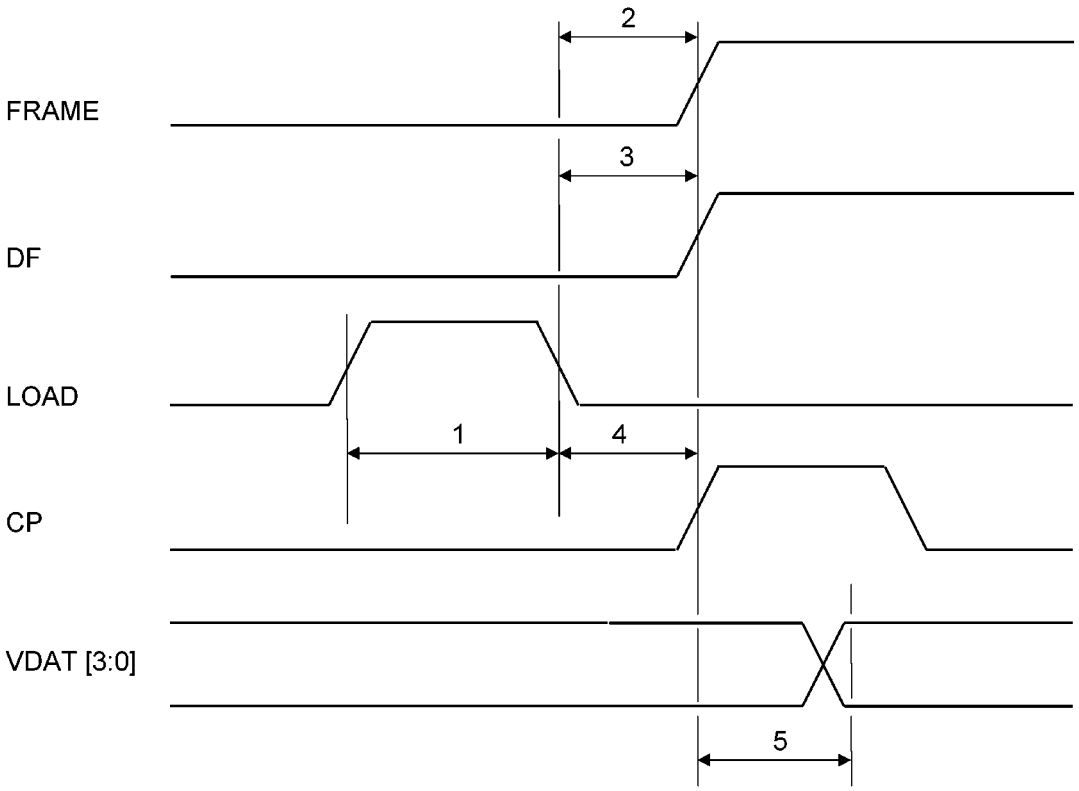


SPI Timing (PHAPOL=0)

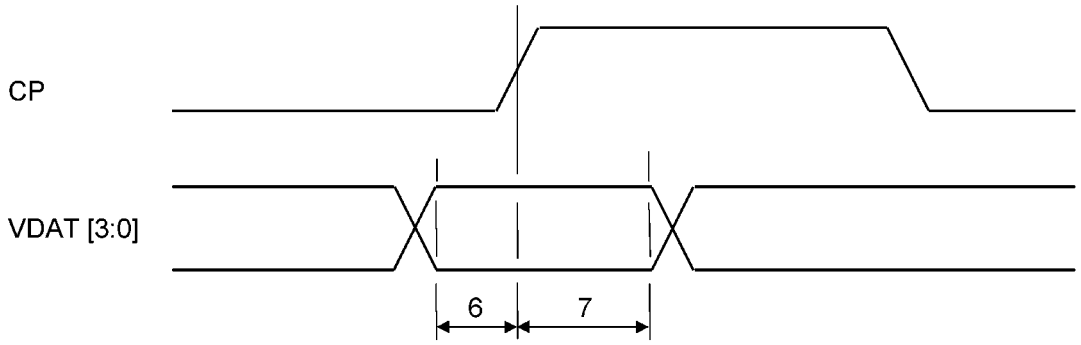
<VIDEO>

Item	Parameter	Rising / Falling	MIN.	MAX.	Unit
1	LOAD Pule width	–	100	1600	ns
2	Delay LOAD Falling to FRAME	–	100	3200	ns
3	Delay LOAD Falling to DF	–	100	3200	ns
4	Delay LOAD Falling to CP	–	100	3200	ns
5	Delay CP Rising to VDAT[3:0]	–	–	5	ns
6	VDAT to CP Rising Setup	–	15	25	ns
7	VDAT to CP Rising Hold	–	15	25	ns

Note: Values shown assume a 75MHz clock for the CPU. Min and Max values are programmable using Video Control Registers.



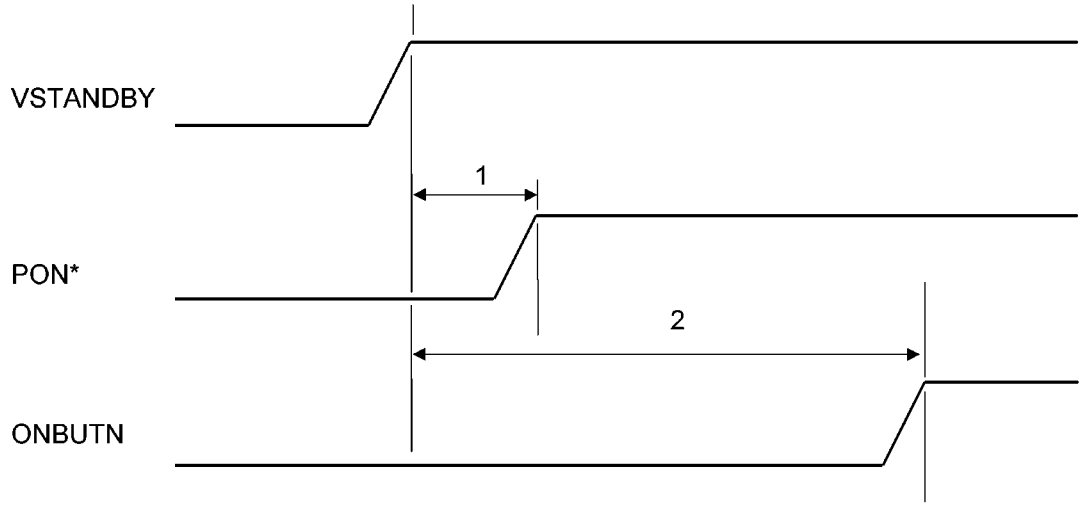
Video Timing, 4 bit non-split LCD



Video Data Timing, 4 bit split LCD and 8 bit non-split LCD

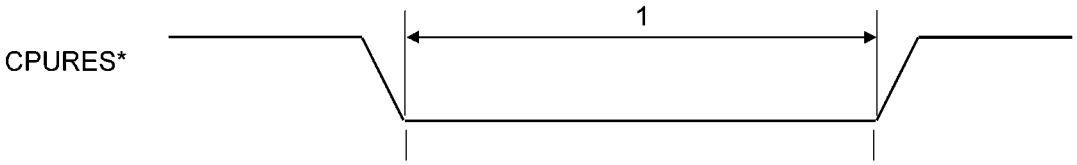
<POWER>

Item	Parameter	Rising / Falling	MIN.	MAX.	Unit
1	VSTANDBY to PON* Rising	–	50	–	ms
2	VSTANDBY to ONBUTN delay time	–	2	–	s



<CPU RESET>

Item	Parameter	Rising / Falling	MIN.	MAX.	Unit
1	CPURES* low time	–	10	–	ns



7. PACKAGE DIMENSION

7.1 TMPR3912AU

LQFP208-P-2828-0.50A Unit : mm