TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

T C 7 M Z 5 4 0 F K

Low Voltage Octal Bus Buffer (inverted) with 5 V Tolerant Inputs and Outputs

The TC7MZ540FK is a high performance CMOS octal bus buffer. Designed for use in 3.3 V systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

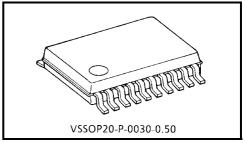
The device is designed for low-voltage $(3.3 \text{ V}) \text{ V}_{CC}$ applications, but it could be used to interface to 5 V supply environment for both inputs and outputs.

The TC7MZ540FK is an inverting 3-state buffer having two active-low output enables. When either $\overline{OE1}$ or $\overline{OE2}$ are high, the terminal outputs are in the high-impedance state. This device is designed to be used with 3-state memory address drivers, etc.

All inputs are equipped with protection circuits against static discharge.



- Low voltage operation: $VCC = 2.0 \sim 3.6 V$
- High speed operation: $t_{pd} = 6.5 \text{ ns} (max) (V_{CC} = 3.0 \sim 3.6 \text{ V})$
- Output current: $|I_{OH}|/I_{OL} = 24 \text{ mA} (\text{min}) (V_{CC} = 3.0 \text{ V})$
- Latch-up performance: ±500 mA
- Package: VSSOP (US20)
- Power down protection is provided on all inputs and outputs.
- Pin and function compatible with the 74 series (74AC/VHC/HC/F/ALS/LS etc.) 540 type.



Weight: 0.03 g (typ.)

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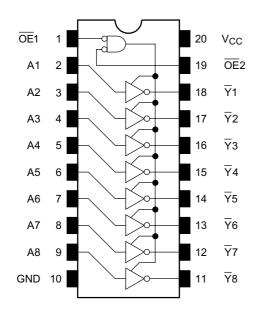
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Pin Assignment (top view)



Truth Table

	Inputs	Outputs	
OE1	OE2	A _n	Outputs
Н	Х	Х	Z
Х	Н	Х	Z
L	L	Н	L
L	L	L	Н

X: Don't care

Z: High impedance

Maximum Ratings

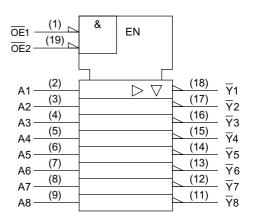
Characteristics	Symbol	Rating	Unit
Supply voltage range	V _{CC}	-0.5~7.0	V
DC input voltage	V _{IN}	-0.5~7.0	V
DC output voltage	Vout	-0.5~7.0 (Note1)	V
DC output voltage	VOUT	-0.5~V _{CC} + 0.5 (Note2)	v
Input diode current	I _{IK}	-50	mA
Output diode current	I _{ОК}	±50 (Note3)	mA
DC output current	IOUT	±50	mA
Power dissipation	PD	180	mW
DC V _{CC} /ground current	I _{CC} /I _{GND}	±100	mA
Storage temperature	T _{stg}	-65~150	°C

Note1: Output in off-state

Note2: High or low state. IOUT absolute maximum rating must be observed.

Note3: $V_{OUT} < GND, V_{OUT} > V_{CC}$

IEC Logic Symbol



Recommended Operating Conditions

Characteristics	Symbol	Rating	Unit	
Supply voltage	V _{CC}	2.0~3.6	V	
Supply vollage	VCC	1.5~3.6 (Note4)	v	
Input voltage	V _{IN}	0~5.5	V	
Output voltage	Value	0~5.5 (Note5)	V	
Output voltage	V _{OUT}	0~V _{CC} (Note6)	v	
Output current	IOH/IOI	±24 (Note7)	mA	
Output current	'OH/'OL	±12 (Note8)	ma	
Operating temperature	T _{opr}	-40~85	°C	
Input rise and fall time	dt/dv	0~10 (Note9)	ns/V	

Note4: Data retention only

Note5: Output in off-state

Note6: High or low state

Note7: V_{CC} = 3.0~3.6 V

Note8: V_{CC} = 2.7~3.0 V

Note9: $V_{IN} = 0.8 \sim 2.0 \text{ V}, V_{CC} = 3.0 \text{ V}$

Electrical Characteristics

DC Characteristics (Ta = -40~85°C)

Characteristics Sv		Symbol	Test Condition			Min	Max	Unit
Cilalacte	ensues	Symbol	Test Condition		V _{CC} (V)	IVIIII	wax	Unit
Input voltage	High level	VIH		—	2.7~3.6	2.0	_	v
input voltage	Low level	V _{IL}		—	2.7~3.6	_	0.8	v
			$V_{IN} = V_{IH} \text{ or } V_{IL}$	I _{OH} = -100 μA	2.7~3.6	V _{CC} - 0.2	_	V
	High level	Vон		$I_{OH} = -12 \text{ mA}$	2.7	2.2	—	
				I _{OH} = -18 mA	3.0	2.4	—	
Output voltage				$I_{OH} = -24 \text{ mA}$	3.0	2.2	—	
	Mai	VIN = VIH or VII	$I_{OL} = 100 \ \mu A$	2.7~3.6	_	0.2		
			I _{OL} = 12 mA	2.7	_	0.4		
	Low level V _{OL}	VOL		I _{OL} = 16 mA	3.0	_	0.4	
				I _{OL} = 24 mA	3.0	_	0.55	
Input leakage cu	urrent	I _{IN}	V _{IN} = 0~5.5 V		2.7~3.6	_	±5.0	μA
3 state output of	ff state current	107	$V_{IN} = V_{IH} \text{ or } V_{IL}$		2.7~3.6	_	±5.0	
3-state output off-state current I _{OZ}		V _{OUT} = 0~5.5 V		2.7-5.0		±3.0	μA	
Power off leaka	ge current	IOFF	$V_{IN}/V_{OUT} = 5.5 V$		0		10.0	μA
Quiescent supply current		1	$V_{IN} = V_{CC}$ or GND		2.7~3.6	—	10.0	
Quiescent supp	younent	Icc	V _{IN} /V _{OUT} = 3.6~5.5 V		2.7~3.6	—	±10.0	μA
Increase in I _{CC}	per input	ΔI_{CC}	$V_{IH} = V_{CC} - 0.6 V$		2.7~3.6	_	500	

AC Characteristics (Ta = -40~85°C)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Min	Max	Unit
Propagation delay time	t _{pLH}	Figure 1, Figure 2	2.7	_	7.5	ns
r topagation delay time	t _{pHL}		$\textbf{3.3}\pm\textbf{0.3}$	1.5	6.5	115
Output enable time	t _{pZL}	Figure 1, Figure 3	2.7		9.5	ns
	t _{pZH}		3.3 ± 0.3	1.5	8.5	
Output disable time	t _{pLZ}	Figure 1, Figure 3	2.7	_	8.5	ns
	t _{pHZ}		3.3 ± 0.3	1.5	7.5	115
Output to output skew	t _{osLH}	(NI-1-10)	2.7		_	ns
	t _{osHL}	(Note10)	3.3 ± 0.3	_	1.0	115

Note10: This parameter is guaranteed by design.

 $(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$

Dynamic Switching Characteristics (Ta = 25°C, Input: $t_r = t_f = 2.5 \text{ ns}$, $C_L = 50 \text{ pF}$, $R_L = 500 \Omega$)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Тур.	Unit
Quiet output maximum dynamic V_{OL}	V _{OLP}	$V_{IH} = 3.3 V, V_{IL} = 0 V$	3.3	0.8	V
Quiet output minimum dynamic VOL	V _{OLV}	$V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$	3.3	0.8	V

Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Тур.	Unit
Input capacitance	C _{IN}	—	3.3	7	pF
Output capacitance	C _{OUT}		3.3	8	pF
Power dissipation capacitance	C _{PD}	$f_{IN} = 10 \text{ MHz}$ (Note11)	3.3	40	pF

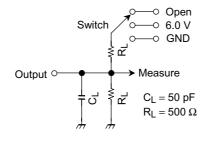
Note11: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation:

 $I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$

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AC Test Circuit



Parameter	Switch
t _{pLH} , t _{pHL}	Open
t _{pLZ} , t _{pZL}	6.0 V
t _{pHZ} , t _{pZH}	GND

Figure 1

AC Waveform

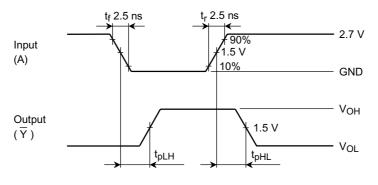
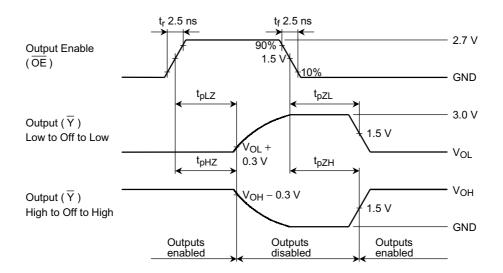
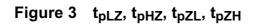


Figure 2 t_{pLH}, t_{pHL}

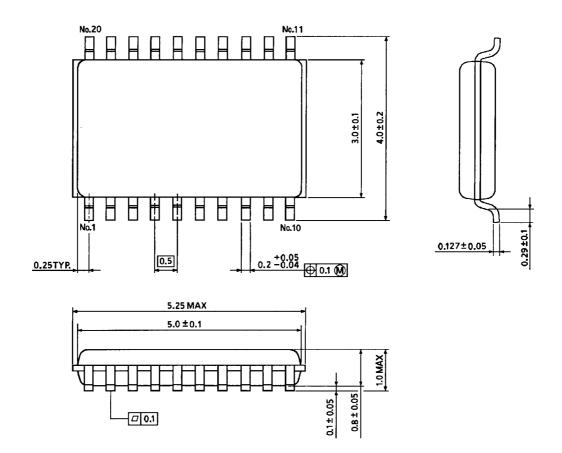




Package Dimensions

VSSOP20-P-0030-0.50

Unit : mm



Weight: 0.03 g (typ.)