TOSHIBA Power Module

M P 7 0 0 3

1. Maximum Ratings (Ta = 25°C)

Diode

Characteristics	Symbol	Rating	Unit
Repetitive peak reverse voltage	V_{RRM}	600	V
Peak one cycle surge forward current (D1, D2, D3, D4) (50 Hz, non-repetitive)	I_{FSM}	220	A
Forward current	I_F	25	A
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40~125	°C

IGBT

Characteristics		Symbol	Rating	Unit
Collector-emitter voltage		V_{CES}	600	V
Gate-emitter voltage		V_{GES}	±20	V
Collector current	DC	I_C	40	A
	1 ms	I_{CP}	80	A
Collector power dissipation (Tc = 25°C)		P_C	37	W
Junction temperature		T_j	150	°C
Storage temperature range		T_{stg}	−40~125	°C

All system

Characteristics	Symbol	Condition	Rating	Unit
Isolation voltage	V_{ISO}	AC 1 minute	2500	V

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2. Electrical Characteristics (Ta = 25°C)

Diode

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Peak forward voltage (1)	V_{FM} (1)	I_F = 12.5 A	—	1.0	1.2	V
Peak forward voltage (2)	V_{FM} (2)	I_F = 30 A	—	1.20	1.55	V
Repetitive peak reverse Current	I_{RRM}	V_{RRM} = 600 V			10	μA
Peak reverse current (D1, D2, D3, D4)	I_{rr}	I_F = 30 A			100	A
Thermal resistance	$R_{th\ (j\text{-}c)}$	—	—	—	3.5	°C/W

IGBT

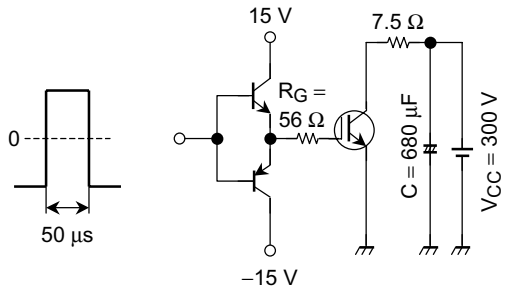
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GES}	V_{GE} = ±20 V, V_{CE} = 0	—	—	±500	nA
Collector cut-off current		I_{CES}	V_{CE} = 600 V, V_{GE} = 0	—	—	1.0	mA
Gate-emitter cut-off voltage		$V_{GE\ (OFF)}$	I_C = 40 mA, V_{CE} = 5 V	3.0	—	6.0	V
Collector-emitter saturation voltage		$V_{CE\ (sat)}$	I_C = 40 A, V_{GE} = 15 V	—	1.9	2.7	V
Input capacitance		C_{ies}	V_{CE} = 10 V, V_{GE} = 0, f = 1 MHz	—	2900	—	pF
Switching time	Rise time	t_r	Load resistance	—	0.4	—	μs
	Turn-on time	t_{on}	V_{CC} = 300 V, I_C = 40 A	—	0.7	—	
	Fall time	t_f	V_{GE} = ±15 V, (R_G = 56 Ω)	—	0.3	0.42	
	Turn-off Time	t_{off}	(Note)	—	0.7	—	
Thermal Resistance		$R_{th\ (j\text{-}c)}$		—	—	3.3	°C/W

3. Mechanical Rating

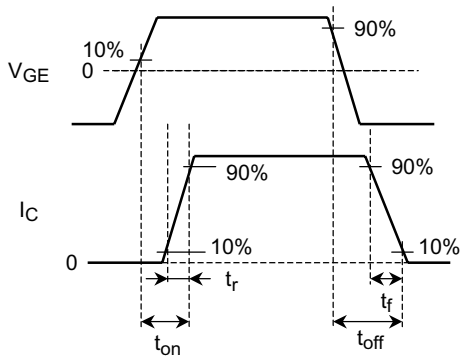
Characteristics	Min	Typ.	Max	Unit
Fastening torque	—	—	1.5	Nm

Note: Switching time test circuit & timing chart

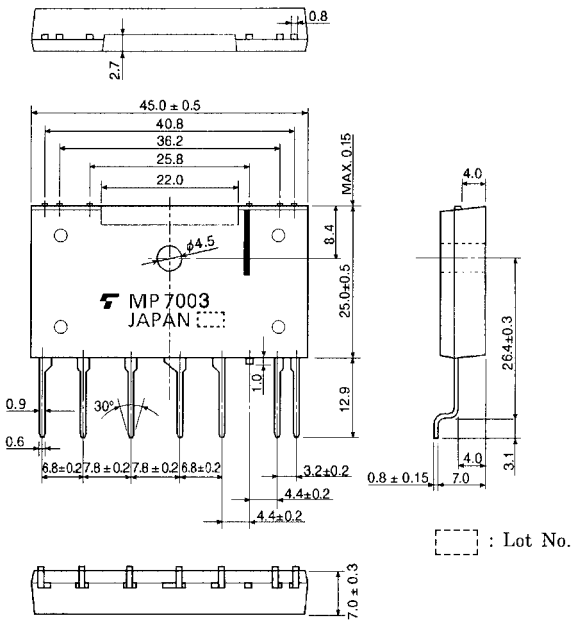
Load Resistance Test Circuit



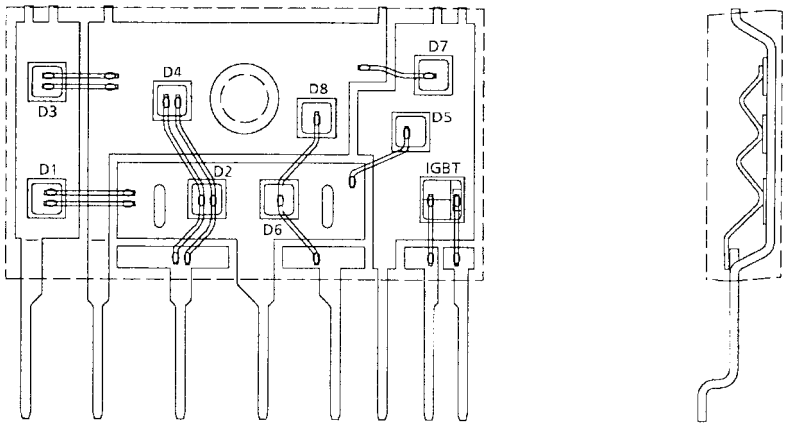
Waveform



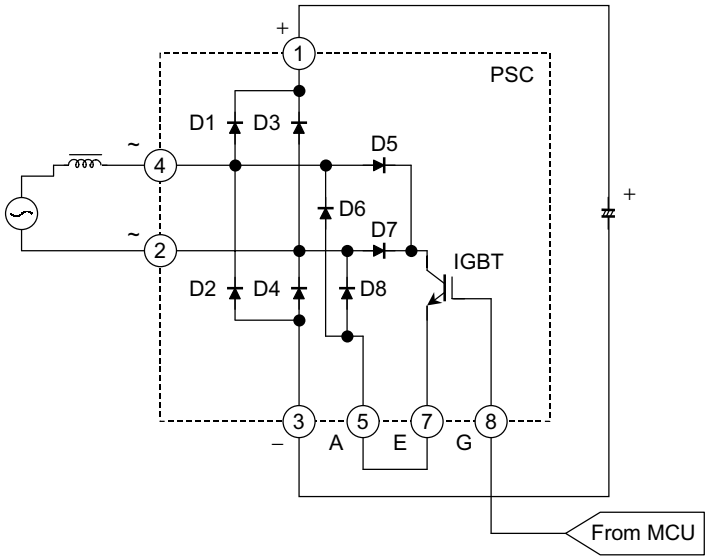
4. Package Dimension



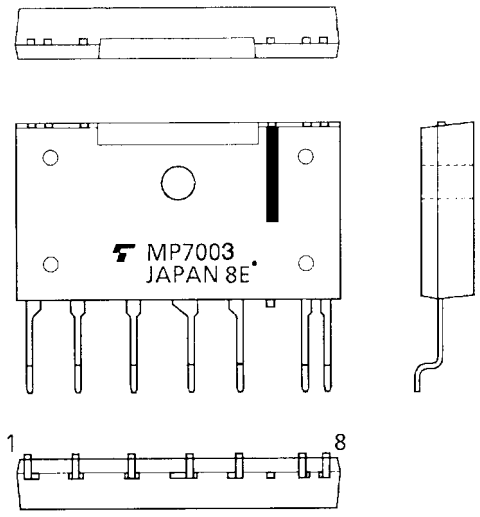
5. Image of Chips Mounting



6. PSC Equivalent Circuit Diagram (including application circuit)

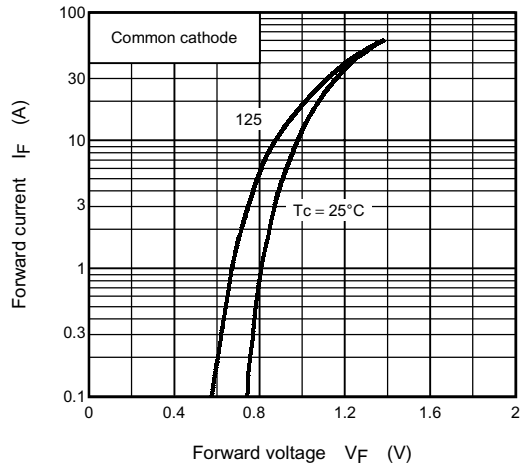


7. Pin Assignment

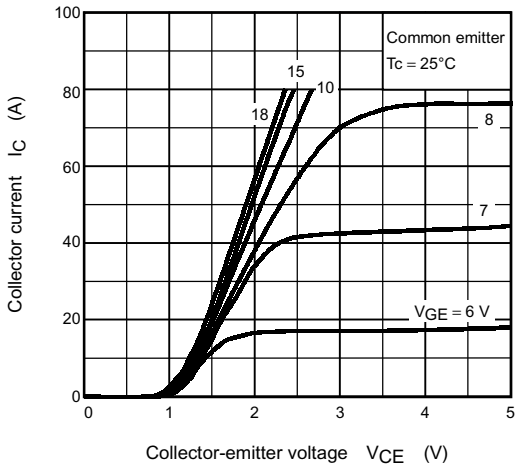


1. + pin
2. ~ pin
3. – pin
4. ~ pin
5. A pin
6. C pin (TOSHIBA test pin)
7. E pin
8. G pin

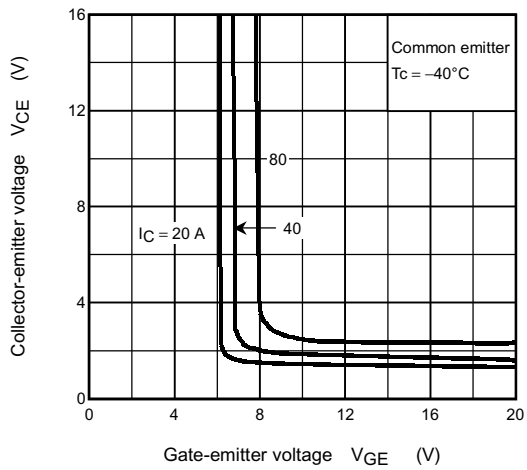
$I_F - V_F$



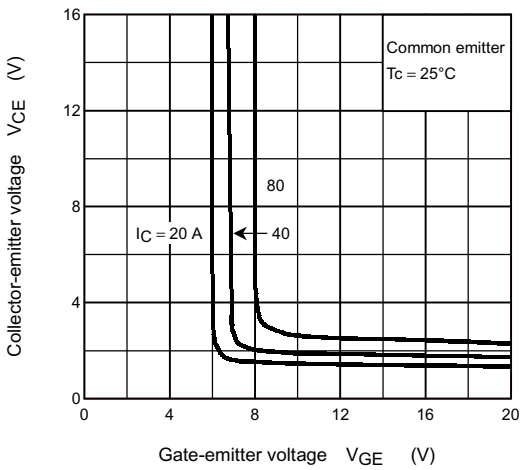
$I_C - V_{CE}$



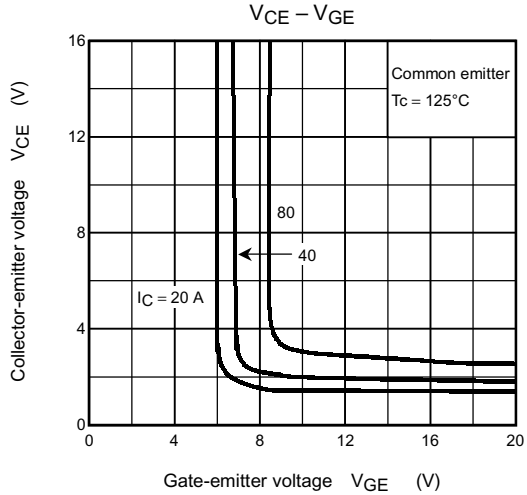
$V_{CE} - V_{GE}$



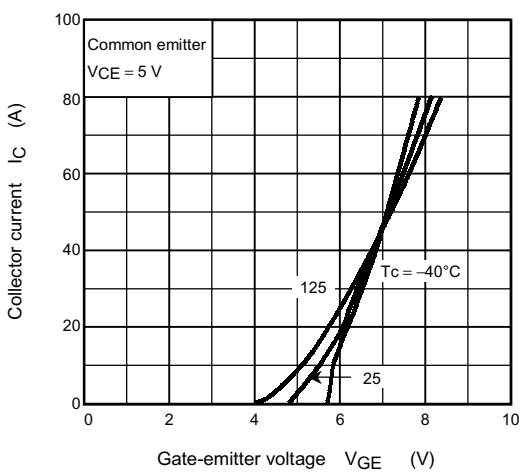
$V_{CE} - V_{GE}$



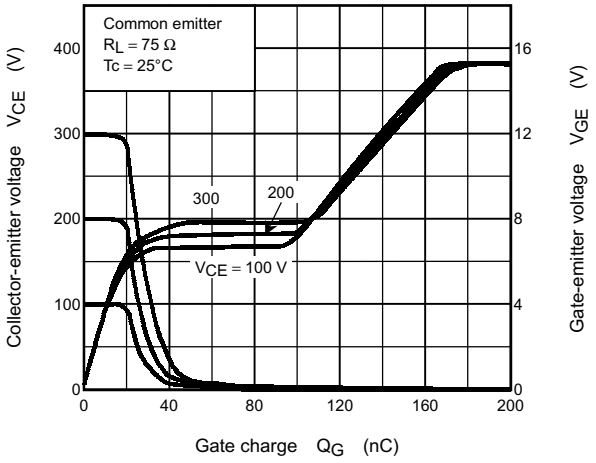
$V_{CE} - V_{GE}$



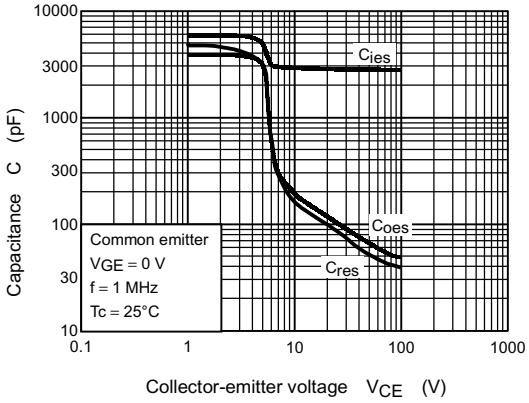
$I_C - V_{GE}$



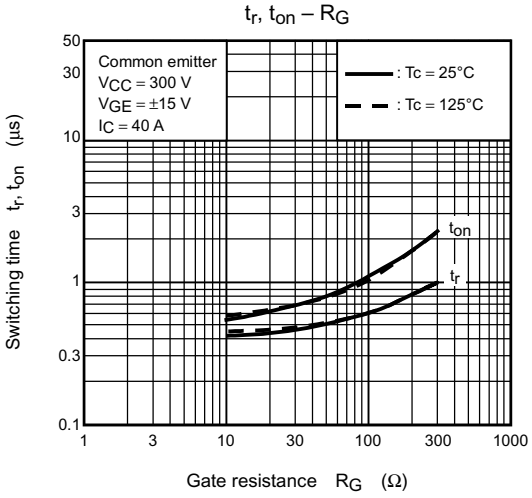
V_{CE}, V_{GE} – Q_G



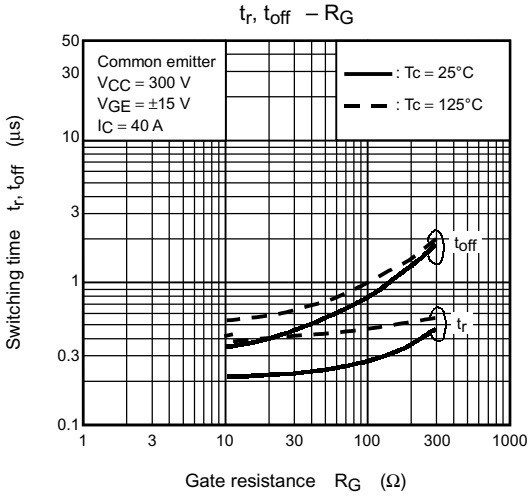
C – V_{CE}



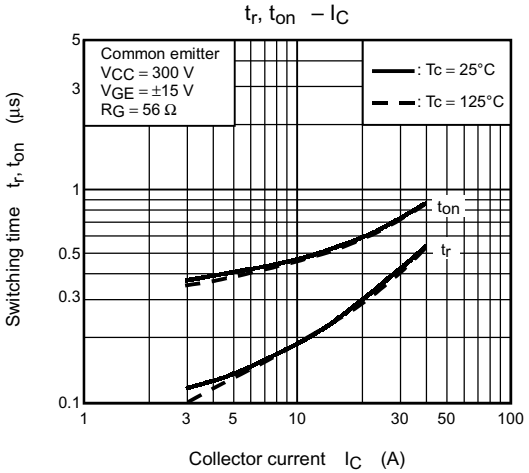
t_r, t_{on} – R_G



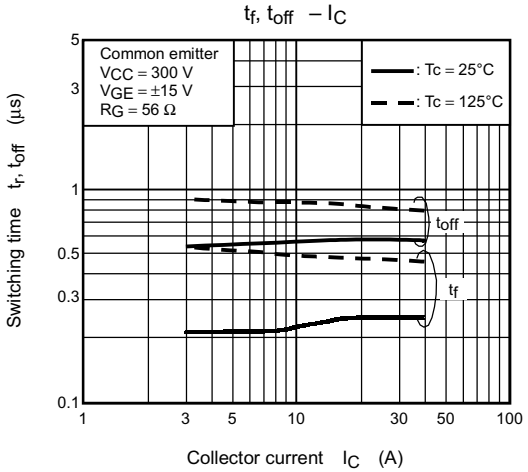
t_r, t_{off} – R_G



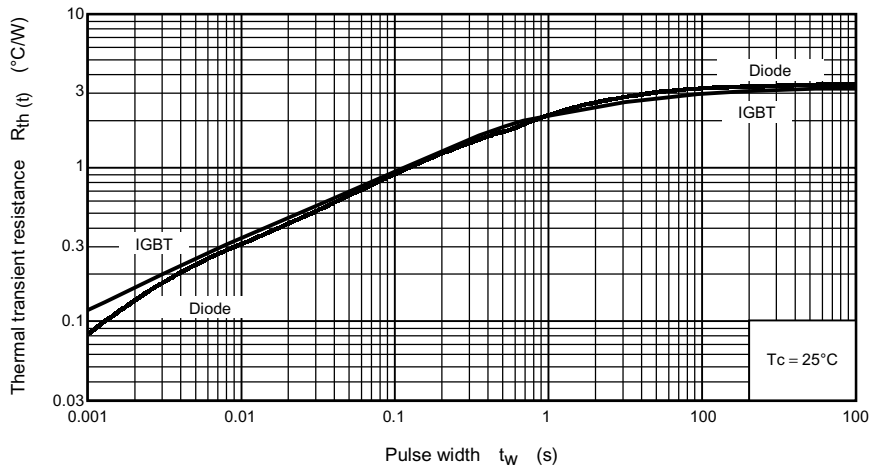
t_r, t_{on} – I_C



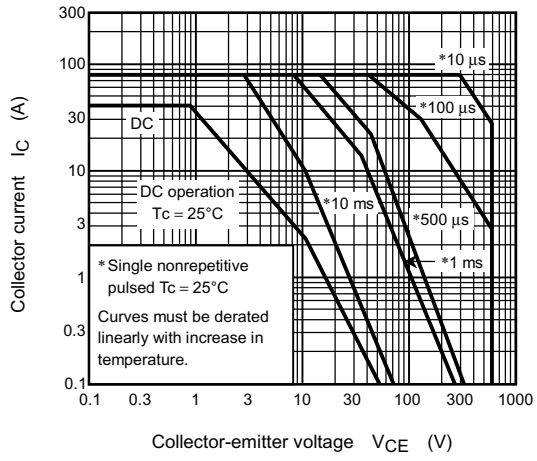
t_f, t_{off} – I_C



$R_{th\ (t)} - t_w$



Safe Operating Area



Reverse Bias SOA