1. GENERAL

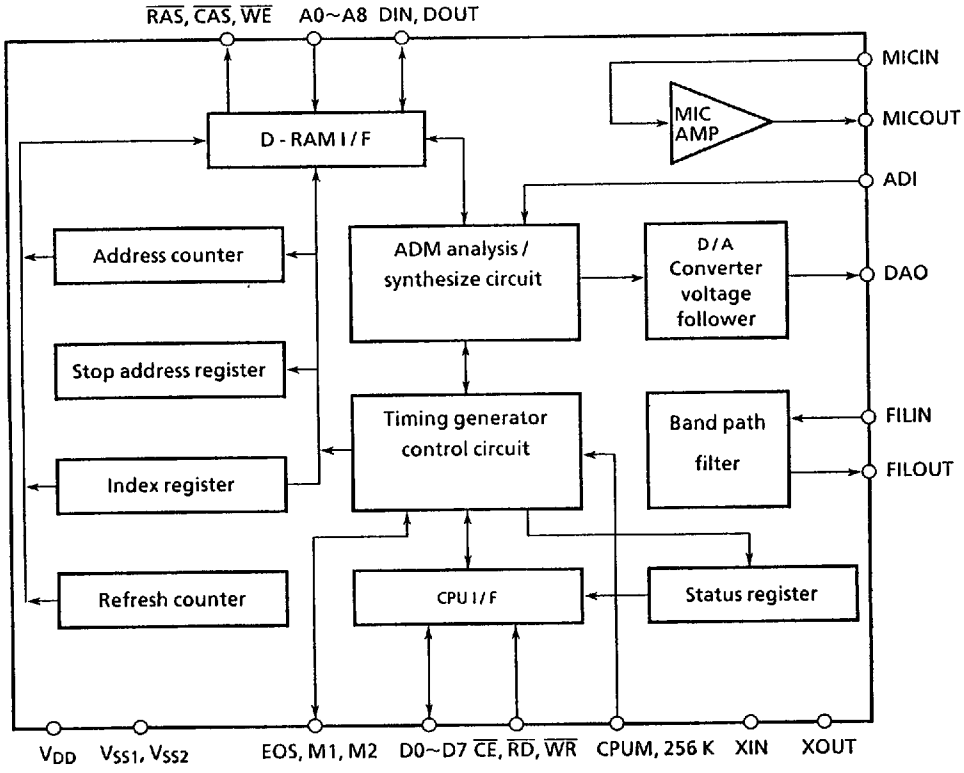
The T6668 is a single chip CMOS LSI for voice recording and reproducing using the ADM (Adaptive Delta Modulation) system. When a dynamic RAM is used as a voice data memory and an audio circuit including a microphone, speaker, amplifier, etc. is externally connected, a voice recording / reproducing system can be composed.

2. FEATURES

- ☐ A single chip LSI for voice recording / reproducing.
- ☐ D - RAM (Dynamic RAM) used as a voice data memory with the capacity up to 4pcs. of 64Kbit or 4pcs. of 256Kbit.
- ☐ Built - in counter to refresh D - RAMs.
- ☐ Easy connection with CPU. Control by 9 kinds of commands.
- ☐ Capable of recording / reproducing of max. 16 phrases.
- ☐ Selectable 4 kinds of bit rates (32k, 16k, 11k, 8kbps).
- ☐ Recording tone of each phrase is variable (MAX. 128 sec. at 256KD - RAM×4, bit rate 8kbps).
- ☐ Built in microphone amplifier for sound recording and band path filter for sound reproducing.
- ☐ Built in 10 bit D - A converter, voltage follower output.
- ☐ Built in oscillation circuit for ceramic resonator.
- ☐ Single 5V power supply ..... Low power consumption by CMOS structure.
- ☐ 60 pin mini flat package.

3. BLOCK DIAGRAM

3.1 T6668 Block Diagram



3.2 Block Diagram Description

(1) Address Counter

The 20 bit counter to show addresses of the external D - RAMs. Values can be set or read out by commands under CPU control. (Note 1)

(2) Stop Address Register

The 20 bit register to show addresses to stop recording / reproducing. Values can be set by commands, but values can not read out by commands under CPU control.

(3) Index Register

The register to show addresses of the index area on D - RAMs in the label index mode (refer to 5.5). User cannot directly operate this register.

(4) Refresh Counter

The 8 bit counter to refresh the external D - RAMs.

(5) Status Register

The 8 bit register to show the status of T6668. The status outputs by setting $\overline{RD}$ to L level.

(6) CPU I/F

The interface circuit for the external microprocessor, etc. This circuit has also the chattering preventing circuit in the manual control. (Note 1)

This chattering preventing circuit acts on D4 and D5 terminals (start and stop inputs), and chattering time is approx. 16 ms.

(7) Microphone Amplifier

The microphone amplifier for sound recording. Output of MICOUT terminal can be connected directly with the ADI pins.

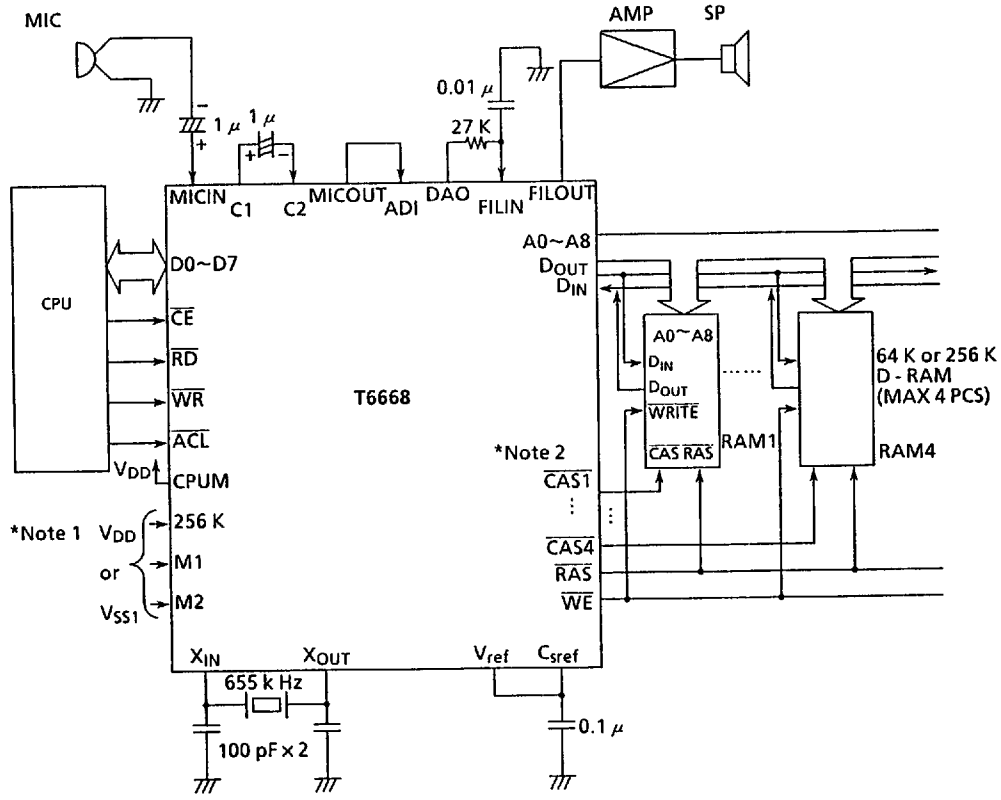
(8) Band - pass Filter

The band pass filter for sound reproducing. The 1st stage high pass filter and the 2nd stage low pass filter are built in.

Note 1. There are two controls available for the T6668; CPU control using a microcomputer, etc. and the manual control using SW, etc.

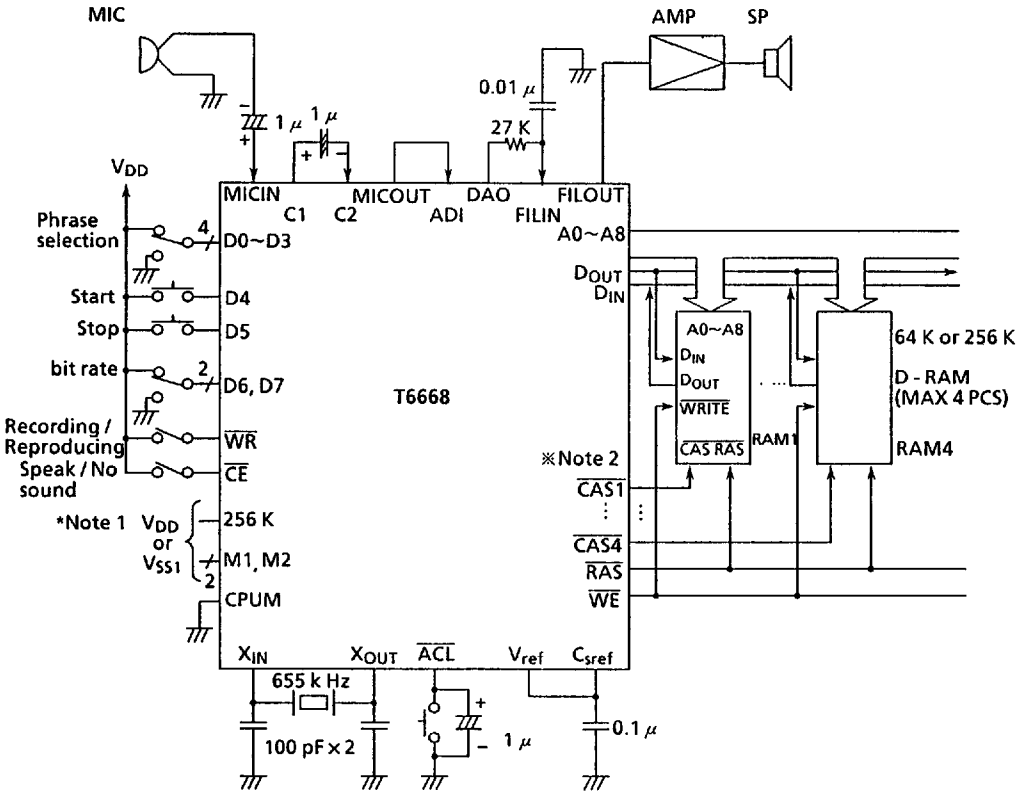
3.3 Example of Voice Recording / Reproducing LSI System Configuration

3.3.1 CPU Control



* Note 1 , Note 2 : For connections of 256K , M1 M2 and $\overline{CAS1}$~$\overline{CAS4}$, refer to 5.10 Connection to D - RAMs.

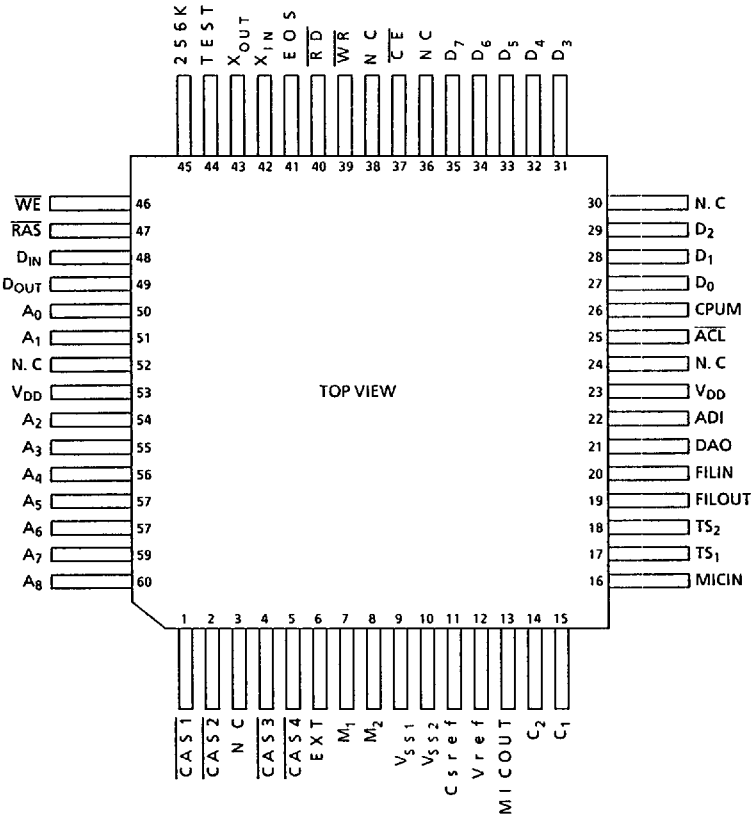
3.3.2 Manual Control



Note1 , Note2 : For connections of 256 k, M1 M2 and $\overline{CAS1}$~$\overline{CAS4}$, refer to 5.10 Connection to D - RAMs .

4. PIN DESCRIPTION

4.1 Pin Assignments



※ NC : NON - CONNECTION

4.2 Pin Description

Pin name	Pin no.	Structure: Manual control I/O	Structure: Manual control Pull - up Pull - down	Structure: CPU control I/O	Structure: CPU control Pull - up Pull - down	Functional explanation
$\overline{CAS1}$ $\overline{CAS2}$ $\overline{CAS3}$ $\overline{CAS4}$	1 2 4 5	Out	–	Out	–	Column address strobe output Used from $\overline{CAS1}$ to that required corresponding to the number of D - RAMs.
EXT	6	Out	–	Out	–	Output pins for test circuit.
M1 M2	7 8	In	None	In	None	Input pins for programming of the number of D - RAMs. M2 M1 1 pcs 0 0 2 pcs 0 1 3 pcs 1 0 4 pcs 1 1 0 = L level 1 = H level
VSS1 VSS2	9 10	Power Supply	–	Power Supply	–	Power supply pin to be connected to minus. V_{SS1} is for digital circuit and V_{SS2} is for analog one.
Csref Vref	11 12	I/O	–	I/O	–	Pins for connecting the decoupling capacitor to the reference voltage circuit of the built - in OP - AMP.
MICOUT	13	Out	–	Out	–	Output pin of built - in MIC. AMP. Output signal must be oscillating signal centering around 1 / 2 V_{DD}.
C2	14	In	None	In	None	Pins for connecting the coupling capacitor of built - in MIC. AMP.
C1	15	Out	–	Out	–	
MICIN	16	In	None	In	None	Input pin for built - in MIC. AMP. MIC must be connected to this pin through capacitor.
TS1	17	In	Pull - down	In	Pull - down	Pins for test circuit. Must be open.
TS2	18	Out	–	Out	–	
FILOUT	19	Out	–	Out	–	Output and input pins of built - in band pass filter (for reproducing)
FILIN	20	In	None	In	None	
DAO	21	Out	–	Out	–	Voice Output pin of voice synthesizing circuit. Voltage follower output. Monitor output for input voice is obtained during recording. Output signal must be oscillating signal centering around 1 /2 V_{DD}

Pin name	Pin no.	Structure				Functional explanation
		Manual control		CPU control		
		I/O	Pull - up Pull-down	I/O	Pull - up Pull - down	
ADI	22	In	None	In	None	Voice input pin of voice analyzing circuit. Input signal must be oscillating signal centering around 1 / 2 V_{DD} and MAX. 1.6 Vp-p.
V_{DD}	23 / 53	Power Supply	–	Power Supply	–	Power supply pins ··· + 5 V
$\overline{ACL}$	25	In	Pull - up	In	Pull - up	Input pin for reset signal.
CPUM	26	In	None	In	None	Mode change pin. Must be fixed to low level under manual control mode, fixed to high level under CPU control mode.
D0 D1 D2 D3 D4 D5 D6 D7	27 28 29 31 32 33 34 35	In	Pull-down	I/O	None	In the CPU control mode, these are bidirectional data bus for commands or data between CPU and T6668. In the manual control mode, these are used in such a way as shown below. (1) D0 ~ D3 inputs for phrase selection. MAX. 16 phrases can be selected by these 4-bit codes. (2) D4 START input Recording or reproducing starts by setting this pin at high level. (3) D5 STOP input Recording or reproducing starts by setting this pin at high level. (4) D6, D7 Inputs for bit rate selection Usable bit rates are as follows D7 / D6: 8 Kbps 0 0; 11 Kbps 0 1; 16 Kbps 1 0; 32 Kbps 1 1 0 = L level 1 = H level
$\overline{CE}$	37	In	Pull - down	In	None	Chip enable input pin under the CPU control mode. This pin is used for inputting voice / no voice in the MANUAL control mode. When the pin is set at high level under reproducing, DAO output becomes no voice condition. The pin must be put low level during recording.

Pin name	Pin no.	Structure				Functional explanation
		Manual control		CPU control		
		I/O	Pull - up Pull - down	I/O	Pull - up Pull - down	
$\overline{WR}$	39	In	Pull - down	In	None	Write pulse input pin under the CPU control mode. Under the manual control mode, this pin is for selection of recording / reproducing. High level to this pin makes recording mode, respectively.
$\overline{RD}$	40	In	Pull - down	In	None	Read pulse input pin under the CPU control mode.
EOS	41	Out	–	Out	–	Output of "End of Speech." It becomes low level after the start of recording or reproducing, and returns to high level after the stop of those.
X_{IN}	42	In	None	In	None	Input and output pins of oscillator circuit. 655 kHz ceramic oscillator and capacitors are connected.
X_{OUT}	43	Out	–	Out	–	
TEST	44	In	Pull - down	In	Pull - down	Pin for test circuit. Must be open.
256K	45	In	None	In	None	Input pin for the selection of the type of D-RAMs. It must be set at low level for 64Kbit D - RAM and high level for 256Kbit D - RAM.
$\overline{WE}$	46	Out	–	Out	–	Write pulse output pin. Connect this to $\overline{WRITE}$ pins of D - RAMs.
$\overline{RAS}$	47	Out	–	Out	–	Low address strobe output. Connect this to $\overline{RAS}$ input pins of D - RAMs.
D_{IN}	48	In	Pull - up	In	Pull - up	Data input pin. Connect this to data input pins of D - RAMs.
D_{OUT}	49	Out	–	Out	–	Data output pin. Connect this to data input pins of D - RAMs.
A0 A1 A2 A3 A4 A5 A6 A7 A8	50 51 54 55 56 57 58 59 60	Out	–	Out	–	Address output. Connect this to address input pins of D - RAMs. Only A8 is not needed when 64Kbit D - RAMs are used.

5. SPECIFICATION

5.1 Recording / Reproducing

System	ADM System
D / A Converter	10bit voltage type
Bit rate	32K / 16K / 11K / 8Kbps
Max. phrase number	In manual control ··· 16 phrases Label index mode in CPU control ··· 16 phrases Direct mode in CPU control ··· No restriction
Address counter	Built in counter to refresh D - RAMs

5.2 Others

Input Microphone amplifier	Two - stage, gain TYP = 46 dB
Output filter	Built in 2nd stage low pass + 1st stage high pass filter
RAM for storing voice data	64K or 256K D - RAM, maximum 4 pcs each
Oscillation frequency	655kHz (TYP.)

5.3 Operational Description

When composing a voice recording / reproducing system by the T6668, there are CPU control using a microcomputer, etc. and the manual control using external SW, etc.

5.4 Manual Control

5.4.1 Selection of Phrase

Using 4 input pins of D0~D3, the sound recording / reproducing of maximum 16 phrases can be performed. Before starting the sound recording / reproducing, phrase No. shall be specified in 4-bit code.

Phrase numbers are as follows, and can be selected at random. (Fig. 5.1)

Table 5.1 Phrase no.

Phrase No. \ Pin name	MSB D3	D2	D1	LSB D0
No.0	0	0	0	0
No.1	0	0	0	1
↓	↓	↓	↓	↓
No.15	1	1	1	1

0 = L level
1 = H level

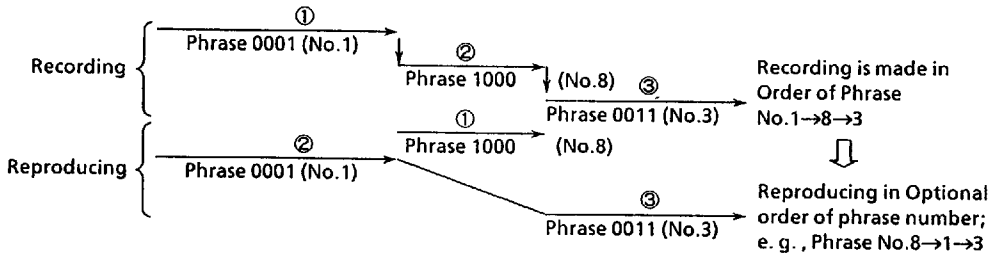


Fig.5.1 Example of phrase selection

5.4.2 Selection of Bit Rate

The T6668 can use 4 kinds of bit rates as shown in Table 5.2; 8k, 11k, 16k and 32kbps, which are selected by D6 and D7. Since a bit rate is independently specified for sound recording / reproducing, it is possible to change reproduced voice to slow / fast speaking. However, the phrases are reproduced at low tone when slowly spoken and at high tone when rapidly spoken. Bit rate should be specified prior to recording / reproducing.

Table 5.2 Bit rate selection

	D_7	D6
8 K bps	0	0
11 K bps	0	1
16 K bps	1	0
32 K bps	1	1

0 = L level
1 = H level

(Caution) Selection of phrase and bit rate is decided when D4 pin is set at "H" level (start input).

Switching of Recording / Reproducing Mode

Switching of recording / reproducing of the T6668 is made by the $\overline{WR}$ pin.
"H" level is ready to accept the recording and "L" level is ready to accept the reproducing.

5.4.3 Recording Mode

The T6668 has the 20 bit address counter, and voice data is written into RAM from the address designated by that value. When making the sound recording newly, first, reset the address counter by the $\overline{ACL}$ input. Setting of the $\overline{WR}$ pin to "H" level results in the recording waiting state.

When the D4 pin is set to "H" level (start input), the recording starts and the address counter is added successively. When the D5 pin is set at "H" level (stop input) or when the value on the address counter reaches the maximum address (see 5.7) of RAM, the sound recording is stopped.

Since this maximum address is changed when the 256K, M1 and M2 pins are set, the full capacity of RAM can be effectively used. However, when the RAM's capacity is fully used, subsequent recording is not allowed. Therefore, to make the recording newly, reset the address counter again of the $\overline{ACL}$ input.

In T6668, when the sound recording starts, a value of the address counter at time of the start (start address) and when the sound recording ends, that at time of the stop (stop address) are automatically written into a part of RAM, respectively. Further, it is possible to monitor synthesized voices from input voices through analysis and synthesis during the recording.

5.4.4 Reproducing Mode

When the $\overline{WR}$ pin is set at "L" level, the T6668 is placed in the sound reproducing waiting state. When the D4 pin is set at "H" level at this times the T6668 starts the sound reproducing after loading the start address and stop address, which have been written at time of the sound recording, into the address counter and stop address register, respectively. The sound reproducing is terminated when the D5 pin is set at "H" level or when the value of the address counter agrees with the stop address.

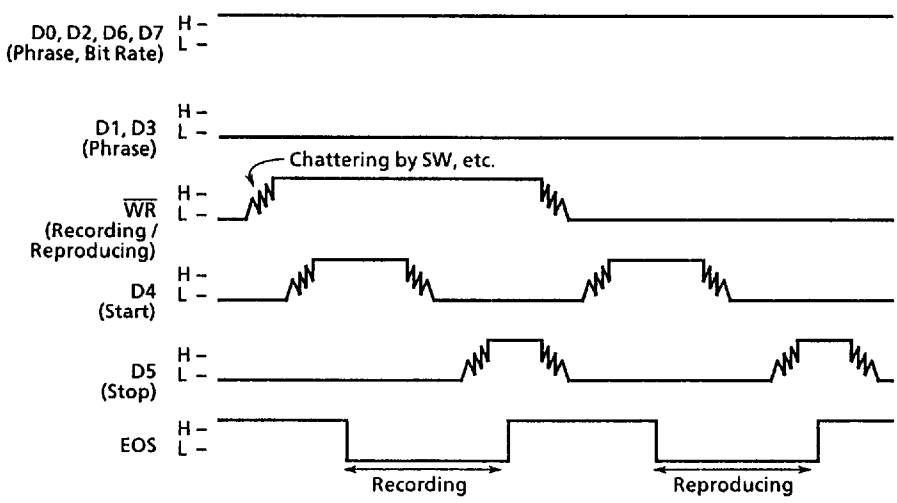


Fig.5.2 Recording / reproducing at phrase No.5, bit rate 32 kbps

* Refer to 5.6 Recording / Reproducing via Index Area for details of recording / reproducing, addition of phrases and change of phrase contents when many phrases are involved, and refer to 5.9 Operation of Address Counter for the address counter operation.

5.4.5 Start, Stop Input and Internal Status

Phrase No., bit rate and recording / reproducing status are all held at the leading edge of internal start pulse. Further, external start input and internal start pulses are at the timings shown in Fig. 5.3.

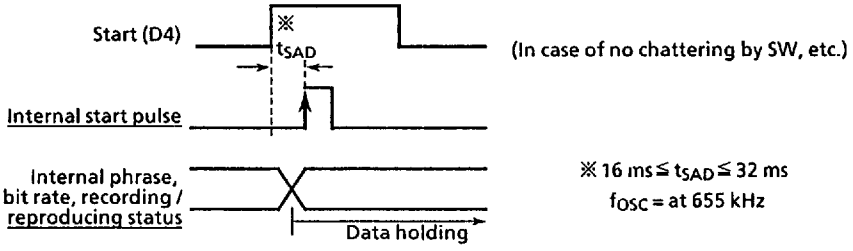


Fig.5.3 Start input and internal status

From Fig. 5.3, it is possible to input externally given D0~D3 (Phrase), D6~D7 (bit rate), $\overline{WR}$ (recording / reproducing), D4 (start) and D5 (stop) as shown Fig. 5.4.

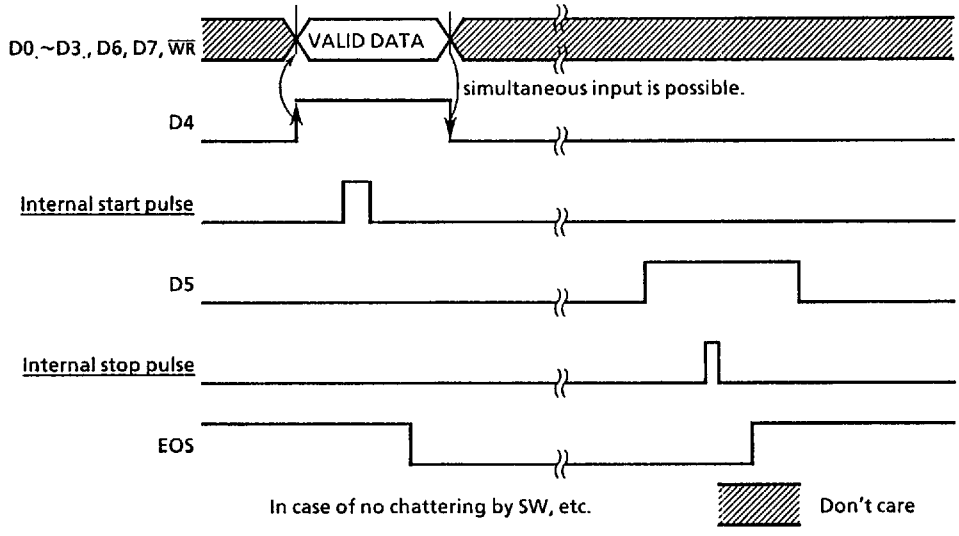


Fig.5.4 How to give start input and stop input

5.4.6 Chattering Preventing Circuit

In the manual control mode, the chattering preventing circuit is actuated to prevent malfunction by chattering of the switches connected to the D4 pin (start input) and D5 pin (stop input).

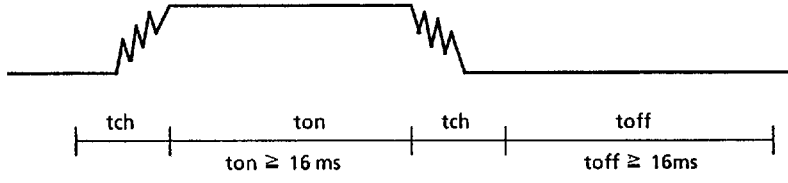


Fig.5.5 Chattering preventing circuit

In case of operating in manual mode, start and stop inputs should be set to min. 16ms.

5.5 CPU Control

In the CPU control, the operation of T6668 is controlled by 9 kinds of commands. In addition, the T6668 has a 8 bit status register and the external CPU is able to read the status of T6668 at any time.

In addition, the T6668 has the address overflow detector (Note 1) and the address comparator flip-flop (Note 2), which control the sound recording and reproducing operations.

(Note 1) Address overflow detector ..... (Refer to 5.5.5)

(Note 2) Address comparator flip-flop ..... (Refer to 5.5.6)

5.5.1 How to Write CPU Command

As shown Fig. 5.6, using ① $\overline{RD}$ pulse, read data from LSI and check BUSY bit. If not in ② BUSY state, after setting up command data in D0~D7, write a command using $\overline{WR}$ pulse. In case of such 3 byte commands as ADLD1, ADLD2, etc., after rechecking BUSY bit by ③ $\overline{RD}$ pulse, write the ④ 2nd and 3rd byte bits. After the 1st and 2nd byte bits of a 3 byte command, other command bits cannot be written.

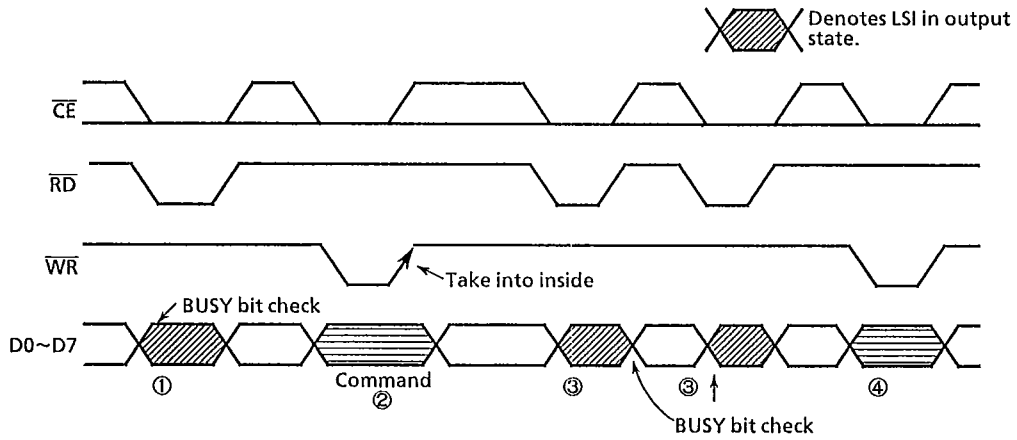


Fig.5.6 How to write command

5.5.2 Commands of T6668

0 = L level
1 = H level
X = Don't Care

(1) NOP (1 byte)

MSB							LSB
0	0	0	0	X	X	X	X

No operation. In the sound recording mode, this command is set in the sound reproducing mode. In addition, this command is used to reset ERR and OVR (refer to 5.2.3) in the status register.

(2) START (1 byte)

MSB							LSB
0	0	0	1	X	X	X	X

This command is used to start the sound recording or reproducing in the direct mode from the RAM address shown by the contents of the address counter.

(3) STOP (1 byte)

MSB							LSB
0	0	1	0	X	X	X	X

This command is used to stop the sound recording or reproducing. If this command is given during the sound recording by the LABEL command, the contents of the address counter at time of stop are written into the index area of RAM.

(4) ADLD1 (3 bytes)

MSB							LSB
0	0	1	1	A19	A18	A17	A16

This command is used to set address in the address counter together with 2 bytes following that address. When the 64Kbit RAM is specified, A19 and A18 are made to "00" by force.

(5) ADLD2 (3 bytes)

MSB							LSB
0	1	0	0	A19	A18	A17	A16

This command is used to set address in the stop address register together with 2 bytes following that address. When the 64Kbit RAM is specified, A19 and A18 are made to "00" by force.

(6) CNDT (1 byte)

MSB							LSB
0	1	0	1	X	SL	BR1	BR0

(For SL, BR1, BR0, refer to the command list)

This command specifies a bit rate and silent state. When the silent state is specified, the DAO pin is forced to become $1/2 \cdot V_{DD}$ level. The silent state should not be specified at time of sound recording.

(7) LABEL (1 byte)

MSB							LSB
0	1	1	0	LB3	LB2	LB1	LB0

(For LB3,LB2, LB1, and LB0, refer to the command list)

This command specifies phase No. (0~15) and starts the sound recording / reproducing. When this command is given in the sound recording mode, the contents of the address counter is written into the index area of RAM and then, the sound recording is started. In case of the sound reproducing mode, start address, stop address, and bit rate are read from the index area and then, the sound reproducing is started.

(8) ADRD (1 byte)

MSB							LSB
0	1	1	1	X	X	X	X

This command is used to read out the contents of the address counter. By successive 3 times of read access, high order 4bits, middle order 8 bits, and low order 8bits are output to D0~D7 in that order. If next command is given without performing 3 times of read access, the ADRD code interrupted and the next command process is started, enabling read out of the status register.

(9) REC (1 byte)

MSB							LSB
1	0	0	0	X	X	X	X

This command is used to set the T6668 to the sound recording mode when it is in the sound reproducing mode. The T6668 is returned to the sound reproducing mode by NOP command.

(Caution) During the sound recording / reproducing (that is, when the EOS pin or EOS bit of the status register is 0), do not give any command other than STOP.

Table 5.3 Command list

Command	1st byte	2nd byte	3nd byte
Input Pin	D7 —— D0	D7 —— D0	D7 —— D0
NOP	0 0 0 0 X X X X	–	–
START	0 0 0 1 X X X X	–	–
STOP	0 0 1 0 X X X X	–	–
$ADLD_1$	0 0 1 1 A19 A18 A17 A16	A15 A14 A13 A12 A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0
$ADLD_2$	0 1 0 0 A19 A18 A17 A16	A15 A14 A13 A12 A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0
	0 1 0 1 X SL BR1 BR0	–	–

	SL
Sound	0
Silent	1

Bit Rate	BR1	BR0
8 K	0	0
11 K	0	1
16 K	1	0
32 K	1	1

LABEL	0 1 1 0 LB3 LB2 LB1 LB0	–	–

MSB ____ LSB

LB3 LB2 LB1 LB0 = Phrase No. (0~15)

ADRD	0 1 1 1 X X X X	–	–

Read	Output Data D7 —— D0							
1st	0	0	0	0	A19	A18	A17	A16
2nd	A15	A14	A13	A12	A11	A10	A9	A8
3rd	A7	A6	A5	A4	A3	A2	A1	A0

	1 0 0 0 X X X X	–	–

5.5.3 Status Register

The status register consists of 8 bits. When the $\overline{RD}$ pin is set to L level (read access) under CPU control, data of the status register is output to D0~D7 and the internal operating status of the T6668 can be checked. Each bit of the status register is explained in the following. (Table 5.4)

(1) BUSY

When this bit is 1, it indicates that the T6668 is in reset state or processing a command internally. Do not give any command from CPU. If the command is given, the internal status may possible becomes uncertainty.

(2) EOS

This bit becomes 1 during the not sound recording / reproducing and 0 when the sound recording / reproducing is started. This value is the same as the value that is output at the EOS pin.

(3) ERR

Command error. This bit becomes 1 when any undefined is given to the T6668. This bit is reset by NOP command.

(4) OVR

Address over. It is indicated that the sound recording ends as the address counter exceeded max. address (refer to 5.3) of RAM during the sound recording by LEBEL command. This status bit is reset by NOP command.

(5) M2, M1

values of these bits are the same as those set at pin M2 and M1.

Table 5.4 Status register

Terminal Name	D7	D6	D5	D4	D3	D2	D1	D0
Status Register	BUSY	EOS	ERR	OVR	M_2	M_1	0	0

0 = L Level 1 = H Level

5.5.4 Busy Bit

Conditions for setting BUSY bit of the status register to 1 are broadly classified into the following 3 conditions. That is, BUSY bit is set to 1 during the reset period of T6668, during the process of command given externally, and during the process after stop of the sound recording due to address overflow. (Table 5.5)

(1) Reset Process

When the $\overline{ACL}$ pin becomes L level, BUSY bit becomes 1. When the $\overline{ACL}$ pin returns to H level again, the internal state of T6668 is initialized and after all are completed, BUSY bit becomes 0.

(2) Command Process

When it is detected that both of the $\overline{CE}$ and $\overline{WR}$ pins have become L level in the CPU control, BUSY bit become 1. When the process of all command is completed, BUSY bit returns to 0 again. The command process is actually started after return of the least either one of the $\overline{CE}$ or $\overline{WR}$ pin to H level has been detected. (The table shown below also indicates times for BUSY bit to become 0 after the $\overline{CE}$ or $\overline{WR}$ pin returned to "II" level.)

(3) Address overflow process

When the address counter is overflow during the sound recording in the label index mode, the T6668 automatically stops the sound recording. During this period, BUSY bit also becomes 1.

Table 5.5 BUSY generating length

BUSY Generating Conditions		General Length (max)
Reset process (after $\overline{ACL}\uparrow$)		3 tϕ
NOP, START, CNDT, REC Command		3 tϕ
ADLD1, ADLD2 Command	1st byte	4 tϕ
	2nd, 3rd byte	3 tϕ
ADRD Command		4 tϕ
ADLD1, ADLD2 Command	Sound recording mode	35 tϕ
	Sound reproducing mode	67 tϕ
STOP Command	During sound recording in label indexmode	40 tϕ
	Others	3 tϕ
Address Overflow Process		34 tϕ

tϕ ≒5.3 μs @ fCLK = 655 kHz

5.5.5 Address Overflow Detector

When the address counter exceeds maximum address that is determined by the pin 256K, M2 and M1, it is detected by this detector. When the LABEL command is given in the sound recording mode, it becomes valid and is kept until the NOP command is given. When the address overflow is detected, the sound recording is stopped, a value of the maximum address is written into the index area as the stop address and then, the address counter is preset at address 00400H. In addition, the OVR bit of status register is set.

During this period of processing, BUSY bit of the status register also become 1.

5.5.6 Address Comparator Flip - Flop

The sound recording / reproducing is stopped if the contents of the address counter agrees with those of the stop address register when this flip - flop has been set. When it has been reset, the sound recording / reproducing is not stopped until the STOP command is given. (Exception: Address overflow in the preceding item)

This flip - flop is set when the ADLD2 command is given or when the LABEL command is given in the sound reproducing mode, and is reset when the ADLD1 command is given or when the LABEL command is given in the sound recording mode.

5.5.7 Modes in CPU Control

There are two ways about both recording and reproducing of T6668 when it is under CPU control. That is, one is the Direct mode and another is Label / Index mode. The former is the way to write start address, stop address and bit rate of each phrase by command, and the latter is to designate phrase number so that T6668 write the above mentioned parameters into the certain part of RAM.

So, at the Label / Index mode, the certain part of RAM (s) is used for Index area. On the contrary at the direct mode, such a part can used for data area (Fig. 5-7).

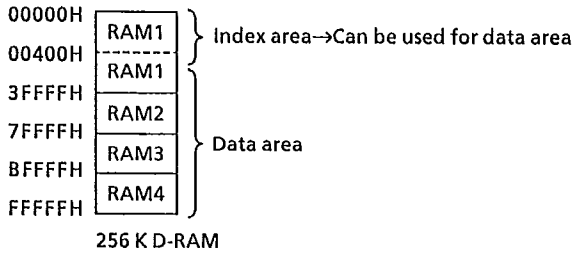


Fig.5.7 Memory map at direct mode

* Refer to 5.6 RECORDING VIA INDEX AREA for details of recording / reproducing, addition of phrases and change of phrase contents many phrases are involved, and 5.9 OPERATION OF ADDRESS COUNTER for address counter operation.

5.5.8 The Flowchart of Recording / Reproducing in Label Index Mode

(1) Recording

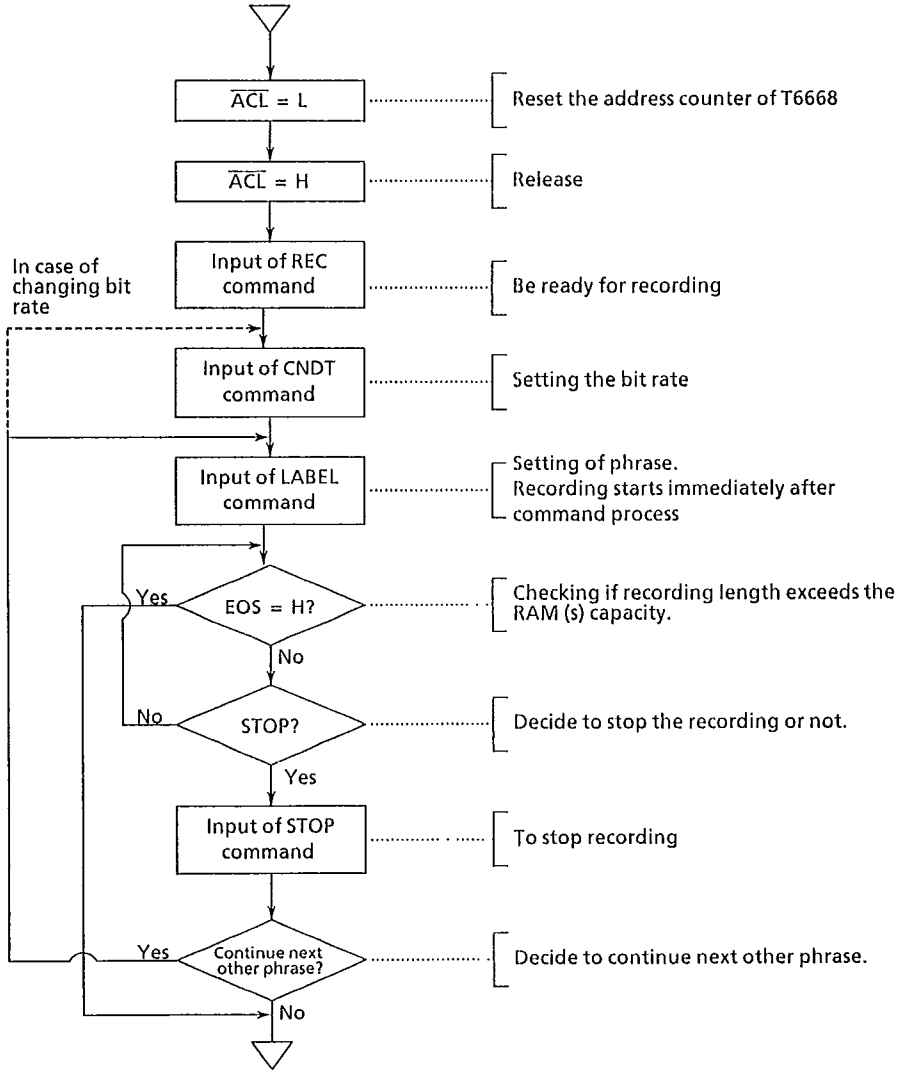
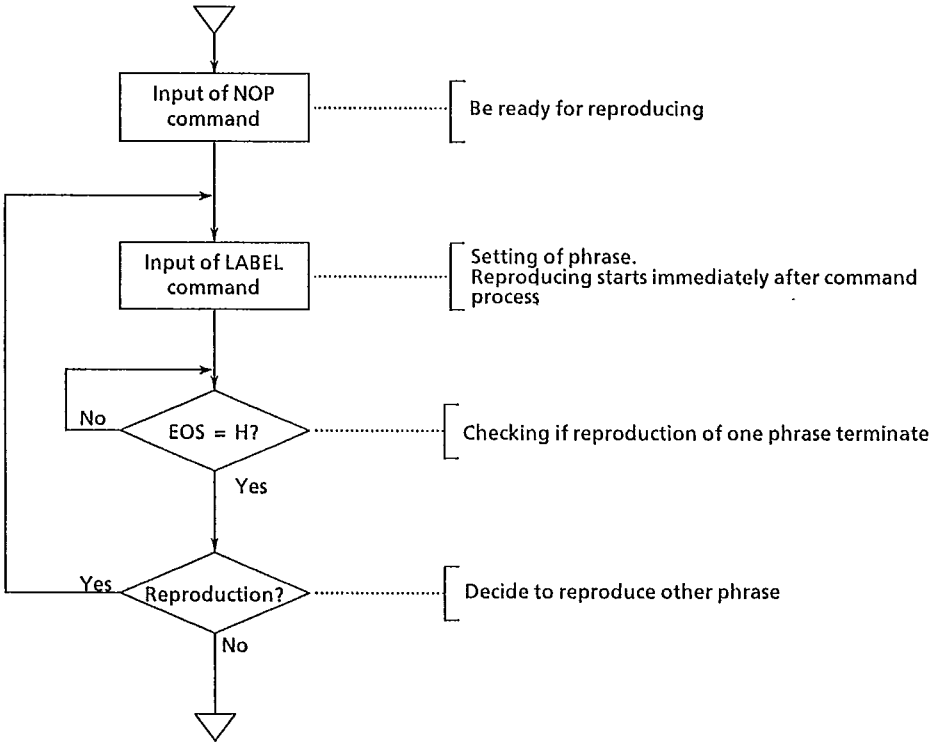


Fig.5.8 Recording in label / index mode

(2) Reproducing

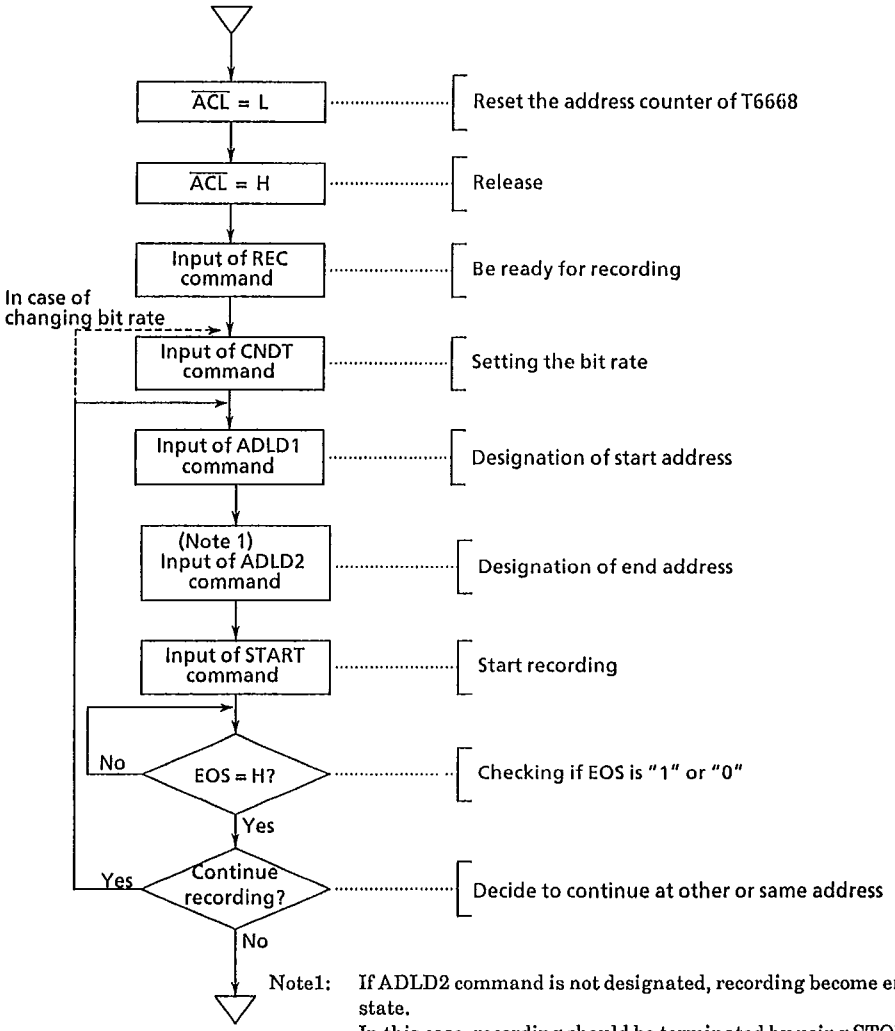


Note : In CPU control mode, bit rate is that settled previously at the recording and fast / slow speaking cannot be specified as in manual control mode.

Fig.5.9 Reproducing in label / index mode

5.5.9 The Flowchart of Recording / Reproducing AT "DIRECT MODE"

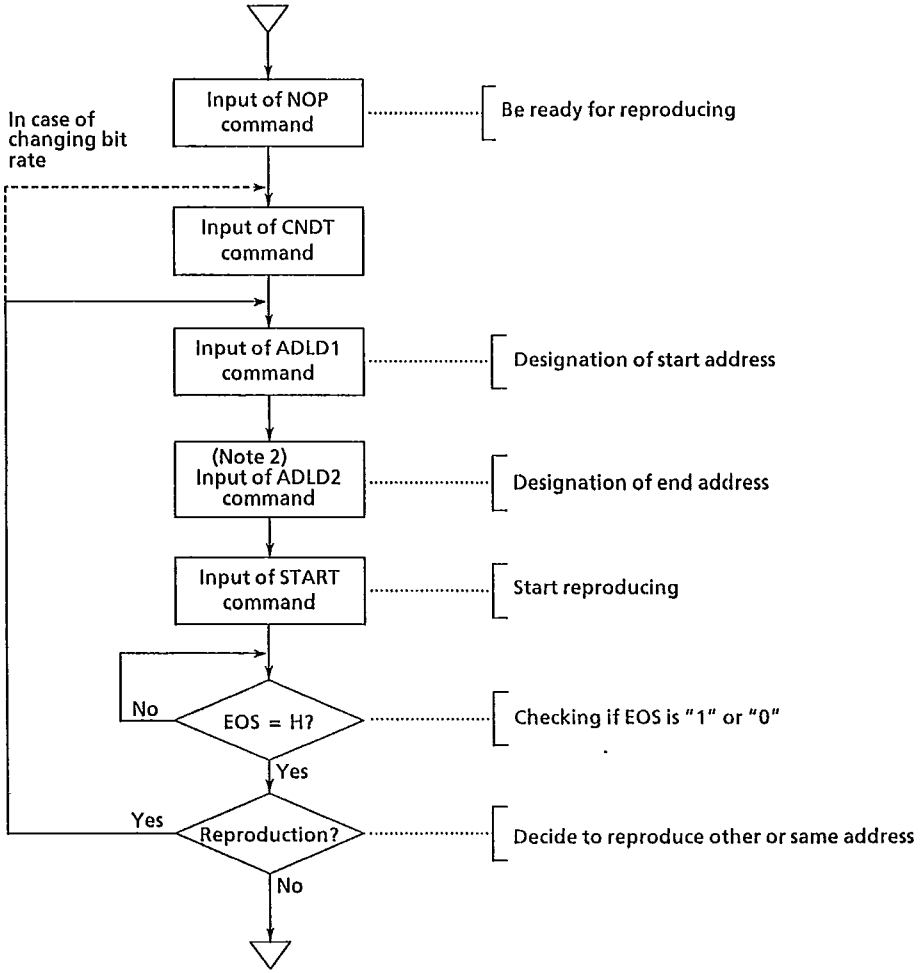
(1) Recording



Note1: If ADLD2 command is not designated, recording become endless state.
In this case, recording should be terminated by using STOP command

Fig.5.10 Recording in direct mode

(2) Reproducing



Note 2 : When ADLD2 is used as the maximum address of RAM during recording and omitted during reproducing, endless speaking becomes possible. STOP command is used to terminate it.

Fig.5.11 Reproducing in direct mode

5.6 Recording / Reproducing Via Index Area

The recording / reproducing methods by the manual control of the T6668 and the label index mode in CPU control are described here. In the manual control (LABEL command under CPU control), the recording / reproducing is indirectly performed as the T6668 writes start addresses, stop address and bit rate of each phrase into a part of RAM and selects phrase number. The memory maps of RAMs in the label index mode are as follows.

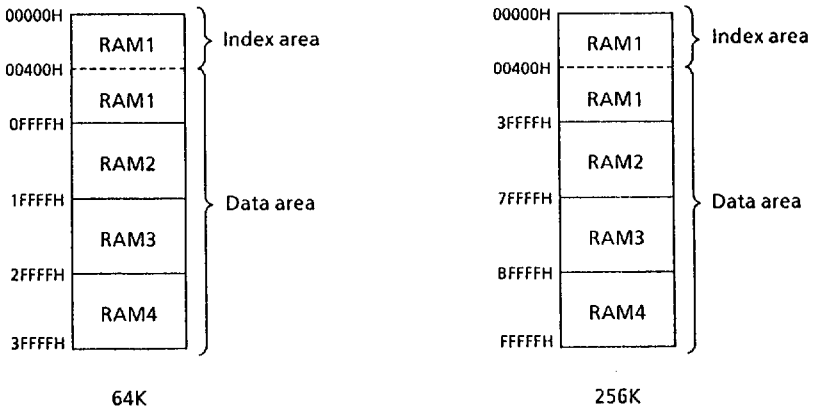


Fig.5.12 Memory map in level index mode

Maximum number of addresses that can be used varies depending upon type and number of externally connected D - RAM. In may case, addresses 00000H~003FFH are used as the index area, and the succeeding address 00400H and up become the voice data area.

Start address, stop address, and bit rate are recorded in the index area by the T6668 at time of sound recording, and data read out from this area are loaded on the address counter, etc. at time of sound reproducing.

5.6.1 Recording of Phrase

In performing the recording newly, first reset the T6668 by the $\overline{ACL}$ input. The internal address counter is preset to 004000H at this time.

Then, when the start signal is input by specifying a bit rate and phrase No., the recording starts. After the contents of the address counter at this time; that is, start address is written into the index area of RAM, actual recording is started. During the recording, the contents of the address counter are added successively.

When the stop signal is input during the recording, the recording ends. The contents of the address counter at the time; that is, the end address and bit rate are written into the index area of RAM. Thereafter, the contents of the address counter are added with one (+1) and preparation for next recording is performed.

To perform the recording with other phrase successively, Phrase No. is newly designated and the start signal is input (Fig. 5.19).

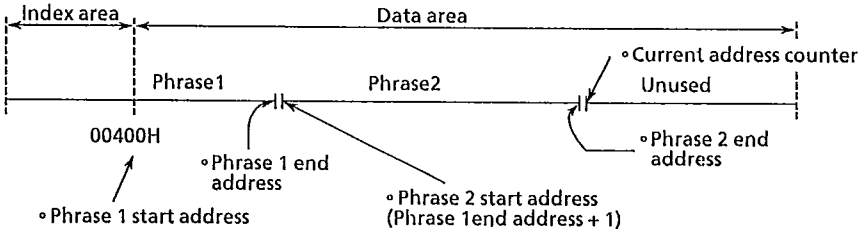


Fig.5.13 In case of recording phrase 2

5.6.2 Reproducing of Phrase

If any already recorded phrase No. is selected and start input is give, voice corresponding to that phrase No. is reproduced. Phrase No. at this time can be designated irrespective of sequence of the recording. Further, it is also possible to stop speaking by giving the stop input in the middle of the reproducing. Thereafter, when the start input is given again using the same phrase No., the reproducing is performed from the beginning of that phrase. If the reproducing is started by designating phrase No. that was not used for the recording, what sound is reproduced is uncertain. However, it is possible to stop the sound reproducing by giving stop input. The reproducing is started after the start address, end address and bit rate are set in the T6668 from the index area. When the start input signal is given by specifying next phrase No. during the reproducing in the manual control mode, this next phrase is spoken successively after end of the preceding phrase generation, because T6668 has a buffer for phrase No. When the start input signal is given several times during speaking of one phrase, the last phrase specification remains in the buffer. As the bit rate has no buffer, however, the bit rate of a phrase during the reproducing becomes the bit rate of next phrase in change the phrases with different bit rates.

5.6.3 Addition of Phrase

First, reproduce the last phrase at the recording to the last in the reproducing mode. At this time, the address counter stops while indicating address next to the end address of the last phrase. Change the reproducing mode to the recording mode. Do not reset the T6668 at this time. When the recording is made by designating any unrecorded phrase No., phrase can be added.

5.6.4 Change of Phrase Contents

To change the contents of phrases that have been once recorded, reproduce a phrase preceding the phrase that is to be changed to have the address counter indicate the start address of the phrase to be changed. (For example, when Phrase No. has been recorded in order of 5-7-3-6 and the contents of phrase No. 3 are to be changed, reproduce phrase No. 7 to the last.) Do not reset the T6668 at this stage. When the recording is made by designating phrase No. that is to be changed successively, the contents of that phrase are changed to the new contents. At this time, if the recording time of the changed phrase is longer than that of the phrase before changed, the first part of next phrase may be changed. When the changed phrase is reproduced under this state, the new contents are spoken properly but when it is tried to reproduce next phrase, the reproducing is started at the middle of the changed phrase and when the reproducing ends, sound is produced successively from the middle of next phrase. This is phenomenon that is taken place as the start address of next phrase written in the index area remains unchanged from the previous address. On the contrary, when the recording time of the changed phrase is shorter than that before change, the latter part data of the phrase before change is left. When this part is reproduced, the last speaking of the changed phrase stops. Needless to say, next phase is also properly reproduced.

Under this state, a RAM for the part between the end address of the changed phrase and the start address of next phrase is not used. (Fig. 5.20)

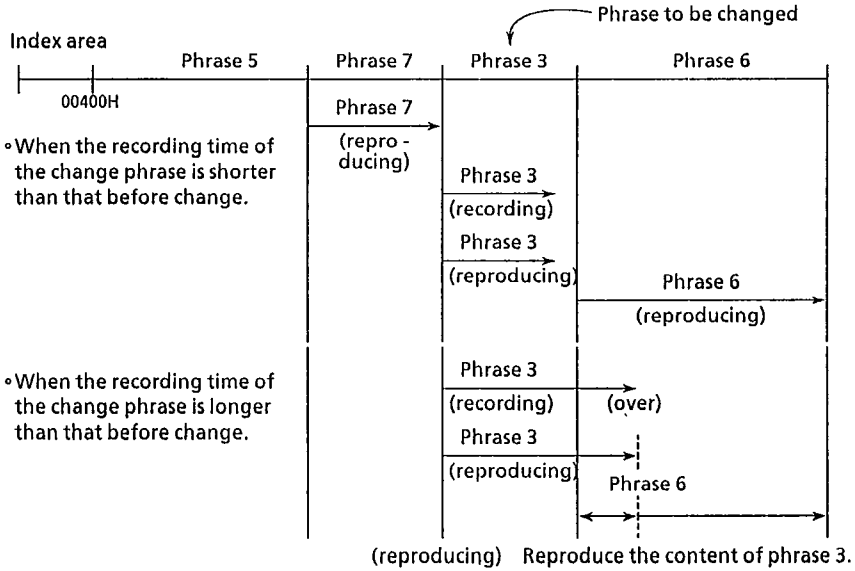
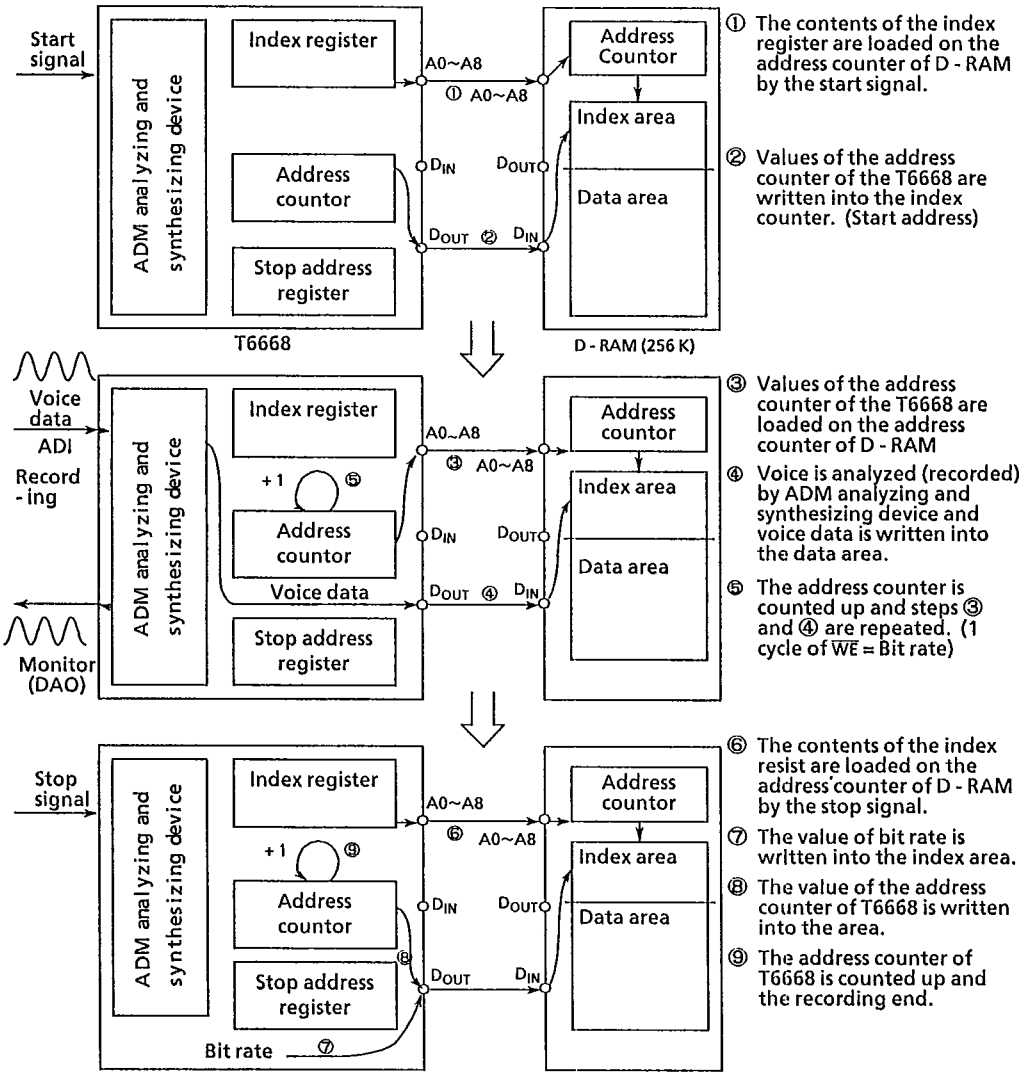


Fig.5.14 Change of phrase contents

5.6.5 Address and Data in Label Index Mode

The operations of the T6668 and D - RAM in the label index mode are described in the following.

(1) At time recording



① The contents of the index register are loaded on the address counter of D - RAM by the start signal.

② Values of the address counter of the T6668 are written into the index counter. (Start address)

③ Values of the address counter of the T6668 are loaded on the address counter of D - RAM

④ Voice is analyzed (recorded) by ADM analyzing and synthesizing device and voice data is written into the data area.

⑤ The address counter is counted up and steps ③ and ④ are repeated. (1 cycle of $\overline{WE}$ = Bit rate)

⑥ The contents of the index resist are loaded on the address counter of D - RAM by the stop signal.

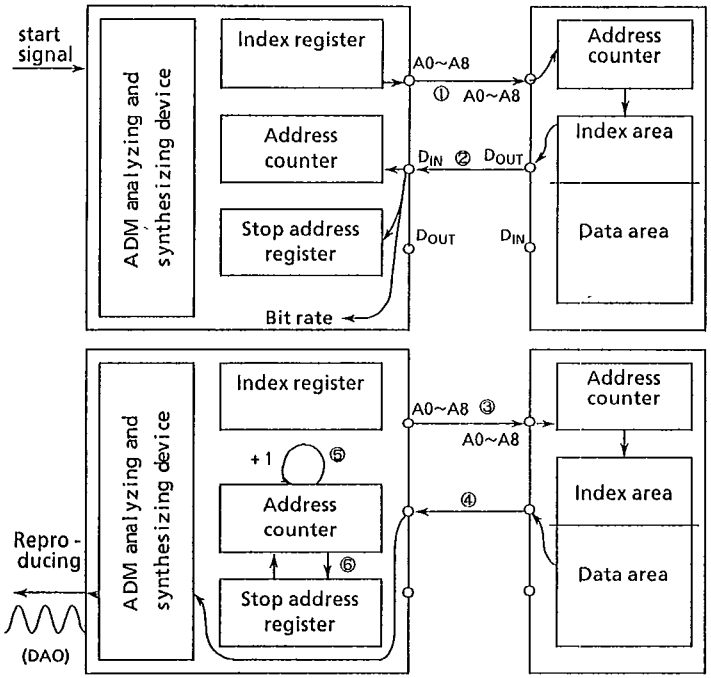
⑦ The value of bit rate is written into the index area.

⑧ The value of the address counter of T6668 is written into the area.

⑨ The address counter of T6668 is counted up and the recording end.

Fig.5.15 Access to memory in recording

(2) At time of reproducing



① The contents of the index register are loaded on the address counter of D - RAM by the start signal.

② Start address is loaded to the address counter of T6668 and end address as well as bit rate are loaded to the stop address register, respectively, from the index area.

③ Values of the address counter of the T6668 are loaded on the address counter of D - RAM.

④ Voice data is out into ADM analyzing and synthesizing device to reproduce voice waveform.

⑤ The address counter of the T6668 is counted up.

⑥ The address counter and the stop address register of the T6668 are compared and when they agree with each other, the reproducing stop at next address.
If not, steps ③ - ⑥ are repeated.

Fig.5.16 Access to memory in reproducing

5.7 Maximum Address of RAM

When the contents of the address counter reach the maximum address during the recording in the label index mode at the manual and CPU controls, the T6668 stops the recording automatically. In this case, the maximum address is stored as the the end address of a phrase at that time. Further, the address counter is preset at 00400H address and stops there.

Therefore, in the recording / reproducing of the one phrase only, the stop switch (D5) becomes unnecessary. In other words, when a certain time has passed after starting the recording (when the recording is made to the last of RAM), the recording ends and also, the reproducing stops after the contents of RAM were spoken to the last.

This maximum address changes according to the settings of the pin 256 K, M1 and M2 of the T6668. These pins shall be set according to kind and quantity of externally connected RAM. (Table 5.6)

Table 5.6 External RAMs and maximum addresses

External RAM	256 K * Note	M2	M1	Maximum Address
64K D - RAM 1 pc.	0	0	0	FFFFH
64K D - RAM 2 pcs.	0	0	1	1FFFFH
64K D - RAM 3 pcs.	0	1	0	2FFFFH
64K D - RAM 4 pcs.	0	1	1	3FFFFH
256K D - RAM 1 pc.	1	0	0	3FFFFH
256K D - RAM 2 pcs.	1	0	1	7FFFFH
256K D - RAM 3 pcs.	1	1	0	BFFFFH
256K D - RAM 4 pcs.	1	1	1	FFFFFH

HEX CODE

* Note
0 = L level
1 = H level

5.8 Reset Operation

5.8.1 The Status during Reset Operation

Low level to $\overline{ACL}$ pin causes the reset to T6668 in both of the manual control and CPU control, and all operations such as recording / reproducing stop. However, the refresh counter continues to operate and therefore, the data stored in D - RAM(s) remain unchanged. Further, BUSY bit of status register becomes 1 during this period and therefore, recording / reproducing start inputs under the manual control mode and command input under CPU control mode should not be given.

5.8.2 The Status after Reset Operation

When $\overline{ACL}$ pin becomes from L to H level, the internal state of T6668 is initialized as shown below.

(1) In CPU control mode, it becomes reproducing mode.

(2) Address counter and stop address register are preset to 00400H.

(3) Address overflow detector and address comparator flip - flop are reset.

(4) In CPU control mode, bit rate becomes 8Kbps, and "Silence Status" is released.

(5) ERR and OVR bits in status register are reset.
After terminating the above completely, BUSY bit in status register is set to "0".

5.8.3 Reset Processing after Power ON

After Power ON, the following items become instable;

(1) Change - over of recording / reproducing modes

(2) Address counter

(3) ADM arithmetic system

(4) Other processing registers such as start and stop processing

Therefore, to initialize this instable condition and assure proper operations, apply $\overline{ACL}$ signal. (System reset)

$\overline{ACL}$ signal to be given after power ON and its pulse width are shown in Fig.5.13.

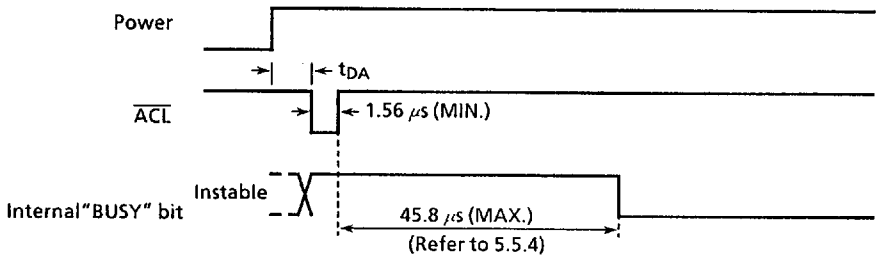


Fig.5.17 $\overline{ACL}$ pulse width

However, if width of t_{DA} after power ON is long, the instable status lasts and causes malfunction (start of recording / reproducing, etc.) in Fig.5.18. So, in [10] Application Circuit in the manual control mode, an automatic clear circuit is configured to input integral waveform by time constant of a pull-up resistor (7 k~20 kΩ) housed in the $\overline{ACL}$ pin by attaching a 1μF capacitor to the $\overline{ACL}$ pin, making the system initialization possible immediately after power ON as illustrated in Fig.5.18.

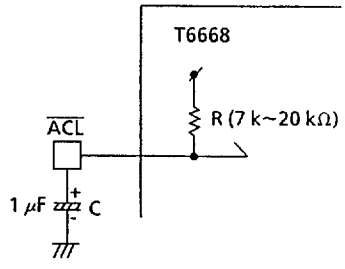


Fig.5.18 Circuit for power on reset

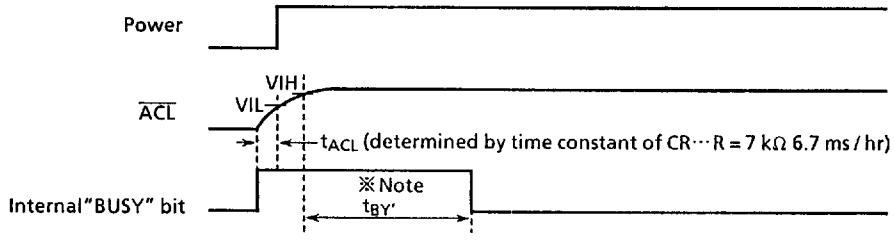


Fig.5.19 $\overline{ACL}$ input at power on reset

However, the power on reset is effective only for a step power rise and when power rise is gentle, no system initialization is performed. (Fig.5.20)

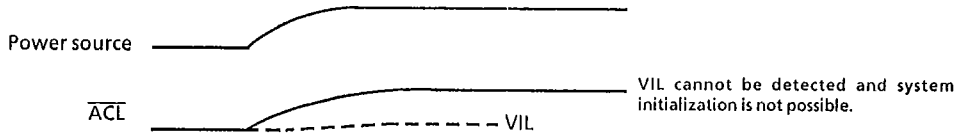


Fig.5.20 In case power rise is gentle

Further, if the $\overline{ACL}$ pin can be controlled under CPU control mode regardless of power ON / OFF at T6668 side, the system initialization can be applied as shown in Fig.5.21.

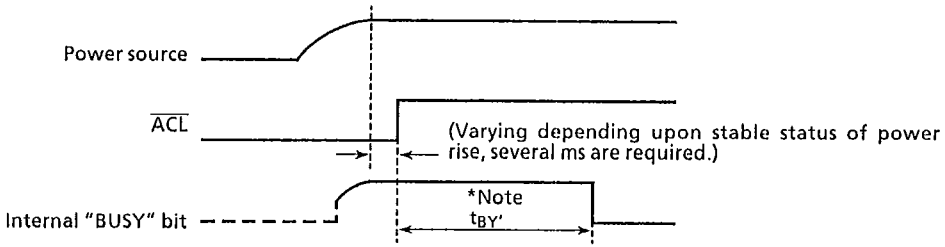
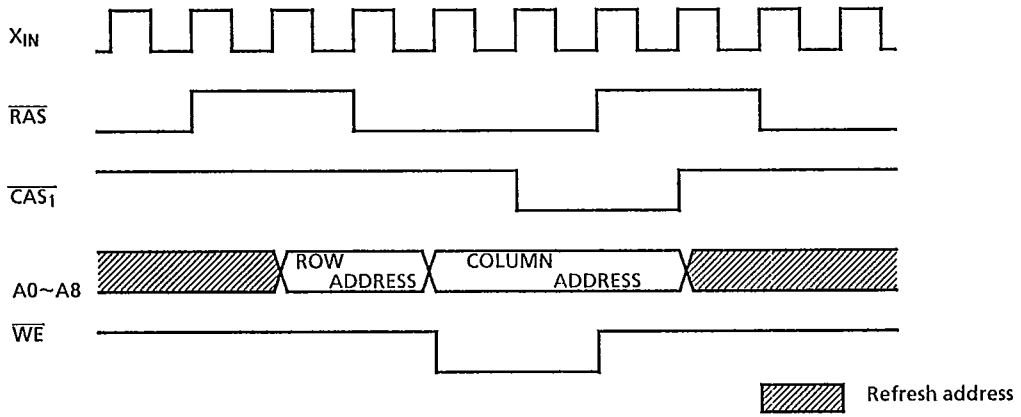


Fig.5.21 System initialization by CPU control

* Note $t_{BY'}$ is a time from power ON till oscillation is stabilized and varies depending on an external oscillator. (Several ms in case if CSB655)

5.9 Operation of Address Counter

The operation of address counter of the T6668 and the memory map of the index area are described here.



	Pin name →	A8	A1	A8	A1
Designate address	256 K	COLUMN A17 — A9		ROW A8 — A0	
	64 K	A15 — A8		~~A7~~ — ~~A0~~	

Fig.5.22 Address output

5.10 Connection to D - RAMS

The T6668 needs outer D - RAMs (dynamic RAMs) for the storage of recorded voice data.

Maximum four 64K D - RAMs or four 256K D - RAMs are directly connected to the T6668. But is impossible to connect 64K D - RAMs and 256K D - RAMs at the same time.

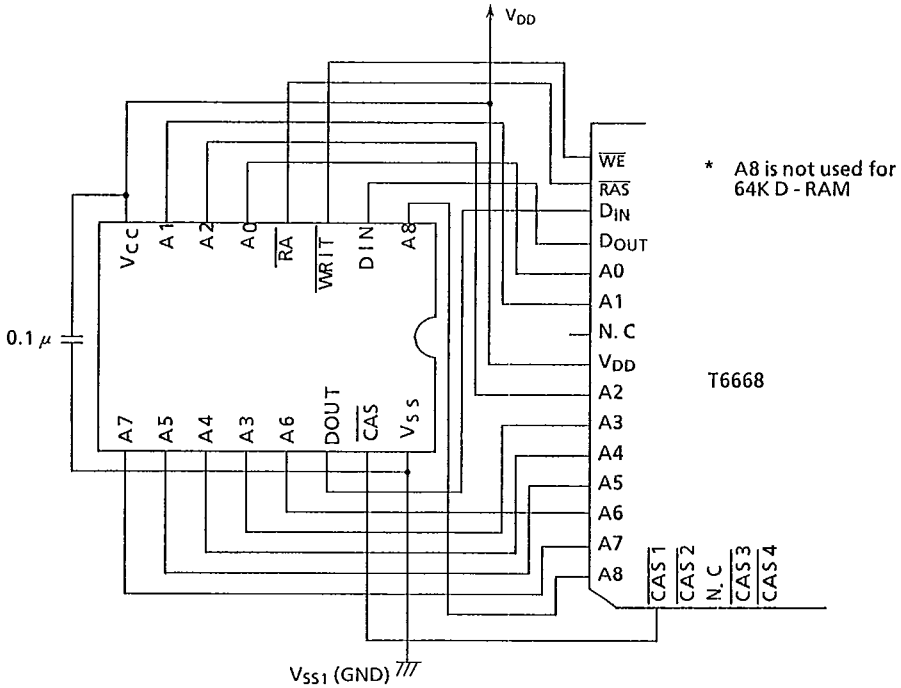


Fig.5.23 Connection with D - RAM

Fig. 5.23 shows the connection with D - RAM. In case of two or more D - RAMs, $\overline{CAS1}$ pin T6668 must be connected to the $\overline{CAS}$ pin of 1st D - RAM, the $\overline{CAS2}$ pin of T6668 to the $\overline{CAS}$ pin of 2nd D - RAM and so on. That is, $\overline{CAS1}$~$\overline{CAS4}$ pins must be connected to the $\overline{CAS}$ pin of D - RAMs, respectively. Other pins about D - RAM of T6668 may be connected in parallel to every D - RAMs. (See 3.3 "Example of Voice Recording / Reproducing LST System Configuration".) Some pins of T6668 must be settled high or low according to the type and number of outer D - RAMs. Table 5.7 shows the setting conditions. These conditions shown in Table must not be changed during recording or reproducing operation.

Table 5.7 Pin setting according to type and number of D - RAMs

Type of D - RAM \ Pin name	256K
256K	1
64K	0

Number of D - RAM \ Pin name	M2	M1
1 pc	0	0
2 pcs	0	1
3 pcs	1	0
4 pcs	1	1

0 = L level
1 = H level

5.11 Analog Function

The T6668 has built in microphone amplifier and 2nd stage low pass+1st stage high pass filter. Therefore, voice recording / reproducing system is easily available by connecting input to MIC and output to audio Amplifier circuit.

5.11.1 Microphone Amplifier

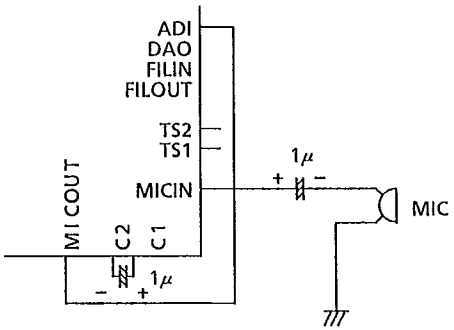


Fig.5.24 Connection of MIC

Note: Be careful for wiring. The signal from microphone is so small that noise from surroundings tends to have influence.

There are two MIC. AMP. s.

① between MICIN and C1 ..... Gain is about 26 dB

② between C2 and MICOUT ..... Gain is about 20 dB

So, there are three ways ①, ② and ① + ②. One is selected by the type of MIC. C1 or MICOUT pin must be connected to ADI pin at the case of ① or ② and ① + ②, respectively.

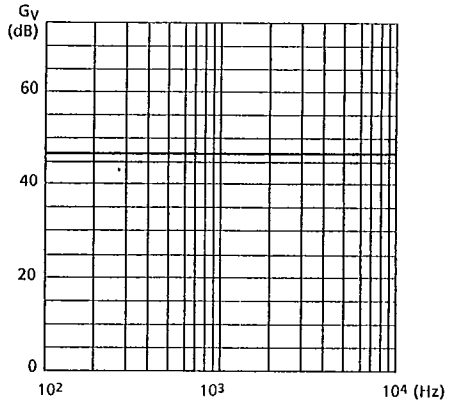


Fig.5.25 Frequency characteristics of MIC. AMP.

This characteristics is between MICIN and MICOUT with couplings C1 and C2. Further, when MIC Amp is not used, it is possible to input voice directly input ADI. In this case, however, the input level should be max. 1.6 Vp-p, centering around 1 / 2 V_{DD}.

5.11.2 Filter

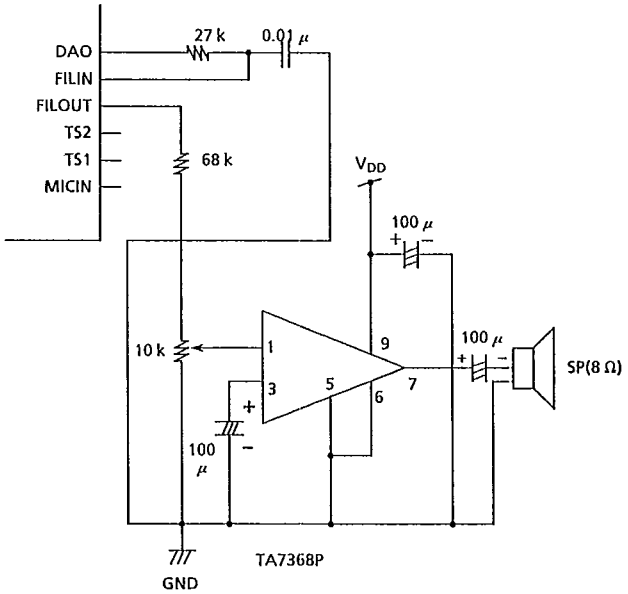


Fig.5.26 Connection of audio amp.

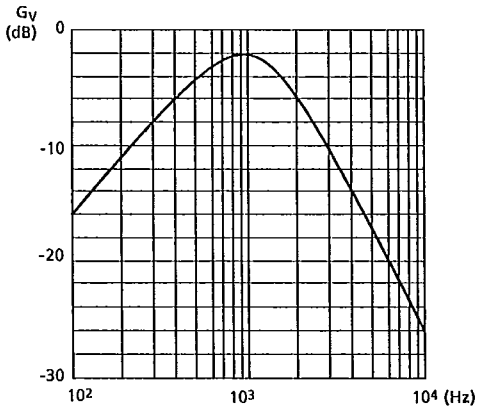


Fig.5.27 Frequency characteristics of band pass filter

This characteristic is between FILIN and FILOUT.

5.11.3 Equivalent Circuits

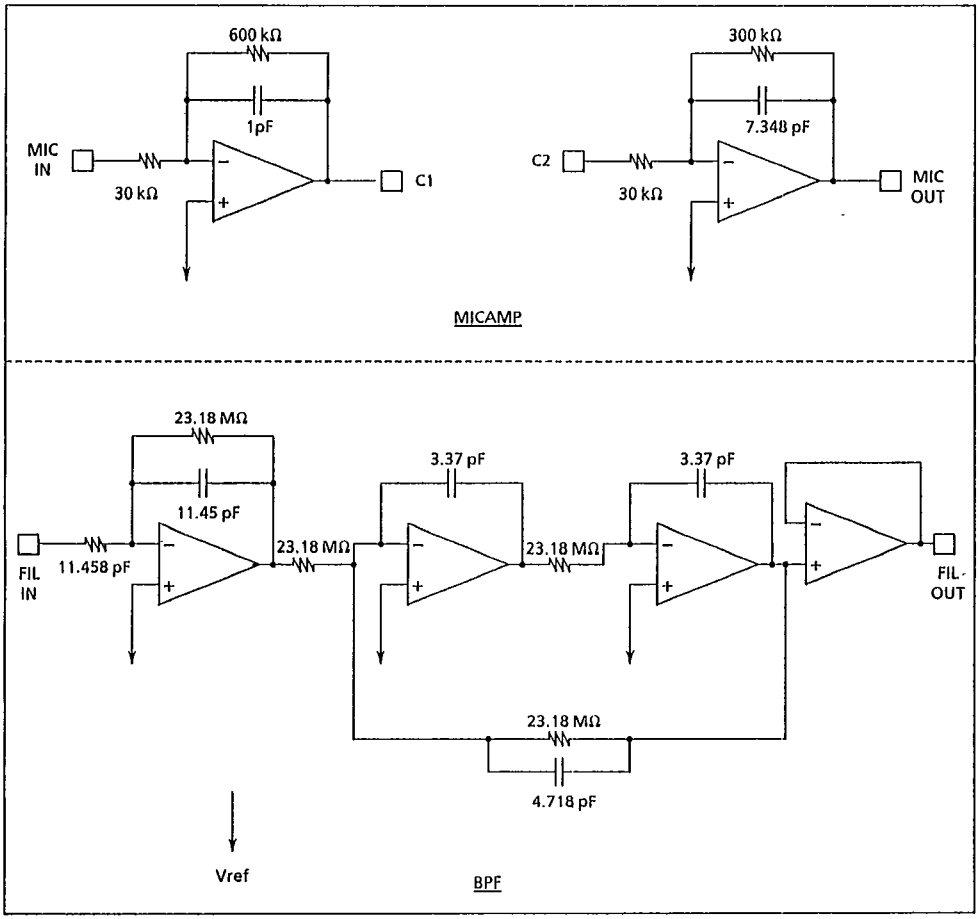


Fig.5.28 Equivalent circuits of analog circuits

5.12 Precautions

(1) Under manual and CPU control mode

- During recording or reproducing operation, pins of M1, M2 and 256K must not be changed.
- During the reset, the address counter, flag, etc. only are reset and oscillation does not stop; that is, the refresh of D - RAM is performed.

(2) Under manual control mode

- The conditions of phrase, bit rate and recording / reproducing are kept held by START input and not changed until next START input is given. That is, T6668 does not care those conditions after START operation has done.
- During recording, START input is not accepted. This is to protect RAM data in the index area from being destructed when phrase number etc. are changed by START input during recording.
- During reproducing, START input is accepted as the buffer function is available.
  In this case, the operation must not be started with $\overline{WR}$ placed in H level (recording mode). RAM data change and the reproducing is not properly performed.
- The START input during the recording is inhibited at address over condition (when the maximum RAM capacity is already used.). Resets address by $\overline{ACL}$ for recording.

(3) Under CPU control mode

- During recording / reproducing, do not give any other commands other than STOP command. When other commands are input to the T6668, the operation becomes unstable.

6. ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Rating

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Supply Voltage	− 0.3 ~ 6.0	V
V_{IN}	Input Voltage	− 0.3 ~ V_{DD} + 0.3	V
V_{OUT}	Output Voltage	− 0.3 ~ V_{DD} + 0.3	V
T_{STG}	Storage Temperature	− 55 ~ 125	°C

6.2 Recommended Operating Condition

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	4.5 ~ 5.5	V
Input Voltage	V_{IN}	0 ~ V_{DD}	V
Output Voltage	V_{OUT}	0 ~ V_{DD}	V
Oscillation Frequency	f_{CLK}	640 ~ 1000	KHz
Operating Temperature	T_{opr}	− 10 ~ 70	°C

6.3 DC Characteristics (V_{DD} = 5 V ± 10 %, Ta = 25 °C)

SYMBOL	ITEM	CONDITION	MIN.	TYP.	MAX.	UNIT
I_{IH}	Input Current (D_0~D_7, TEST, $\overline{CE}$, $\overline{RD}$, $\overline{WR}$)	$V_{IN} = V_{DD}$, CPUM = L	20	100	500	μA
I_{IL1}	Input Current 1 D_{IN})	V_{IN} = 0	50	100	350	
I_{IL2}	Input Current 2 ($\overline{ACL}$)	V_{IN} = 0	250	500	700	
I_{ILK}	Input Leak Current	V_{IN} = 0~V_{DD}, CPUM = H	–	–	± 10	
V_{IHI1}	High Level Input Voltage1	D0~D7, $\overline{CE}$, $\overline{RD}$, $\overline{WR}$, DIN	2.4	–	–	V
V_{IHI2}	High Level Input Voltage2	Except above	4.1	–	–	
V_{IL1}	Low Level Input Voltage1	D0~D7, $\overline{CE}$, $\overline{RD}$, $\overline{WR}$, DIN	–	–	0.8	
V_{IL2}	Low Level Input Voltage2	Except above	–	–	0.4	
I_{OH}	High Level Output Current	V_{OUT} = 2.4 V	0.5	–	–	mA
I_{OL}	Low Level Output Current	V_{OUT} = 0.8 V	0.5	–	–	
I_{SS1}	Supply Current 1 (V_{SS1})	Under no signal, I_{OUT} = 0 mA	–	1.0	3.0	
I_{SS2}	Supply Current 2 (V_{SS2})	Under no signal, I_{OUT} = 0 mA	–	1.0	3.0	

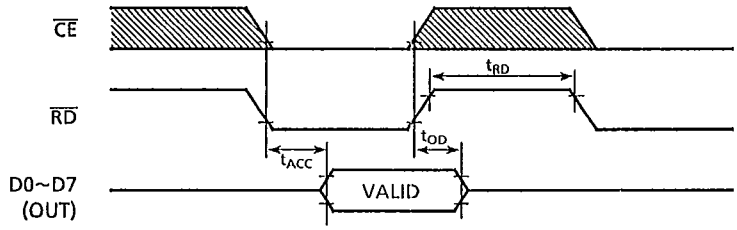
Note: Each TYP. value is under V_{DD} = 5.0 V, Ta = 25 °C
MIN. and MAX. values are defined by their absolute values.

6.4 AC Characteristics (V_{DD} = 5 V ± 10%, Ta = 25 °C, f_{CLK} = 655 kHz, C_L = 50 pF)

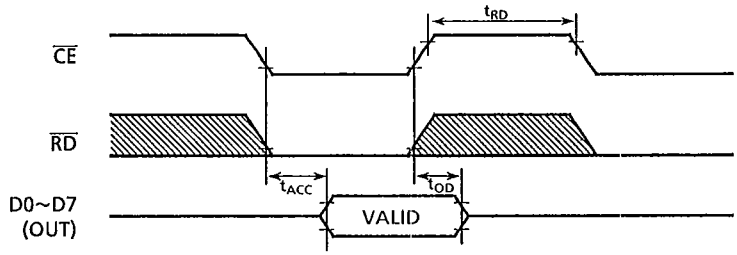
6.4.1 For Data Read (Status Reading)

SYMBOL	ITEM	MIN.	TYP.	MAX.	UNIT
t_{RD}	Read Disable Time (ADRD Command)	21	–	–	μs
t_{ACC}	Read Access Time	–	–	300	ns
t_{OD}	Output Disable Time	–	–	150	

Data Read (1)



Data Read (2)

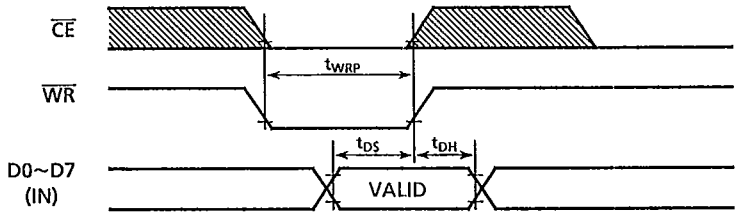


Don't Care

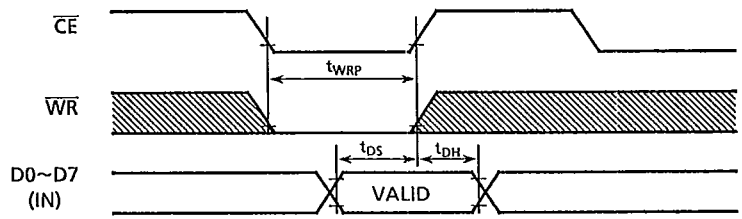
6.4.2 For Data Write (Command Write)

SYMBOL	ITEM	MIN.	TYP.	MAX.	UNIT
t_{DS}	Data Set Up Time	500	–	–	ns
t_{DH}	Data Hold Time	0	–	–	ns
t_{WRP}	$\overline{WR}$ Pulse Width	300	–	–	ns

Data Write (1)



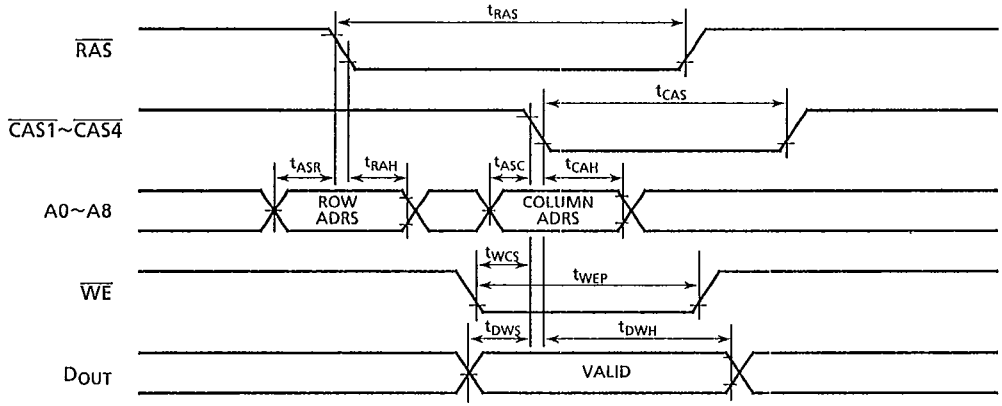
Data Write (2)



Don't Care

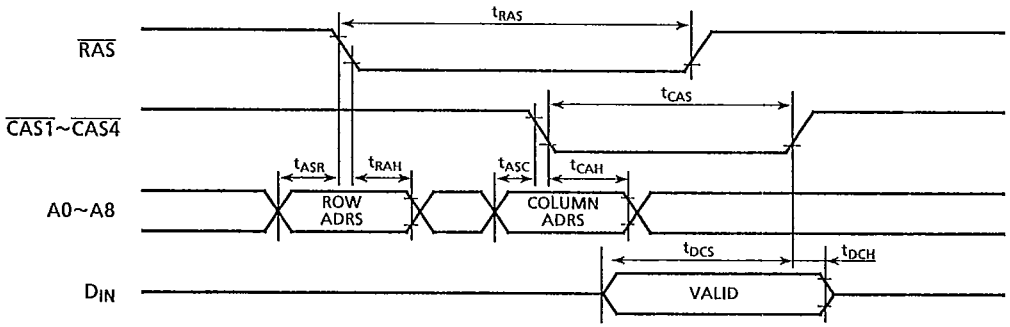
6.4.3 For Voice Analysis (At Recording)

SYMBOL	ITEM	MIN.	TYP.	MAX.	UNIT
t_{ASR}	Low Address Set - up Time	150	–	–	ns
t_{RAH}	Low Address Hold Time	500	–	–	
t_{RAS}	$\overline{RAS}$ Pulse Width	–	4.58	–	μs
t_{ASC}	Column Address Set - up Time	150	–	–	ns
t_{CAH}	Column Address Hold Time	500	–	–	
t_{CAS}	$\overline{CAS}$ Pulse Width	–	3.05	–	μs
t_{WCS}	Write Command Set - up Time	–	1.53	–	μs
t_{WEP}	$\overline{WE}$ Pulse Width	–	3.05	–	
t_{DWS}	Data Output Set - up Time	500	–	–	ns
t_{DWH}	Data Output Hold Time	500	–	–	



6.4.4 For Voice Synthesis (At Reproducing)

SYMBOL	ITEM	MIN.	TYP.	MAX	UNIT
t_{DCS}	Data Input Set - up Time	500	–	–	ns
t_{DCH}	Data Input Hold Time	0	–	–	ns



6.5 Characteristics of Analog Function

6.5.1 Micamp. ($V_{SS1} = V_{SS2} = OV$, $V_{DD} = 5$ V, Ta = 25 °C, $f_{in} = 1$ kHz, UNLESS OTHERWISE SPECIFIED)

SYMBOL	ITEM	PIN NAME	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{IN1}	Allowable Input Voltage Range	MICIN	MICAMP (1) + (2)	–	6	8	mVp-p
V_{IN2}		MICIN	MICAMP (1) only	–	60	80	
V_{IN3}		C2	MICAMP (2) only	–	120	160	
G_{V1}	Pass Band Gain	MICIN -MICOUT	V_{IN} = 6 mVp-p f_{IN} = 100 Hz ~ 10 kHz	–	46	–	dB
G_{V2}		MICIN -C1		–	26	–	
G_{V3}		C2 -MICOUT		–	20	–	
THD	Total Harmonic Distortion	MICIN -MICOUT	V_{IN} = 6 mVp-p f_{IN} = 100 Hz ~ 10 kHz	–	–	2	%
R_{IN1}	Input Resistance	MICIN	–	20	30	40	kΩ
R_{IN2}		C2		20	30	40	
R_{OUT1}	Output Resistance	C1	–	–	1	–	kΩ
R_{OUT2}		MICOUT		–	1	–	

6.5.2 Band Pass Filter (DITTO)

SYMBOL	ITEM	PIN NAME	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{IN}	Allowable Input Voltage Range	FILIN	–	–	2.4	2.6	Vp-p
G_V	Pass Band Gain	FILIN -FILOUT	V_{IN} = 1.0 Vp-p f_{IN} = 100 Hz ~ 10 kHz	-27	–	-1	dB
THD	Total Harmonic Distortion	FILIN -FILOUT	V_{IN} = 1.0 Vp-p f_{IN} = 100 Hz ~ 10 kHz	–	–	4	%
R_{IN}	Input Resistance	FILIN	–	5	14	20	MΩ
R_{OUT}	Output Resistance	FILOUT	–	–	1	–	kΩ

6.5.3 Audio In (DITTO)

SYMBOL	ITEM	PIN NAME	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{IN}	Allowable Input Voltage Range	ADI	–	–	1.2	1.6	Vp-p
R_{IN}	Input Resistance	ADI	–	1	–	–	MΩ

6.5.4 Audio Out (DITTO)

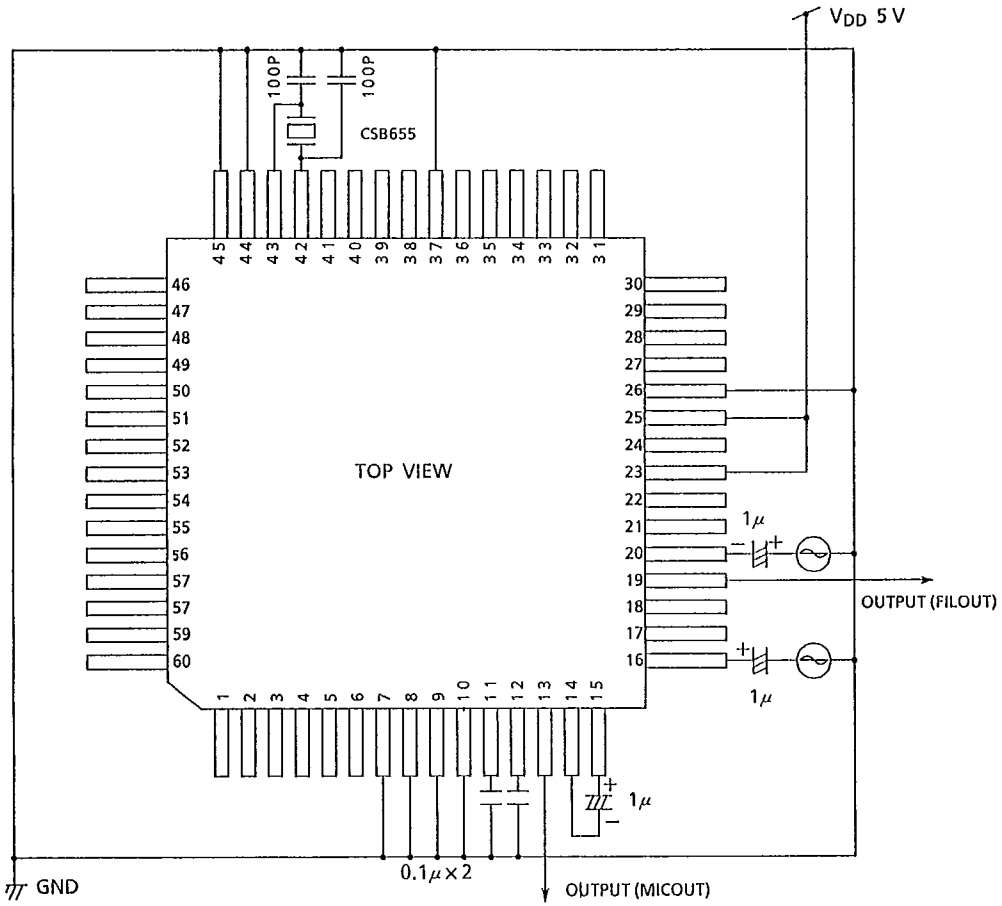
SYMBOL	ITEM	PIN NAME	CONDITION	MIN.	TYP.	MAX.	UNIT
R_{OUT}	Output Resistance	DAO	–	–	5	–	kΩ

Note : Values centering around 1/2 V_{DD} are used in allowable input voltage range.

6.5.5 Measuring Circuit

(V_{IN}, G_V, THD)

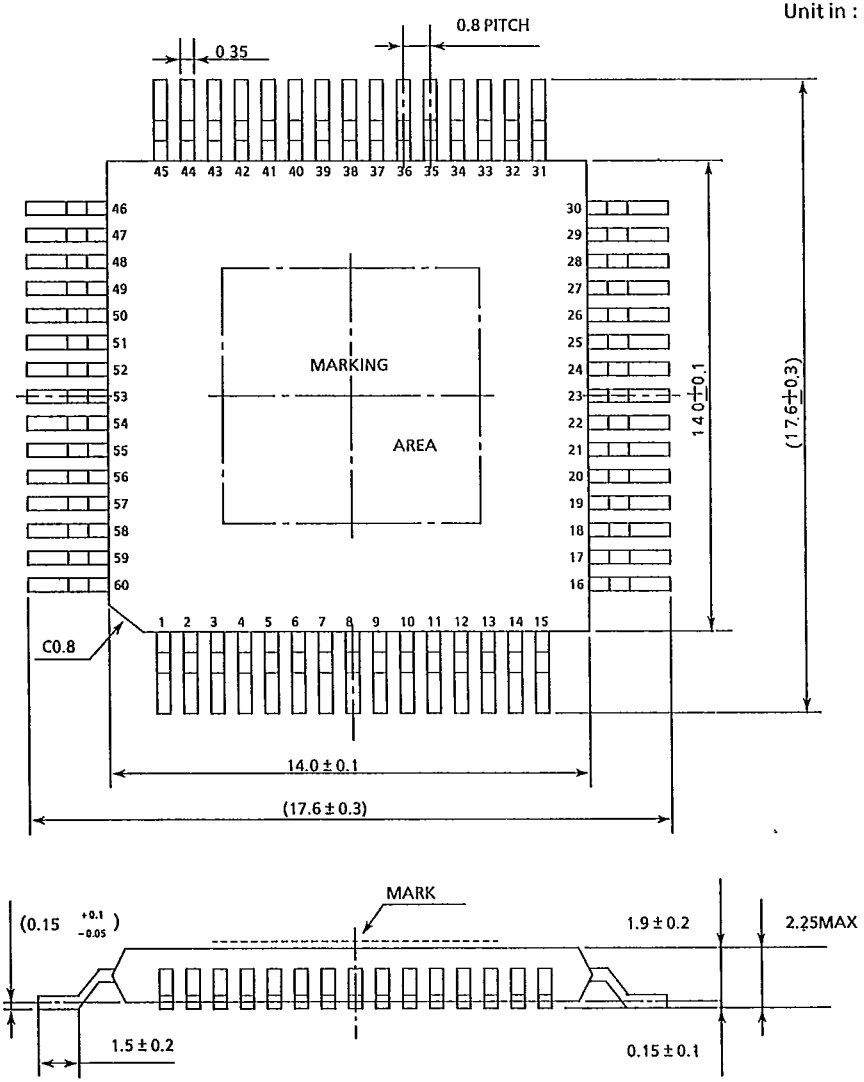
Refer to [4] Pin Connections for pin name.



7. OUTLINE DRAWINGS

60 PIN MINI FLAT PACKAGE

Unit in : mm



8. APPLICATION CIRCUIT