TOSHIBA Field Effect Transistor Silicon P Channel MOS Type (U-MOSⅣ)

TPCA8103

Lithium Ion Battery Applications
Notebook PC Applications
Portable Equipment Applications

- Small footprint due to small and thin package
- Low drain-source ON resistance: $R_{DS\ (ON)}$ = 3.1 mΩ (typ.)
- High forward transfer admittance: $|Y_{fs}|$ = 45S (typ.)
- Low leakage current: I_{DSS} = −10 μA (max) (V_{DS} = −30 V)
- Enhancement mode: V_{th} = −0.8 to −2.0 V (V_{DS} = −10 V, I_D = −1 mA)

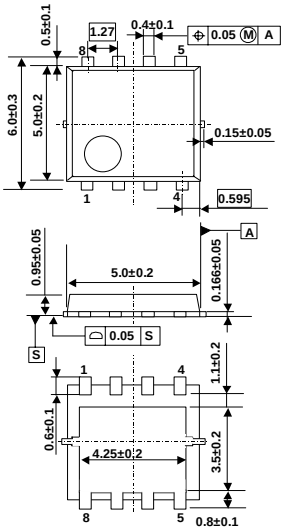
Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	−30	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	−30	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	DC (Note 1)	I_D	− 40	A
	Pulsed (Note 1)	I_{DP}	−120	
Drain power dissipation (Tc=25°C)		P_D	45	W
Drain power dissipation (t = 10 s) (Note 2a)		P_D	2.8	W
Drain power dissipation (t = 10 s) (Note 2b)		P_D	1.6	W
Single pulse avalanche energy (Note 3)		E_{AS}	208	mJ
Avalanche current		I_{AR}	− 40	A
Repetitive avalanche energy (Tc=25°C) (Note 4)		E_{AR}	4.5	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

Note: For (Note 1), (Note 2), (Note 3), (Note 4), please refer to the next page.

This transistor is an electrostatic sensitive device. Please handle with caution.

Unit: mm

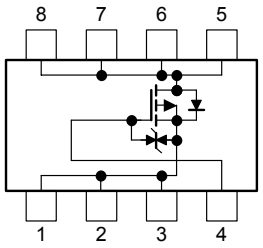


1,2,3 : SOURCE
4 : GATE
5,6,7,8 : DRAIN

JEDEC	—
JEITA	—
TOSHIBA	2-5Q1A

Weight: 0.076 g (typ.)

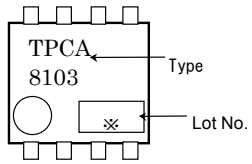
Circuit Configuration



Thermal Characteristics

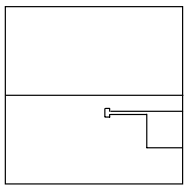
Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case (Tc=25°C)	$R_{th\ (ch\text{-}c)}$	2.78	°C/W
Thermal resistance, channel to ambient (t = 10 s) (Note 2a)	$R_{th\ (ch\text{-}a)}$	44.6	°C/W
Thermal resistance, channel to ambient (t = 10 s) (Note 2b)	$R_{th\ (ch\text{-}a)}$	78.1	°C/W

Marking (Note 5)



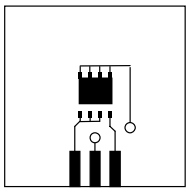
Note 1: Please use devices on condition that the channel temperature is below 150°C.

Note 2: (a) Device mounted on a glass-epoxy board (a) (b) Device mounted on a glass-epoxy board (b)



FR-4
25.4 × 25.4 × 0.8
(Unit: mm)

(a)



FR-4
25.4 × 25.4 × 0.8
(Unit: mm)

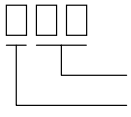
(b)

Note 3: V_{DD} = 24 V, T_{ch} = 25°C (initial), L = 100μH, R_G = 25 Ω, I_{AR} = − 40 A

Note 4: Repetitive rating: pulse width limited by max channel temperature

Note 5: ○ on lower left of the marking indicates Pin 1.

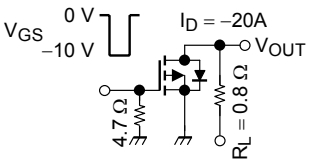
※ Weekly code: (Three digits)



Week of manufacture
(01 for first week of year, continues up to 52 or 53)

Year of manufacture
(One low-order digits of calendar year)

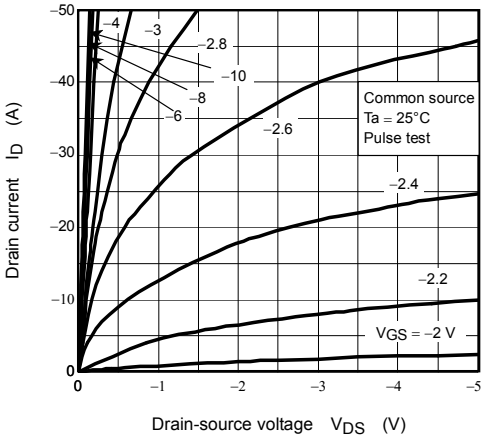
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±10	μA
Drain cut-OFF current		I_{DSS}	V_{DS} = −30 V, V_{GS} = 0 V	—	—	−10	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = −10 mA, V_{GS} = 0 V	−30	—	—	V
		$V_{(BR)\ DSX}$	I_D = −10 mA, V_{GS} = 20 V	−13	—	—	
Gate threshold voltage		V_{th}	V_{DS} = −10 V, I_D = − 1 mA	−0.8	—	−2.0	V
Drain-source ON resistance		$R_{DS\ (ON)}$	V_{GS} = −4 V, I_D = −20 A	—	5.2	6.8	mΩ
			V_{GS} = −10 V, I_D = −20 A	—	3.1	4.2	
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = −10 V, I_D = −20 A	22.5	45	—	S
Input capacitance		C_{iss}	V_{DS} = −10 V, V_{GS} = 0 V, f = 1 MHz	—	7880	—	pF
Reverse transfer capacitance		C_{rss}		—	1340	—	
Output capacitance		C_{oss}		—	1450	—	
Switching time	Rise time	t_r	 Duty ≦ 1%, t_w = 10 μs	—	15	—	ns
	Turn-ON time	t_{on}		—	13	—	
	Fall time	t_f		—	251	—	
	Turn-OFF time	t_{off}		—	596	—	
Total gate charge (gate-source plus gate-drain)		Q_g	V_{DD} ≃ −24 V, V_{GS} = −10 V, I_D = −40 A	—	184	—	nC
Gate-source charge 1		Q_{gs1}		—	12	—	
Gate-drain (“miller”) charge		Q_{gd}		—	58	—	

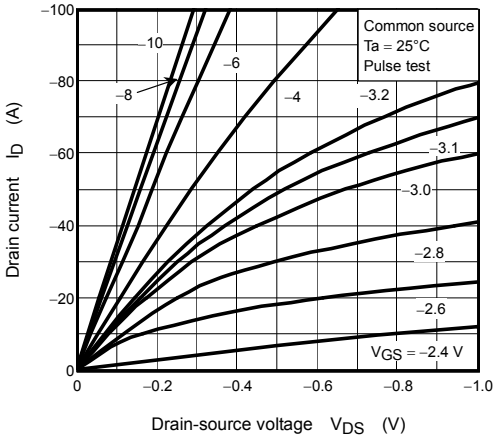
Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain reverse current	Pulse (Note 1)	I_{DRP}	—	—	—	−120	A
Forward voltage (diode)		V_{DSF}	I_{DR} = −40 A, V_{GS} = 0 V	—	—	1.2	V

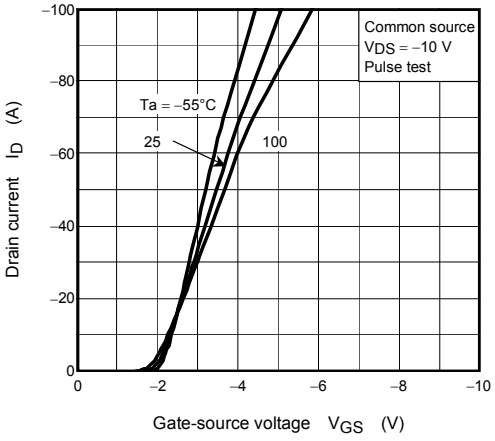
$I_D - V_{DS}$



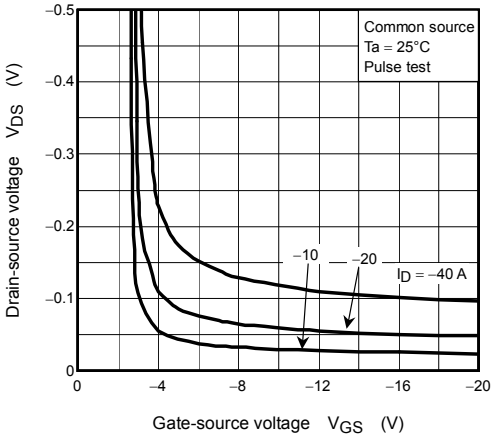
$I_D - V_{DS}$



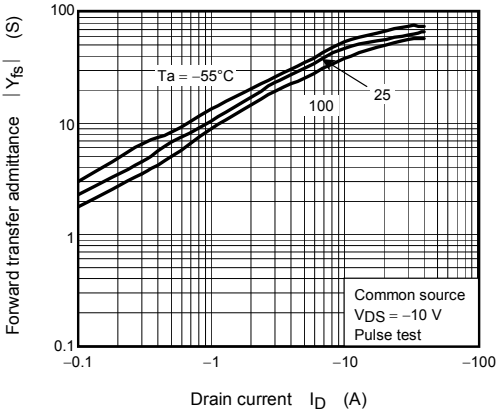
$I_D - V_{GS}$



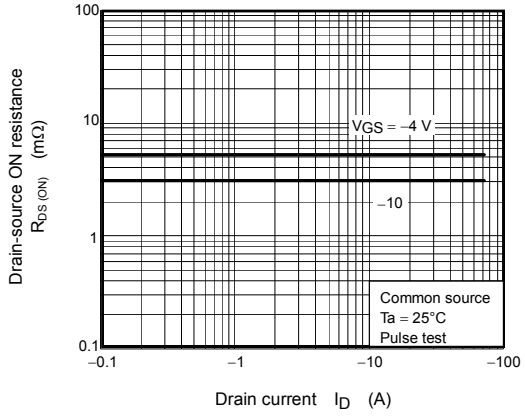
$V_{DS} - V_{GS}$



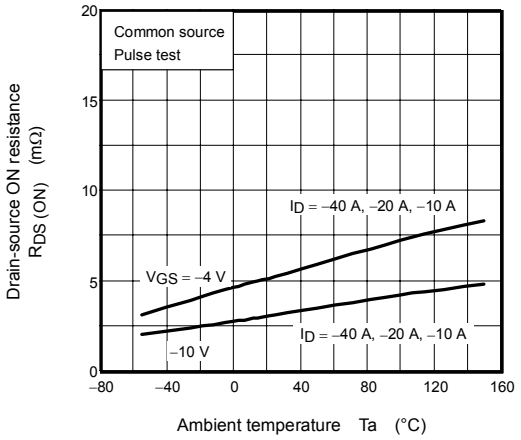
$|Y_{fs}| - I_D$



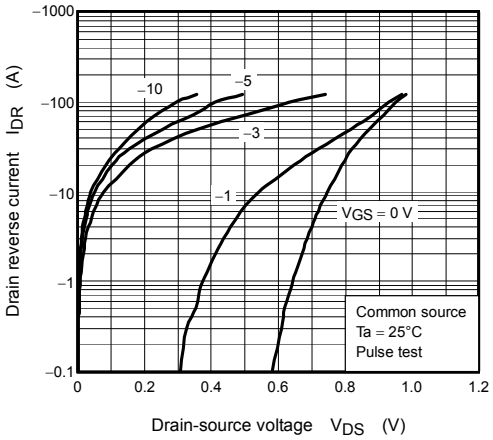
$R_{DS\ (ON)} - I_D$



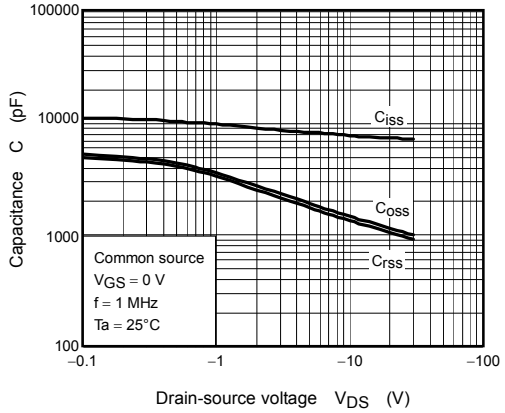
$R_{DS\ (ON)}$ – Ta



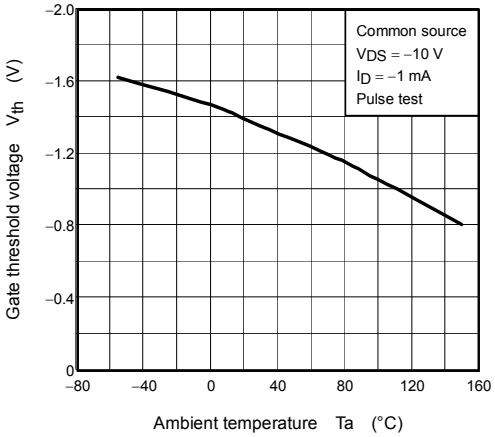
I_{DR} – V_{DS}



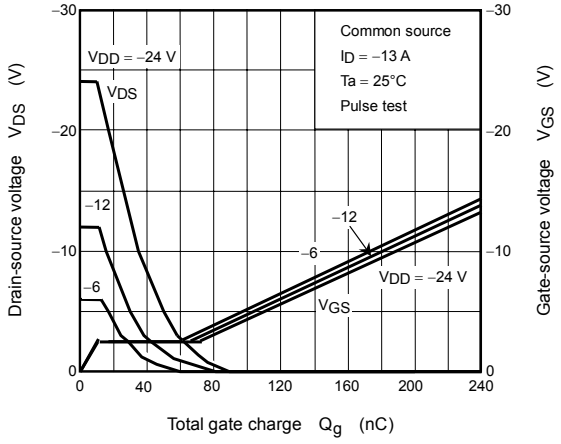
Capacitance – V_{DS}



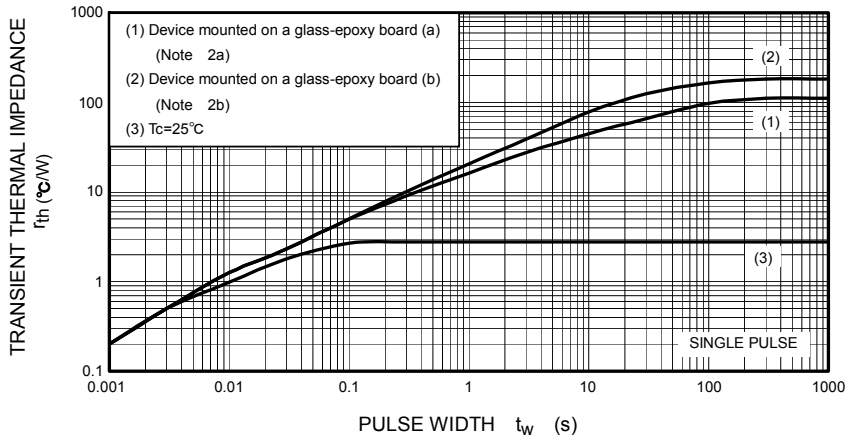
V_{th} – Ta



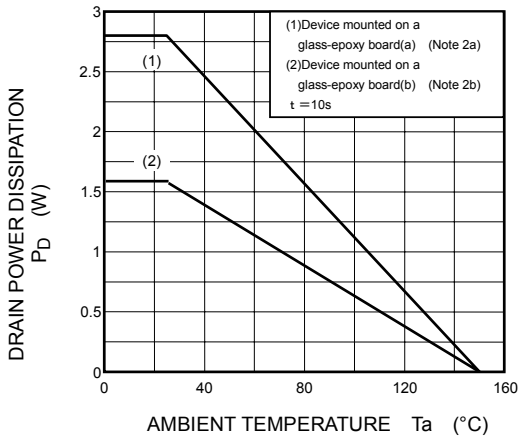
Dynamic input/output characteristics



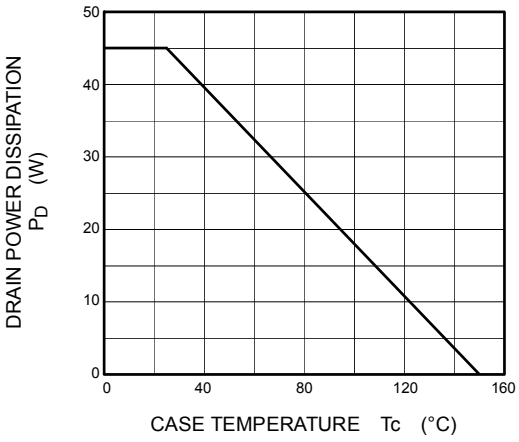
$r_{th} - t_w$



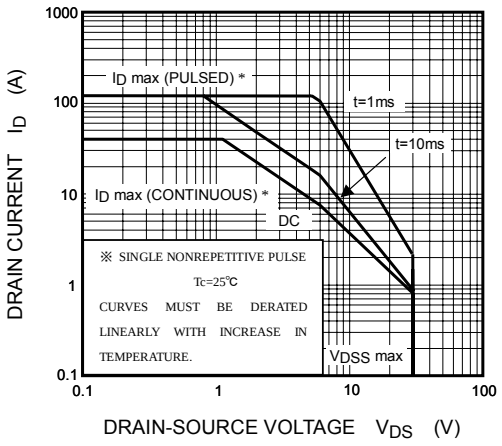
$P_D - Ta$



$P_D - Tc$



SAFE OPERATING AREA



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