TOSHIBA BI-DIRECTIONAL TRIODE THYRISTOR SILICON PLANAR TYPE

## SM12G48, USM12G48, SM12J48, USM12J48 SM12G48A, USM12G48A, SM12J48A, USM12J48A

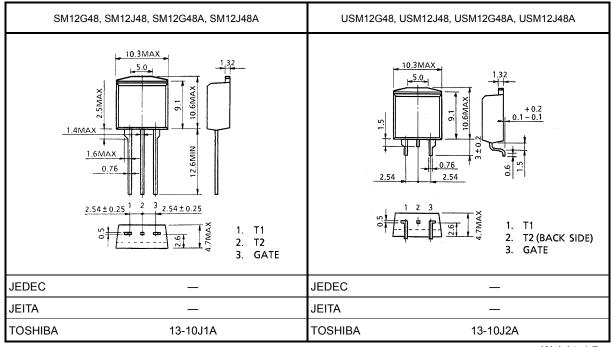
#### AC POWER CONTROL APPLICATIONS

Repetitive Peak Off-State Voltage : VDRM=400V, 600V
 R.M.S. On-State Current : IT (RMS) =12A

• Gate Trigger Current : IGT=30mA Max.

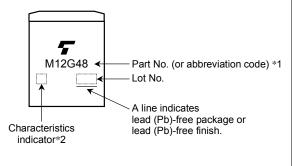
: IGT=20mA Max. ("A"Type)

Unit: mm



Weight: 1.7g

#### **MARKING**



	Part No. (or abbreviation code)	Part No.		
*1	M12G48	SM12G48, SM12G48A		
	W12G46	USM12G48, USM12G48A		
	M12J48	SM12J48, SM12J48A		
		USM12J48, USM12J48A		
*2	Nothing	SM12G48, SM12J48		
	Nouning	USM12G48, USM12J48		
	А	SM12G48A, SM12J48A		
		USM12G48A, USM12J48A		

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## **MAXIMUM RATINGS**

CHARACT	ERISTIC	SYMBOL RATING		UNIT	
Repetitive Peak	(U)SM12G48 (U)SM12G48A	$V_{DRM}$	400	·	
Off-State Voltage	(U)SM12J48 (U)SM12J48A	V DRM	600		
R.M.S On-State Cur	rent	I <sub>T (RMS)</sub>	12	Α	
Peak One Cycle Sur	ge On-State	I <sub>TSM</sub>	120 (50Hz)	Α	
Current (Non-Repeti	tive)		132 (60Hz)	A	
I <sup>2</sup> t Limit Value		1 <sup>2</sup> t	72	A <sup>2</sup> s	
Critical Rate of Rise On-State Current	of (Note 1)	di /dt	50	A / μs	
Peak Gate Power Di	ssipation	$P_{GM}$	5	W	
Average Gate Power	r Dissipation	P <sub>G (AV)</sub>	P <sub>G (AV)</sub> 0.5		
Peak Forward Gate	Voltage	$V_{GM}$	10	V	
Peak Forward Gate	Current	I <sub>GM</sub>	2	Α	
Junction Temperatur	re	Tj	-40~125	°C	
Storage Temperature	e Range	T <sub>stg</sub>	-40~125	°C	

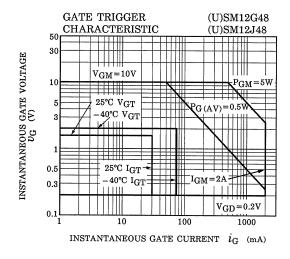
 $\begin{tabular}{ll} Note 1: & V_{DRM}=0.5\times Rated \\ & I_{TM}\le 15A \\ & t_{gw}\ge 10\mu s \\ & t_{gr}\le 250ns \\ & i_{gp}=I_{GT}\times 2.0 \\ \end{tabular}$ 

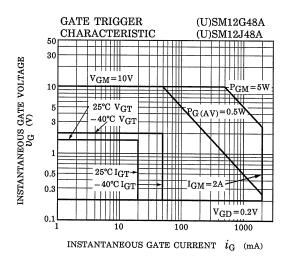
## **ELECTRICAL CHARACTERISTICS (Ta=25°C)**

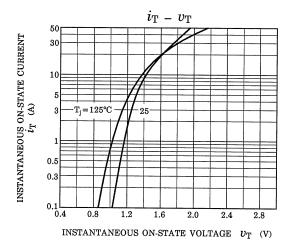
CHARACTERISTIC			SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT	
Repetitive Peak Off-State Current			I <sub>DRM</sub>	V <sub>DRM</sub> =Rated		_	_	20	μА	
Gate Trigger Voltage  II  II  IV		V <sub>GT</sub>	$V_D$ =12V $R_L$ =20 $\Omega$	T2 (+) , Gate (+)	_	_	1.5	V		
				T2 (+) , Gate (-)	_	_	1.5			
				T2 (-) , Gate (-)	_	_	1.5			
				T2 (-) , Gate (+)	_	_	_			
Gate Trigger		SM12G48 SM12J48			V <sub>D</sub> =12V	T2 (+) , Gate (+)	_	_	30	mA
	SM12					T2 (+) , Gate (-)	_	_	30	
	SM12					T2 (-) , Gate (-)	_	_	30	
						T2 (-) , Gate (+)	_	_	_	
Current			1	I <sub>GT</sub>	R <sub>L</sub> =20Ω	T2 (+) , Gate (+)	_	_	20	- MA
	SM12	2G48A	II			T2 (+) , Gate (-)	_	_	20	
	SM12J48	2J48A	III			T2 (-) , Gate (-)	_	_	20	
						T2 (-) , Gate (+)	_	_	_	
Peak On-State Voltage			V <sub>TM</sub>	I <sub>TM</sub> =17A		_	_	1.5	٧	
Gate Non-Trigger Voltage			$V_{GD}$	V <sub>D</sub> =Rated, Tc=125°C		0.2	_	_	٧	
Holding Current				lΗ	V <sub>D</sub> =12V, I <sub>TM</sub> =1A		_	_	50	mA
Thermal Resistance			R <sub>th (j-c)</sub>	Junction to Case, AC		_	_	2.4	°C/W	
Critical Rate of Rise of Off-State Voltage		(U)SM12G48 (U)SM12J48 (U)SM12G48A (U)SM12J48A		dv / dt	V <sub>DRM</sub> =Rated, T <sub>j</sub> =125°C Exponential Rise		_	300	_	- V / μs
				dv / dt			_	200	_	
Critical Rate of F			(dv / dt) c	V <sub>DRM</sub> =400V, T <sub>i</sub> =125°C (di / dt) c=-6.5A / ms		10	_	_	- V / μs	
Off-State Voltage at Commutation		(U)SM12G48A (U)SM12J48A				(dv / dt) c	4	_		_

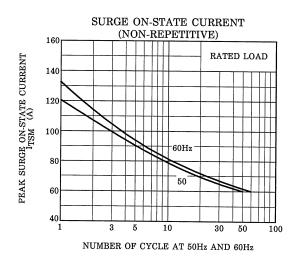
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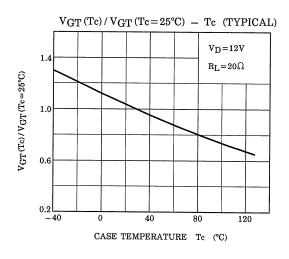
## **TOSHIBA** SM12(G,J)48,USM12(G,J)48,SM12(G,J)48A,USM12(G,J)48A

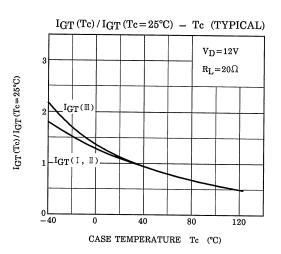






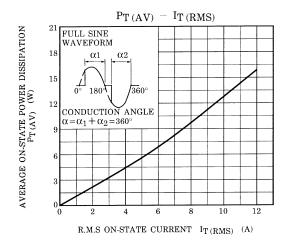


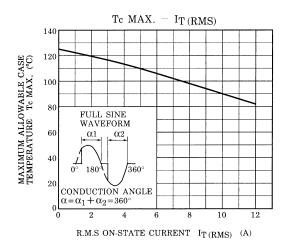


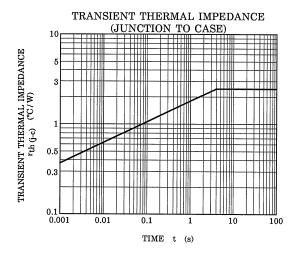


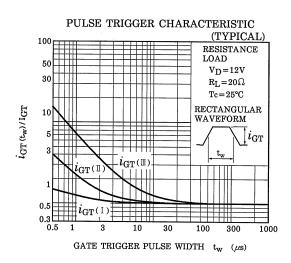
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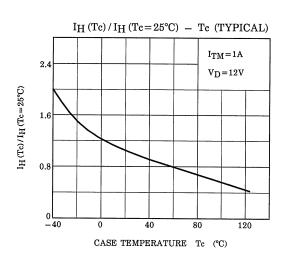
# **TOSHIBA** SM12(G,J)48,USM12(G,J)48,SM12(G,J)48A,USM12(G,J)48A











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