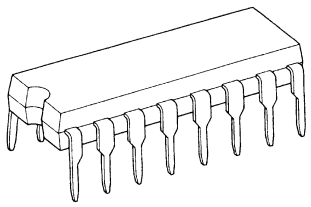
TOSHIBA Digital Integrated Circuit Silicon Monolithic

TC9216PG,TC9217PG,TC9217FG

High Speed PLL for DTS

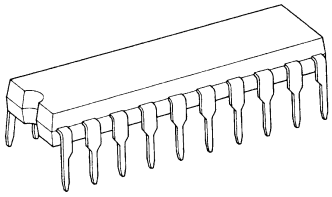
TC9216PG, TC9217PG, TC9217FG are a high speed PLL-LSI with built-in 2 modulus prescaler. Each function is controlled through 3 serial bus lines and high performance digital tuning system can be constituted.

TC9216PG



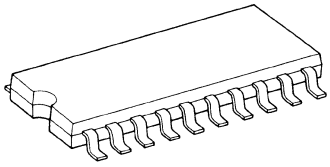
DIP16-P-300-2.54A

TC9217PG



DIP20-P-300-2.54A

TC9217FG



SOP20-P-300-1.27

Weight
DIP16-P-300-2.54A: 0.1 g (typ.)
DIP20-P-300-2.54A: 1.4 g (typ.)
SOP20-P-300-1.27: 0.48 g (typ.)

Features

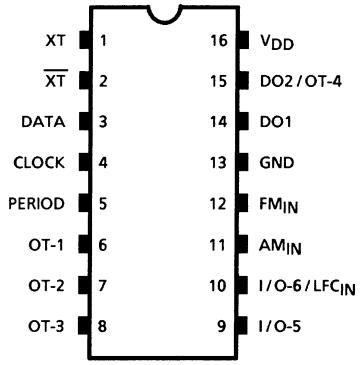
- Suitable for DTS of Hi-Fi tuner and car stereo
- Built-in prescaler, and it can operate 30~140 MHz (2 modulus type) at FM band and 0.5~40 MHz (2 modulus type or direct frequency dividing type) at AM band.
- Built-in 16 bit programmable counter, two parallel outputs phase comparator, crystal oscillator and reference counter.
- Crystal resonator can be used 4.5 MHz or 7.2 MHz.
- 15 kinds of reference frequency can be selected.
  (when crystal is used 4.5 MHz) (ref = 0.5 k, 1 k, 2.5 k, 3 k, 3.125 k, 3.90625 k, 5 k, 6.25 k, 7.8125 k, 9 k, 10 k, 12.5 k, 25 k, 50 k, 100 kHz)
- Frequency measurement (HFC_{IN}, LFC_{IN}) of intermediate frequency etc. and periodic measurement (SC_{IN}) of low frequency pilot signal etc. are possible by built-in 16 bit universal type frequency counter.

  (Note 1: TC9216PG does not have periodic measurement function.)

- Built-in abundant general purpose input/output terminal and usable for control radio circuit part.
- All of function controls are performed through 3 serial bus lines.
- Operating voltage range: V_{DD} = 5.0 0.5 V, and it is CMOS structure.
- Package is DIP-16 pin (TC9216PG) and DIP-20 pin (TC9217PG) and SOP-20 pin (TC9217FG).

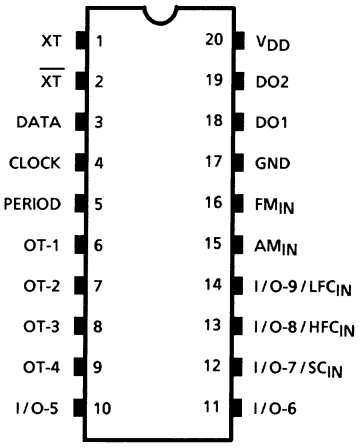
Pin Assignment (top view)

TC9216PG



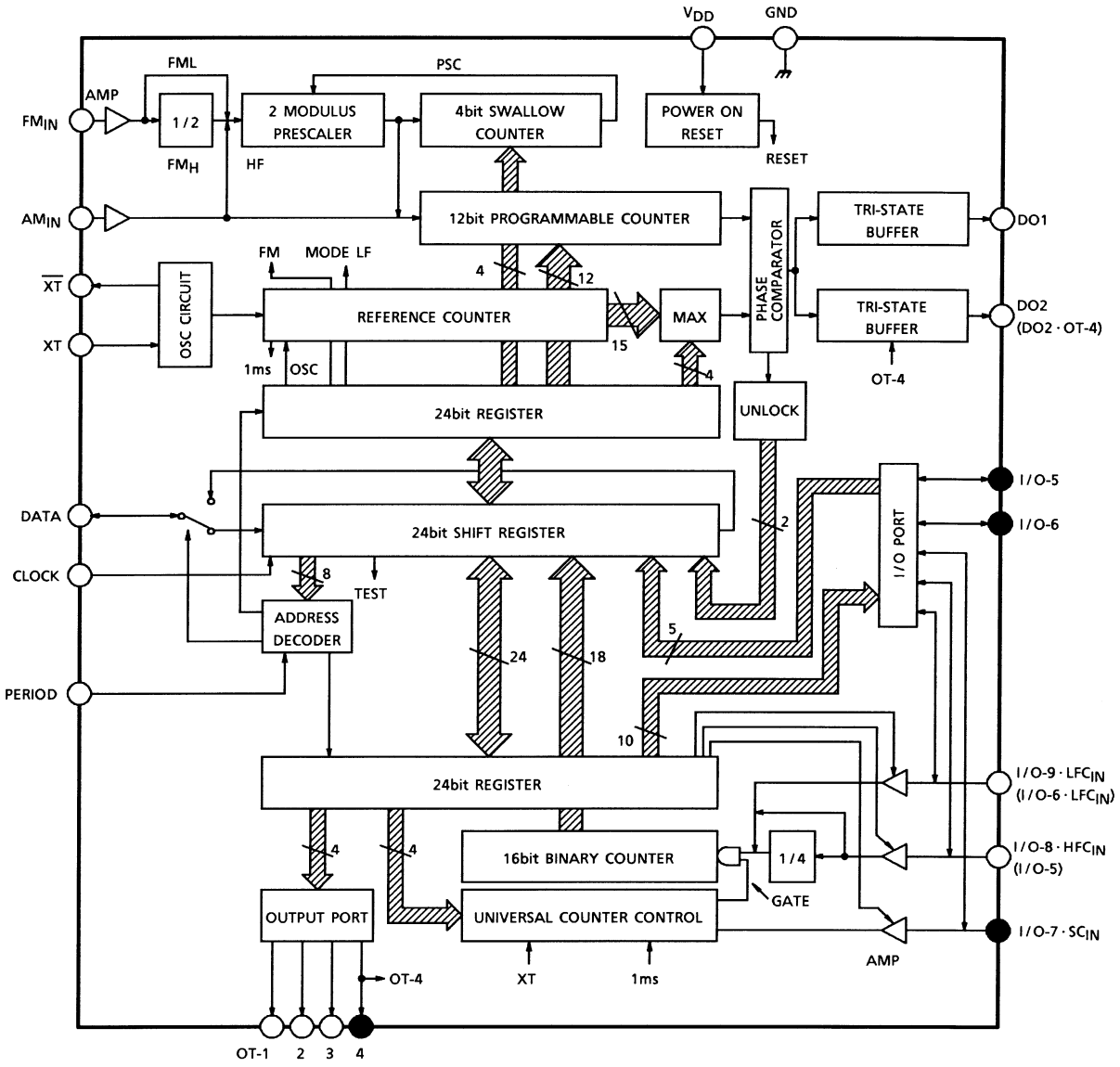
DIP-16 pin

TC9217PG, TC9217FG



DIP-20 pin, SOP-20 pin

Block Diagram

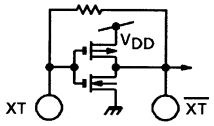
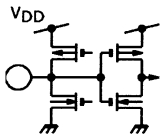
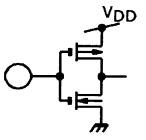
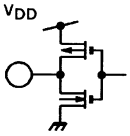
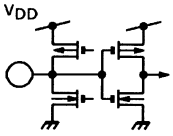
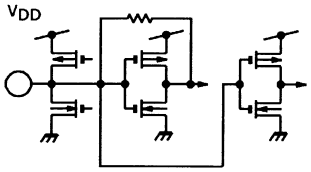
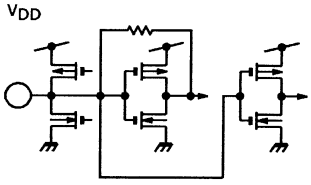


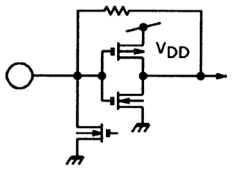
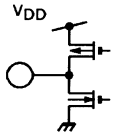
Note 2: ● Mark terminals are not existence in TC9216PG.

Terminal name of TC9216PG is shown in parentheses.

Others are common terminals.

Pin Function

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
1	XT	Crystal Oscillator Terminal	Crystal resonator of 7.2 MHz or 4.5 MHz shall be connected to this terminal to generate reference frequency and internal clock.	
2	$\overline{XT}$			
3	DATA	Serial Data Input/Output	Serial I/O port. Serial data transfer is performed between controller and these terminals to control universal counter and I/O port, and sets frequency dividing numbers and frequency dividing mode.	 DATA  CLOCK, PERIOD
4	CLOCK	Clock Signal Input		
5	PERIOD	Period Signal Input		
6	OT-1	General Purpose Output Port	These terminals are CMOS structure and used as output of control signal etc. They are set to “L” level at power “ON”. (OT-4 of TC9216PG can be used by switching DO2.)	
7	OT-2			
8	OT-3			
9 (—)	OT-4			
10 (9)	I/O-5	General Purpose I/O Port	These terminals are CMOS structure and can be used freely as input or output. It becomes input port at power “ON”. (Exclusive terminal of I/O port is only I/O-5 in TC9216PG.)	
11 (—)	I/O-6			
12 (—)	I/O-7・SC_{IN}	General Purpose I/O Port/Universal Counter Periodic Measurement Input	This terminal is general purpose I/O port. It can be also used as signal input terminal which performs periodic measurement of low frequency signal by program control. Note: It is set input mode of I/O port at power “ON”.	
13 (—)	I/O-8・HFC_{IN}	General Purpose I/O port/Universal Counter Frequency Measurement Input	These terminals are general purpose I/O ports. They can be also used as input terminals for frequency measurement of universal counter by program control. Frequency measurement is available for intermediate frequency measurement etc. It is with built-in amp. and can operate small amplitude signal with capacitor coupling. (TC9216PG does not have HFC_{IN} input.) Note: It is set input mode of I/O port at power “ON”.	
14 (10)	I/O-9・LFC_{IN} (I/O-6・LFC_{IN})			

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
15 (11)	AM_{IN}	Programmable Counter Input	The local oscillator signal of each FM/AM band is input to these terminals. It is with built-in amp. and can operate small amplitude signal with capacitor coupling.	
16 (12)	FM_{IN}			
18 (14)	DO1	Phase Comparator Output (general purpose output port)	These terminals are tristate outputs of phase comparator. DO1 and DO2 are parallel output. (DO2 of TC9216PG can be also used as general purpose output port by program control.)	
19 (15)	DO2 (DO2・OT-4)			
17 (13)	GND	Power Supply Terminal	Power supply voltage of 5.0 V ± 10% is applied to this terminal.	—
20 (16)	V_{DD}			

Note 3: No.1~8 pins are common terminals of TC9216PG, TC9217PG, TC9217FG.

Note 4: Terminal name and number of TC9216PG are shown in parentheses.

Operating Description

Serial I/O Port

Each function is controlled by the data setting to a pair of 24 bit registers, total of 48 bits. Each data of these registers is exchanged with controller side by 3 terminals of DATA, CLOCK and PERIOD through serial port.

Address 8 bits and data 24 bits, total of 32 bits, are transferred in serial at the same time.

Since all functions are controlled in the unit of register, so here explanations of address 8 bits and each register function are described chiefly. These registers are constituted in unit of 24 bits and selected by address of 8 bits. Address assignment table of each register is shown as the allocation of register in next page.

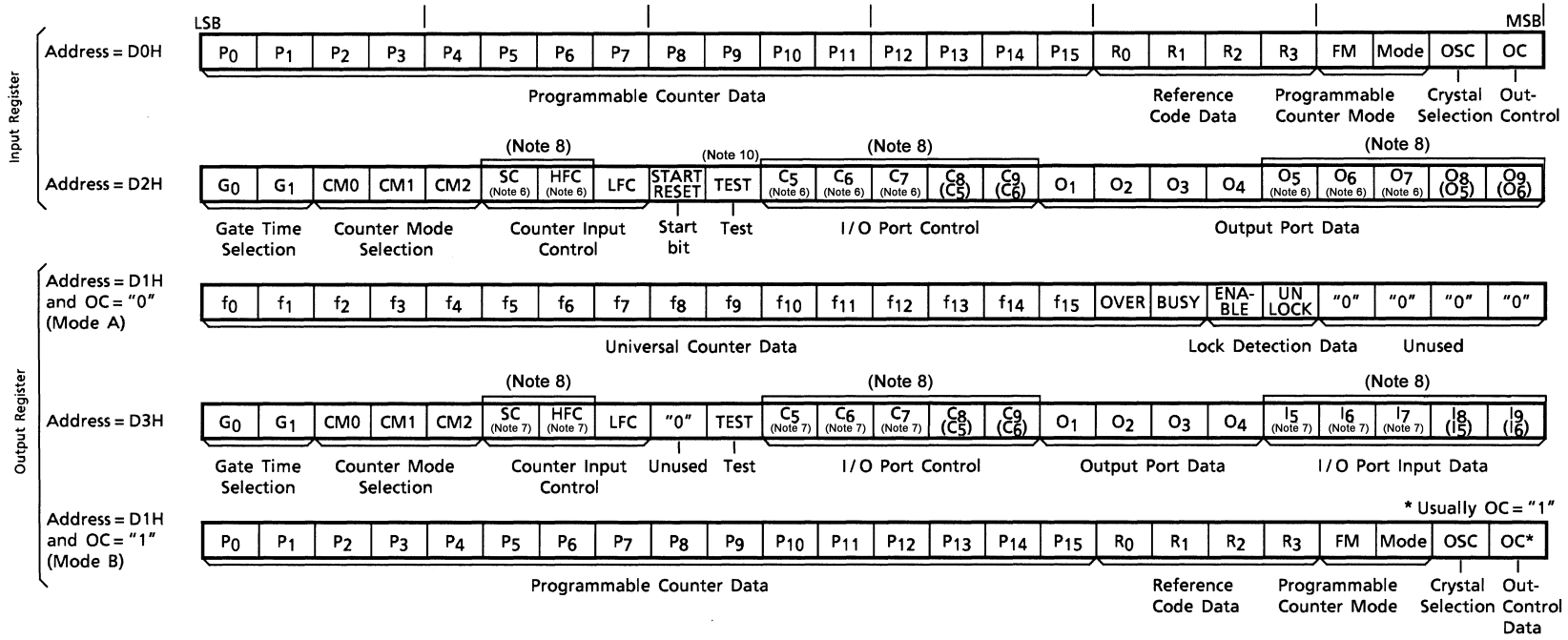
Register	Address	Constitution of 24 Bit	Number of Bit
Input Register-1	D0H	Setting of PLL frequency dividing number.	16
		Selection of reference frequency.	4
		Setting of PLL input and operation mode.	2
		Selection of crystal oscillation frequency.	1
		Out-control OC.	1
			(total of 24)
Input Register-2	D2H	Control of universal counter (control of PLL lock detection bit is included.)	9
		Test bit	1
		I/O port control	5
		Output data	9
			(total of 24)
Output Register	D1H	Data of Register-1	24
	(OC = 1)	(mode B)	(total of 24)
	D1H (OC = 0)	Count data of universal counter	18
		PLL lock detection data	2
		Unused	4
		(mode A)	(total of 24)
Output Register	D3H	Data of Register-2	19
		Input data	5
			(total of 24)

Input data is latched to register-1 or -2 at the fall timing of PERIOD signal and each function is operated.

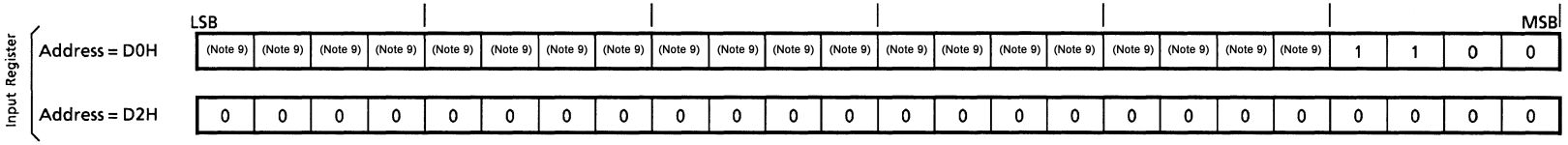
Each output data is latched to output register in parallel at the fall timing of the 9th of CLOCK signal and output from DATA terminal serially. Serial data of DATA, CLOCK and PERIOD is synchronized with crystal oscillation clock and taken into the internal circuit of LSI. By this reason if crystal oscillation is stopped, serial data can not be input.

Note 5: When power is turned on, some internal circuits have undefined states to set internal circuit states, execute a dummy data transfer at least once before performing regular data transfer.

Allocation of Register



At POWER ON RESET operation, each data of input register is set as shown below.



Note 6: Don't care in TC9216PG.

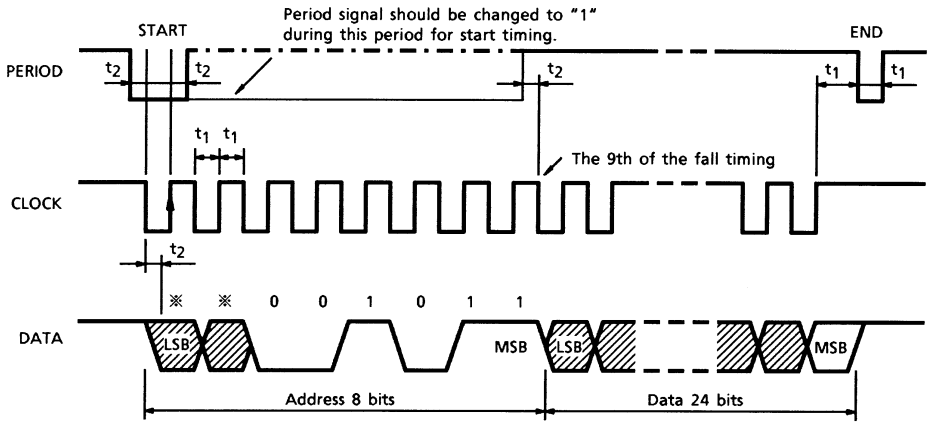
Note 7: Data is set to "0" in TC9216PG.

Note 8: Bit name of TC9216PG is shown in parentheses.

Note 9: Don't care

Note 10: TEST bit is set to "0".

Serial Transmission Format



min

$t_1 \geqq 1.0\ \mu s$

$t_2 \geqq 0.3\ \mu s$

- Serial transmission format consists of address 8 bits and data 24 bits as mentioned above. Address of D0H~D3H is used in this LSI.

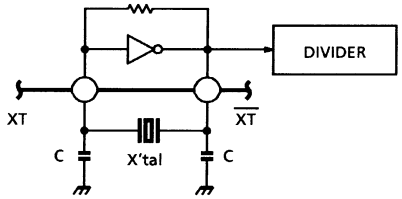
Crystal Resonator Connecting Terminal (XT, $\overline{XT}$)

It can generate the clock signal necessary for inside operation of LSI by connecting crystal resonator and capacitors as shown in Figure 1.

Crystal resonator can be selected either 4.5 MHz or 7.2 MHz.

Serial Data "OSC" bit should be set to "0" at 4.5 MHz selection.

Serial Data "OSC" bit should be set to "1" at 7.2 MHz selection.



C = 30 pF typ.

Figure 1

Programmable Counter

Programmable counter part consists of 1/2 prescaler, 2 modulus prescaler and 4 bits + 12 bits programmable binary counter.

1. Setting of Programmable Counter

16 bits data of frequency dividing number and 2 bits of frequency dividing mode is set to programmable counter.

(1) Setting of frequency dividing mode

Input terminal and frequency dividing mode (pulse swallow mode or direct frequency dividing mode) shall be selected by FM and MODE bit.

Since 4 kinds of modes are prepared as shown below, so it shall be selected according to the frequency band used.

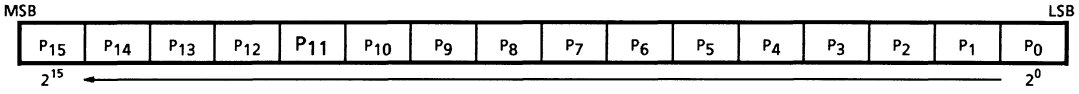
Mode	Mode	FM	Frequency Dividing Mode	Example of Receiving Band	Input Frequency Range	Input Terminal	Frequency Dividing Number
LF	0	0	Direct frequency dividing mode	LW, MW, SW_L	0.5~10 MHz	AM_{IN}	n
HF	1	0	Pulse swallow mode	SW_H	2~40 MHz	AM_{IN}	n
FM_L	0	1		FM	30~140 MHz	FM_{IN}	n
FM_H	1	1	1/2 + pulse swallow mode	FM	50~140 MHz	FM_{IN}	2·n

Note 11: n represents programmed numeral value.

(2) Setting of frequency dividing number

Frequency dividing number of programmable counter is set to P0~P15 bits in binary.

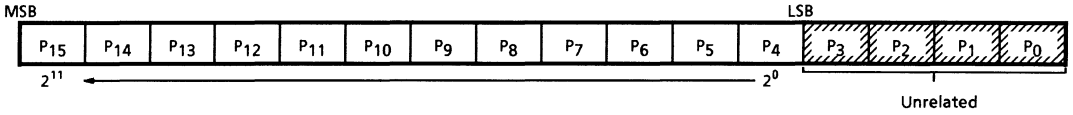
- Pulse swallow mode (16 bits)



Setting range of frequency dividing number (pulse swallow mode): n = 210H~FFFFH (528~65535)

Note 12: Actual dividing number becomes the double of programmed numeral value in 1/2 + pulse swallow mode.

- Direct frequency dividing mode (12 bits)

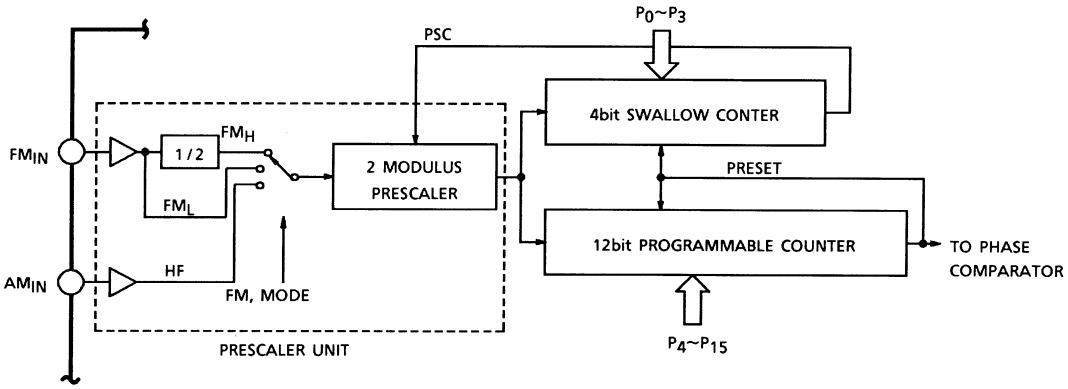


Setting range of frequency dividing number (direct frequency dividing mode): n = 10H~FFFH (16~4095)

Data of P0~P3 is unrelated and P4 bit becomes LSB at direct frequency dividing mode.

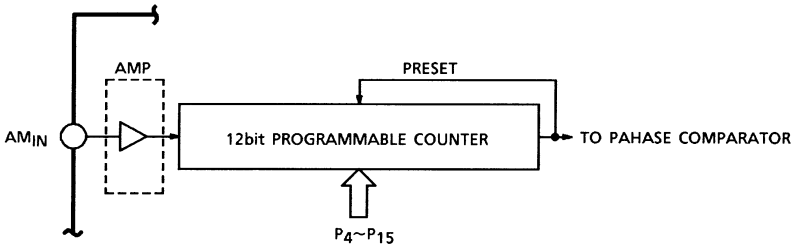
2. Circuit Construction of Prescaler and Programmable Counter

(1) Circuit construction at pulse swallow mode



It consists of 2 modulus prescaler, 4 bit swallow counter and 12 bit programmable counter. 1/2 prescaler is added to the front stage of 2 modulus prescaler at FM_{IN} (FM_H mode).

(2) Circuit construction at direct frequency dividing mode



Prescaler unit becomes unused at direct frequency dividing mode and 12 bit programmable counter is only used.

(3) Each input of FM_{IN}/AM_{IN} has built-in amp. and can operate small amplitude signal with capacitor coupling.

Reference Divider (Frequency divider for reference frequency)

Reference divider unit consists of crystal oscillator and counter. Crystal resonator can be selected either 4.5 MHz or 7.2 MHz and 15 kinds (max) of reference frequencies are generated.

1. Setting of Reference Frequency

Reference frequency is setting by R0~R3 bits.

R_3	R_2	R_1	R_0	Reference Frequency	R_3	R_2	R_1	R_0	Reference Frequency
0	0	0	0	0.5 kHz	1	0	0	0	* 7.8125 kHz
0	0	0	1	1 kHz	1	0	0	1	9 kHz
0	0	1	0	2.5 kHz	1	0	1	0	10 kHz
0	0	1	1	3 kHz	1	0	1	1	12.5 kHz
0	1	0	0	3.125 kHz	1	1	0	0	25 kHz
0	1	0	1	* 3.90625 kHz	1	1	0	1	50 kHz
0	1	1	0	5 kHz	1	1	1	0	100 kHz
0	1	1	1	6.25 kHz	1	1	1	1	—

* Mark frequencies are only available at 4.5 MHz crystal resonator used.

Crystal oscillation frequency is selected by crystal select bit (OSC).

OSC = "0"..... 4.5 MHz

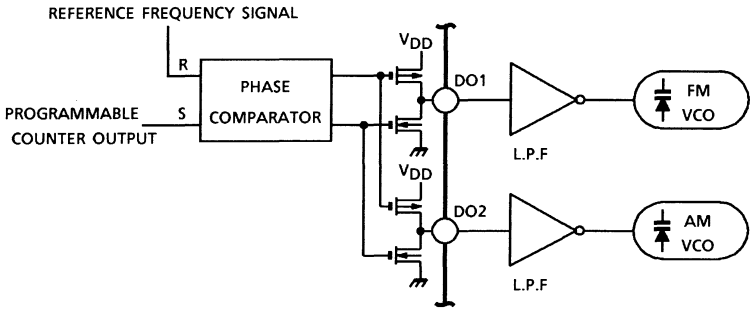
OSC = "1"..... 7.2 MHz

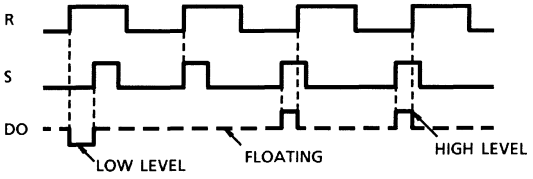
Note 13: OSC bit is set "0" (4.5 MHz) when power supply is "ON".

Phase Comparator

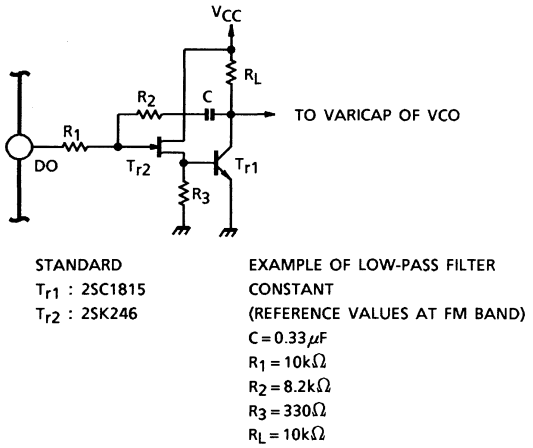
Phase comparator compares reference frequency signal supplied from reference frequency divider and programmable counter frequency dividing output. It outputs the observational error and controls VCO through low-pass filter to make frequency and phase difference between these two signals accord.

Filter constant can be designed suitably for every band of FM/AM because Tri-state buffer DO1 and DO2 terminals are output from phase comparator in parallel.





DO Output Timing Chart



Example of Active Low-Pass Filter Circuit

DO output timing chart and an example of active low-pass filter circuit through the darlington connection of FET and transistor are shown in the above diagram.

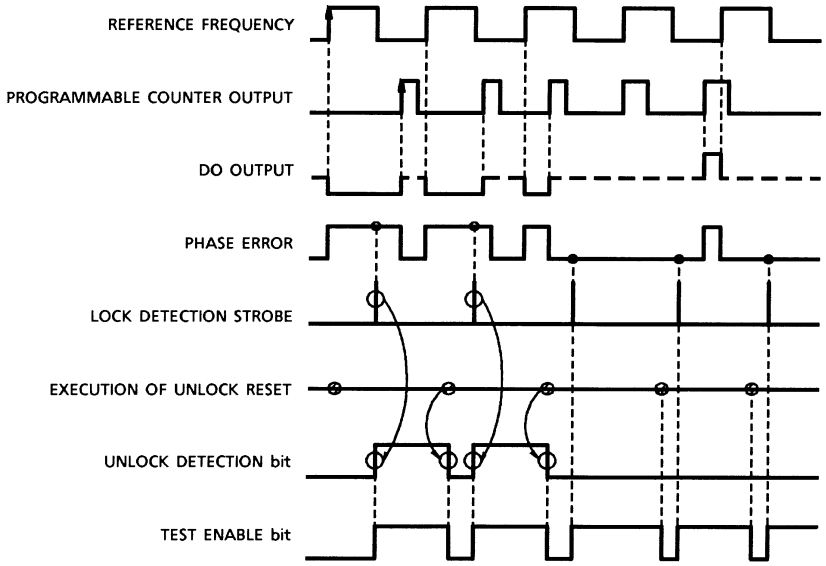
Besides, the filter circuit shown in the above diagram is one of example for reference and so, an actual circuit shall be examined and designed according to the receiving band constitution of the system and required characteristics.

Note 14: DO2 terminal of TC9216PG can be switched and used as OT-4 terminal by program control.

Unlock Detection Bit

This bit is to detect the lock condition of PLL system. Phase error pulses are output to unlock F/F from phase comparator at timing of reference frequency period in the PLL unlocked state, that is, when reference frequency does not accord with programmable counter frequency dividing output (unlock condition). The unlock F/F is set by these pulses. And whenever START/RESET bit (unlock reset bit) of register-2 is set to "1", unlock F/F is reset. Lock condition can be detected by access of unlock detection bit after resetting the unlock F/F. It is necessary to access the unlock detection bit (UNLOCK) after having a time more than reference period after resetting the unlock F/F because error pulses are input at reference period. If this time was shorter, the correct lock condition can not be detected. Therefore, the test enable F/F is provided.

This F/F is reset whenever unlock reset bit is set to "1", and it is set to "1" at the unlock detection timing. That is, the unlock condition can be detected correctly when this test enable bit (ENABLE) is set to "1".



Universal Frequency Counter

Universal frequency counter is used as frequency calculation of FM/AM band intermediate frequency (IF) for auto stop signal detection at auto search tuning, etc.

Two types of measurement mode are available by use of universal counter. One is the frequency measurement mode (HFC_{IN}, LFC_{IN} input) that counts the input pulses enter the universal counter in a constant time (gate-time), and the other is the period measurement mode (SC_{IN} input) that counts the reference clock pulses (period measurement pulses) enter the universal counter in a period of the input pulses. Measurement mode is selected according to the frequency measured. but in TC9216PG SC_{IN}, HFC_{IN} inputs are not provided and period measurement mode is not available. Besides, each terminal can be also used as I/O port.

1. Universal Counter Control Bit

(1) G_0, G_1 bit ..... Gate-time of universal counter is selected by these bits.

G_1	G_2	Gate-Time	Period Measurement Pulse
0	0	1 ms	50 k (20 μs)
0	1	4 ms	150 k (6.6 μs)
1	0	16 ms	900 k (1.1 μs)
1	1	Manual (Note 15)	Crystal oscillator frequency

Note 15: Gate-time can be set freely in the manual mode by using time base of controller. (the gate-time less than 2 cycles of serial transmission format can not be set because it is controlled by START bit)

(2) START bit ..... Measurement starts whenever START bit is set to "1".

Note 16: In manual mode the count starts when START bit is set to "1" and stops when START is set to "0".

(3) CM0, CM1, CM2 bit..... Each measurement mode of universal counter and input terminal are selected by these bits. Besides, it also controls the switching of DO2/OT-4 function in TC9216PG.

CM2	CM1	CM0	TC9216PG			TC9217PG・TC9217FG	
			Counter Input Terminal	Counter Mode	DO2・OT-4 Terminal	Counter Input Terminal	Counter Mode
0	0	0	LFC_{IN}	LFC Mode	DO2	LFC_{IN}	LFC Mode
0	0	1	LFC_{IN}	LFC Mode	DO2	LFC_{IN}	LFC Mode
0	1	0	(Note 17)	(Note 17)	(Note 17)	HFC_{IN}	MFC Mode
0	1	1	(Note 17)	(Note 17)	(Note 17)	HFC_{IN}	HFC Mode
1	0	0	LFC_{IN}	LFC Mode	OT-4	(Note 17)	(Note 17)
1	0	1	LFC_{IN}	LFC Mode	OT-4	(Note 17)	(Note 17)
1	1	0	(Note 17)	(Note 17)	(Note 17)	(Note 17)	(Note 17)
1	1	1	(Note 17)	(Note 17)	(Note 17)	SC_{IN}	SC Mode

Note 17: Don't use

	Mode	Input Frequency Range
LFC Mode	Frequency Measurement	F_{IN} = 0.3~15 MHz
MFC Mode		F_{IN} = 5~20 MHz
HFC Mode		F_{IN} = 5~60 MHz
SC Mode	Period Measurement	F_{IN} = ~100 kHz

Note 18: 1/4-prescaler is added to the front stage of the universal counter (16 bits binary counter) in HFC mode. Therefore, signal input to HFC_{IN} is divided by 4 in the prescaler and transmitted to the universal counter.

(4) LFC, HFC, SC bit ..... Input terminals of universal counter are controlled by these bits. Switching between universal counter input and I/O port are controlled by these bits.

	Data	TC9217PG·TC9217FG	TC9216PG
LFC	0	I/O Port (I/O-9)	I/O Port (I/O-6)
	1	Frequency Counter Input (LFC_{IN})	Frequency Counter Input (LFC_{IN})
HFC	0	I/O Port (I/O-8)	Unprepared
	1	Frequency Counter Input (HFC_{IN})	
SC	0	I/O Port (I/O-7)	
	1	Period Measurement Input (SC_{IN})	

2. Universal Counter Data Output Register

(1) Universal counter calculation data bits (f_0~f_{15})

The calculated result in the universal counter can be read out from output registers of f_0~f_{15} in binary. In this case, OC bit of input register-1 should be set to "0".

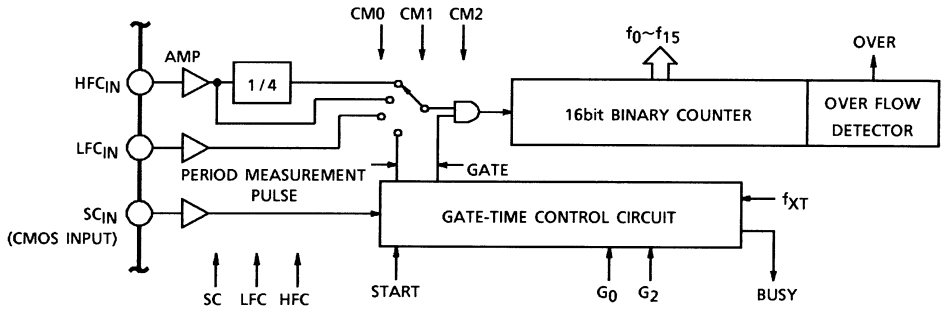
(2) Universal counter operational detection bit

- OVER.....niversal counter over flow bit
  - "1" ..... Universal counter over flow condition
  - "0" ..... Universal counter data normal condition
- BUSY.....niversal counter operation monitor bit
  - "1" ..... Under universal counter calculation
  - "0" ..... Universal counter calculation end

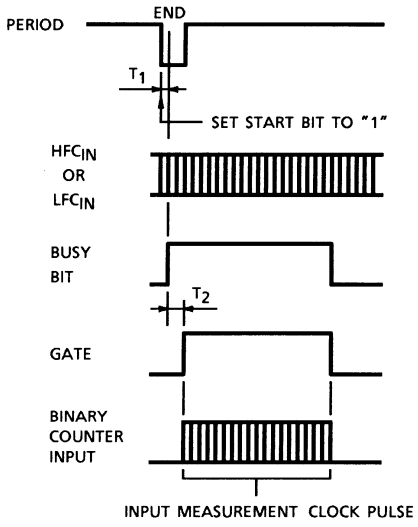
Note 19: Refer to the contents of universal counter calculation data bits (f_0~f_{15}) after confirmation of BUSY bit = "0" (END of calculation) and OVER bit = "0" (data normal condtion) at the use of universal counter.

3. Circuit Construction of Universal Counter

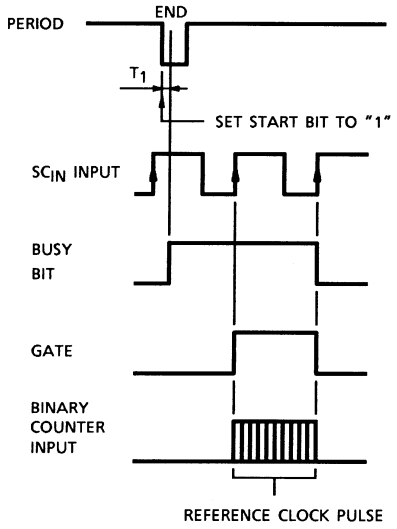
Universal counter unit consists of input amp., gate-time control circuit and 16 bit binary counter.



4. Measurement Timing of Universal Counter



Frequency Measurement Timing Chart



Period Measurement Timing Chart

$0 < T_1 \leqq 0.25$ (μs), $0 < T_2 \leqq 1$ (ms)

Note 20: HFC_{IN} and LFC_{IN} are with built-in amp. and can operate small amplitude signal with capacitor coupling.

Note 21 SC_{IN} signal should be used with logic level because its input is CMOS structure.

Note 22: Calculation at manual mode is started at rise timing of PERIOD signal end (START bit is set to “1”) and is also finished at the same timing (START bit is set to “0”).

General Purpose Input/Output Port

It has general purpose I/O port controlled through serial port.

Input/Output	TC9217PG・TC9217FG	TC9216PG	Input/Output Construction
Output Port	Exclusive: 4	Exclusive: 3, (max: 4)	CMOS
I/O Port	Exclusive: 2, (max: 5)	Exclusive: 1, (max: 2)	CMOS

1. General Purpose Output Port (OT-1~OT-4)

The data set to 01~04 bits of input register-2 is output in parallel from each exclusive output port OT-1~OT-4 terminal. TC9216PG does not have OT-4 exclusive output port but DO2 terminal can be switched and used as OT-4 output port by that CM1 bit is set to "0" and CM2 bit is set to "1" in input register-2 respectively.

2. General Purpose I/O Port (I/O-5~I/O-9)

Input or output mode of I/O port is set according to the contents of C_5~C_9 bits in input register-2.

Set each bit of C_5~C_9 to "0" at input mode setting.

The data input from I/O-5~ I/O-9 terminals in parallel can be read out from DATA terminal as serial data of I_5~I_9.

Input data is latched to the internal register at the fall timing of the 9th of serial clock.

Set each bit of C_5~C_9 to "1" at output mode setting. The data set to O_5~O_9 bits of input register-2 is output from I/O port of I/O-5~I/O-9 terminal in parallel respectively.

Note 23: Since I/O-7~ I/O-9 terminal of TC9217PG and I/O-6 of TC9216PG are also combined with input terminal of universal counter, each bit of SC, HFC and LFC of input register-2 shall be set to "0" at the use of I/O port.

Note 24: I/O control port and output port are set to "0" at power "ON".

(General purpose I/O port is set to input mode. General purpose I/O port terminals combined with universal counter inputs are set to input mode of I/O port and output condition of general purpose output port is set to "L" level.)

Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{DD}	−0.3~6.0	V
Input voltage	V_{IN}	−0.3~V_{DD} + 0.3	V
Power dissipation	P_D	300	mW
Operating temperature	T_{opr}	−40~85	°C
Storage temperature	T_{stg}	−65~150	°C

Electrical Characteristics (unless otherwise specified, Ta = –40~85°C, V_{DD} = 4.5~5.5 V)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Operating power supply voltage	V_{DD}	—	—	4.5	5.0	5.5	V
Operating power supply current	I_{DD}	—	V_{DD} = 5.0 V, X_T = 7.2 MHz, FM_{IN} = 140 MHz	—	15	25	mA

Operating frequency range

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Crystal oscillation frequency	f_{XT}	—	Connect crystal resonator to XT- $\overline{XT}$ terminal	4.0	~	8.0	MHz
FM_{IN} (FM_H, FM_L)	f_{FM}	—	FM_H, FM_L mode, V_{IN} = 0.3 V_{p-p}	50	~	140	MHz
FM_{IN} (FM_L)	f_{FML}	—	FM_L mode, V_{IN} = 0.4 V_{p-p}	30	~	140	MHz
AM_{IN} (HF)	f_{HF}	—	HF mode V_{IN} = 0.3 V_{p-p}	2	~	40	MHz
AM_{IN} (LF)	f_{LF}	—	LF mode V_{IN} = 0.3 V_{p-p}	0.5	~	10	MHz
LFC_{IN} (LFC)	f_{LFC}	—	LFC mode V_{IN} = 0.3 V_{p-p}	0.3	~	15	MHz
HFC_{IN} (MFC)	f_{MFC}	—	MFC mode V_{IN} = 0.3 V_{p-p}	5	~	20	MHz
HFCIN (HFC)	f_{HFC}	—	HFC mode V_{IN} = 0.3 V_{p-p}	5	~	60	MHz
SC_{IN}	f_{SC}	—	V_{IH} = V_{DD} × 0.7, V_{IL} = V_{DD} × 0.3, Square wave input	—	~	100	kHz

Operating input amplitude range

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
FM_{IN} (FM_H, FM_L)	V_{FM}	—	FM_H, FM_L mode f_{IN} = 50~140 MHz	0.3	~	V_{DD} − 0.5	V_{p-p}
FM_{IN} (FM_L)	V_{FML}	—	FM_L mode f_{IN} = 30~140 MHz	0.4	~	V_{DD} − 0.5	V_{p-p}
AM_{IN} (HF)	V_{HF}	—	HF mode f_{IN} = 2~40 MHz	0.3	~	V_{DD} − 0.5	V_{p-p}
AMIN (LF)	V_{LF}	—	LF mode f_{IN} = 0.5~10 MHz	0.3	~	V_{DD} − 0.5	V_{p-p}
LFC_{IN} (LFC)	V_{LFC}	—	LFC mode f_{IN} = 0.3~15 MHz	0.3	~	V_{DD} − 0.5	V_{p-p}
HFC_{IN} (MFC)	V_{MFC}	—	MFC mode f_{IN} = 5~20 MHz	0.3	~	V_{DD} − 0.5	V_{p-p}
HFC_{IN} (HFC)	V_{HFC}	—	HFC mode f_{IN} = 5~60 MHz	0.3	~	V_{DD} − 0.5	V_{p-p}

OT-1~OT-4

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	$I_{OH\ 1}$	—	V_{OH} = 4.0 V	−2.0	−4.0	—	mA
	"L" level	$I_{OL\ 1}$	—	V_{OL} = 1.0 V	2.0	4.0	—	

DATA, CLOCK, PERIOD, I/O-5~I/O-9

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input voltage	"H" level	V_{IH}	—	—	V_{DD} × 0.7	~	V_{DD}	V
	"L" level	V_{IL}	—	—	0	~	V_{DD} × 0.3	
Input current	"H" level	I_{IH}	—	V_{IH} = 5 V	—	—	2.0	μA
	"L" level	I_{IL}	—	V_{IL} = 0 V	—	—	−2.0	
Output current	"H" level	$I_{OH\ 4}$	—	V_{OH} = 4.0 V, Except CLOCK, PERIOD	−2.0	−4.0	—	mA
	"L" level	$I_{OL\ 4}$	—	V_{OL} = 1.0 V, Except CLOCK, PERIOD	2.0	4.0	—	

DO1, DO2

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	$I_{OH\ 3}$	—	V_{OH} = 4.0 V	−2.0	−4.0	—	mA
	"L" level	$I_{OL\ 3}$	—	V_{OL} = 1.0 V	2.0	4.0	—	
DO tri-state leakage current		I_{TL}	—	V_{TLH} = 5 V, V_{TLL} = 0 V	—	—	±1	μA

$\overline{XT}$

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	$I_{OH\ 2}$	—	V_{OH} = 4.0 V	−0.1	−0.3	—	mA
	"L" level	$I_{OL\ 2}$	—	V_{OL} = 1.0 V	0.1	0.3	—	

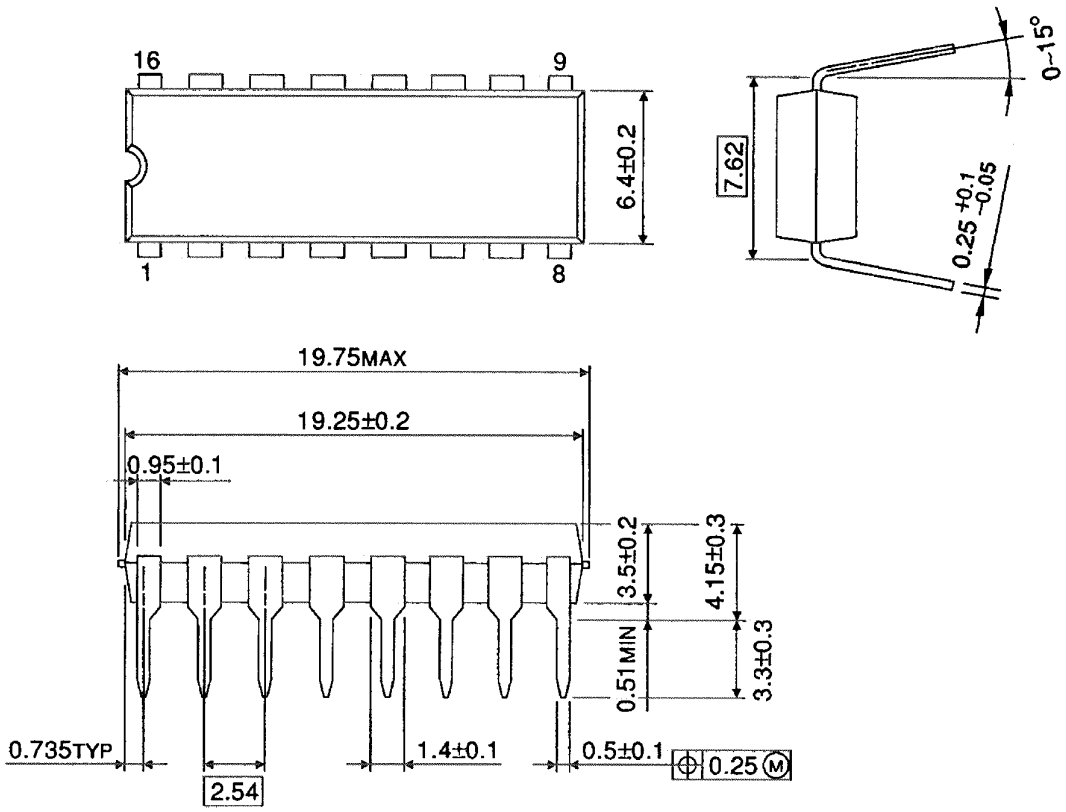
Input feedback resistance

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input feedback resistance	R_{f1}	—	FM_{IN}, AM_{IN}, LFC_{IN}, HFC_{IN}, SC_{IN}	250	500	1000	Ω
	R_{f2}	—	XT- $\overline{XT}$	250	500	1250	

Note 25: Ta = 25°C

Package Dimensions

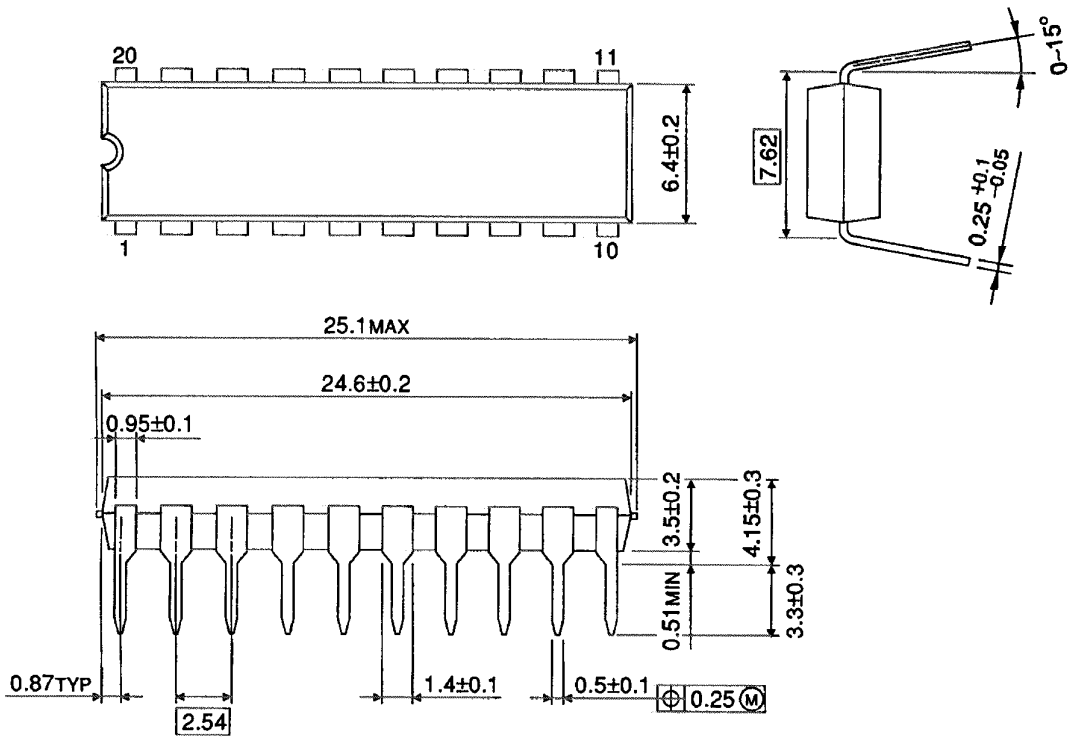
DIP16-P-300-2.54A Unit : mm



Weight: 1.0 g (typ.)

Package Dimensions

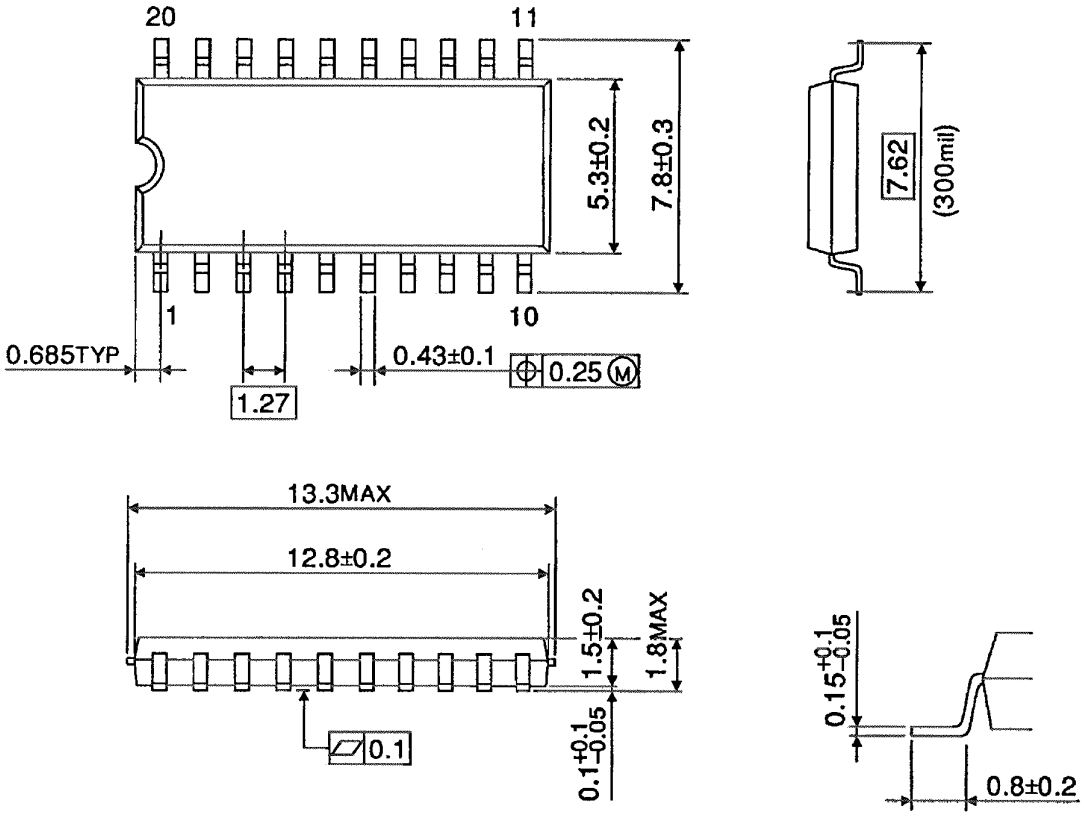
DIP20-P-300-2.54A Unit : mm



Weight: 1.4 g (typ.)

Package Dimensions

SOP20-P-300-1.27 Unit : mm



Weight: 0.48 g (typ.)

About solderability, following conditions were confirmed

- Solderability

  (1) Use of Sn-63Pb solder Bath
  - solder bath temperature = 230°C
  - dipping time = 5 seconds
  - the number of times = once
  - use of R-type flux

  (2) Use of Sn-3.0Ag-0.5Cu solder Bath
  - solder bath temperature = 245°C
  - dipping time = 5 seconds
  - the number of times = once
  - use of R-type flux

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