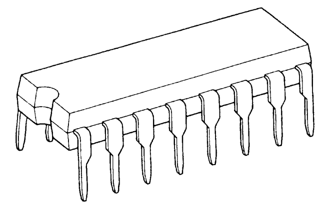
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC9223PG,TC9223FG

PLL Frequency Synthesizer LSI for Communication Use

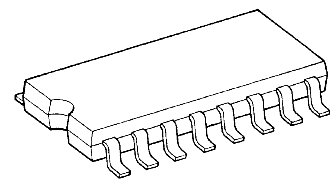
TC9223PG, TC9223FG are developed as PLL frequency synthesizer LSI for communication use and has the following features.

TC9223PG



DIP16-P-300-2.54A

TC9223FG



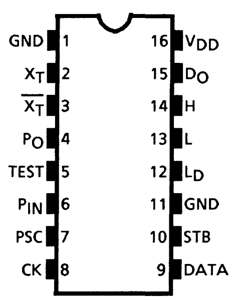
SOP16-P-300-1.27

Weight
DIP16-P-300-2.54A: 1.00 g (typ.)
SOP16-P-300-1.27: 0.16 g (typ.)

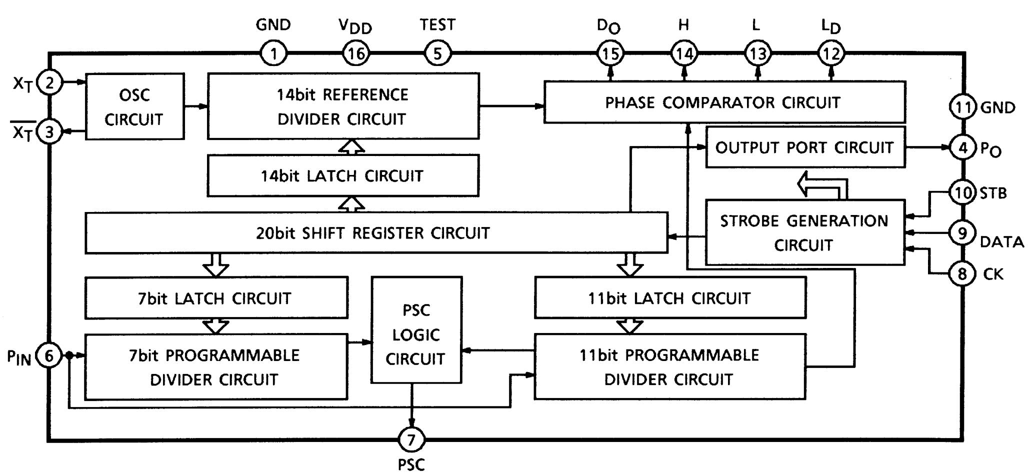
Features

- Can be used as PLL LSI in many communication equipment, e.g., personal radio, mobile radio telephone, CB radio and so on because of its system design for wide applications.
- With a built-in 14 bit reference frequency divider, capable of frequency division ranging from 5 to 16,383 divisions.
- Built-in 7 bit and 11 bit programmable dividers of pulse swallow type.
- Provided with 2 systems of phase comparator outputs.
- Provided with one general purpose output port.
- PSC (prescaler control) output can be switched according to input signal rising or falling timing by program.
- DIP16 pin and SOP16 pin packages.

Pin Assignment



Block Diagram



Pin Function

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
1	GND	Ground-1	Logic ground terminal.	—
2 3	X_T $\overline{X_T}$	Crystal oscillator terminal	Reference frequency crystal oscillator input and output.	Feedback resistor built in
4	P_O	General purpose output port	General purpose output port externally controllable by serial data.	CMOS output
5	TEST	Test terminal	Used normally at "L" level or Open state. Test mode operation at "H" level.	Pull-down resistor built in
6	P_{IN}	Programmable counter input	Programmable counter input terminal. Input an external prescaler output through a coupling capacitor.	Built in amps
7	PSC	Prescaler control	2 modulus prescaler frequency division control signal output. "H" level: P, "L" level: P + 1	CMOS output
8 9 10	CK DATA STB	Serial data input	Serial data input terminals to control this LSI externally. Schmitt trigger input.	Built in schmitt trigger circuit
11	GND	Ground-2	Ground terminal of phase comparator charge pump.	—
12	L_D	Lock detector	Outputs "H" level pulse when phase difference is detected by the phase comparator. Can be set compulsorily by data given externally.	CMOS output
13 14	L H	Phase comparator output	Phase comparator output terminals to connect external high voltage charge pump.	CMOS output N-ch open drain output
15	D_O	Phase comparator charge pump output	D_O is tri-state output.	—
16	V_{DD}	Power supply	+5 V power supply terminal.	—

Operation

1. Serial Data Input

Serial data can control 4 group functions separately. Data is always input from.
LSB and final 2 bits data selects the group.

- Group 1 ——— Reference divider frequency division ratio
- Group 2 ——— Programmable counter frequency division ratio
- Group 3 ——— PSC control
  - Phase comparator S, R inputs replace
- Group 4 ——— General purpose output ports
  - Lock detector compulsory set

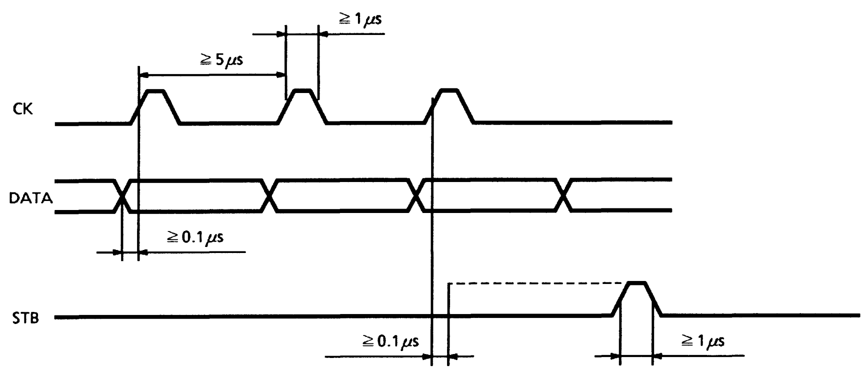
The serial data input circuit is composed of 3 lines of DATA, CK and STB. Data is taken in order into the internal shift register at the leading edge of CK.

By setting STB at "H" level after all data are input, data are transferred to the latch selected by the group code and this LSI is controlled.

Each of 3 serial data input terminals has a built-in Schmitt trigger circuit that prevent data error by noise, etc.

For details of data construction of each group, refer to the explanations of respective blocks.

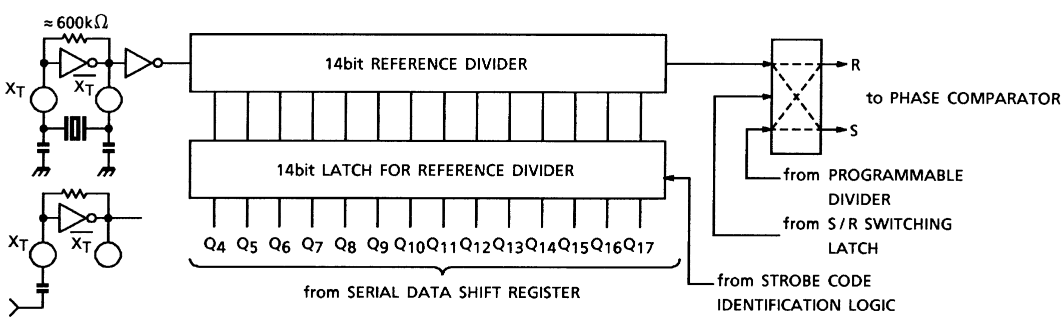
- Serial data transfer timing



Note 1: Set a time from the last CK rising to STB rising at 0.1 μs or above.

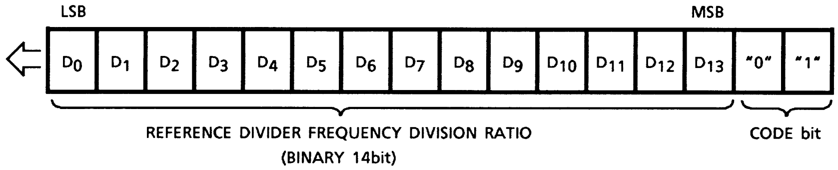
2. Reference Divider

This block generates PLL reference frequency and is composed of an amplifier for a crystal oscillator and 14 bit programmable divider.



- The programmable divider is composed of binary 14 bits and is capable frequency division from 5 to 16,383 divisions by serial data given externally.
  Therefore, a crystal needed to generate reference frequency is freely selectable and common use of the crystal for other purpose is also possible.

- Serial data to control reference divider block is of 16 bits as following construction.

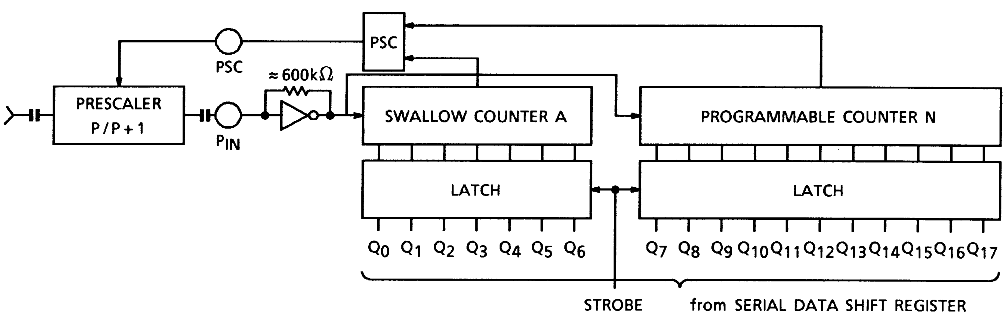


Note 2: D_0~D_{13} is binary code N of frequency division ratio intended.

$5 \leqq N \leqq 16,383$

3. Programmable Counter

Programmable counter circuit adopts swallow system to generate high frequency and is composed of 7 bits swallow counter, 11 bits programmable counter and prescaler control logic to switch frequency division ratio of 2 modulus prescaler connected externally.



- Total frequency division ratio is defined as below.

  Frequency division ratio $= (P + 1)\cdot A + P\cdot(N - A)$

  $= P\cdot N + A$

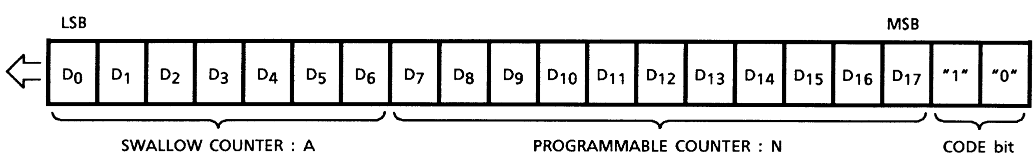
  Note 3: $N > A$

- Frequency division ratio of the external perscaler should be "P + 1" when PSC is "L" level and "P" when PSC is "H" level.

- Serial data

  Serial data which defines frequency division ratio of programmable counter is composed of 20 bits but changes according to "P" of external prescaler.

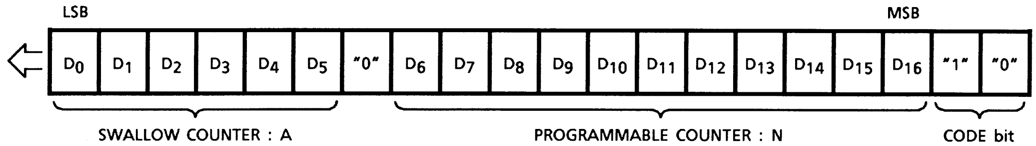
  (1) When used with an external prescaler of $P = 128$



Note 4: D_0~D_{17} is binary code D of frequency division ratio intended.

Generally $16,384 \leqq D \leqq 262,143$

(2) When used with an external prescaler of P = 64

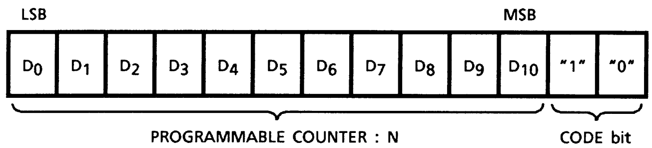


Note 5: D0~D16 is binary code D of frequency division ratio intended.

The 7th bit should be fixed at "L".

Generally 4,096 $\leqq$ D $\leqq$ 131,071

(3) When used as a normal programmable counter



Note 6: D_0~D_{10} is binary code D of frequency division ratio intended.

5 $\leqq$ D $\leqq$ 2,047

4. Inversion of S/R Input to PSC Control/Phase Comparator

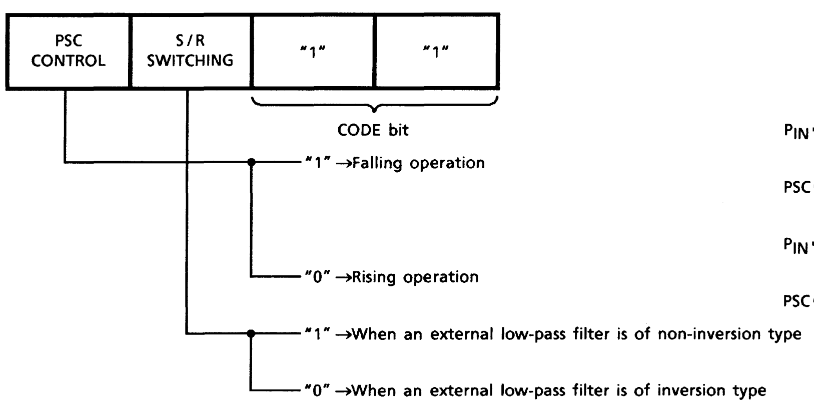
- PSC control

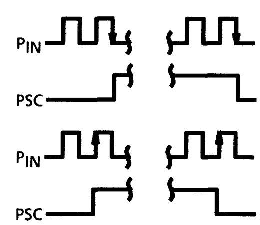
  "PSC" (prescaler) output is capable of switching operation according to rising or falling timing of "PIN" input signal.

- Inversion of S/R inputs to phase comparator

  S/R switching bit is a control latch for mutual replacement of reference divider output and programmable divider output when they are led to the phase comparator.

- Serial data





5. General Purpose Output Port/Lock Detector

- General purpose output port

  "PO" output port is available for many functions, e.g., transmitter/receiver switching signal, band switching signal, sensitivity switching and frequency band switching according to serial data.

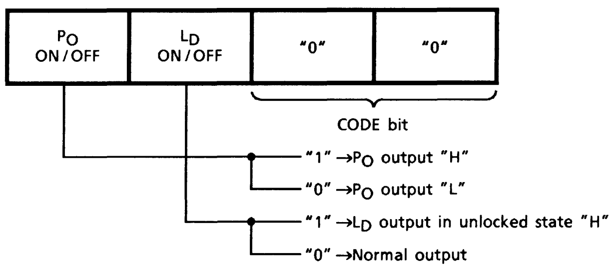
- Lock detector

  The lock detector output pulse signal for a phase difference time detected by the phase detector circuit.

  In addition, this lock detector output can be fixed in the unlocked state by force by serial data given externally.

  By fixing the lock detector in the unlocked state immediately before channel changing to stop transmission output and releasing the detector from the unlocked state at a definite time after the channel change, troubles at channel changing, e.g., by overshoot can be prevented.

- Serial data



Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{DD}	−0.3~7.0	V
Input voltage	V_{IN}	−0.3~V_{DD} + 0.3	V
Power dissipation	P_D	300	mW
Operating temperature	T_{opr}	−40~85	°C
Storage temperature	T_{stg}	−65~150	°C

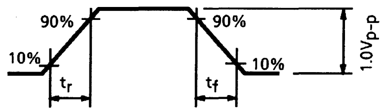
Electrical Characteristics (unless otherwise specified, Ta = 25°C, V_{DD} = 5 V)

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
Oerating supply voltage		V_{DD}	—	f_{XT} = 30 MHz, 0.5 V_{p-p} $f_{P\ IN}$ = 30 MHz, 1.0 V_{p-p} (Note 7)		4.5	5.0	5.5	V
Operating supply current		I_{DD}	—	f_{XT} = 30 MHz, 0.5 V_{p-p} $f_{P\ IN}$ = 30 MHz, 1.0 V_{p-p} (Note 7)		—	15.0	20.0	mA
Operating input frequency		f_{XT1}	—	V_{DD} = 4.5~5.5 V, V_{IN} = 0.5 V_{p-p} (Note 8)		1.0	—	30.0	MHz
		f_{XT2}	—	V_{DD} = 3.0 V, V_{IN} = 0.5 V_{p-p} (Note 8)		1.0	—	10.0	
		$f_{P\ IN1}$	—	V_{DD} = 4.5 ~5.5 V, V_{IN} = 1.0 V_{p-p} (Note 9)		0.1	—	30.0	
		$f_{P\ IN2}$	—	V_{DD} = 3.0 V, V_{IN} = 1.0 V_{p-p} (Note 9)		0.1	—	10.0	
X'tal oscillation frequency		f_{OSC}	—	V_{DD} = 4.5~5.5 V (Note 11)		1.0	—	30.0	MHz
Operating input voltage		V_{XT}	—	V_{DD} = 4.5~5.5 V		0.5	—	V_{DD}	V_{p-p}
		$V_{P\ IN}$	—	V_{DD} = 4.5~5.5 V		1.0	—	V_{DD}	
Input voltage	"H" level	V_{IH}	—	CK, DATA, STB		3.8	—	5.0	V
	"L" level	V_{IL}	—			0.0	—	1.2	
Input current	"H" level	I_{IH}	—	CK, DATA, STB	V_{IH} = 5 V	—	—	1.0	μA
	"L" level	I_{IL}	—		V_{IL} = 0 V	−1.0	—	—	
Breakdown voltage		V_{OH}	—	I_{OH} ≦ 0.1 μA		—	—	12.0	V
Tri-state off-leak current		I_{OZ}	—	D_O	V_{OH} = 5 V, V_{OL} = 5 V	−0.1	—	0.1	μA
Output current	"H" level	I_{OH1}	—	D_O, L	V_{OH} = 4 V	—	−1.0	−0.5	mA
	"L" level	I_{OL1}	—	D_O, H, L	V_{OL} = 1 V	0.5	1.0	—	
	"H" level	I_{OH2}	—	L_D, PSC, P_O	V_{OH} = 4 V	—	−1.5	−1.0	
	"L" level	I_{OL2}	—	L_D, PSC, P_O	V_{OL} = 1 V	1.0	1.5	—	
Input frequency		f_{CK}	—	CK		—	—	200	kHz

Note 7: Ta = −40~85°C

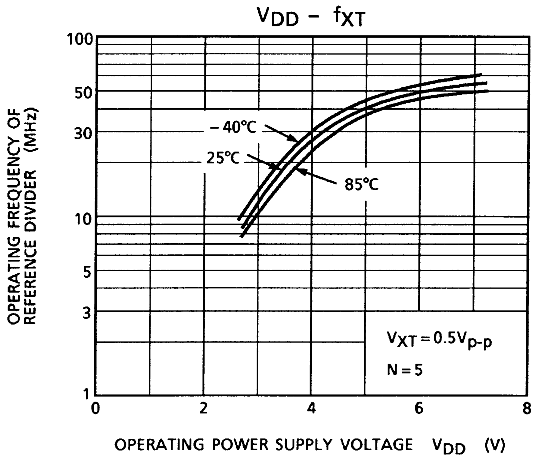
Note 8: X_T is SIN wave input.

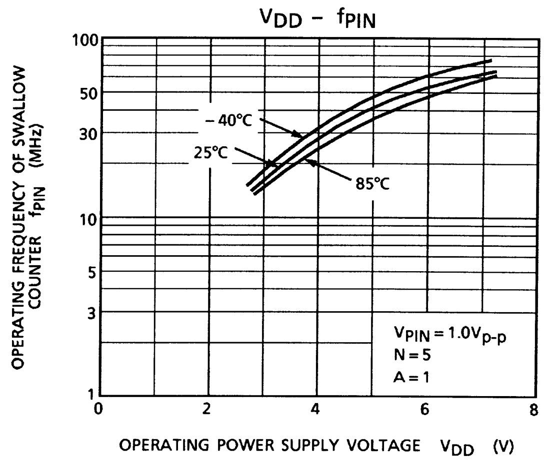
Note 9: P_{IN} is SQ wave input. Rising and falling slopes of input waveform are specified as follows.

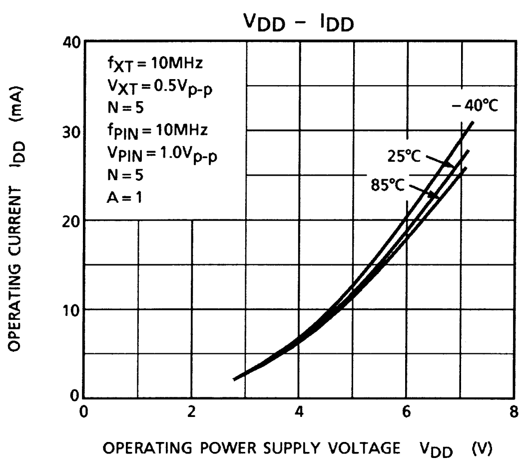


Note 10: $t_r = t_f < 200$ ns

Note 11: Use a crystal oscillator that has a low CI value and a good starting characteristic.

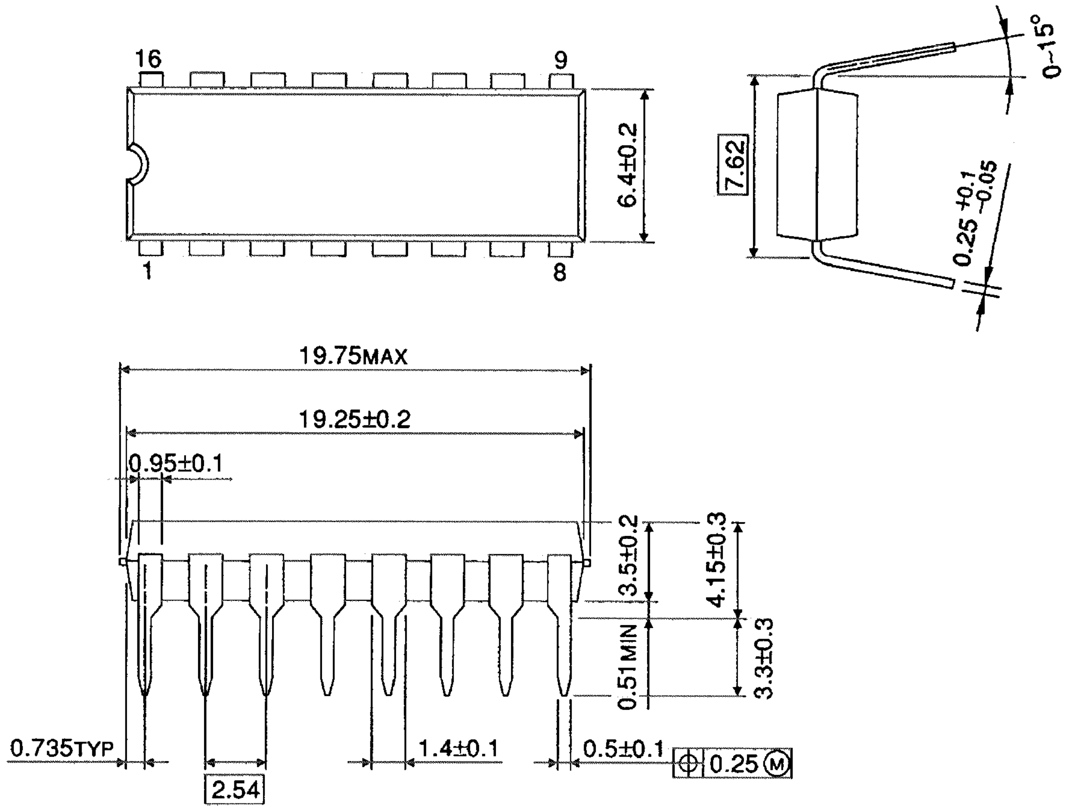

VDD – fXT
OPERATING FREQUENCY OF REFERENCE DIVIDER (MHz)
– 40°C
25°C
85°C
VXT = 0.5Vp-p
N = 5
OPERATING POWER SUPPLY VOLTAGE VDD (V)


VDD – fPIN
OPERATING FREQUENCY OF SWALLOW COUNTER fPIN (MHz)
– 40°C
25°C
85°C
VPIN = 1.0Vp-p
N = 5
A = 1
OPERATING POWER SUPPLY VOLTAGE VDD (V)


VDD – IDD
OPERATING CURRENT IDD (mA)
fXT = 10MHz
VXT = 0.5Vp-p
N = 5
fPIN = 10MHz
VPIN = 1.0Vp-p
N = 5
A = 1
– 40°C
25°C
85°C
OPERATING POWER SUPPLY VOLTAGE VDD (V)

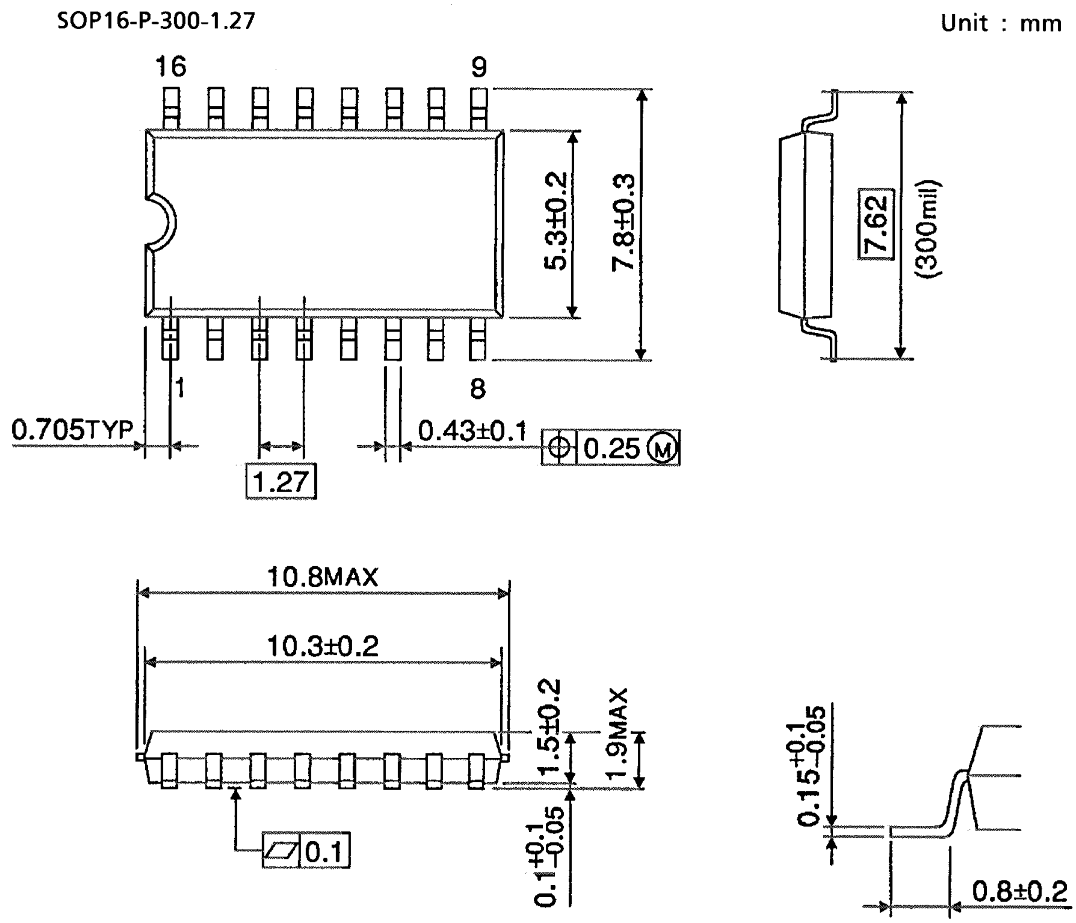
Package Dimensions

DIP16-P-300-2.54A Unit : mm



Weight: 1.00 g (typ.)

Package Dimensions



Weight: 0.16 g (typ.)

About solderability, following conditions were confirmed

- Solderability

(1) Use of Sn-63Pb solder Bath
- · solder bath temperature = 230°C
- · dipping time = 5 seconds
- · the number of times = once
- · use of R-type flux

(2) Use of Sn-3.0Ag-0.5Cu solder Bath
- · solder bath temperature = 245°C
- · dipping time = 5 seconds
- · the number of times = once
- · use of R-type flux