Preliminary TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

T6K19

COLUMN AND ROW DRIVER LSI FOR A DOT MATRIX GRAPHIC LCD

The T6K19 is an MLA driver for small-to-medium-sized dot matrix graphic LCD panels. It supports an 8-bit (80 Series/68 Series) parallel-MPU or serial interface, and can drive the LCD asynchronously from the MPU.

Since the T6K19 contains an RC oscillator, it can generate the timing signals required for the LCD. The display data can be stored in the built-in display RAM, each cell of which corresponds to a dot on the dot-matrix LCD. The display data written to the RAM is in a one-to-one correspondence with the LCD drive signals output by the device. Furthermore, the T6K19 has 132 outputs for the LCD drive (segment) signals which constitute the display data and 33 outputs for the LCD drive (common) signals which constitute the scanning signals. Thus, this single chip allows you to drive an LCD panel of up to 132 × 33 dots using minimal power. The T6K19 has a two-fold display RAM which allows the display data to be switched using a command. To minimize its power consumption, the T6K19 has various built-in analog circuits such as a DA converter for the LCD drive power supply, a DC-DC converter (or doubler) and a contrast control (electronic V_R) circuit. The fact that all these circuits are built into the device allows the LCD panel to be driven from a single power supply.

Unit: mm

T6K19	Lead Pitch	
	IN	OUT
(UAW, 5NS)	0.6	0.23

Please contact Toshiba or an authorized Toshiba dealer for information on package dimensions.

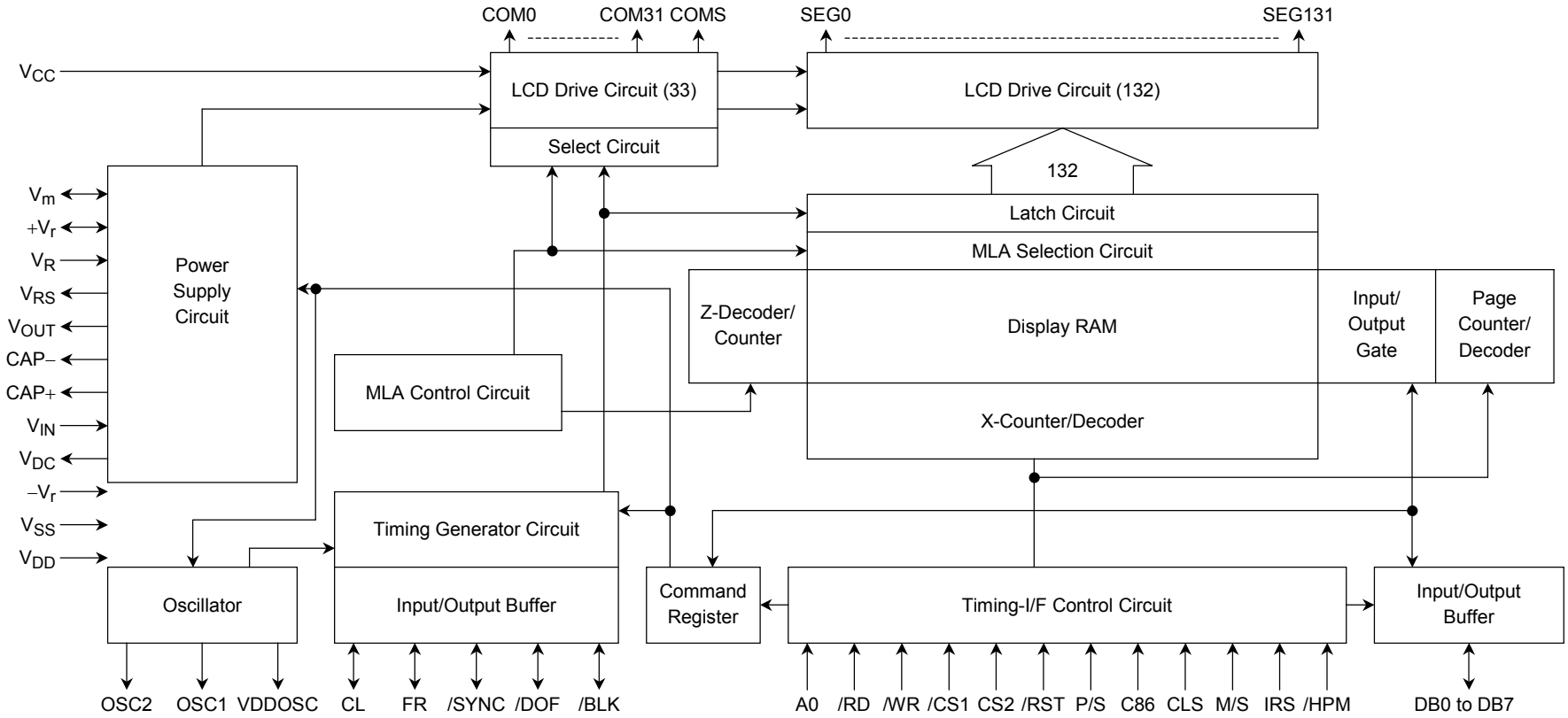
TCP (Tape Carrier Package)

Features

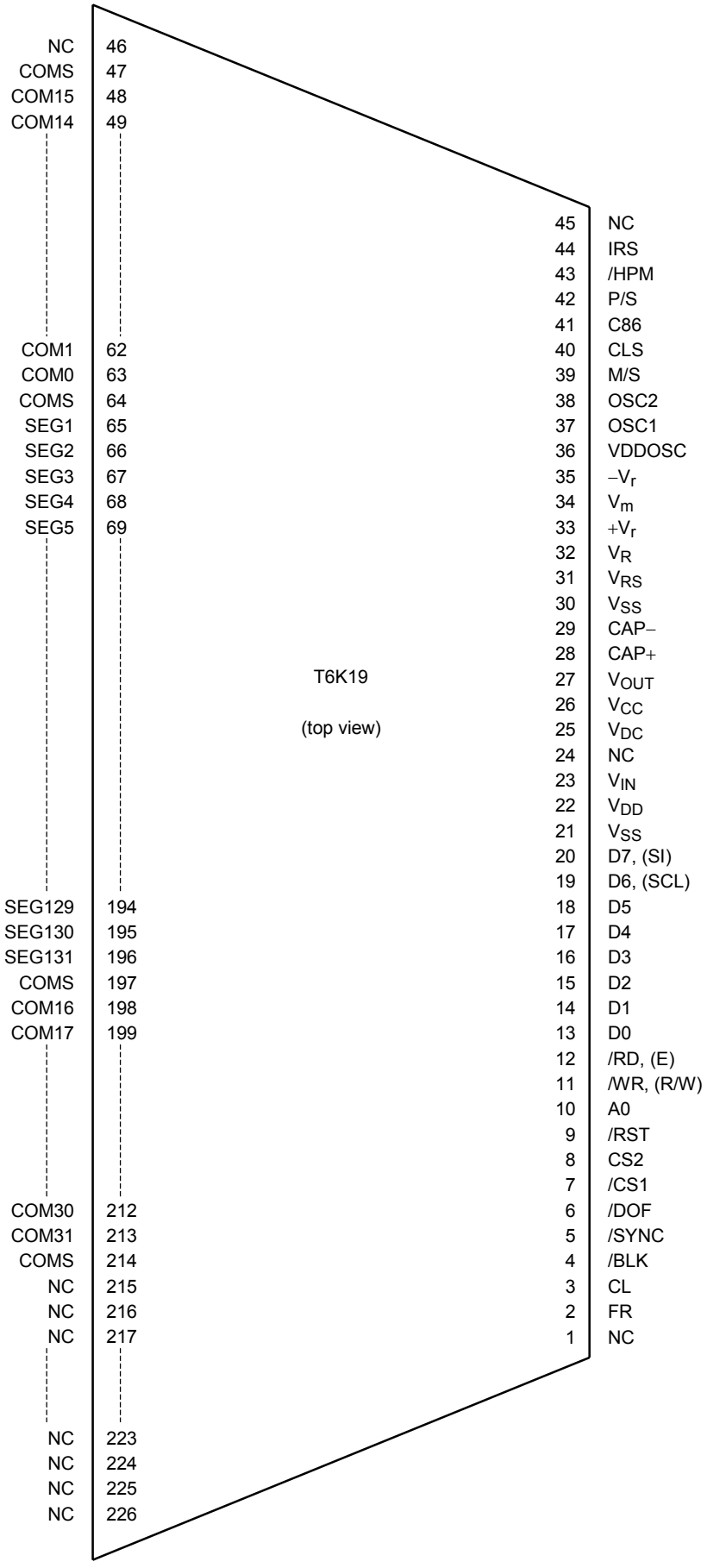
- Display RAM : 132 × (64 + 1) = 8580 dots
- LCD drive outputs : 132 segment outputs
  33 common outputs
- RAM data direct display: Turned ON when corresponding data bit in RAM = 1
  Turned OFF when corresponding data bit in RAM = 0
- Display duty cycle : 1/33 duty
- MPU : 8-bit (80 Series/68 Series) parallel or serial interface
- Oscillator : On-chip CR (capacitance-resistance) oscillator, external clock input also acceptable
- Special circuit : The T6K19 is a driver for medium-to-small-sized dot matrix LCD panels developed in co-operation with LCD manufacturers.
- Power supply circuits : DA converter for LCD drive power supply, DC-DC converter (doubler) and contrast control (electronic V_R) circuit built-in
- Operating voltage : V_{DD} = 2.4 V to 3.3 V
- LCD drive voltage : Vrp-p = 2.5 V to 5.0 V
- CMOS process
- Low power consumption: V_{DD} = 3.0 V, DC-DC converter used (in Doubler Mode), LCD non-loaded, Ta = 25°C, display data = all-white, no data access from MPU
  I_{SS} = 29.0 μA (typ.)
- Packages

Product	Package
T6K19 (xxx, xxx)	TCP (tape carrier package)
JBT6K19-AS	Gold bump chip

Block Diagram



Pin Assignment



Note 1: The above diagram shows the pin configuration of the LSI chip, not that of the tape carrier package. The above TCP pin assignment is shown for reference purposes only.

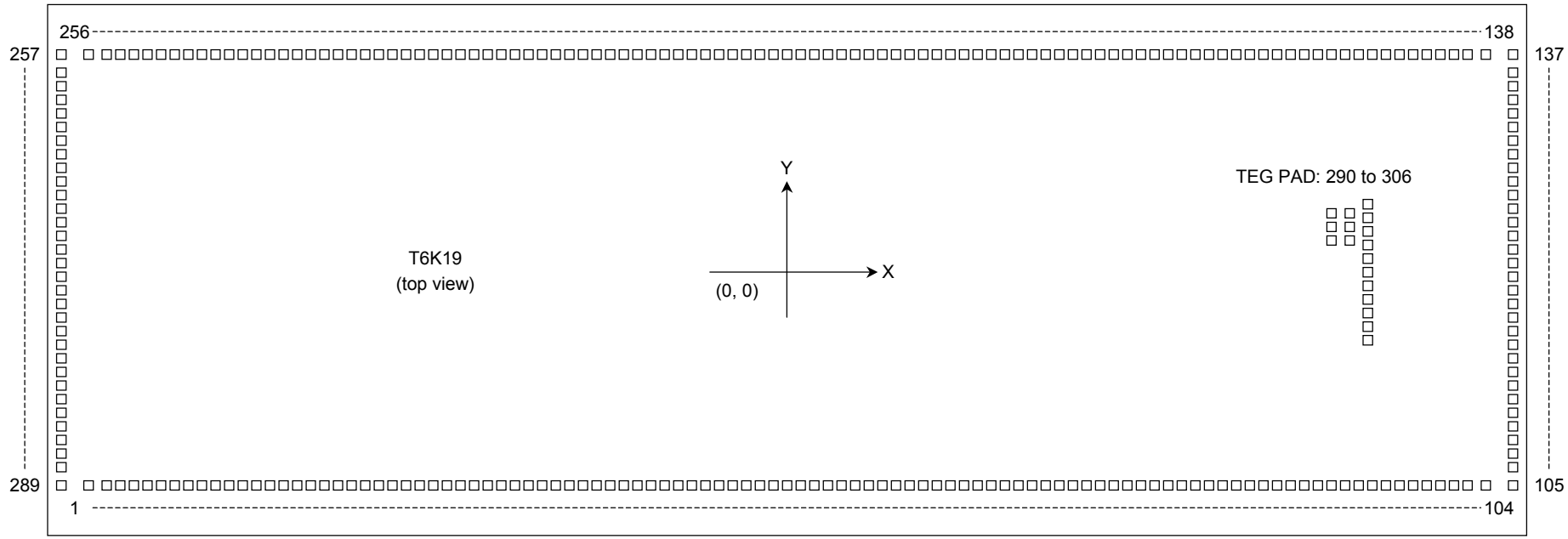
Pad Specification

Parameter		Size	Unit
Chip size		9380 × 2760	μm
Chip tip coordinates	(1)	−4190, −1380	μm
	(2)	−4190, 1380	
	(3)	4190, 1380	
	(4)	4190, −1380	
Bump pitch		70	μm
Bump height		14 ± 4	μm

Parameter	Number of Pins
Input pin	87 (including dummy pins)
Output pin	185 (including dummy pins)
FUSE pin	17
TEG pin	17

Note 2: The FUSE pins (No. 86 to 102) and TEG pins (No. 290 to 306) are LSI test pins, and are not used in the normal operation of the T6K19. These pins should be left open.

Pad Layout


256
138
257
137
289
105
1
104
T6K19
(top view)
Y
X
(0, 0)
TEG PAD: 290 to 306

Pad Coordinates

[unit: μm]

No.	Name	X-Point	Y-Point	No.	Name	X-Point	Y-Point	No.	Name	X-Point	Y-Point
1	NC	−4149	−1139	43	V_{CC}	−775	−1139	85	NC	2586	−1139
2	FR	−4055	−1139	44	V_{CC}	−695	−1139	86	FUSE11	2666	−1139
3	CL	−3975	−1139	45	V_{OUT}	−615	−1139	87	FUSE12	2746	−1139
4	/BLK	−3895	−1139	46	V_{OUT}	−535	−1139	88	FUSE13	2826	−1139
5	/SYNC	−3815	−1139	47	V_{OUT}	−455	−1139	89	FUSE1G	2906	−1139
6	/DOF	−3735	−1139	48	CAP+	−375	−1139	90	FUSE14	2986	−1139
7	V_{SS}	−3655	−1139	49	CAP+	−295	−1139	91	FUSE15	3066	−1139
8	/CS1	−3575	−1139	50	CAP+	−215	−1139	92	FUSE21	3146	−1139
9	CS2	−3495	−1139	51	CAP−	−135	−1139	93	FUSE22	3226	−1139
10	V_{DD}	−3415	−1139	52	CAP−	−54.5	−1139	94	FUSE23	3306	−1139
11	/RST	−3335	−1139	53	CAP−	25.5	−1139	95	FUSE2G	3386	−1139
12	A0	−3255	−1139	54	V_{SS}	105.5	−1139	96	FUSE24	3466	−1139
13	V_{SS}	−3175	−1139	55	V_{SS}	185.5	−1139	97	FUSE25	3546	−1139
14	/WR	−3095	−1139	56	V_{RS}	265.5	−1139	98	FUSE31	3626	−1139
15	/RD	−3015	−1139	57	V_{RS}	345.5	−1139	99	FUSE32	3706	−1139
16	V_{DD}	−2935	−1139	58	V_R	425.5	−1139	100	FUSE3G	3786	−1139
17	D0	−2855	−1139	59	V_R	505.5	−1139	101	FUSE33	3866	−1139
18	D1	−2775	−1139	60	V_{SS}	585.5	−1139	102	FUSE34	3946	−1139
19	D2	−2695	−1139	61	V_{SS}	665.5	−1139	103	NC	4026	−1139
20	D3	−2615	−1139	62	NC	745.5	−1139	104	NC	4120	−1139
21	D4	−2535	−1139	63	V_{r+}	825.5	−1139	105	NC	4449	−1139
22	D5	−2455	−1139	64	V_{r+}	905.5	−1139	106	COMS	4449	−1050
23	D6	−2375	−1139	65	V_m	985.5	−1139	107	COM15	4449	−980
24	D7	−2295	−1139	66	V_m	1066	−1139	108	COM14	4449	−910
25	V_{SS}	−2215	−1139	67	V_{r-}	1146	−1139	109	COM13	4449	−840
26	V_{SS}	−2135	−1139	68	V_{r-}	1226	−1139	110	COM12	4449	−770
27	V_{SS}	−2055	−1139	69	NC	1306	−1139	111	COM11	4449	−700
28	V_{SS}	−1975	−1139	70	VDDOSC	1386	−1139	112	COM10	4449	−630
29	V_{DD}	−1895	−1139	71	OSC1	1466	−1139	113	COM9	4449	−560
30	V_{DD}	−1815	−1139	72	OSC2	1546	−1139	114	COM8	4449	−490
31	V_{DD}	−1735	−1139	73	V_{DD}	1626	−1139	115	COM7	4449	−420
32	V_{DD}	−1655	−1139	74	V_{DD}	1706	−1139	116	COM6	4449	−350
33	V_{IN}	−1575	−1139	75	M/S	1786	−1139	117	COM5	4449	−280
34	V_{IN}	−1495	−1139	76	CLS	1866	−1139	118	COM4	4449	−210
35	V_{IN}	−1415	−1139	77	V_{SS}	1946	−1139	119	COM3	4449	−140
36	V_{IN}	−1335	−1139	78	C86	2026	−1139	120	COM2	4449	−70
37	NC	−1255	−1139	79	P/S	2106	−1139	121	COM1	4449	0
38	V_{DC}	−1175	−1139	80	V_{DD}	2186	−1139	122	COM0	4449	70
39	V_{DC}	−1095	−1139	81	/HPM	2266	−1139	123	COMS2	4449	140
40	NC	−1015	−1139	82	V_{SS}	2346	−1139	124	SEG0	4449	210
41	V_{CC}	−935	−1139	83	IRS	2426	−1139	125	SEG1	4449	280
42	V_{CC}	−855	−1139	84	V_{DD}	2506	−1139	126	SEG2	4449	350

No.	Name	X-Point	Y-Point	No.	Name	X-Point	Y-Point	No.	Name	X-Point	Y-Point
127	SEG3	4449	420	171	SEG45	1820	1139	215	SEG89	−1260	1139
128	SEG4	4449	490	172	SEG46	1750	1139	216	SEG90	−1330	1139
129	SEG5	4449	560	173	SEG47	1680	1139	217	SEG91	−1400	1139
130	SEG6	4449	630	174	SEG48	1610	1139	218	SEG92	−1470	1139
131	SEG7	4449	700	175	SEG49	1540	1139	219	SEG93	−1540	1139
132	SEG8	4449	770	176	SEG50	1470	1139	220	SEG94	−1610	1139
133	SEG9	4449	840	177	SEG51	1400	1139	221	SEG95	−1680	1139
134	SEG10	4449	910	178	SEG52	1330	1139	222	SEG96	−1750	1139
135	SEG11	4449	980	179	SEG53	1260	1139	223	SEG97	−1820	1139
136	SEG12	4449	1050	180	SEG54	1190	1139	224	SEG98	−1890	1139
137	NC	4449	1139	181	SEG55	1120	1139	225	SEG99	−1960	1139
138	NC	4149	1139	182	SEG56	1050	1139	226	SEG100	−2030	1139
139	SEG13	4060	1139	183	SEG57	980	1139	227	SEG101	−2100	1139
140	SEG14	3990	1139	184	SEG58	910	1139	228	SEG102	−2170	1139
141	SEG15	3920	1139	185	SEG59	840	1139	229	SEG103	−2240	1139
142	SEG16	3850	1139	186	SEG60	770	1139	230	SEG104	−2310	1139
143	SEG17	3780	1139	187	SEG61	700	1139	231	SEG105	−2380	1139
144	SEG18	3710	1139	188	SEG62	630	1139	232	SEG106	−2450	1139
145	SEG19	3640	1139	189	SEG63	560	1139	233	SEG107	−2520	1139
146	SEG20	3570	1139	190	SEG64	490	1139	234	SEG108	−2590	1139
147	SEG21	3500	1139	191	SEG65	420	1139	235	SEG109	−2660	1139
148	SEG22	3430	1139	192	SEG66	350	1139	236	SEG110	−2730	1139
149	SEG23	3360	1139	193	SEG67	280	1139	237	SEG111	−2800	1139
150	SEG24	3290	1139	194	SEG68	210	1139	238	SEG112	−2870	1139
151	SEG25	3220	1139	195	SEG69	140	1139	239	SEG113	−2940	1139
152	SEG26	3150	1139	196	SEG70	70	1139	240	SEG114	−3010	1139
153	SEG27	3080	1139	197	SEG71	0	1139	241	SEG115	−3080	1139
154	SEG28	3010	1139	198	SEG72	−70	1139	242	SEG116	−3150	1139
155	SEG29	2940	1139	199	SEG73	−140	1139	243	SEG117	−3220	1139
156	SEG30	2870	1139	200	SEG74	−210	1139	244	SEG118	−3290	1139
157	SEG31	2800	1139	201	SEG75	−280	1139	245	SEG119	−3360	1139
158	SEG32	2730	1139	202	SEG76	−350	1139	246	SEG120	−3430	1139
159	SEG33	2660	1139	203	SEG77	−420	1139	247	SEG121	−3500	1139
160	SEG34	2590	1139	204	SEG78	−490	1139	248	SEG122	−3570	1139
161	SEG35	2520	1139	205	SEG79	−560	1139	249	SEG123	−3640	1139
162	SEG36	2450	1139	206	SEG80	−630	1139	250	SEG124	−3710	1139
163	SEG37	2380	1139	207	SEG81	−700	1139	251	SEG125	−3780	1139
164	SEG38	2310	1139	208	SEG82	−770	1139	252	SEG126	−3850	1139
165	SEG39	2240	1139	209	SEG83	−840	1139	253	SEG127	−3920	1139
166	SEG40	2170	1139	210	SEG84	−910	1139	254	SEG128	−3990	1139
167	SEG41	2100	1139	211	SEG85	−980	1139	255	SEG129	−4060	1139
168	SEG42	2030	1139	212	SEG86	−1050	1139	256	NC	−4149	1139
169	SEG43	1960	1139	213	SEG87	−1120	1139	257	NC	−4449	1139
170	SEG44	1890	1139	214	SEG88	−1190	1139	258	SEG130	−4449	1050

No.	Name	X-Point	Y-Point	No.	Name	X-Point	Y-Point	No.	Name	X-Point	Y-Point
259	SEG131	−4449	980	303	TEG14	3472	261.6				
260	COMS3	−4449	910	304	TEG15	3292	61.6				
261	COM16	−4449	840	305	TEG16	3292	161.6				
262	COM17	−4449	770	306	TEG17	3292	261.6				
263	COM18	−4449	700								
264	COM19	−4449	630								
265	COM20	−4449	560								
266	COM21	−4449	490								
267	COM22	−4449	420								
268	COM23	−4449	350								
269	COM24	−4449	280								
270	COM25	−4449	210								
271	COM26	−4449	140								
272	COM27	−4449	70								
273	COM28	−4449	0								
274	COM29	−4449	−70								
275	COM30	−4449	−140								
276	COM31	−4449	−210								
277	COMS4	−4449	−280								
278	NC	−4449	−350								
279	NC	−4449	−420								
280	NC	−4449	−490								
281	NC	−4449	−560								
282	NC	−4449	−630								
283	NC	−4449	−700								
284	NC	−4449	−770								
285	NC	−4449	−840								
286	NC	−4449	−910								
287	NC	−4449	−980								
288	NC	−4449	−1050								
289	NC	−4449	−1139								
290	TEG1	3751	−718								
291	TEG2	3751	−618								
292	TEG3	3751	−513								
293	TEG4	3751	−413								
294	TEG5	3751	−313								
295	TEG6	3751	−213								
296	TEG7	3751	−113								
297	TEG8	3751	−12.5								
298	TEG9	3751	87.5								
299	TEG10	3751	187.5								
300	TEG11	3751	287.5								
301	TEG12	3472	61.6								
302	TEG13	3472	161.6								

Pin Functions (1)

Pin Name	I/O	Functions
SEG0 to SEG131	Output	LCD drive segment signal output pins
COM0 to COM31	Output	LCD drive common signal output pins
COMS	Output	Indicator-only common signal output pin Four CMOS lines output the same signal.
S0 to S9	Output	Segment signal output pins for the static drive icon
D6 (SCL)	I/O	Data bus This pin is used as the Data-Synchronizing Clock (SCL) for the serial interface when P/S = Low.
D7 (SI)	I/O	Data bus This pin is used as a data input pin (SI) for the serial interface when P/S = Low.
A0	Input	Data/instruction select signal input pin ● D7 to D0 is display data when A0 = Low. ● D7 to D0 is control data (instruction data) when A0 = High.
/RD (E)	Input	Read Select signal pin ● When C86 = Low (80 Series MPU selected), this pin outputs data while /RD = Low. The data is latched on either signal edge. ● When C86 = High (68 Series MPU selected), this pin is used as the Enable Signal Input pin (E).
/WR (R/W)	Input	Write Select signal pin ● When C86 = Low (80 Series MPU selected), data is latched on the rising edge of /WR. ● When C86 = High (68 Series MPU selected), Data Read is selected when R/W = High and Data Write is selected when R/W = Low.
/CS1	Input	Chip Select signal pin (1) Data/command can be input or output while /CS1 is Low.
CS2	Input	Chip Select signal pin (2) Data/command can be input or output while CS2 is High.
/RST	Input	Reset signal pin The device is reset when /RST = Low.
P/S	Input	Parallel/Serial Interface Select signal pin ● The parallel interface is selected when P/S = High. ● The serial interface is selected when P/S = Low.
C86	Input	MPU Interface Switch signal pin ● The 68 Series MPU interface is selected when C86 = High. ● The 80 Series MPU interface is selected when C86 = Low.
CLS	Input	Display Clock Driver ON/OFF Select signal pin ● The on-chip oscillator is enabled when CLS = High. ● The on-chip oscillator is disabled when CLS = Low and the device enters External Clock Input Mode.

Pin Functions (2)

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Functions</th></tr>
<tr><td>M/S</td><td>Input</td><td>Master/Slave Select signal pin
● The device operates in Master Mode when M/S = High.
● The device operates in Slave Mode when M/S = Low.
<table>
<tr><th>M/S</th><th>CLS</th><th>Oscilla -tion Circuit</th><th>Power Supply Circuit</th><th>CL</th><th>FR</th><th>/DOF</th><th>/SYNC</th><th>/BLK</th><th>S0 to S9</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>Valid</td><td>Valid</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>L</td><td>Invalid</td><td>Valid</td><td>Input</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>Invalid</td><td>Invalid</td><td>Input</td><td>Input</td><td>Input</td><td>Input</td><td>Input</td><td>Output</td></tr>
<tr><td>L</td><td>Invalid</td><td>Invalid</td><td>Input</td><td>Input</td><td>Input</td><td>Input</td><td>Input</td><td>Output</td></tr>
</table></td></tr>
<tr><td>CL</td><td>I/O</td><td>Display clock input/output pin</td></tr>
<tr><td>FR</td><td>I/O</td><td>Alternating signal input/output pin
● FR is set for output when M/S = High.
● FR is set for input when M/S = Low.</td></tr>
<tr><td>/DOF</td><td>I/O</td><td>LCD blanking control input/output pin
● /DOF is set for output when M/S = High.
● /DOF is set for input when M/S = Low.</td></tr>
<tr><td>IRS</td><td>Input</td><td>$+V_r$ voltage adjusting resistor select pin
● The internal resistor for $+V_r$ voltage adjustment is used when IRS = High.
● The external resistor for $+V_r$ voltage adjustment is connected between V_R and V_{RS} when IRS = Low.</td></tr>
<tr><td>/HPM</td><td>Input</td><td>LCD drive power control pin
● Normal Power Mode is entered when /HPM = High.
● High Power Mode is entered when /HPM = Low.</td></tr>
<tr><td>CAP+</td><td>Output</td><td>Positive side of capacitor-connecting pin for DC-DC converter</td></tr>
<tr><td>CAP−</td><td>Output</td><td>Negative side of capacitor-connecting pin for DC-DC converter</td></tr>
<tr><td>V_{OUT}</td><td>Output</td><td>DC-DC converter output pin</td></tr>
<tr><td>V_R</td><td>Input</td><td>Voltage adjustment pin
A voltage in the range of $+V_r$ to $-V_r$ is developed across a dividing resistor. This pin is effective only when the internal resistor for $+V_r$ voltage adjustment is unused (IRS = Low). This pin cannot be used when IRS = High.</td></tr>
<tr><td>V_{DD}</td><td>—</td><td>MPU power supply pin</td></tr>
<tr><td>V_{SS}</td><td>—</td><td>System GND (0 V) pin</td></tr>
<tr><td>V_{IN}</td><td>—</td><td>Reference power supply pin for DC-DC converter</td></tr>
<tr><td>V_{CC}</td><td>—</td><td>Power supply pin for LCD driver circuit</td></tr>
<tr><td>V_{RS}</td><td>—</td><td>Externally input VREG power supply pin for the LCD power supply voltage adjusting circuit</td></tr>
<tr><td>$+V_r$, $-V_r$, V_m</td><td>—</td><td>Power supply pins for LCD driver circuit
In Master Mode, when the power supply is on, a proper voltage is provided for MLA driving by the built-in power supply circuit.
The power supply level for liquid crystal drive is shown below.
$+V_r \geq V_m \geq -V_r$ (0 V)
Connect $-V_r$ to V_{SS}.</td></tr>
<tr><td>OSC1, OSC2</td><td>—</td><td>Oscillation-circuit-adjusting-resistor select pins.
The adjustment resistor for the oscillation circuit is connected between OSC1 and OSC2
If it is necessary to adjust the oscillation frequency, connect a resistor between OSC1 and OSC2.</td></tr>
</table>

Pin Functions (3)

Pin Name	I/O	Functions
VDDOSC	—	Oscillator circuit regulator monitor pin Connect a capacitor between VDDOSC and V_{SS}.
V_{DC}	—	Power supply DC-DC converter monitor pin Connect a capacitor between V_{DC} and V_{SS}.
/SYNC	I/O	• /SYNC is set for output when M/S = High. • /SYNC is set for input when M/S = Low.
/BLK	I/O	• /BLK is set for output when M/S = High. • /BLK is set for input when M/S = Low.

Pin Functions (4)

P/S	C86	Interface Method	/CS1	CS2	A0	/WR	/RD	D7	D6	D5	D4	D3	D2	D1	D0
H	L	80MPU (/CS1)	/CS1	H	A0	/WR	/RD	D7	D6	D5	D4	D3	D2	D1	D0
		80MPU (CS2)	L	CS2	A0	/WR	/RD	D7	D6	D5	D4	D3	D2	D1	D0
	H	68MPU	L	H	A0	R/W	E	D7	D6	D5	D4	D3	D2	D1	D0
L	—	Serial	L	H	A0	—	—	SI	SCL	—					

The symbol 'L' indicates that the V_{SS}-level voltage is input.

The symbol 'H' indicates that the V_{DD}-level voltage is input.

The symbol '—' means that either the V_{SS}-level or the V_{DD}-level voltage is input.

Function of Each Block

- Interface logic

  The T6K19 can be operated by an 80 Series MPU, a 68 Series MPU or via a serial interface. Figure 1 shows examples of the various possible interface configurations.

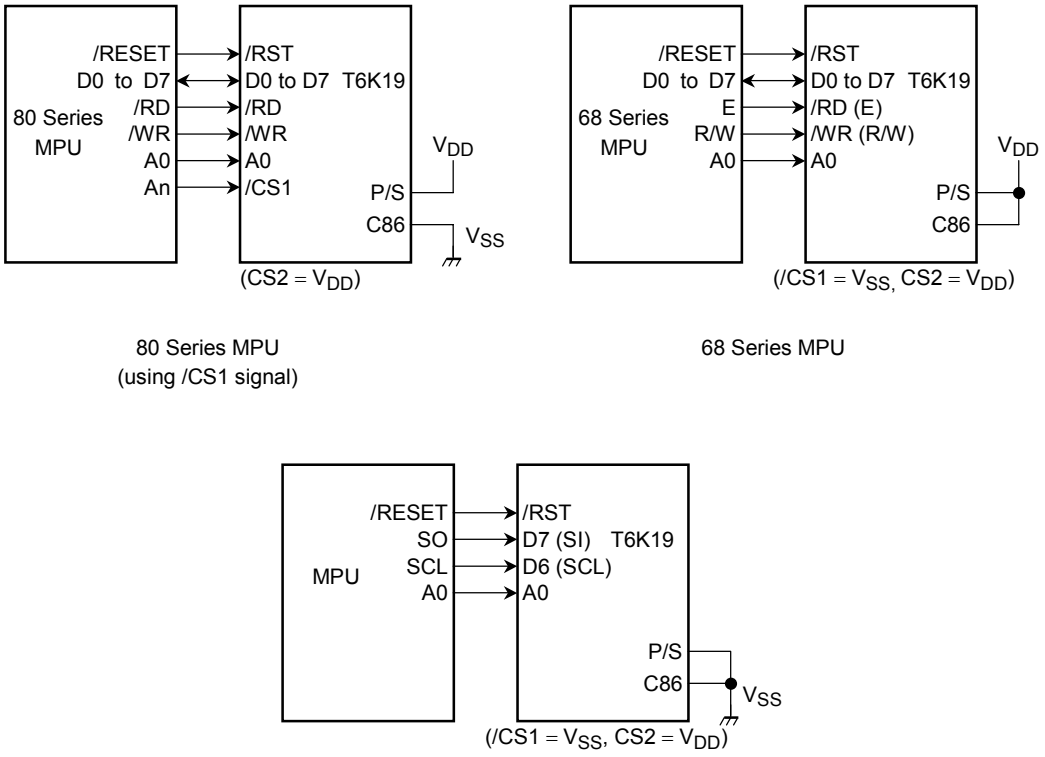


Figure 1

- Oscillator

  By setting the CLS signal to High or Low respectively, either the built-in RC oscillator or an external clock can be selected as the clocking source. This is shown in Figure 2. When CLS = High, the RC oscillator is enabled, supplying the display clock to the internal logic. When CLS = Low, the CL pin is selected for input, and an external clock can be input.

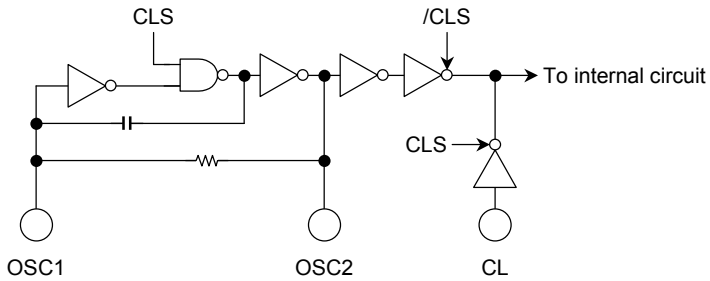


Figure 2

- Timing signal generation circuit

  This circuit generates the display timing signals and operation clock required for display by dividing the clock frequency derived from the RC oscillator circuit or an external source.

- MLA control circuit

  This circuit controls the display timing signals for the MLA.

- Timing interface control circuit

  This circuit receives the control signals from the MPU and converts them into the timing signals required by the T6K19, as determined by the interface mode selection signals.

- Command Register

  This register holds the command data from the MPU which is used to control the T6K19.

Command Definitions

No.	Command Name	A0	/WR	/RD	D7	D6	D5	D4	D3	D2	D1	D0	Function
1	Display ON/OFF	0	1	0	1	0	1	0	1	1	1	1/0	Turns LCD display ON or OFF. 0: OFF; 1: ON
2	Set Display Start Line	0	1	0	0	1	Display start address (0 to 63)						Sets display RAM's display start line address.
3	Set Page Address	0	1	0	1	0	1	1	Page address (0 to 8)				Sets display RAM's page address.
4	Set Column Address (high-order bits)	0	1	0	0	0	0	1	High-order column address (0 to 15)				Sets high-order bits of display RAM column address.
	Set Column Address (low-order bits)	0	1	0	0	0	0	0	Low-order column address (0 to 15)				Sets low-order bits of display RAM column address.
5	Read Status	0	0	1	Status				0	0	0	0	Reads status information.
6	Write Display Data	1	1	0	Write data								Writes to display RAM.
7	Read Display Data	1	0	1	Read data								Reads from display RAM.
8	Select ADC	0	1	0	1	0	1	0	0	0	0	1/0	Selects display RAM address and segment output correspondence. 0: Normal 1: Reverse
9	Normal/Reverse Display	0	1	0	1	0	1	0	0	1	1	1/0	Normal/reverse of LCD 0: Normal 1: Reversed
10	Entire Display ON/OFF	0	1	0	1	0	1	0	0	1	0	1/0	Turns on entire Display. 0: Normal display 1: All ON
11	Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Sets column address counter. When writing +1 When reading No change
12	End	0	1	0	1	1	1	0	1	1	1	0	Cancels read-modify-write operation.
13	Reset	0	1	0	1	1	1	0	0	0	1	0	Resets the internal circuits.
14	Select Common Output State	0	1	0	1	1	0	0	1/0	*	*	*	(D3) Selects common scanning direction. 0: Forward 1: Reverse

No.	Command Name	A0	/WR	/RD	D7	D6	D5	D4	D3	D2	D1	D0	Function
15	Set Power Control	0	1	0	0	1	0	0	1	Operating state			Selects operating state for internal power supply.
16	Set $+V_r$ Output Voltage Adjust Width	0	1	0	0	0	1	0	0	Adjustment width value setting			Sets $+V_r$ output voltage adjustment width.
17	Set Electronic V_R Mode	0	1	0	1	0	0	0	0	0	0	1	—
	Set Electronic V_R Register	0	1	0	*	*	Electronic V_R value						Sets $+V_r$ output voltage in Electronic V_R Register.
18	Display Double-Size	0	1	0	1	0	1	0	1	0	0	1/0	0: Normal display 1: Double-size display position setting
	Set Double-Size Start Line	0	1	0	*	*	Double-size start line (0 to 63)						Sets double-size start line.
	Set Double-Size Stop Line	0	1	0	*	*	Double-size stop line (0 to 63)						Sets double-size stop line.
19	Set Alternating Period	0	1	0	1	1	0	1	1/0	*	Alternating period		0: Frame inverted 1: Alternating period set
20	Write to Display RAM in Burst	0	1	0	1	1	1	0	0	1	0	1	Sets display RAM burst write.
		0	1	0	Burst write data								Sets burst write data.
21	NOP	0	1	0	1	1	1	0	0	0	1	1	Command for no-operation.
22	Test Mode	0	1	0	1	1	1	1	Test mode				IC Command for testing the chip

1. Display ON/OFF

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	1	1	1	0	LCD OFF
0	1	0	1	0	1	0	1	1	1	1	LCD ON

This command turns the display ON/OFF.

If the Entire Display ON command is executed while the display is off, the device enters Power Save Mode.

For details, please refer to the explanation of Power Save Mode.

2. Set Display Start Line

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	Display start address (0 to 63)					

This command sets the display start line address of the display RAM. The display area starts from the specified line address and continues in the line address increment direction by a number of lines equivalent to the display duty cycle. A dynamic change of line addresses using this command allows the display to be scrolled smoothly or pages to be switched in the vertical direction.

3. Set Page Address

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	Page address (0 to 7)			

This command sets the page address of the display RAM. One of the eight pages which comprise the display RAM is selected. Any display RAM address can be accessed as desired by setting its page address and column address. Changing the page addresses does not affect the state of the display.

4. Set Column Address

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	0	0	1	A7	A6	A5	A4	High-order bits
0	1	0	0	0	0	0	A3	A2	A1	A0	Low-order bits

This command sets the column address of the display RAM. The column address is set using two separate but successive operations, one of which sets the 4 high-order bits while the other sets the 4 low-order bits. The column address is automatically incremented by 1 after data has been read from or written to the display RAM. When the column address is incremented so that it wraps around from 83H to 00H, the page address is automatically incremented by 1.

5. Read Status

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	B	A	D	R	0	0	0	0

This command can be used to ascertain the status of the T6K19.

B (busy): When B = 1, the display RAM is being written in a burst, so commands cannot be accepted.
When B = 0, commands are accepted.

A (ADC): When A = 1, the display RAM address segment outputs are normal.
When A = 0, the display RAM address segment outputs are reversed.

D (display): When D = 1, display is turned OFF.
When D = 0, display is turned ON.

R (reset): When R = 1, the device is being reset.
When R = 0, the device is active (i.e. is not being reset).

6. Write Display Data

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

This command writes 8-bit data to a specified display RAM address. The column address is automatically incremented by 1 after data has been written to the display RAM. Thus, the MPU can write several items of display data in succession.

7. Read Display Data

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

This command reads 8-bit data from a specified display RAM address. The column address is automatically incremented by 1 after data has been read from the display RAM. Thus, the MPU can read out several items of display data in succession. However, one dummy read must be performed immediately after the column address is set.

If the device is being operated via a serial interface, this command cannot be used to read out display data.

8. Select ADC

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	0	0	0	0	Normal
0	1	0	1	0	1	0	0	0	0	1	Reverse

This command can be used to select the correspondence between display RAM column addresses and segment driver outputs. The sequence of the segment driver output pins can be reversed using this command.

The column address is incremented (by 1) during data reading or writing as determined by the display RAM's mapped column addresses.

9. Normal/Reverse Display

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	0	1	1	0	Normal
0	1	0	1	0	1	0	0	1	1	1	Reverse

This command reverses the display without rewriting the contents of the display RAM, which are retained.

10. Entire Display ON/OFF

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	0	1	0	0	Normal display
0	1	0	1	0	1	0	0	1	0	1	Entire display ON

This command turns the entire display ON, irrespective of the contents of the display RAM, which are retained. This command overrides the effect of the Normal/Reverse Display command.

If this command is executed while the display is off, the device will enter Power Save Mode.

For details, please refer to the explanation of Power Save Mode.

11. Read-Modify-Write

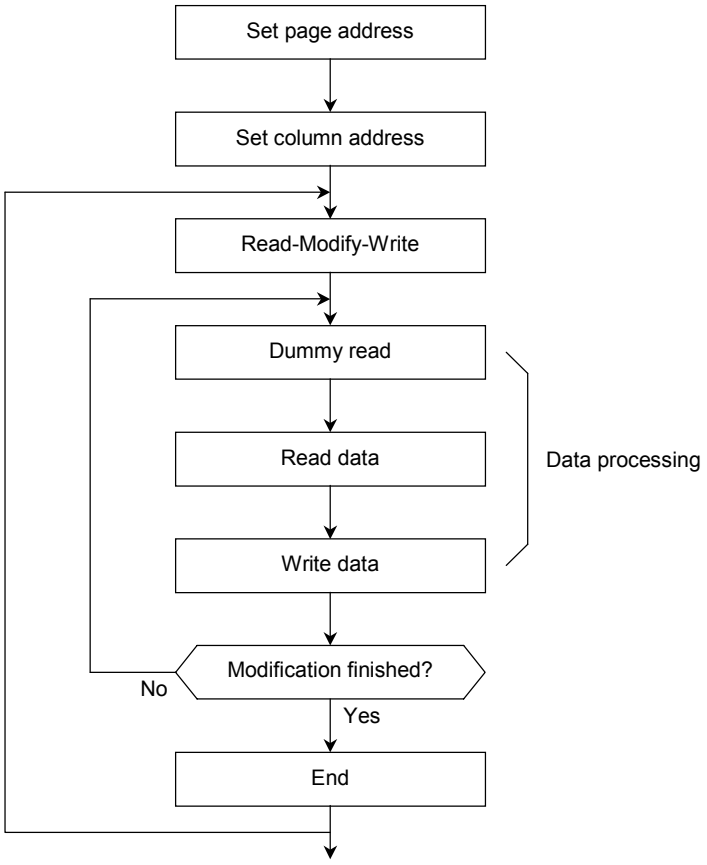
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

This command is used in combination with the End command. Once this command has been input, the column address can only be incremented (by 1) by the Write Display Data command; the Read Display Data command will have no effect on it until an End command has been input.

When an End command is input, the column address reverts to the address value at the time the Read-Modify-Write command was input. This function helps to reduce the MPU load when the data in a specific display area (such as a blinking cursor) needs to be modified repeatedly.

While the device is in the Read-Modify-Write Mode, any command other than the Write Display Data, Read Display Data and Set Column Address commands can be used.

- Sequence for Read-Modify-Write



12. End

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

This command causes the device to exit Read-Modify-Write Mode and restores the column address value which was current at the time the device entered Read-Modify-Write Mode.

13. Reset

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

This command initializes all parameters: the display start line, column address, page address, common output state, $+V_r$ output voltage adjustment width and electronic V_R, and cancels Read-Modify-Write Mode or Test Mode. This command does not affect the display RAM.

To initialize the device at power-on, pull the /RST input Low. The Reset command cannot be used for this purpose.

14. Select Common Output State

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	CDR	*	*	*

*: Invalid

CDR: Selects the scanning direction of the COM output pins.
CDR = 0: COM0 → COM31; CDR = 1: COM31 → COM0

15. Set Power Control

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	1	DC	V_{DC}	V_F

DC: Turns the DC-DC converter ON or OFF.
DC = 1: DC-DC converter turned ON; DC = 0: DC-DC converter turned OFF

V_{DC}: Turns the supply voltage adjustment circuit for the DC-DC converter ON or OFF.
V_{DC} = 1: Supply voltage adjustment circuit turned ON;
V_{DC} = 0: Supply voltage adjustment circuit turned OFF

V_F: Turns the voltage follower (V/F) circuit ON or OFF.
V_F = 1: V/F circuit turned ON; V_F = 0: V/F circuit turned OFF

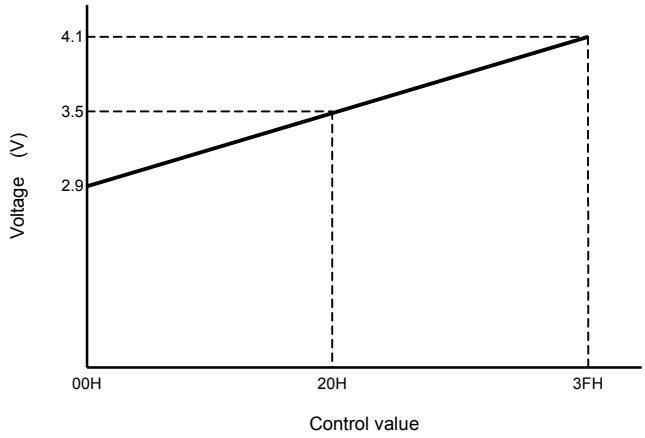
16. Set $+V_r$ Output Voltage Adjustment Width

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	Adjustment width set value		

This command sets the $+V_r$ output voltage adjustment width.
The $+V_r$ pin voltages when the electronic V_R is at its center value (as set by the 17H or 20H command) are shown below.

Register Value (D2 to D0)	$+V_r$ Pin Voltage (17H or 20H command)
000	2.9 V
001	3.1 V
010	3.3 V
011	3.5 V
100	3.7 V
101	3.9 V
110	4.1 V
111	4.4 V

Example of Change in Electronic V_R (when register value = 011)



17. Set Electronic VR (two-byte command)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	0	0	0	0	0	1	Set Electronic V_R Mode
0	1	0	*	*	Electronic V_R value						Set Electronic V_R Register

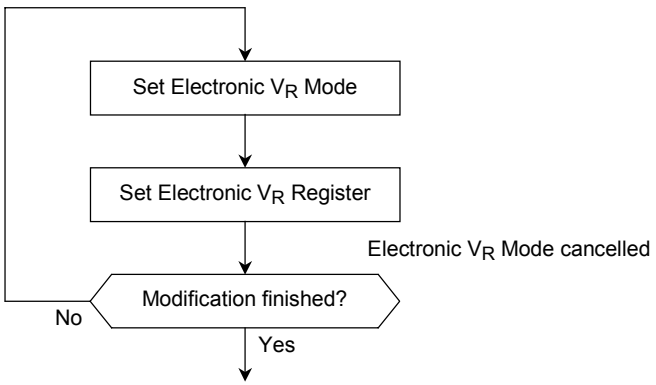
*: Invalid

This command consists of two bytes, one of which is used to set the Electronic V_R Mode, the other of which is used to set the Electronic V_R Register. Ensure that the two bytes are input in the proper sequence.

When the Set Electronic V_R Mode command is input, the device enters Electronic V_R Mode, in which case no command other than the Set Electronic V_R Register command can be used. The device is then freed from this state when the Set Electronic V_R Register command is used to set the Electronic V_R Register.

The Set Electronic V_R Register command sets the display density of the LCD screen. Setting the 6-bit Electronic V_R Register determines the liquid crystal drive power supply level output by the built-in liquid crystal power supply's contrast control circuit. There are 64 possible voltage levels. The 64 display density levels vary from 00H (the lightest) to 3FH (the darkest).

- Sequence for setting Electronic V_R Register



18. Display Double-Size (three-byte command)

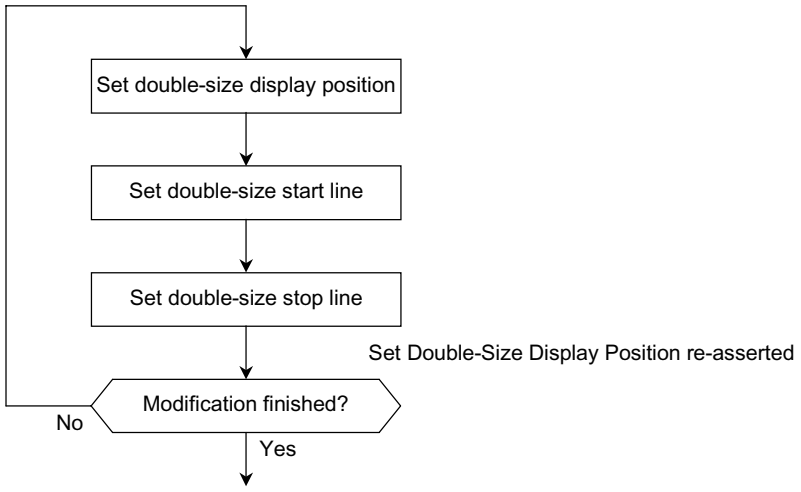
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	1	0	0	0	Normal Display
0	1	0	1	0	1	0	1	0	0	1	Set Double-Size Display Position
0	1	0	*	*	Double-size start line (0 to 63)						Set Double-Size Start Line
0	1	0	*	*	Double-size stop line (0 to 63)						Set Double-Size Stop Line

*: Invalid

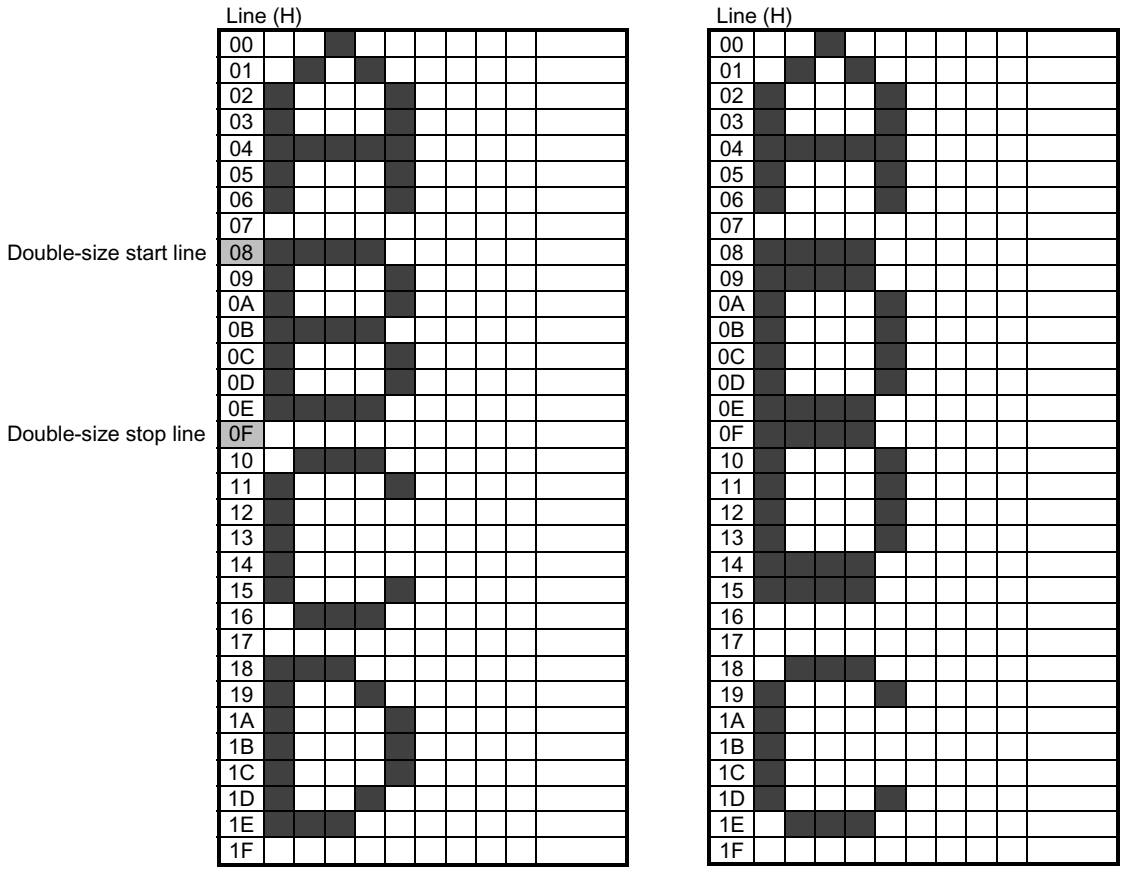
This command consists of three bytes: the first is the Set Double-Size Display Position byte, the second is the Set Double-Size Start Line byte, and the third is the Set Double-Size Stop Line byte. Ensure that the three parts of the command are input in the proper sequence. (Note that the Normal Display command is a 1-byte command.) Once the Set Double-Size Display Position command has been input, no command other than Set Double-Size Start Line can be used. The device is then freed from this state when the double-size start and stop lines are set.

This command sets the range of the display in which double-size characters can be shown. Use line addresses to set the range, the Set Double-Size Start Line byte to set the start position, and the Set Double-Size Stop Line byte to set the end position. The maximum number of lines that can be set is 16.

- Sequence for setting double-size display position



Example: Double-size display (double-size start line = 08H, double-size stop line = 0FH)



19. Set Alternating Period

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	FRS	*	Alternation period	

This command can be used to set the interval at which the polarity of the (alternating) frame signal is switched over. This is set as a number of lines.

FRS = 1: The frame signal is inverted using the specified interval (in lines).

FRS = 0: This setting selects Test Mode. Do not use it.

D1	D0	
0	0	Sub-group of 16
0	1	Sub-group of 32
1	0	Sub-group of 48
1	1	Sub-group of 64

20. Write to Display RAM in Burst (two-byte command)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	1	0	0	1	0	1	Set Display RAM Burst Write
0	1	0	Burst write data								Set Burst Write Data

This command consists of two bytes, the Set Display RAM Burst Write byte, and the Set Burst Write Data byte. Ensure that the two bytes are input in the proper sequence. Once the Set Display RAM Burst Write command has been input, no command other than Set Burst Write Data can be used. The device is then freed from this state when the burst write data is set.

This command rewrites the entire contents of the display RAM using 8-bit burst write data. The execution time of this command is CL × 17 clock periods. The device is in Busy state during this time, and no command can be accepted. Thus the device's status should be read to ascertain whether it is busy (B = 0). If this check is not performed, a wait time of greater than the specified execution time will be required.

21. NOP

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

This command is the No Operation command.

22. Test Mode

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	Test Mode			

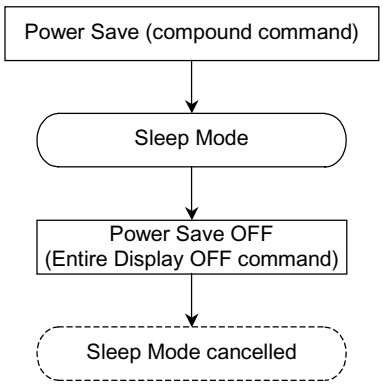
This command selects Test Mode. Do not use it. If this command is invoked inadvertently, it should be cancelled. This can be done by pulling the /RST input low or by executing a Reset or NOP command.

23. Power Save (compound command)

If the Entire Display ON command is executed while the display is off, the device will enter Power Save Mode, in which the device's current consumption can be greatly reduced.

In Power Save Mode, the display data and the previous operating mode are retained. In addition, the MPU can still access the display RAM.

To exit Power Save Mode, use the Entire Display OFF command.



- Sleep Mode

  The entire LCD display system stops operating. Unless the device is accessed by the MPU, the device's power consumption can be reduced to near its inactive-state level. The internal state of the device while it is in Sleep Mode is shown below.

  1) The oscillation circuit and the LCD power supply circuit are turned off.

  2) The entire LCD drive circuit is turned off. The segment and common driver output pins output the V_{SS}-level voltage.

Note 3: If an external power supply is being used, Toshiba recommends that the function of the external power supply circuit be turned off when Power Save Mode is invoked. For example, if each level of LCD drive voltage is provided by an external-resistor divider circuit, Toshiba recommends that a circuit be added to cut the current flowing into the resistor divider circuit when Power Save Mode is invoked. The T6K19 has an LCD-blanking control pin, /DOF, which goes Low when Power Save Mode is invoked.
The /DOF output can be used to stop the external power supply circuit from functioning.

Note 4: If the device is powered on in Master Mode, the oscillation circuit will start oscillating immediately. The oscillation circuit cannot be turned off and will run continuously (except in Sleep Mode).

24. Reset Circuit

When the input to the /RST pin is pulled Low, the T6K19 is reset. All its internal circuits (register contents) will be initialized as shown below.

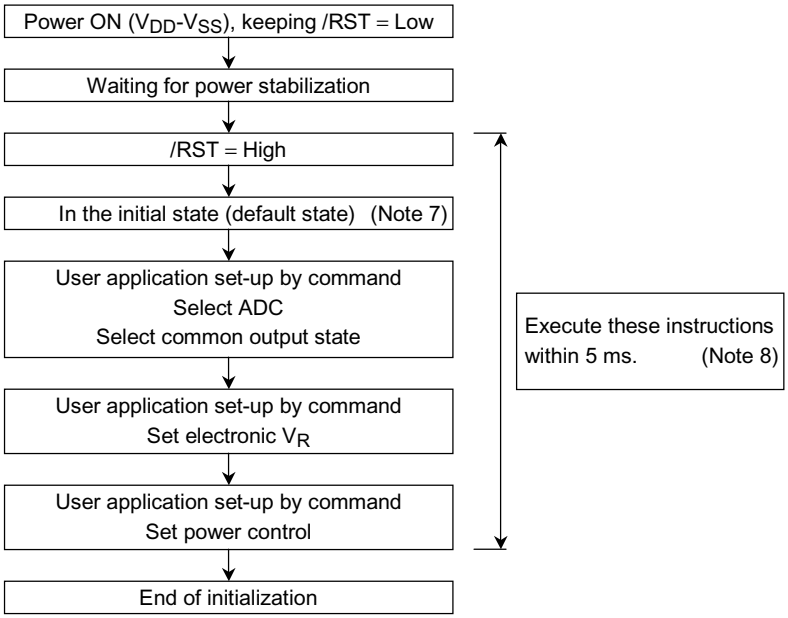
(1)	Display ON/OFF:	OFF
(2)	Normal/reverse display:	Reverse
(3)	ADC select:	Normal
(4)	Power control:	DC OFF, V_{DC} OFF, V_F OFF (D2, D1, D0) = (0, 0, 0)
(5)	Serial interface register data:	The register, which holds 8-bit parallel data converted from serial data, is cleared.
(6)	Entire display ON/OFF:	OFF
(7)	Read-Modify-Write:	OFF
(8)	Display start line:	Line address = 0H
(9)	Column address:	Column address = 0H
(10)	Page address:	Page address = 0H
(11)	$+V_r$ output voltage adjustment width:	(D2, D1, D0) = (0, 0, 0)
(12)	Electronic V_R Mode:	OFF
	Electronic V_R Register:	(D5, D4, D3, D2, D1, D0 = 1, 0, 0, 0, 0, 0)
(13)	Test Mode:	OFF

When an internal RESET command is executed, only settings (7) to (13) are initialized.

Note 5: If the power supply is on, the MPU should use a system reset (/RST = Low), since the internal circuits of the T6K19 are unstable.
If the control signals from the MPU are in High-Impedance state, large currents will flow in the device. Therefore, Toshiba recommends that a circuit be added to ensure that none of the device's input pins are in High-Impedance state while the power supply is on.

- Sequence or referential instruction set-up

(1) Initialization

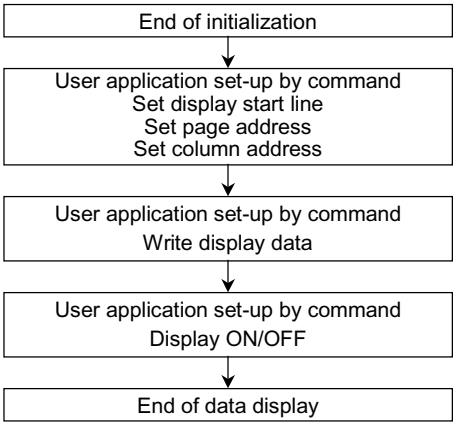


Note 6: If the smoothing capacitors for the LCD drive power supply ($+V_r$ and V_m) retain voltage while the power supply is on, the display may darken for an instant.
Toshiba recommends use of the above power-on sequence in order to prevent this malfunction.

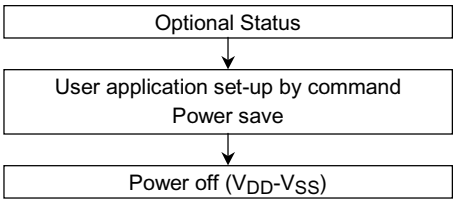
Note 7: See command definitions (reset circuit)

Note 8: The execution time of an instruction depends on the characteristics of the LCD panel and the ratings of the smoothing capacitors. Toshiba recommends that the operation of the LCD panel be checked.

(2) Data display



(3) Power OFF



Note 9: Please turn the built-in power supply circuits off before turning the T6K19's power supply off. If the IC's power supply is turned while the built-in power supply circuits are on, voltage is applied to the built-in LCD drive circuits for an instant. Thus, occasionally, the LCD panel may malfunction. Please use the above power-off sequence in order to prevent this malfunction.

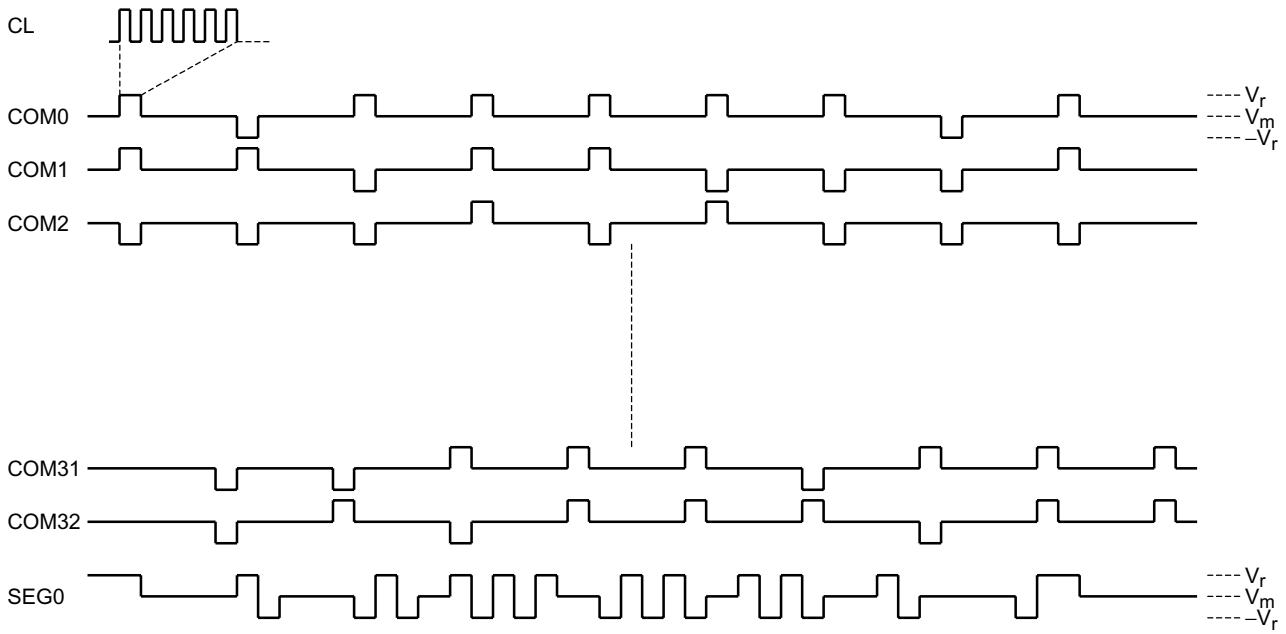
Display Ram Map

Page Address D3	D2	D1	D0	Data										Line Address	COM OUT
0	0	0	0	D0	■	■	■	■	■					00H	COM0
				D1			■							01H	COM1
				D2			■							02H	COM2
				D3			■							03H	COM3
				D4			■					Page 0		04H	COM4
				D5			■							05H	COM5
				D6			■							06H	COM6
				D7										07H	COM7
0	0	0	1	D0		■	■	■						08H	COM8
				D1	■				■					09H	COM9
				D2	■				■					0AH	COM10
				D3	■				■					0BH	COM11
				D4	■				■			Page 1		0CH	COM12
				D5	■				■					0DH	COM13
				D6		■	■	■						0EH	COM14
				D7										0FH	COM15
0	0	1	0	D0		■	■	■	■					10H	COM16
				D1	■									11H	COM17
				D2	■									12H	COM18
				D3		■	■	■						13H	COM19
				D4					■			Page 2		14H	COM20
				D5					■					15H	COM21
				D6	■	■	■	■						16H	COM22
				D7										17H	COM23
0	0	1	1	D0	■				■					18H	COM24
				D1	■				■					19H	COM25
				D2	■				■					1AH	COM26
				D3	■	■	■	■	■					1BH	COM27
				D4	■				■			Page 3		1CH	COM28
				D5	■				■					1DH	COM29
				D6	■				■					1EH	COM30
				D7										1FH	COM31
0	1	0	0	D0		■	■	■						20H	
				D1			■							21H	
				D2			■							22H	
				D3			■							23H	
				D4			■					Page 4		24H	
				D5			■							25H	
				D6		■	■	■						26H	
				D7										27H	
0	1	0	1	D0	■	■	■	■						28H	
				D1	■				■					29H	
				D2	■				■					2AH	
				D3	■	■	■	■						2BH	
				D4	■				■			Page 5		2CH	
				D5	■				■					2DH	
				D6	■	■	■	■						2EH	
				D7										2FH	
0	1	1	0	D0		■	■	■						30H	
				D1	■				■					31H	
				D2	■				■					32H	
				D3	■				■					33H	
				D4	■	■	■	■	■			Page 6		34H	
				D5	■				■					35H	
				D6	■				■					36H	
				D7	■				■					37H	
0	1	1	1	D0										38H	
				D1										39H	
				D2			■							3AH	
				D3	■		■		■					3BH	
				D4		■	■	■				Page 7		3CH	
				D5	■		■		■					3DH	
				D6			■							3EH	
				D7										3FH	
1	0	0	0	D0								Page 8		3FH	COMS

ADC	D0 = "0"	00	01	02	03	04	05	06	07	08		7B	7C	7D	7E	7F	80	81	82	83	Column Address
	D0 = "1"	83	82	81	80	7F	7E	7D	7C	7B		08	07	06	05	04	03	02	01	00	
LCD OUT		SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8		SEG23	SEG24	SEG25	SEG26	SEG27	SEG28	SEG29	SEG30	SEG31	

LCD Drive Waveform

Example: display data = "checkers pattern"



Maximum Ratings (Unless Otherwise Noted, referenced to V_{SS} = 0 V, Ta = 25°C)

Characteristics	Symbol	Rating	Unit	Remark
Power supply voltage (1)	V_{DD}	−0.3 to 7.0	V	(Note 10)
Power supply voltage (2)	$+V_r$, V_m, $-V_r$	−0.3 to 7.0	V	(Note 11)
Input voltage	V_{IN}	−0.3 to V_{DD} + 0.3	V	(Note 10), (Note 12)
Output voltage	V_O	−0.3 to V_{DD} + 0.3	V	(Note 10), (Note 13)
Operating temperature	T_{opr}	−20 to 85	°C	—
Storage temperature	T_{stg}	−55 to 155	°C	—

Note 10: Referenced to V_{SS} = 0 V

Note 11: The condition $+V_r \geqq V_m \geqq -V_r \geqq V_{SS}$ must always met.

Note 12: Applies to all data bus pins and Input pins except $+V_r$, V_m and $-V_r$.

Note 13: Applies to all data bus pins and output pins except V_{OUT}.

Note 14: If the device exceeds its absolute maximum ratings, it may not only break down but also become unreliable and prone to malfunction. Thus, Toshiba recommends that, for normal operation, the device be used within the ranges specified for the device electrical characteristics, as shown on the next page.

Electrical Characteristics

DC Characteristics (1)

Test Conditions (Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 3.0 V, $+V_r$ = 5.0 V and Ta = –20°C to 85°C)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Pin Name
Power supply voltage (1)		V_{DD}	—	—	2.4	—	3.3	V	V_{DD}
Power supply voltage (2)		$+V_r$	—	—	2.5	—	5.0	V	$+V_r$
Input voltage	High level	V_{IH}	—	—	0.8 V_{DD}	—	V_{DD}	V	(Note 15)
	Low level	V_{IL}	—	—	0	—	0.2 V_{DD}	V	
Output voltage	High level	V_{OH}	—	I_{OH} = –400 μA	V_{DD} – 0.2	—	V_{DD}	V	(Note 16)
	Low level	V_{OL}	—	I_{OL} = 400 μA	0	—	0.2	V	
Segment driver ON-resistance		Rcol	—	$\lvert +V_r - (-V_r) \rvert$ = 2.5 V Current load = ±100 μA	—	—	5.0	kΩ	SEG0 to SEG131
Common driver ON-resistance		Rrow	—	$\lvert +V_r - (-V_r) \rvert$ = 2.5 V Current load = ±100 μA	—	—	1.5	kΩ	COM0 to COM31
Accuracy of liquid crystal power supply output voltage		V_{off}	—	—	–100	—	100	mV	$+V_r$, $-V_r$, CMOS (Note 17)
Input leakage current		I_{IL}	—	V_{IN} = V_{DD} to V_{SS}	–1	—	1	μA	(Note 18)
Output leakage current		I_{OL}	—		–3	—	1	μA	(Note 19)
Operating frequency		f_{OSC}	—	—	18.7	23.0	—	kHz	—
External clock frequency		fCL_{ex}	—	—	18.7	23.0	—	kHz	—
External clock duty cycle		fCL_{duty}	—	—	45	50	55	%	—
External clock rise/fall times		t_r/t_f	—	—	—	—	25	ns	—

Note 15: Pins D0 to D5, D6 (SCL), D7 (SI), A0, /RD (E), /WR (R/W), /CS1, CS2, /RST, P/S, C86, CLS, M/S, CL, FR, /DOF, /RS, /HPM and V_R

Note 16: Pins D0 to D7, FR, /DOF and CL

Note 17: Pins $+V_r$ and V_m

Note 18: Pins A0, /RD (E), /WR (R/W), /CS1, CS2, /RST, P/S, C86, CLS, M/S, IRS and /HPM

Note 19: Applies to pins D0 to D5, D6 (SCL), D7 (SI), CL, FR and /DOF when these pins are in High-Impedance state.

DC Characteristics (2)

Test conditions (Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 3.0 V, $+V_r$ = 5.0 V and Ta = –20°C to 85°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Pin Name
DC-DC converter input voltage	V_{IN}	—	(relative to V_{SS})	1.5	—	2.7	V	V_{IN}
DC-DC converter output voltage (Note 20)	V_{OUT}	—	—	5.3	—	5.4	V	V_{OUT}
Voltage-regulating circuit operating voltage	$+V_r$	—	—	2.5	—	5.0	V	$+V_r$
Reference voltage	V_{DC}	—	—	—	1.6	—	V	V_{DC}

Note 20: V_{DD} = 3.0 V, V_{IN} = 2.7 V, DC-DC = ON, CAP+ to CAP– = 1.0 μF, f_{OSC} = 23.0 kHz, Ta = 25°C, I_{LOAD} = 30 μA

DC Characteristics (3)

Test conditions (Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 3.0 V, $+V_r$ = 5.0 V and Ta = –20°C to 85°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Pin Name
Current consumption (1)	I_{SS1}	—	(Note 21)	—	29.0	—	μA	V_{SS}
Current consumption (2)	I_{SS2}	—	(Note 22)	—	19.3	—	μA	V_{SS}
Current consumption (3)	I_{SSSTB}	—	(Note 23)	–1	—	1	μA	V_{SS}

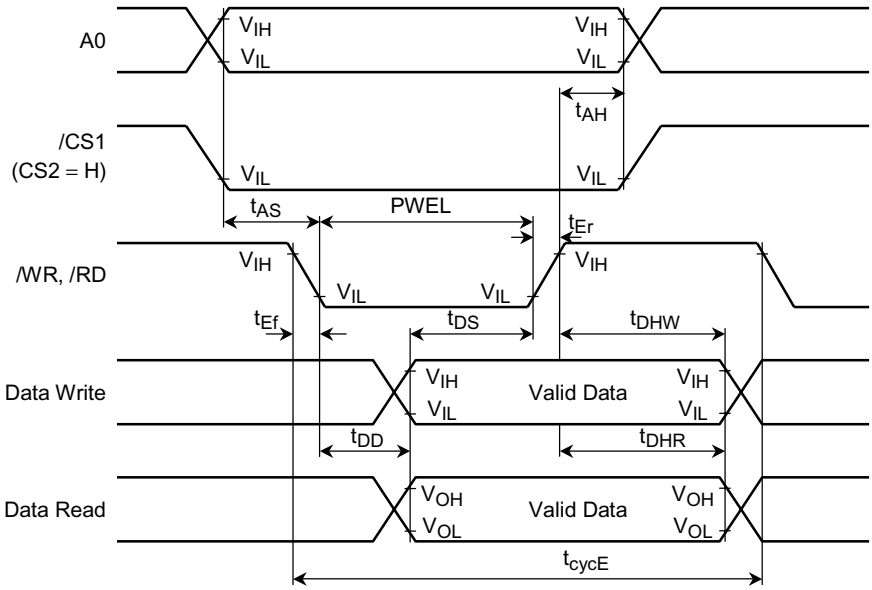
Note 21: V_{DD} = 3.0 V, ×2 step-up (C = 0.1 μF), DC-DC = ON, DC-DC converter regulator = ON, V/F = ON, Ta = 25°C, display (all-white), no interface access.

Note 22: V_{DD} = 3.0 V, V_{CC} = 3.0 V, DC-DC = OFF, DC-DC converter regulator = OFF, V/F = ON, Ta = 25°C, display (all-white), no interface access.

Note 23: Sleep Mode, V_{DD} = 3.0 V, Ta = 25°C

AC Characteristics (1)

Switching Characteristics (80 Series MPU 8-bit interface)



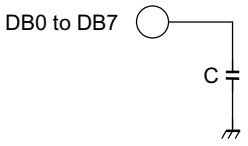
Test Conditions

(Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 2.4 V to 2.7 V, $+V_r$ = 5.5 V and Ta = –20°C to 85°C)

Characteristics	Symbol	Min	Max	Unit
Enable cycle time	t_{cycE}	1000	—	ns
Enable pulse width	PWEL	240	—	ns
Enable rise/fall time	t_{Er}, t_{Ef}	—	15	ns
Address set-up time	t_{AS}	0	—	ns
Address hold time	t_{AH}	0	—	ns
Data set-up time	t_{DS}	80	—	ns
Write data hold time	t_{DHW}	30	—	ns
Data delay time	t_{DD} (Note 24)	—	500	ns
Data hold time	t_{DHR} (Note 24)	100	—	ns

Note 24: Values of t_{DD} and t_{DHR} are shown for when the load circuit shown below is connected.

Load Circuit



C = 100 pF

(including wiring capacitance)

Test Conditions

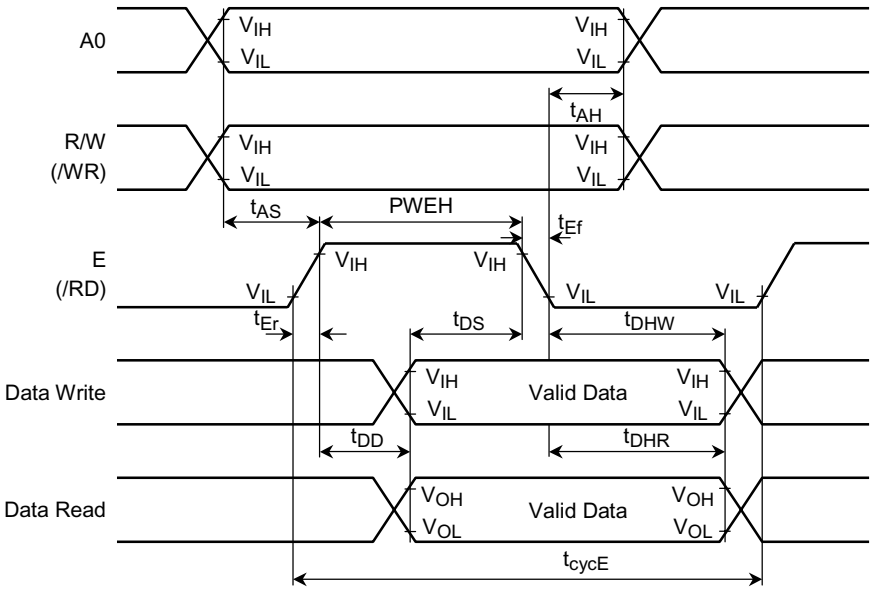
(Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 2.7 V to 3.3 V, +V_r = 5.5 V and Ta = –20°C to 85°C)

Characteristics	Symbol	Min	Max	Unit
Enable cycle time	t_{cycE}	300	—	ns
Enable pulse width	PWEL	100	—	ns
Enable rise/fall time	t_{Er}, t_{Ef}	—	15	ns
Address set-up time	t_{AS}	0	—	ns
Address hold time	t_{AH}	0	—	ns
Data set-up time	t_{DS}	50	—	ns
Write data hold time	t_{DHW}	20	—	ns
Data delay time	t_{DD} (Note 24)	—	140	ns
Data hold time	t_{DHR} (Note 24)	50	—	ns

Note 24: Values of t_{DD} and t_{DHR} are shown for when the load circuit shown above is connected.

AC Characteristics (2)

Switching Characteristics (68 Series MPU 8-bit interface)



Note 26: /CS1 = L, CS2 = H

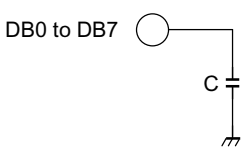
Test Conditions

(Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 2.4 V to 2.7 V, $+V_r$ = 5.5 V and Ta = –20°C to 85°C)

Characteristics	Symbol	Min	Max	Unit
Enable cycle time	t_{cycE}	1000	—	ns
Enable pulse width	PWEH	240	—	ns
Enable rise/fall time	t_{Er}, t_{Ef}	—	15	ns
Address set-up time	t_{AS}	0	—	ns
Address hold time	t_{AH}	0	—	ns
Data set-up time	t_{DS}	80	—	ns
Write data hold time	t_{DHW}	30	—	ns
Data delay time	t_{DD} (Note 24)	—	500	ns
Data hold time	t_{DHR} (Note 24)	100	—	ns

Note 24: Values of t_{DD} and t_{DHR} are shown for when the load circuit shown below is connected.

Load Circuit



C = 100 pF

(including wiring capacitance)

Test Conditions

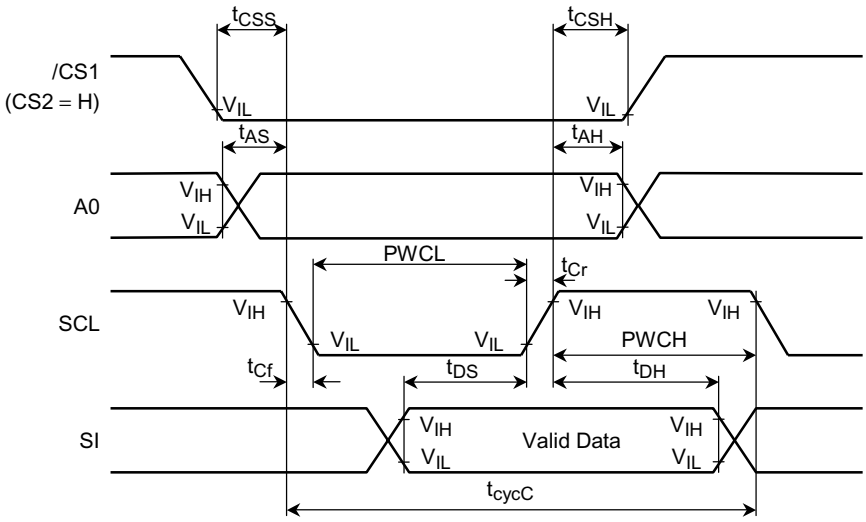
(Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 2.7 V to 3.3 V, $+V_r$ = 5.5 V and Ta = –20°C to 85°C)

Characteristics	Symbol	Min	Max	Unit
Enable cycle time	t_{cycE}	300	—	ns
Enable pulse width	PWEH	100	—	ns
Enable rise/fall time	t_{Er}, t_{Ef}	—	15	ns
Address set-up time	t_{AS}	0	—	ns
Address hold time	t_{AH}	0	—	ns
Data set-up time	t_{DS}	50	—	ns
Write data hold time	t_{DHW}	20	—	ns
Data delay time	t_{DD} (Note 24)	—	140	ns
Data hold time	t_{DHR} (Note 24)	50	—	ns

Note 24: Values of t_{DD} and t_{DHR} are shown for when the load circuit shown above is connected.

AC Characteristics (3)

Serial Interface Write Characteristics



Test Conditions

(Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 2.4 V to 2.7 V, $+V_r$ = 5.5 V and Ta = –20°C to 85°C)

Characteristics	Symbol	Min	Max	Unit
Enable cycle time	t_{cycC}	400	—	ns
Enable pulse width	PWCL, PWCH	150	—	ns
Enable rise/fall time	t_{Cr}, t_{Cf}	—	15	ns
CS set-up time	t_{CSS}	250	—	ns
CS hold time	t_{CSH}	250	—	ns
Address set-up time	t_{AS}	0	—	ns
Address hold time	t_{AH}	250	—	ns
Data set-up time	t_{DS}	150	—	ns
Data hold time	t_{DH}	150	—	ns

Test Conditions

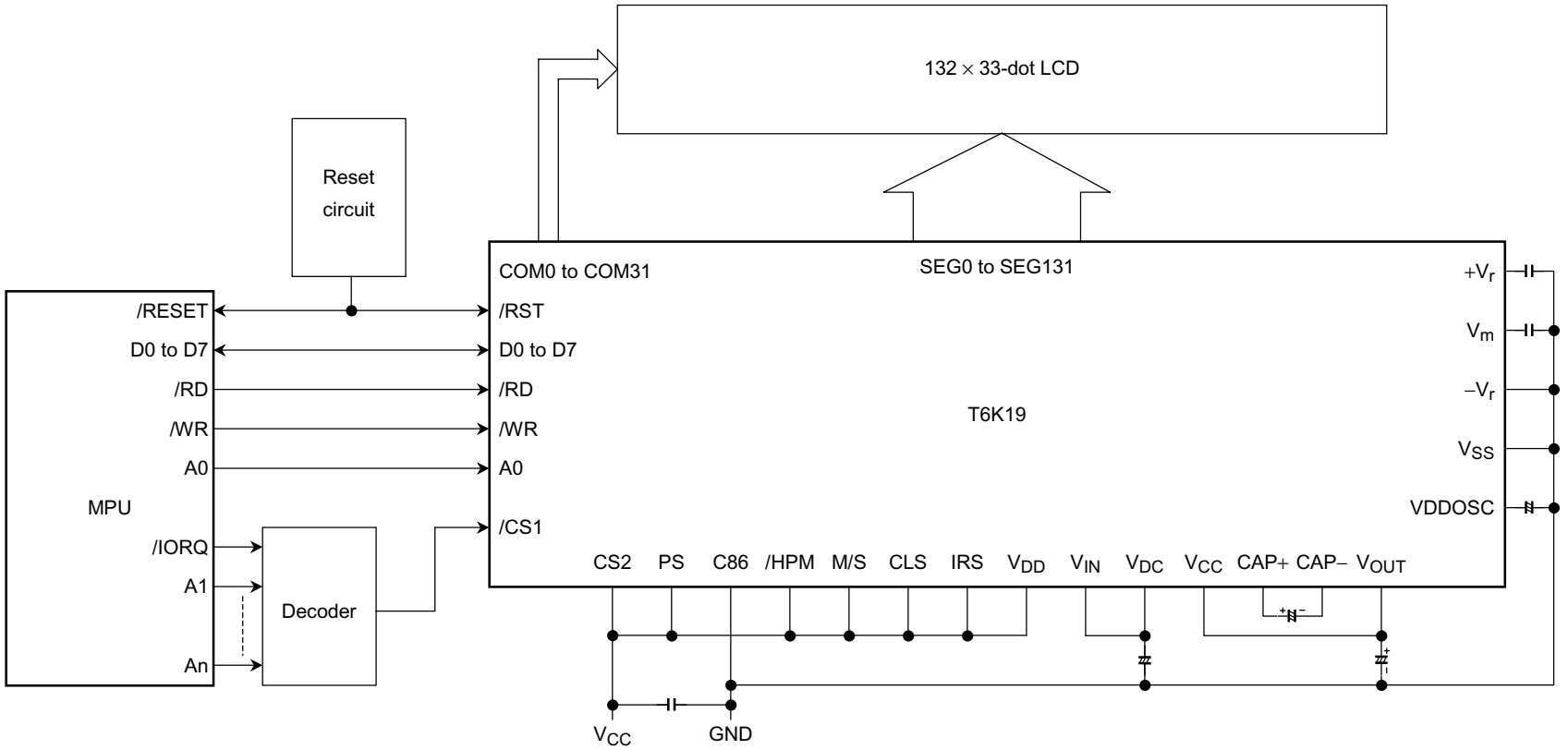
(Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 3.3 V to 4.5 V, $+V_r$ = 5.5 V and Ta = –20°C to 85°C)

Characteristics	Symbol	Min	Max	Unit
Enable cycle time	t_{cycC}	250	—	ns
Enable pulse width	PWCL, PWCH	100	—	ns
Enable rise/fall time	t_{Cr}, t_{Cf}	—	15	ns
CS set-up time	t_{CSS}	150	—	ns
CS hold time	t_{CSH}	150	—	ns
Address set-up time	t_{AS}	0	—	ns
Address hold time	t_{AH}	150	—	ns
Data set-up time	t_{DS}	100	—	ns
Data hold time	t_{DH}	100	—	ns

Application Circuit (1)

T6K19 Single-Chip Mode

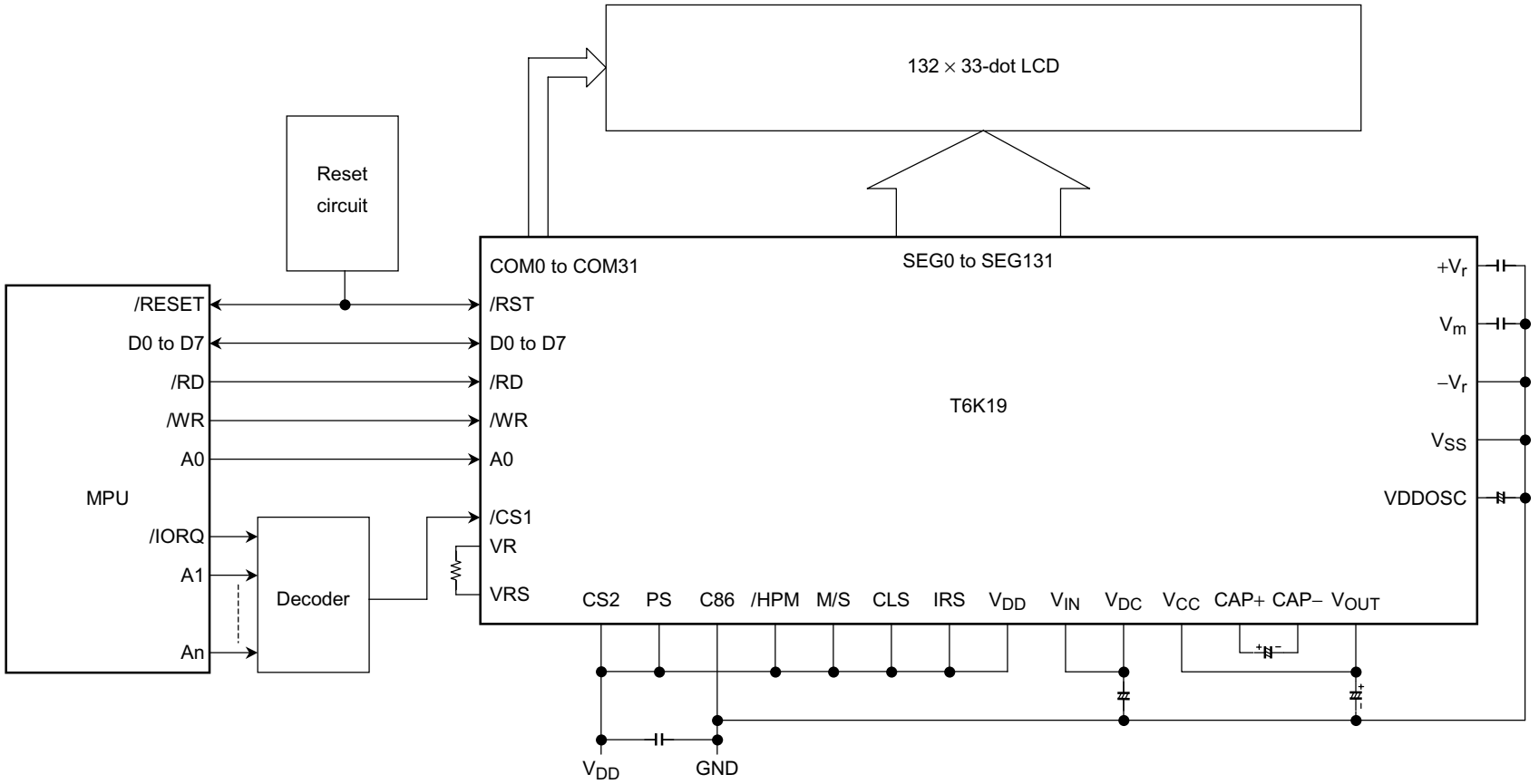
- Master Mode
- Using on-chip oscillator
- Using DC-DC converter
- Using 8-bit parallel MPU interface



Application Circuit (2)

T6K19 Single-Chip Mode

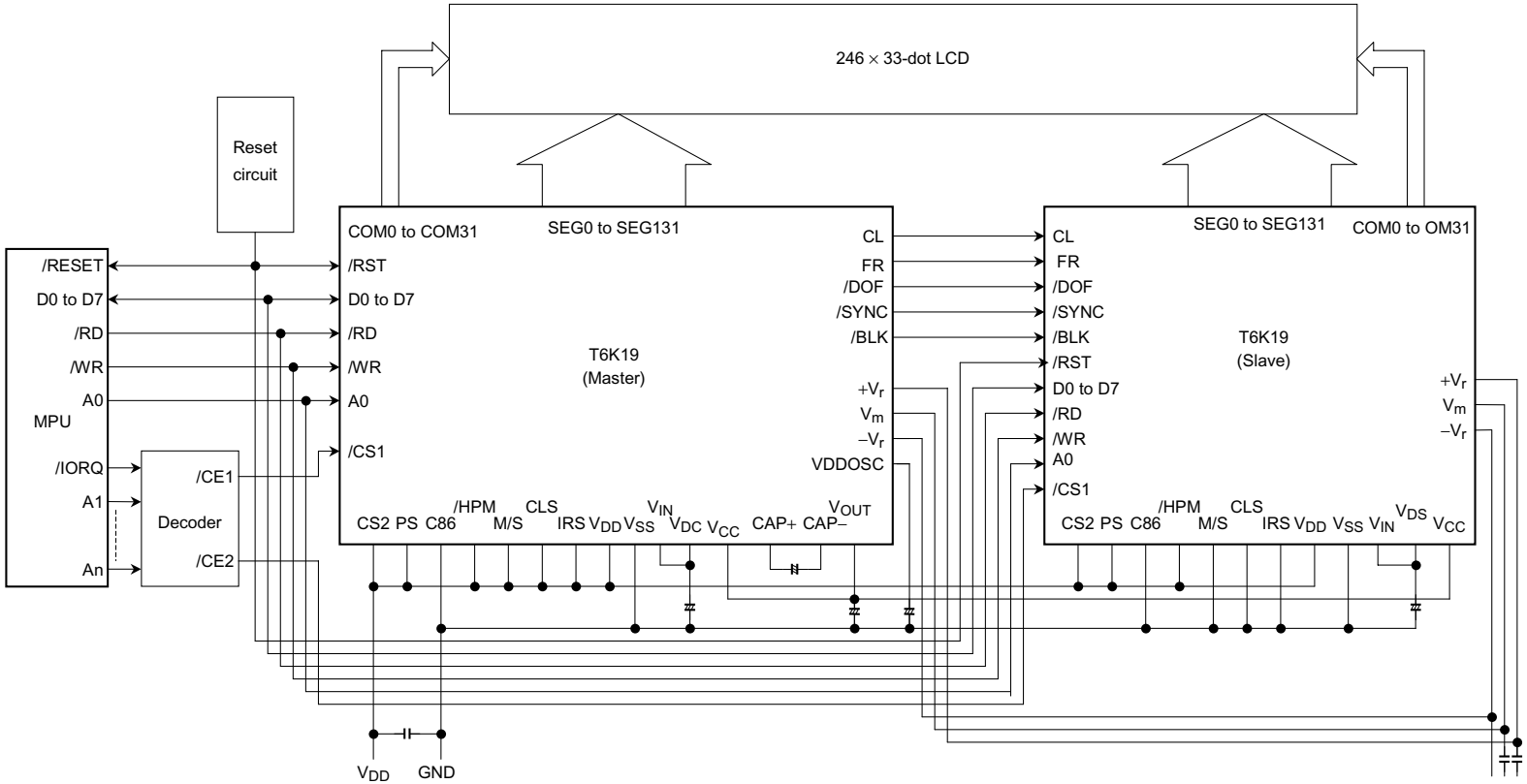
- Master Mode
- Using on-chip oscillator
- Using DC-DC converter
- Using 8-bit parallel MPU interface
- Not using built-in resistance for +VR voltage adjustment (IRS = L)



Application Circuit (3)

T6K19 Dual-Chip Mode

- Using on-chip oscillator
- Using DC-DC converter
- Using 8-bit parallel MPU interface



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