TOSHIBA Bipolar Linear Integrated Circuit Silicon Monolithic

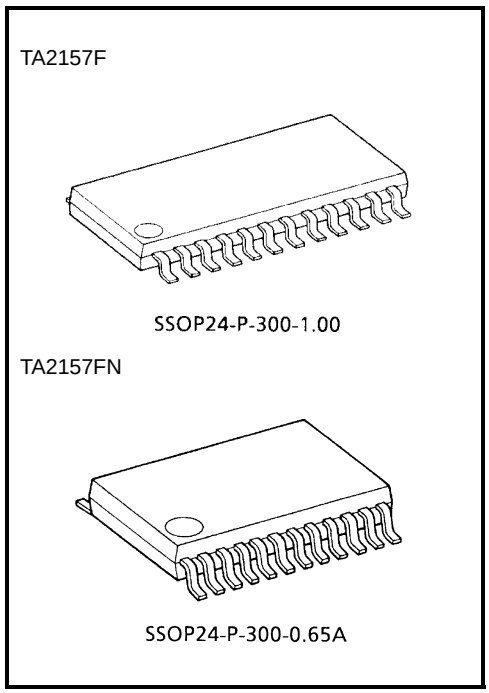
TA2157F,TA2157FN

Digital Servo Head Amp for CD System

TA2157F/FN is a digital servo head amp for a 3-beam pickup used in CD systems.

Gain for RF signal generation amp can be freely set, supporting CD-RW.

Combining with single-chip processor TC94A14F/FA/FB, a CMOS digital servo, makes configuring CD systems simple.

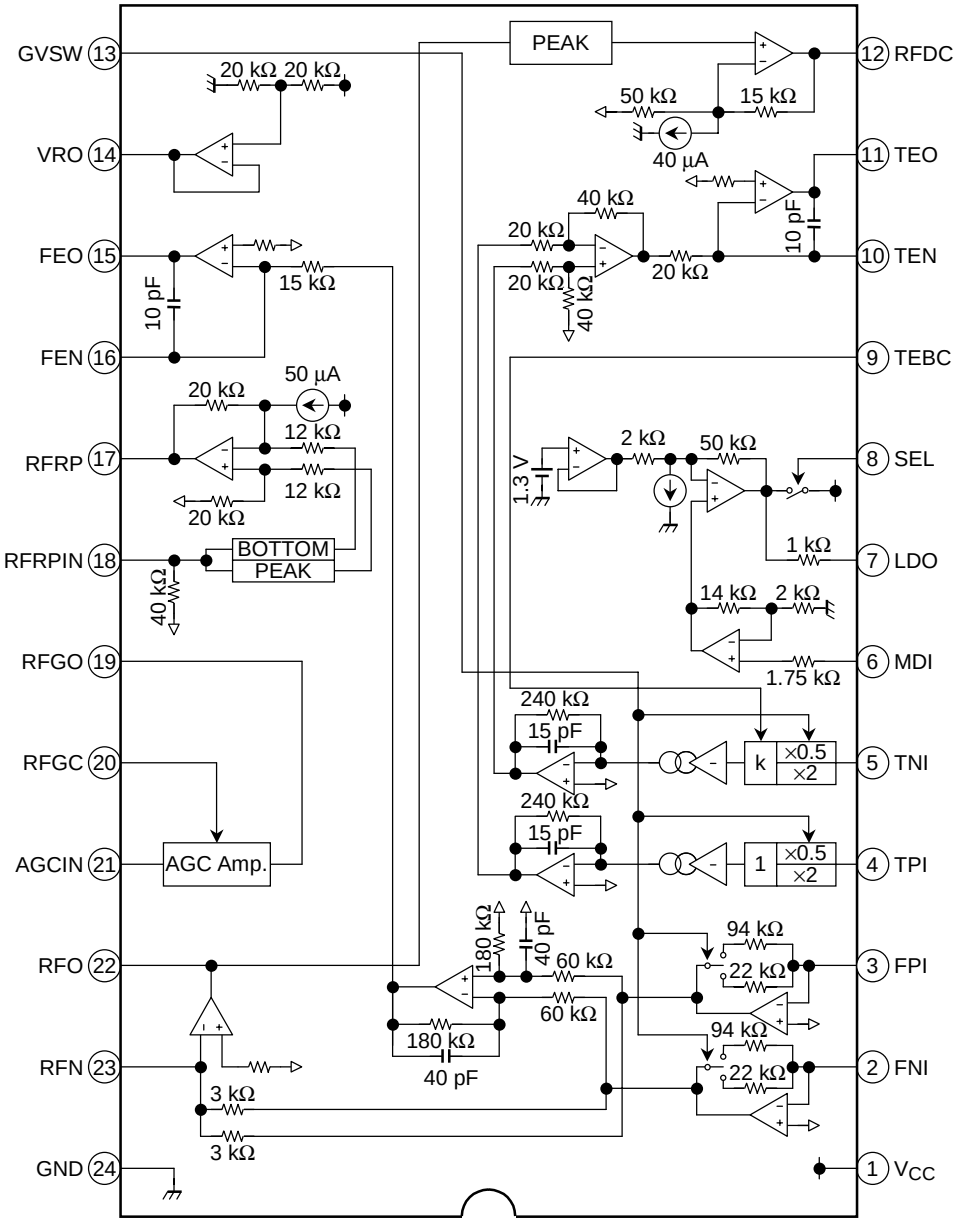


Weight
SSOP24-P-300-1.00: 0.3 g (typ.)
SSOP24-P-300-0.65A: 0.17 g (typ.)

Features

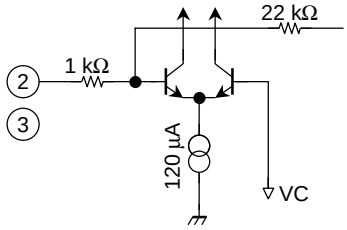
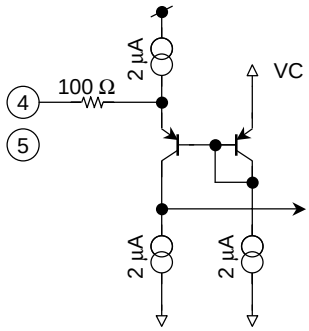
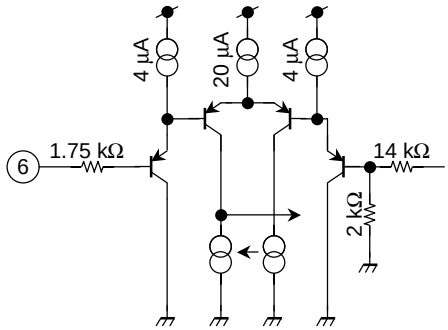
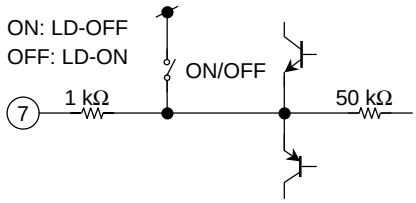
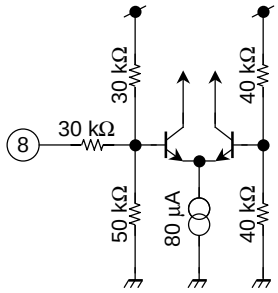
- Low power dissipation digital servo head amp
- Built-in amplifier for generating reference voltage (VRO)
- Built-in auto laser power control (APC) amplifier
- Built-in RF amplifier
- Built-in RF signal automatic gain control (AGC) amplifier
- Built-in gain change circuit for CD-RW
- Built-in focus error and tracking error signal amplifiers
- Built-in track count signal amplifier
- Normal-, double-, and ×4-speed operation
- 24-pin mini flat package

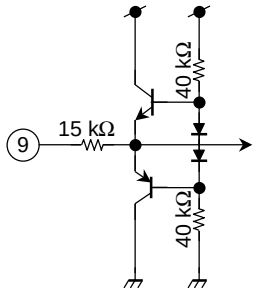
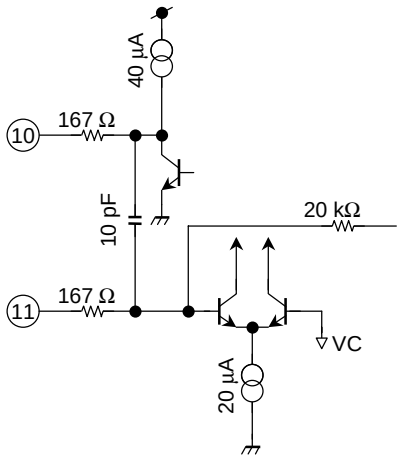
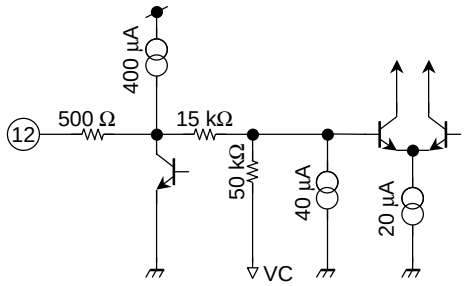
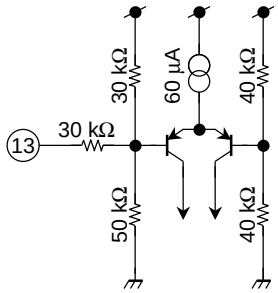
Block Diagram

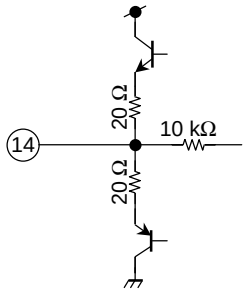
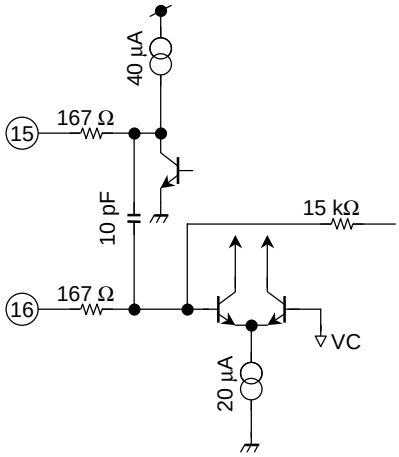
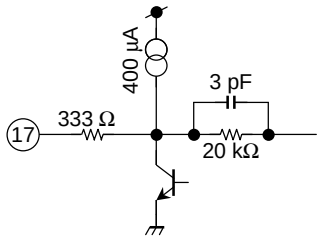
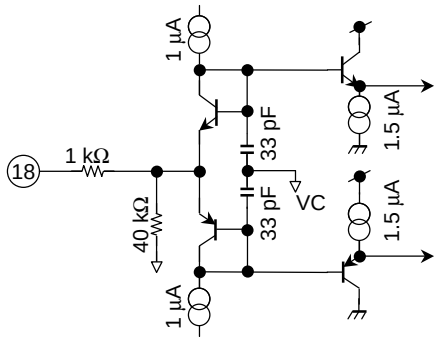


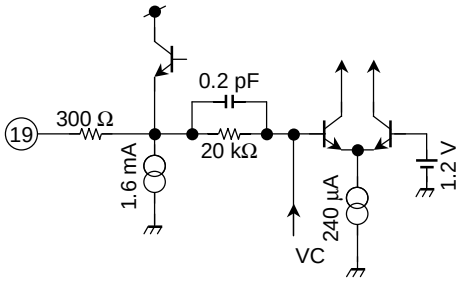
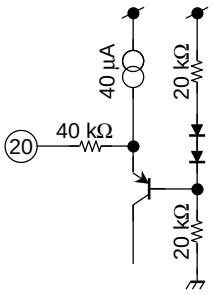
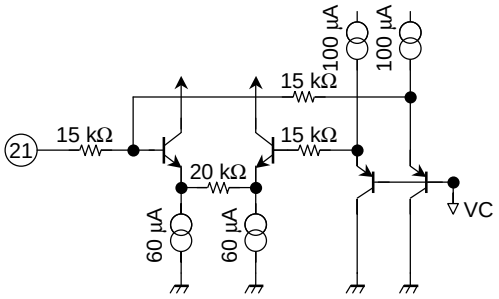
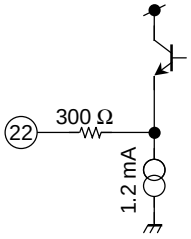
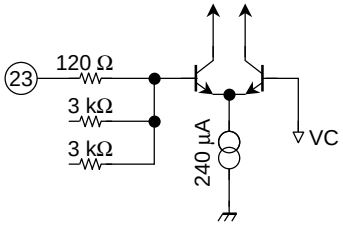
PIN / V_{CTRL}	SEL (APC SW)	TEB (TE BAL)	RFGC (AGC Gain)	GVSW
V_{CC}	APC ON	–50%	+12dB	Normal mode (0dB)
HiZ	APC ON	0%	+6dB	Normal mode (0dB)
GND	APC OFF (LDO = H)	+50%	0dB	CD-RW mode (+12dB)

Pin Function

Pin No.	Symbol	I/O	Function Description	Internal Circuit
1	V_{CC}	—	3.3 V power supply pin	—
2	FNI	I	Main-beam amp input pin	
3	FPI	I	Main-beam amp input pin	
4	TPI	I	Sub-beam amp input pin	
5	TNI	I	Sub-beam amp input pin	
6	MDI	I	Monitor photo diode amp input pin	
7	LDO	O	Laser diode amp output pin	
8	SEL	I	APC circuit ON/OFF control signal, laser diode (LDO) control signal input or bottom/peak detection frequency change pin. SEL: GND — APC Circuit: OFF — LDO: Connected to V_{CC} through 1 kΩ resistor SEL: HiZ — APC Circuit: ON — LDO: Control signal output SEL: V_{CC} — APC Circuit: ON — LDO: Control signal output	

Pin No.	Symbol	I/O	Function Description	Internal Circuit
9	TEBC	I	Tracking error balance adjustment signal input pin Adjusts TE signal balance by eliminating carrier component from PWM signal (3-state output, PWM carrier = 88.2 kHz) output from TC94A14F/FA/FB TEBC pin using RC-LPF and inputting DC. TEBC input voltage: GND~V_{CC}	
10	TEN	I	Tracking error signal generation amp negative-phase input pin	
11	TEO	O	Tracking error signal generation amp output pin. Combining TEO signal and RFRP signal with TC94A14F/FA/FB configures tracking search system.	
12	RFDC	O	RF signal peak detection output pin	
13	GVSW	I	AGC/FE/TE amp gain change pin GVSW: GND, HiZ, V_{CC} Mode: CD-RW, Normal	

Pin No.	Symbol	I/O	Function Description	Internal Circuit
14	VRO	O	Reference voltage (VRO) output pin • VRO = 1/2 V_{CC} when V_{CC} = 3.3 V	
15	FEO	O	Focus error signal generation amp output pin	
16	FEN	I	Focus error signal generation amp negative-phase input pin	
17	RFRP	O	Signal amp output pin for track count Combining RFRP signal and TEO signal with TC94A14F/FA/FB configures tracking search system.	
18	RFRPIN	I	Signal generation amp input pin for track count	

Pin No.	Symbol	I/O	Function Description	Internal Circuit
19	RFGO	O	RF signal amplitude adjustment amp output pin	
20	RFGC	I	RF amplitude adjustment control signal input pin Adjusts RF signal amplitude by eliminating carrier component from PWM signal (3-state output, PWM carrier = 88.2 kHz) output from TC94A14F/FA/FB RFGC pin using RC-LPF and inputting DC. • RFGC input voltage : GND~V_{CC}	
21	AGCIN	I	RF signal amplitude adjustment amp input pin	
22	RFO	O	RF signal generation amp output pin	
23	RFN	I	RF signal generation amp input pin	
24	GND	—	GND pin	—

Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Supply voltage		V_{CC}	5	V
Power dissipation	TA2157F	P_D	600	mW
	TA2157FN		500	
Operating temperature		T_{opr}	–40 ~ +85	°C
Storage temperature		T_{stg}	–55 ~ +150	°C

Note 1: TA2157F: Derated above 25°C in the proportion 4.76 mW/°C.
TA2157FN: Derated above 25°C in the proportion 4 mW/°C.

Electrical Characteristics (unless otherwise specified, V_{CC} = 3.3 V, VRO = 1.65 V, Ta = 25°C, RFGC = VRO, GVSW = V_{CC})

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
Power supply	Assured power supply voltage	V_{CC}	—	—		3.0	3.3	3.6	V
	Power supply current (normal mode)	$I_{CC}1$	—	SEL = HiZ TEBC = HiZ RFGC = HiZ	GVSW = V_{CC}	13	19	25	mA
	Power supply current (CD-RW mode)	$I_{CC}2$			GVSW = GND	12	18	24	
Reference voltage	Reference voltage	VRO	—	When V_{CC} = 3.3 V		1.55	1.65	1.75	V
	Output current	I_{OH}	—	ΔV = –0.1 V		3	—	—	mA
	Input current	I_{OL}		ΔV = +0.1 V		3	—	—	
APC MD → LDO	Voltage gain	G_{VAPC}	—	f = 1 kHz		—	200	—	V/V
	Operating reference voltage	V_{MDI}	—	V_{LDO} = V_{CC} – 1.3 V		170	178	186	mV
	LD off voltage	V_{LDOP}	—	V_{CC} reference, SEL = GND		–0.75	–0.7	—	V
	Input bias current	I_{IAPC}	—	V_{MDI} = 178 mV		–200	–50	0	nA
RF FPI (FNI) → RFO	Transfer resistance 1 (normal mode)	Rt1RF	—	f = 100 kHz Rf = 12 kΩ	GVSW = V_{CC}	74	85	95	kΩ
	Transfer resistance 2 (CD-RW mode)	Rt2RF			GVSW = GND	325	370	414	
	Frequency characteristic 1 (normal mode)	f_{C1RF}	—	–3dB point Rf = 12 kΩ	GVSW = V_{CC}	—	13	—	MHz
	Frequency characteristic 2 (CD-RW mode)	f_{C2RF}			GVSW = GND	—	8	—	
	Output slew rate	SR_{RF}	—	C_{RFO} = 20 pF		—	35	—	V/μs
	Upper limit output voltage	V_{OHRF}	—	GND reference		2.2	2.4	—	V
	Lower limit output voltage	V_{OLRF}				—	0.2	0.4	
	Permissive load resistance	R_{LMRF}	—	—		5	10	—	kΩ

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
AGC AGCI → RFGO	Voltage gain 1	G_{V1AG}	—	f = 1 MHz	RFGC = GND	−1.5	−0.5	0.5	dB
	Voltage gain 2	G_{V2AG}			RFGC = HiZ	5.5	6.5	7.5	
	Voltage gain 3	G_{V3AG}			RFGC = V_{CC}	12	13.5	15	
	Frequency characteristic 1	f_{C1AG}	—	−3dB point	RFGC = GND	—	15	—	MHz
	Frequency characteristic 2	f_{C2AG}			RFGC = HiZ	—	15	—	
	Frequency characteristic 3	f_{C3AG}			RFGC = V_{CC}	—	15	—	
	Output slew rate	SR_{AG}	—	C_{RFO} = 20 pF		—	25	—	V/µs
	Upper limit output voltage	V_{OHAG}	—	GND reference		2.2	2.4	—	V
	Lower limit output voltage	V_{OLAG}				—	0.2	0.4	
	Permissive load resistance	R_{LMAG}	—	—		5	10	—	kΩ
FE FPI (FNI) → FEO	Transfer resistance 1 (normal mode)	Rt1FE	—	f = 1 kHz R_{FIN} = 47 kΩ R_{FEFB} = 33 kΩ	GVSW = V_{CC}	127	145	162	kΩ
	Transfer resistance 2 (CD-RW mode)	Rt2FE			GVSW = GND	545	620	694	
	Gain balance 1 (normal mode)	GB1FE	—	GVSW = V_{CC}, ΔRt1FE		−1	0	+1	dB
	Gain balance 2 (CD-RW mode)	GB2FE		GVSW = GND, ΔRt2FE		−1	0	+1	
	Frequency characteristic 1 (normal mode)	f_{C1FE}	—	−3dB point R_{FEFB} = 33 kΩ	GVSW = V_{CC}	—	20	—	kHz
	Frequency characteristic 2 (CD-RW mode)	f_{C2FE}			GVSW = GND	—	20	—	
	Output offset voltage 1 (normal mode)	V_{OS1FE}	—	VRO reference FPI/FNI open	GVSW = V_{CC}	−50	0	+50	mV
	Output offset voltage 2 (CD-RW mode)	V_{OS2FE}			GVSW = GND	−100	0	+100	
	Upper limit output voltage	V_{OHFE}	—	GND reference		2.9	3.1	—	V
	Lower limit output voltage	V_{OLFE}				—	0.1	0.3	
	Permissive load resistance	R_{LMFE}	—	—		5	10	—	kΩ

Characteristics			Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
TE TPI (TNI) → TEO	Transfer resistance 1 (normal mode)		Rt1TE	—	f = 1 kHz TE_{RFB} = 39 kΩ R_{TIN} = 47 kΩ TEBC = HiZ	GVSW = V_{CC}	411	468	525	kΩ
	Transfer resistance 2 (CD-RW mode)		Rt2TE			GVSW = GND	1647	1872	2092	
	Gain balance adjustment width	H (DA)	ΔRt1	—	GVSW = V_{CC}	TEBC = GND	+40	+50	+60	%
		L (DA)	ΔRt2			TEBC = V_{CC}	−60	−50	−40	
	Gain balance 1 (normal mode)		GB1TE	—	GVSW = V_{CC}, ΔRt1FE		−1	0	+1	dB
	Gain balance 2 (CD-RW mode)		GB2TE		GVSW = GND, ΔRt2FE		−1	0	+1	
	Frequency characteristic 1 (normal mode)		f_{C1TE}	—	−3dB point R_{TEFB} = 39 kΩ	GVSW = V_{CC}	—	40	—	kHz
	Frequency characteristic 2 (CD-RW mode)		f_{C2TE}			GVSW = GND	—	40	—	
	Output offset voltage 1 (normal mode)		V_{OS1TE}	—	VRO reference TPI/TNI open	GVSW = V_{CC}	−50	0	+50	mV
	Output offset voltage 2 (CD-RW mode)		V_{OS2TE}			GVSW = GND	−150	0	+150	
	Upper limit output voltage		V_{OHTE}	—	GND reference		2.9	3.1	—	V
	Lower limit output voltage		V_{OLTE}				—	0.1	0.3	
	Permissive load resistance		R_{LMTE}	—	—		5	10	—	kΩ
RFDC FNI (FPI) → RFDC	Detection frequency		f_{CDC}	—	−3dB point at low-frequency with output amplitude = 0dB when RFO = 1.2 Vpp/350 kHz in relation to V_{OP1DC}		—	15	—	kHz
	Operating reference voltage 1		V_{OP1DC}	—	FNI/FPI open, VRO reference, RFN-Vcc = 47 kΩ		−0.15	0	0.15	V
	Operating reference voltage 2		V_{OP2DC}		VRO reference, RFO = 1.2 Vpp/350 kHz RFN-Vcc = 47 kΩ		0.6	0.75	0.9	
	Upper limit output voltage		V_{OHDC}	—	GND reference		2.9	3.1	—	V
	Lower limit output voltage		V_{OLDC}				—	0.3	0.5	
	Permissive load resistance		R_{LMDC}	—	—		5	10	—	kΩ
RFRP RFRPIN → RFRP	Voltage gain		G_{VRP}	—	AMP gain after detection		—	4.4	—	dB
	Detection frequency		f_{CRP}	—	−3dB point at low-frequency with output amplitude = 0dB when RFO = 1.2 Vpp/700 kHz in relation to V_{OP1RP}		—	35	—	kHz
	Detection time constant		T_{RP}	—	1.2 V_{PP}/5 kHz square wave (Cin > 1 μF)		—	37	—	V/ms
	Operating reference voltage 1		V_{OP1RP}	—	VRO reference, no input		−1.0	−0.85	−0.7	V
	Operating reference voltage 2		V_{OP2RP}		VRO reference, RFO = 700 kHz, 1.2 Vpp		0.7	0.85	1.0	
	Upper limit output voltage		V_{OHRP}	—	GND reference		2.9	3.1	—	V
	Permissive load resistance		R_{LMRP}	—	—		5	10	—	kΩ

Note 2: (DA) : Normal mode

Note 3: If the IC is used abnormally (ex, wrongly mounted), it may be damaged or destroyed.

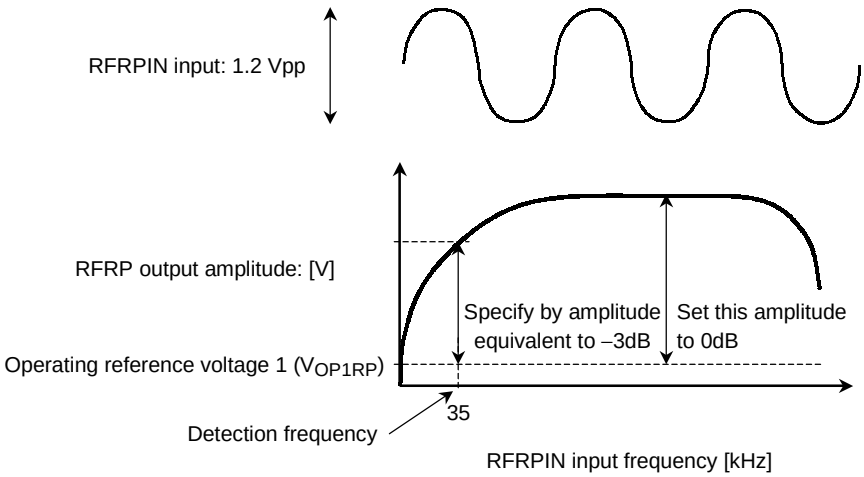
Test Methods (supplementary)

Note: Due to the relation with RFRP detection frequency, use feed search (track cross speed) at 80 kHz or less.

1. Test method for RFRP detection frequency characteristic and detection time constant

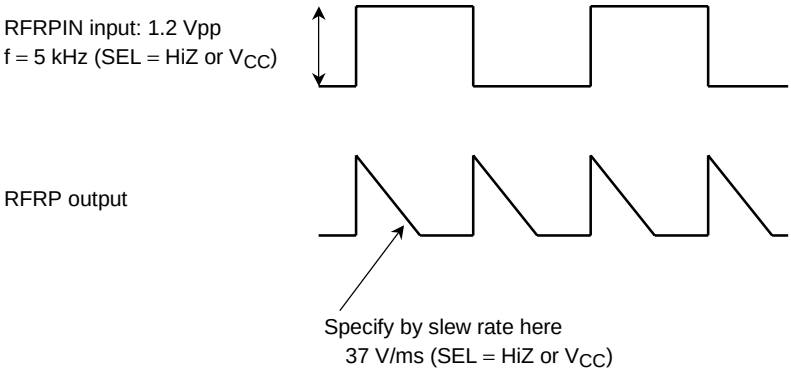
(1) Detection frequency

Set to 0dB the maximum output amplitude of the RFRP pin in relation to the operating reference voltage 1 (V_{OP1RP}) when the sine wave shown in the figure below is input via a capacitor (Cin > 1 μF) to the RFRPIN pin and specify a frequency whose amplitude is –3dB.

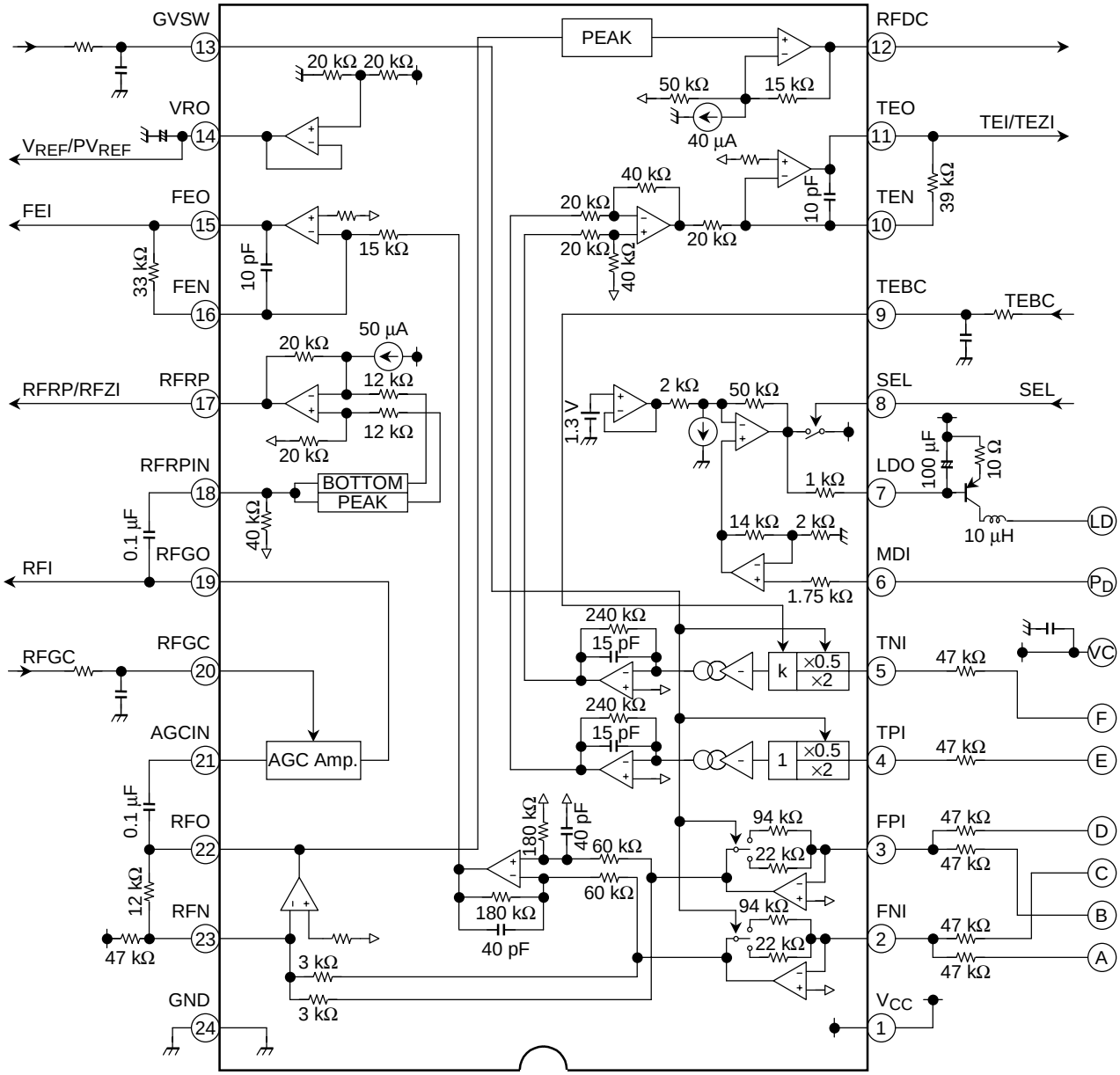


(2) Detection time constant

Specify the time constant for peak and bottom detection frequencies when the square wave shown in the figure below is input via a capacitor (Cin > 1 μF) to the RFRPIN pin at the slew rate of the RFRP pin output sawtooth wave.

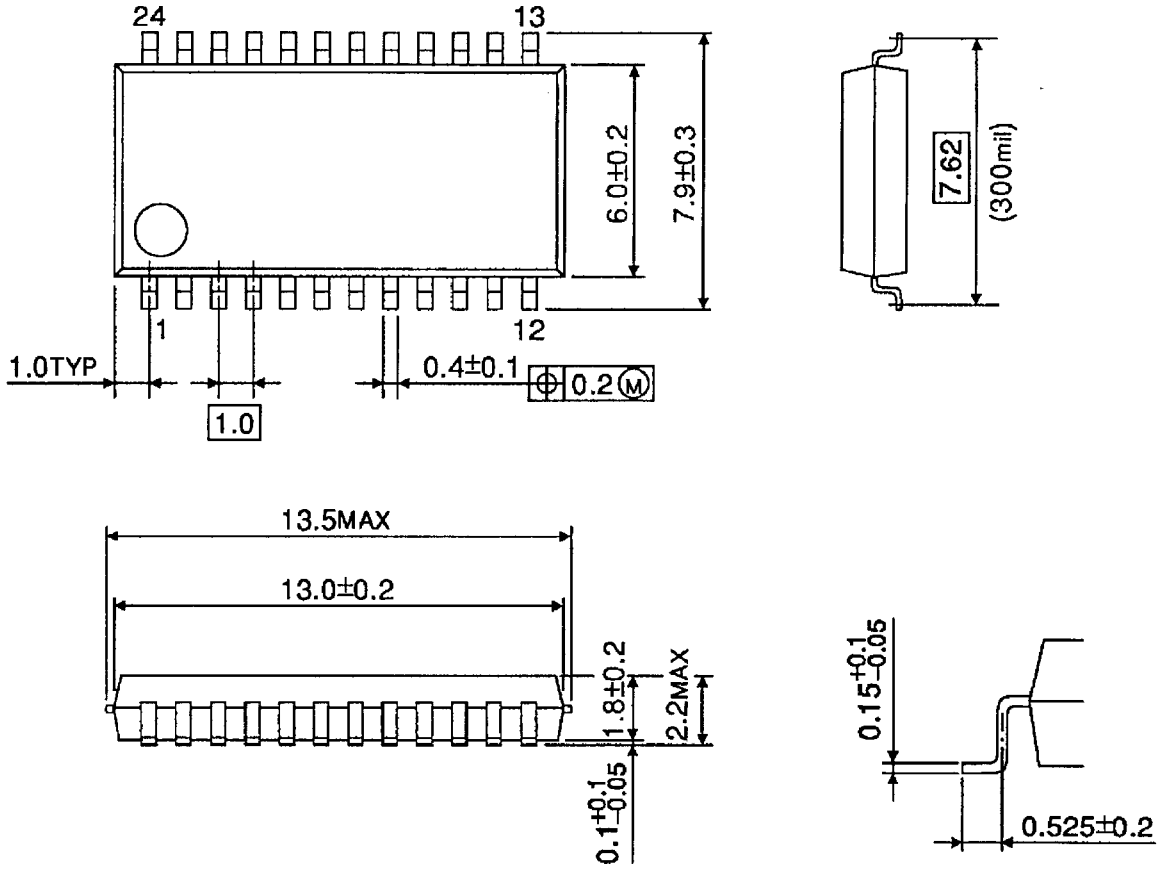


Test Circuit



Package Dimensions

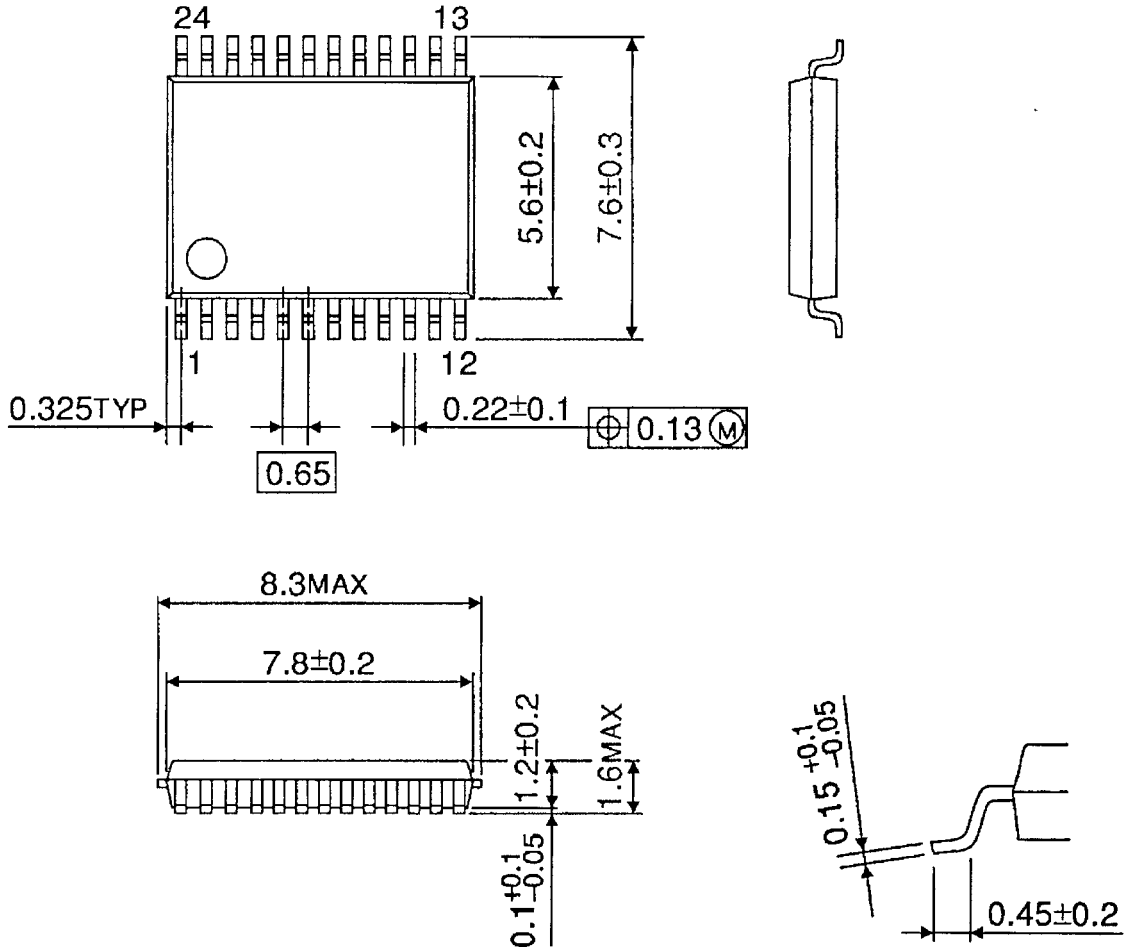
SSOP24-P-300-1.00 Unit : mm



Weight: 0.3 g (typ.)

Package Dimensions

SSOP24-P-300-0.65A Unit : mm



Weight: 0.17 g (typ.)

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