TOSHIBA Field Effect Transistor Silicon P Channel MOS Type

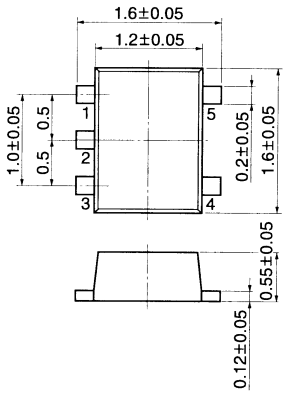
# SSM5P15FE

High Speed Switching Applications

Analog Switch Applications

- Small package
- Low ON resistance : $R_{on}$ = 12 Ω (max) (@$V_{GS}$ = −4 V)
  : $R_{on}$ = 32 Ω (max) (@$V_{GS}$ = −2.5 V)

Unit: mm




1. GATE 1
2. SOURCE
3. GATE 2
4. DRAIN 2
5. DRAIN 1

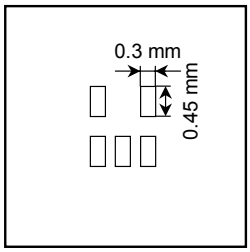
| | |
|---|---|
| ESV | |
| JEDEC | — |
| JEITA | — |
| TOSHIBA | 2-2P1B |

Weight: 0.003g(typ.)

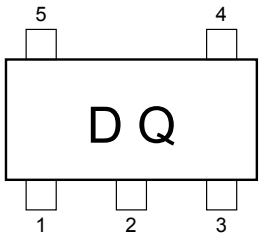
## Maximum Ratings (Ta = 25°C) (Q1, Q2 Common)

| Characteristics | | Symbol | Rating | Unit |
|---|---|---|---|---|
| Drain-Source voltage | | $V_{DS}$ | −30 | V |
| Gate-Source voltage | | $V_{GSS}$ | ±20 | V |
| Drain current | DC | $I_D$ | −100 | mA |
| | Pulse | $I_{DP}$ | −200 | |
| Drain power dissipation (Ta = 25°C) | | $P_D$ (Note) | 150 | mW |
| Channel temperature | | $T_{ch}$ | 150 | °C |
| Storage temperature range | | $T_{stg}$ | −55~150 | °C |

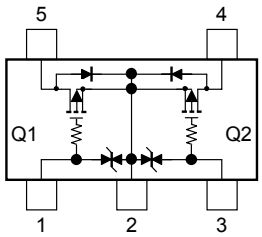
Note: Total rating, mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 t, Cu Pad: 0.135 $mm^2$ × 5)




## Marking




## Equivalent Circuit (top view)




## Handling Precaution

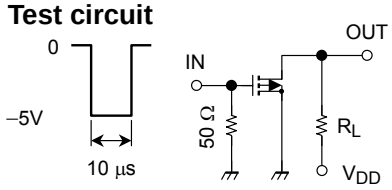
When handling individual devices (which are not yet mounting on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

## Electrical Characteristics (Ta = 25°C) (Q1, Q2 common)

| Characterristic | | Symbol | Test Condition | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| Gate leakage current | | $I_{GSS}$ | $V_{GS}$ = ±16 V, $V_{DS}$ = 0 | — | — | ±1 | μA |
| Drain-Source breakdown voltage | | $V_{(BR)\ DSS}$ | $I_D$ = −0.1 mA, $V_{GS}$ = 0 | −30 | — | — | V |
| Drain cut-off current | | $I_{DSS}$ | $V_{DS}$ = −30 V, $V_{GS}$ = 0 | — | — | −1 | μA |
| Gate threshold voltage | | $V_{th}$ | $V_{DS}$ = −3 V, $I_D$ = −0.1 mA | −1.1 | — | −1.7 | V |
| Forward transfer admittance | | $\|Y_{fs}\|$ | $V_{DS}$ = −3 V, $I_D$ = −10 mA | 20 | — | — | mS |
| Drain-Source ON resistance | | $R_{DS\ (ON)}$ | $I_D$ = −10 mA, $V_{GS}$ = −4 V | — | 8 | 12 | Ω |
| | | | $I_D$ = −1 mA, $V_{GS}$ = −2.5 V | — | 14 | 32 | |
| Input capacitance | | $C_{iss}$ | $V_{DS}$ = −3 V, $V_{GS}$ = 0, f = 1 MHz | — | 9.1 | — | pF |
| Reverse transfer capacitance | | $C_{rss}$ | | — | 3.5 | — | pF |
| Output capacitance | | $C_{oss}$ | | — | 8.6 | — | pF |
| Switching time | Turn-on time | $t_{on}$ | $V_{DD}$ = −5 V, $I_D$ = −10 mA, $V_{GS}$ = 0~−5 V | — | 65 | — | ns |
| | Turn-off time | $t_{off}$ | | — | 175 | — | |

## Switching Time Test Circuit

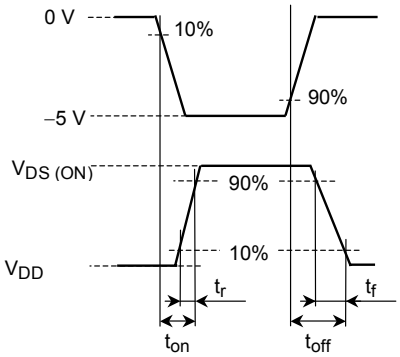
**(a) Test circuit**




$V_{DD}$ = −5 V
Duty ≦ 1%
$V_{IN}$: $t_r$, $t_f$ < 5 ns
($Z_{out}$ = 50 Ω)
Common Source
Ta = 25°C

**(b) $V_{IN}$**

**(c) $V_{OUT}$**

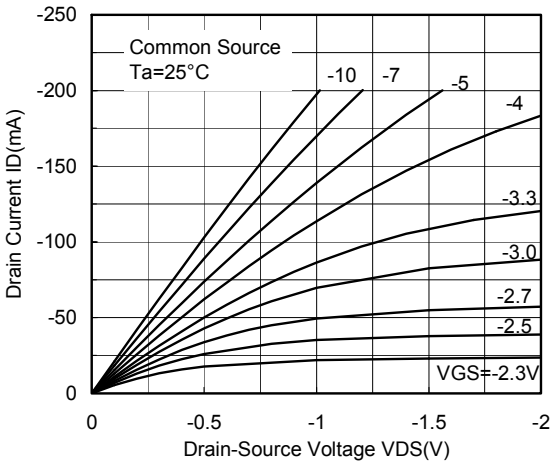



## Precaution

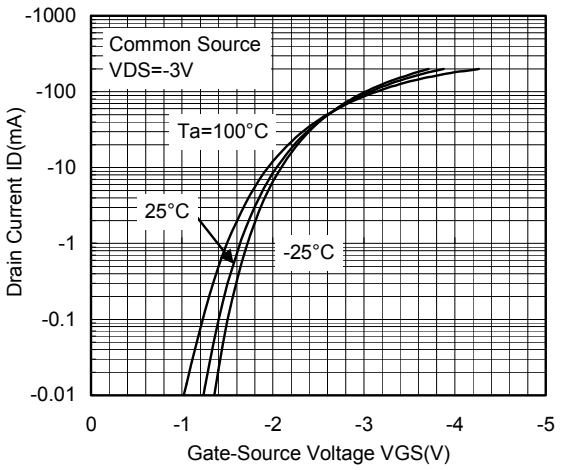
$V_{th}$ can be expressed as voltage between gate and source when low operating current value is $I_D$ = −100 μA for this product. For normal switching operation, $V_{GS\ (on)}$ requires higher voltage than $V_{th}$ and $V_{GS\ (off)}$ requires lower voltage than $V_{th}$. (Relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (on)}$ )

Please take this into consideration for using the device. $V_{GS}$ recommended voltage of −2.5 V or higher to turn on this product.

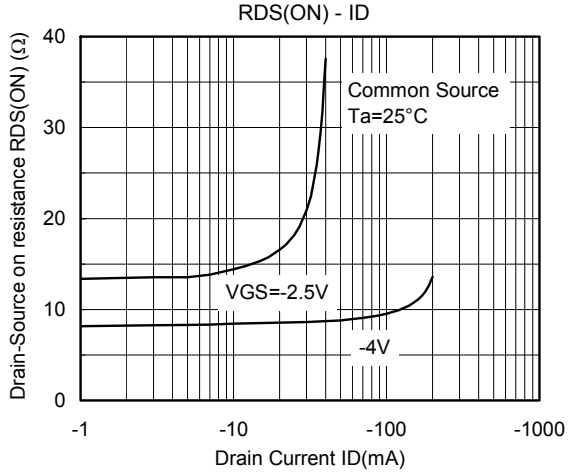
ID - VDS



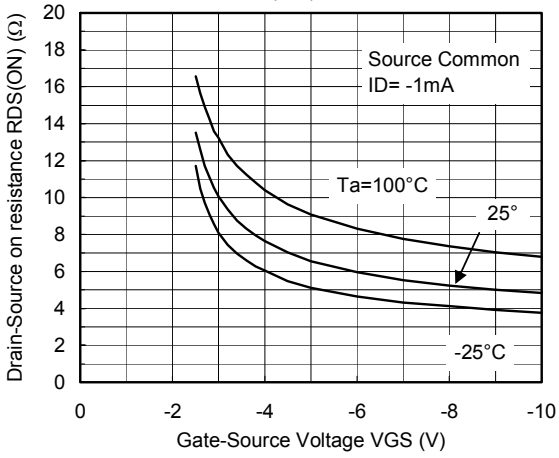

ID - VGS



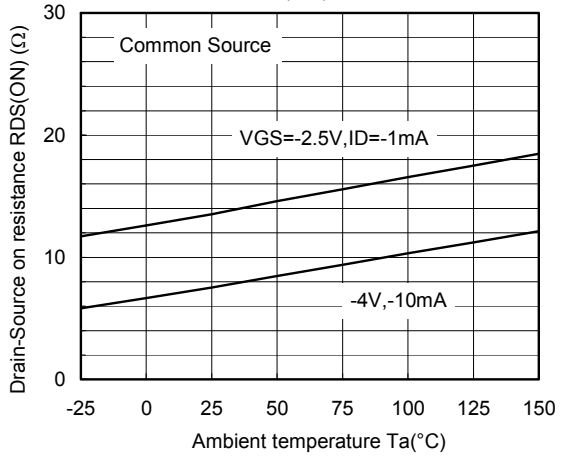

RDS(ON) - ID



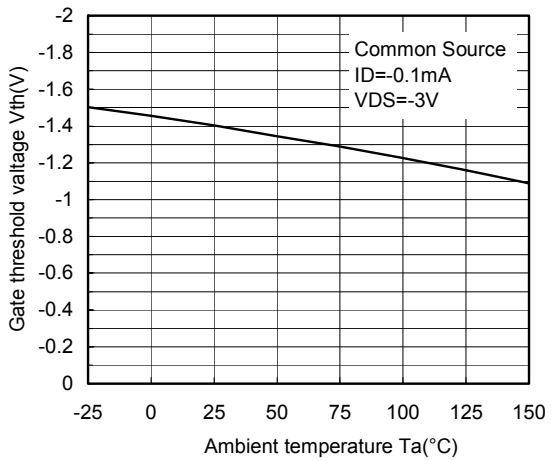

RDS(ON) - VGS



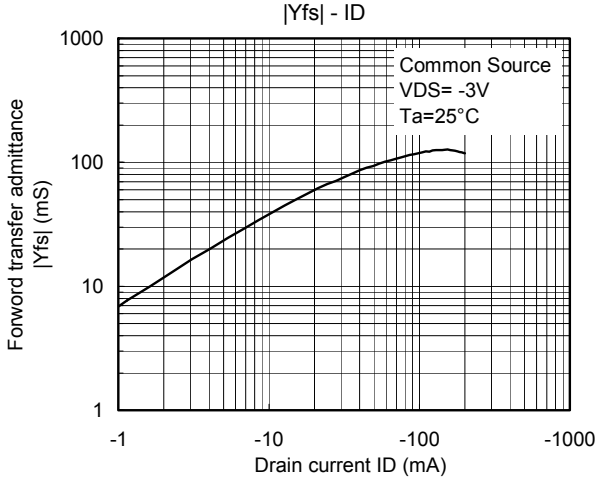

RDS(ON) - Ta



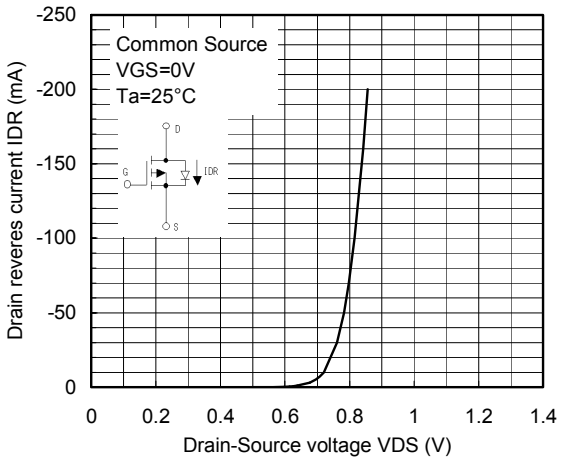

Vth - Ta



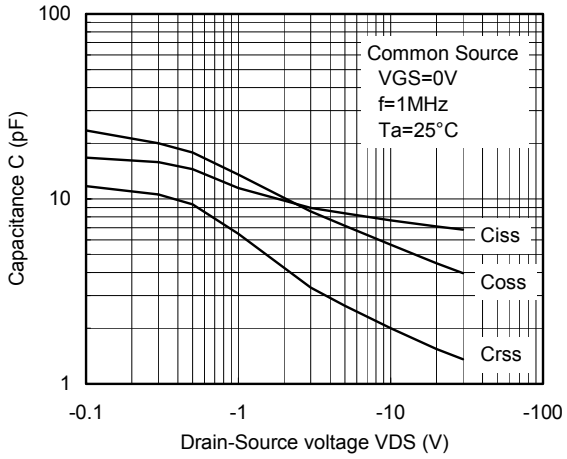
|Yfs| - ID



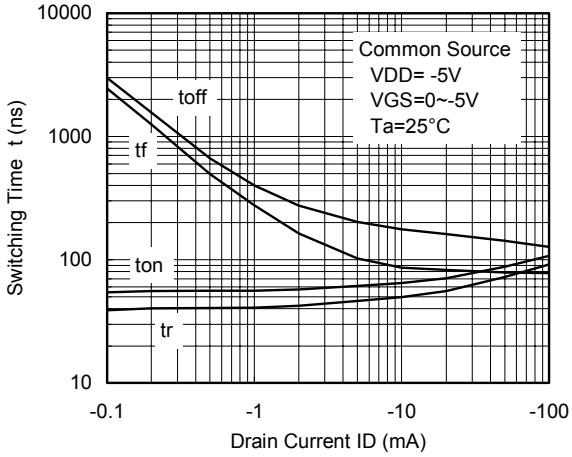

IDR - VDS



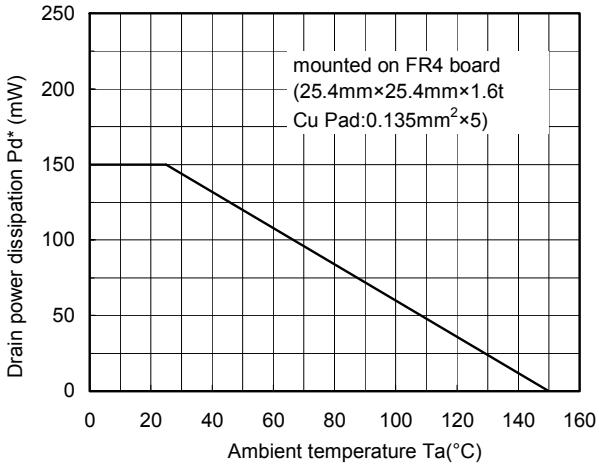

C - VDS




t - ID




PD* - Ta




*: Total Rating

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