TOSHIBA Bi-CMOS Integrated Circuit Silicon Monolithic

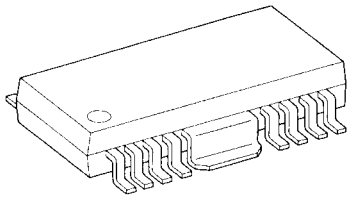
TB62801FG

Linear CCD Clock Driver

The TB62801FG is a clock distribution driver for CCD linear image sensors.

The IC can functionally drive the CCD input capacitance. It also supports inverted outputs, eliminating the need for crosspoint control.

The IC contains a 1 to 4 clock distribution driver for the main clock and 4-bit buffers for control signals.



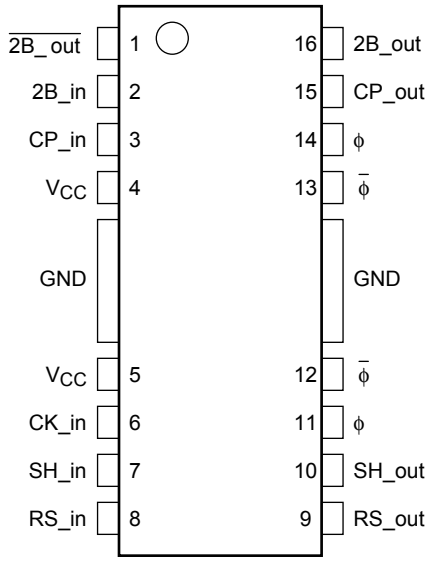
HSOP16-P-300-1.00

Weight: 0.5 g (typ.)

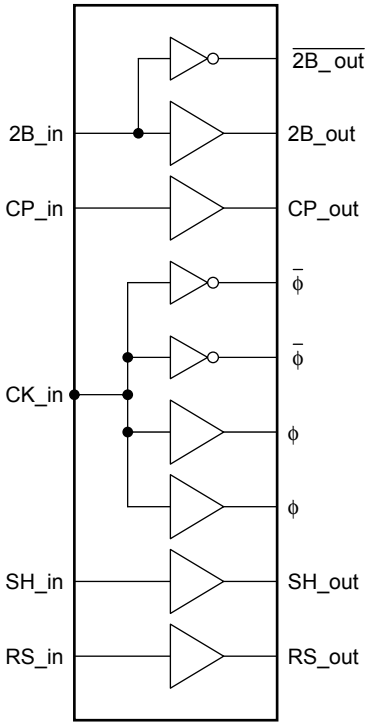
Features

- High drivability: Guaranteed driving 450 [pF] load capacitance @fclock = 20 [MHz]
- Operating temperature range: Ta = −25°C to 60°C

Pin Connection (top view)



Logic Diagram



Pin Description

Pin No.	Pin Name	Functions	Remarks
1	$\overline{2B\_out}$	Light-load drive output (inverted)	Driver output for CCD last-stage clock
2	2B_in	Light-load drive input	Driver input for CCD last-stage clock
3	CP_in	Light-load drive input	CCD clamp gate driver input
4	V_{CC}	Power supply	—
	GND	Ground	—
5	V_{CC}	Power supply	—
6	CK_in	Heavy-load drive input	Driver input for CCD transfer clock
7	SH_in	Light-load drive input	CCD shift gate driver input
8	RS_in	Light-load drive input	CCD reset gate driver input
9	RS_out	Light-load drive output (not inverted)	CCD reset gate driver output
10	SH_out	Light-load drive output (not inverted)	CCD shift gate driver output
11	ϕ	Heavy-load drive output (not inverted)	Driver output for CCD transfer clock
12	$\overline{\phi}$	Heavy-load drive output (inverted)	Driver output for CCD transfer clock
	GND	Ground	—
13	$\overline{\phi}$	Heavy-load drive output (inverted)	Driver output for CCD transfer clock
14	ϕ	Heavy-load drive output (not inverted)	Driver output for CCD transfer clock
15	CP_out	Light-load drive output (not inverted)	CCD clamp gate driver output
16	2B_out	Light-load drive output (not inverted)	Driver output for CCD last-stage clock

Truth Table

Input		Output	
2B_in	L	$\overline{2B\_out}$	H
	H		L
	L	2B_out	L
	H		H
CP_in	L	CP_out	L
	H		H
CK_in	L	ϕ	L
	H		H
	L	$\bar{\phi}$	H
	H		L
SH_in	L	SH_out	L
	H		H
RS_in	L	RS_out	L
	H		H

Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
Power supply voltage		V_{CC}	−0.5 to 7.0	V
Input voltage		V_{IN}	−1.2 to V_{CC}+0.5	V
Output voltage		V_O	−0.5 to V_{CC}	V
Input clamp diode current ($V_i < 0$)		I_{IK}	−50	mA
Output clamp diode current ($V_O < 0$)		I_{OK}	−50	mA
Output current excluding other than ϕ, $\bar{\phi}$ outputs	High level	I_{OH} (O/$\overline{O}$)	−16.0	mA
	Low level	I_{OL} (O/$\overline{O}$)	16.0	mA
ϕ output current	High level	IOH (ϕ/$\bar{\phi}$)	−100	mA
	Low level	IOL (ϕ/$\bar{\phi}$)	150	mA
Operating temperature		Topr	−25 to 60	°C
Storage temperature		T_{stg}	−40 to 100	°C
Junction temperature		T_j	150	°C
Power dissipation		P_D	1.5	W

Note: Output current is specified as follows: V_{OH} = 4.0 V, V_{OL} = 0.5 V.

Recommended Operating Conditions

Characteristic		Symbol	Min	Typ.	Max	Unit
Power supply voltage		V_{CC}	4.7	5.0	5.5	V
Input voltage		V_{IN}	0	—	V_{CC}	V
Output voltage		V_O	0	—	V_{CC}	V
Output current excluding ϕ, $\bar{\phi}$ outputs	High level	I_{OH} (O/$\bar{O}$)	—	—	–8.0	mA
	Low level	I_{OL} (O/$\bar{O}$)	—	—	8.0	mA
ϕ output current (Note)	High level	I_{OH} (ϕ/$\bar{\phi}$)	—	—	–20.0	mA
	Low level	I_{OL} (ϕ/$\bar{\phi}$)	—	—	20.0	mA
Operating temperature		T_{opr}	–25	25	60	°C
Input rise/fall time		t_{ri}/t_{fi}	—	2.5	5.0	ns

Note: Output current is specified as follows: V_{CC} = 4.7 V, V_{OH} = 4.5 V, V_{OL} = 0.2 V.
Input rise/fall time is specified as 10 % to 90 % of waveform amplitude.

Electrical Characteristics

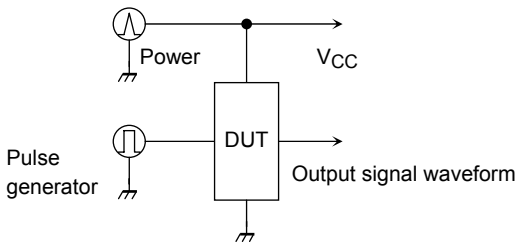
DC Characteristics (unless otherwise specified, V_{CC} = 4.7 to 5.5 V, Ta = –25 to 60°C)

Characteristic		Symbol	Test Circuit	Test Condition	V_{CC}	Min	Typ.	Max	Unit
Input voltage	High	V_{IH}	1, 2	—	4.7	2.0	—	V_{CC}	V
	Low	V_{IL}		—	4.7	0	—	0.8	
Input clamp voltage		V_{IK}	3	I_{IK} = –30 mA	4.7	—	—	1.0	V
ϕ output voltage		V_{OH} (ϕ/$\bar{\phi}$)	4, 5	I_{OH} = –10 mA	4.7	4.5	—	V_{CC}	V
				I_{OH} = –50 mA	4.7	4.0	—	V_{CC}	
				I_{OH} = –300 mA	4.7	2.5	—	V_{CC}	
		V_{OL} (ϕ/$\bar{\phi}$)	6, 7	I_{OL} = 100 μA	4.7	0	—	0.2	
				I_{OL} = 50 mA	4.7	0	—	0.5	
				I_{OL} = 300 mA	4.7	0	—	2.5	
Output voltage excluding ϕ, ϕ outputs		V_{OH} (O/$\bar{O}$)	4, 5	I_{OH} (O/$\bar{O}$) = –4 mA	4.7	4.5	—	V_{CC}	V
				I_{OH} (O/$\bar{O}$) = –16 mA	4.7	4.0	—	V_{CC}	
		V_{OL} (O/$\bar{O}$)	6, 7	I_{OL} (O/$\bar{O}$) = 4 mA	4.7	0	—	0.2	
				I_{OL} (O/$\bar{O}$) = 16 mA	4.7	0	—	0.5	
Input voltage		I_{IN}	8	V_{IN} = V_{CC} or GND	5.5	—	—	1.0	μA
Static current consumption	Total	I_{CC}	9	ϕ outputs: High or Low $\bar{\phi}$ outputs: Low or High Other outputs are High	5.5	—	—	15.0	mA
	Each bit	ΔI_{CC}	10	One input: V_{IN} = 0.5 V Other inputs: V_{CC} or GND	—	—	—	1.5	
Output off mode supply voltage		V_{POR}	—	See description on next page.	—	—	3.0	—	V

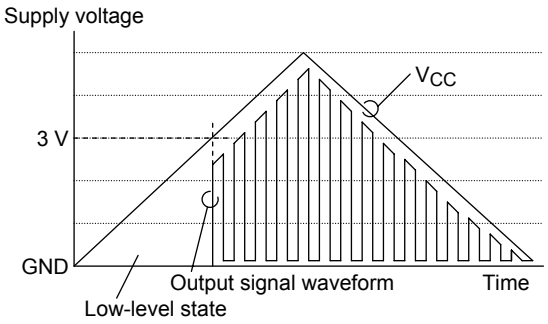
Output Low-Level Fixed Mode at Power-On

To avoid malfunction at power on, this IC incorporates the following functions:

- All outputs are fixed to low level until V_{CC} reaches more than 3 V.
- When V_{CC} reaches 3 V (typ.), internal logic depends on input signals.
- V_{CC} must be more than 4.7 V for normal operation.



Additional circuit (P.O.R) test circuit



AC Characteristics (input transition rise or fall time: t_r/t_f = 2.5 ns)

Characteristic	Symbol	Test Condition	Normal Temperature/ V_{CC} = 5.0 V			All Temperatures/ V_{CC} = 4.7 to 5.5 V		Unit	Reference Measurement Diagram
			Min	Typ.	Max	Min	Max		
Propagation delay time	t_{pLH} (ϕ/$\bar{\phi}$)	C_L = 450 pF	7.0	10.0	14.0	7.0	16.0	ns	Measurement diagram 1
		C_L = 350 pF	6.0	9.0	13.0	6.0	15.0		
	t_{pHL} (ϕ/$\bar{\phi}$)	C_L = 450 pF	7.0	10.0	14.0	7.0	16.0		
		C_L = 350 pF	6.0	9.0	13.0	6.0	15.0		
	t_{pLH} (O/$\bar{O}$)	C_L = 30 pF	3.0	5.0	7.0	2.5	8.0	ns	Measurement diagram 2
		C_L = 15 pF	2.0	4.0	6.0	1.5	7.0		
	t_{pHL} (O/$\bar{O}$)	C_L = 30 pF	3.0	5.0	7.0	2.5	8.0		
		C_L = 15 pF	2.0	4.0	6.0	1.5	7.0		
Output skew excluding ϕ, $\bar{\phi}$ outputs	t_o (skw)	C_L = 30 pF	0	—	2.0	—	2.0	ns	Measurement diagram 3
Output crosspoints (ϕ1/ϕ2)	V_T (crs)	C_L = 300 to 450 pF	—	—	—	1.5	—	V	Measurement diagram 4

Waveform Measuring Point

Propagation Delay Time Setting

Input signal
- 2B_in
- CK_in
- SH_in
- RS_in
- CP_in

Measurement Diagram 1

Output signal
- ϕ

Output signal
- $\overline{\phi}$

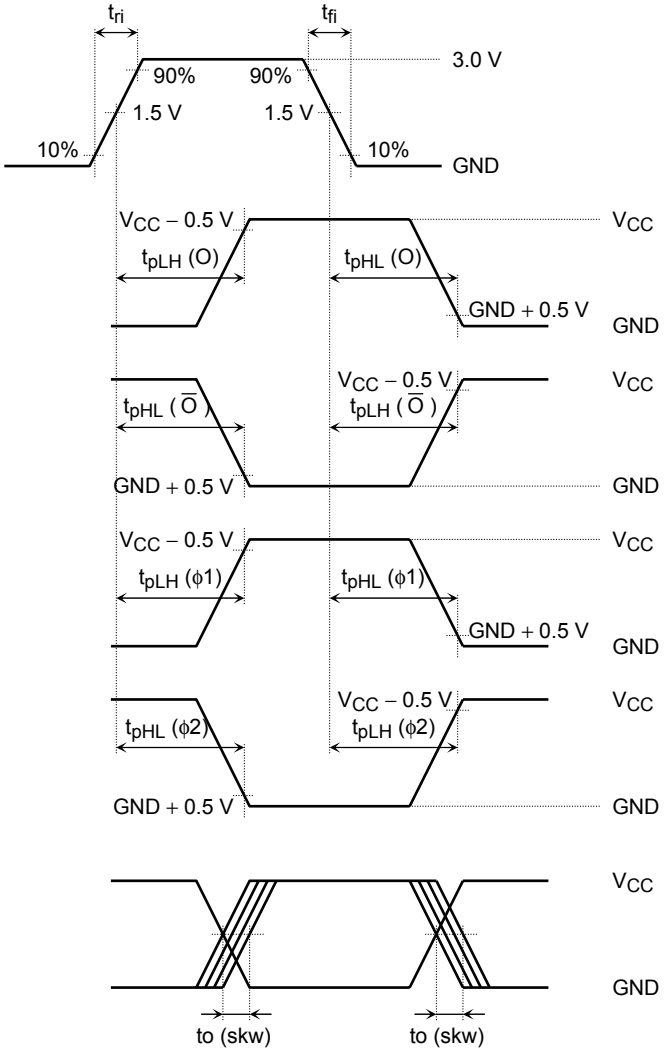
Measurement Diagram 2

Output signal
- 2B_out
- CP_out
- SH_out
- RS_out

Output signal
- 2B_out

Measurement Diagram 3

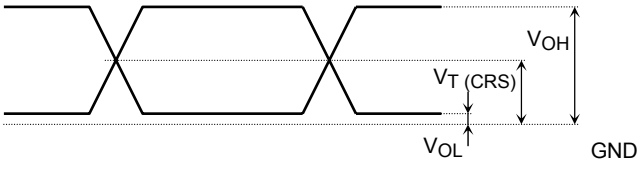
Output signal
- $\overline{2B\_out}$
- 2B_out
- CP_out
- SH_out
- RS_out



Output Waveform Crosspoint/Level Setting

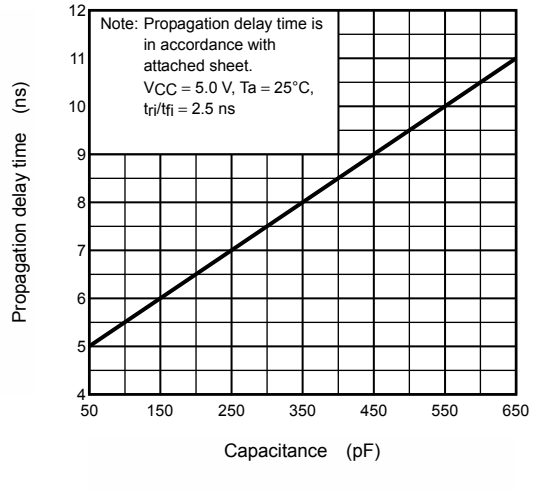
Measurement Diagram 4

- ϕ
- $\overline{\phi}$

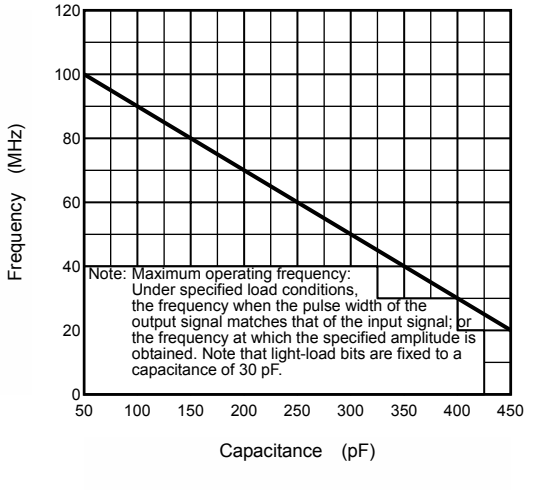


Reference Data (typ. value)

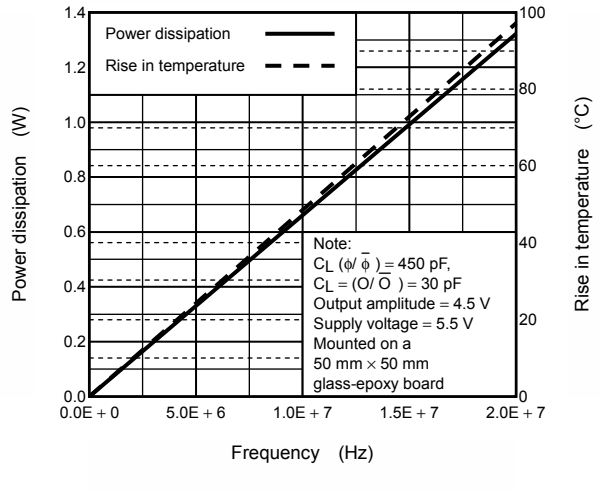
t_{pLH} (ϕ), t_{pHL} (ϕ) – C_L
(characteristics of 1-output, other outputs: no load)



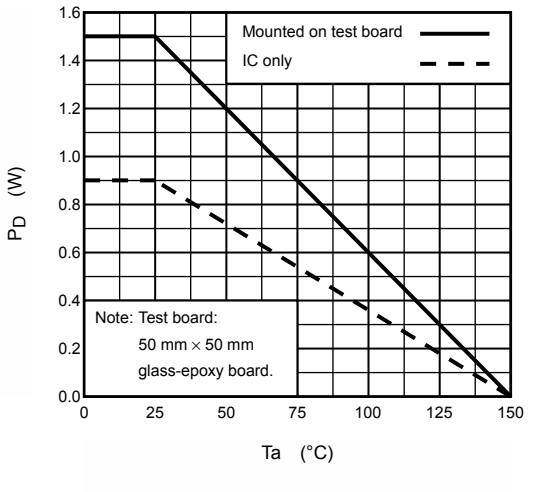
Load capacitance versus maximum operating frequency (all bits in operation)
V_{CC} = 5.0 V, Ta = 25°C, t_{ri}/t_{fi} = 2.5 ns



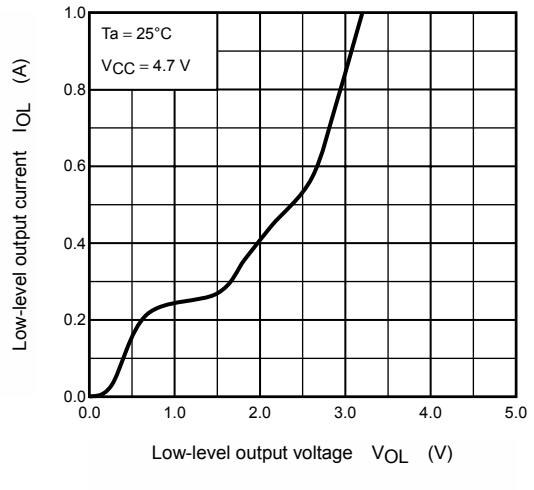
Frequency versus power dissipation, temperature
(@all outputs: maximum load capacitance)



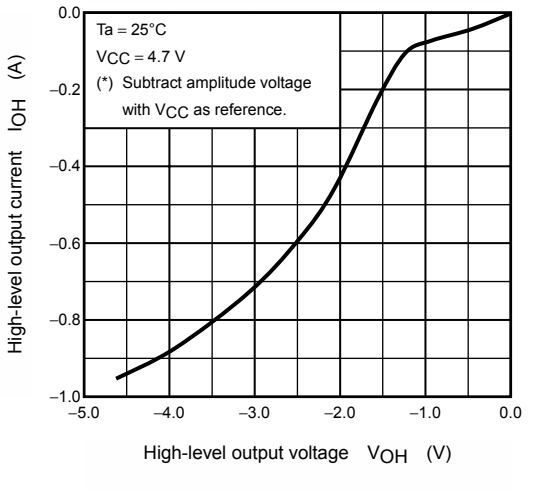
P_D – Ta



$\phi/\bar{\phi}$ output
I_{OL} – V_{OL}



$\phi/\bar{\phi}$ output
I_{OH} – V_{OH}



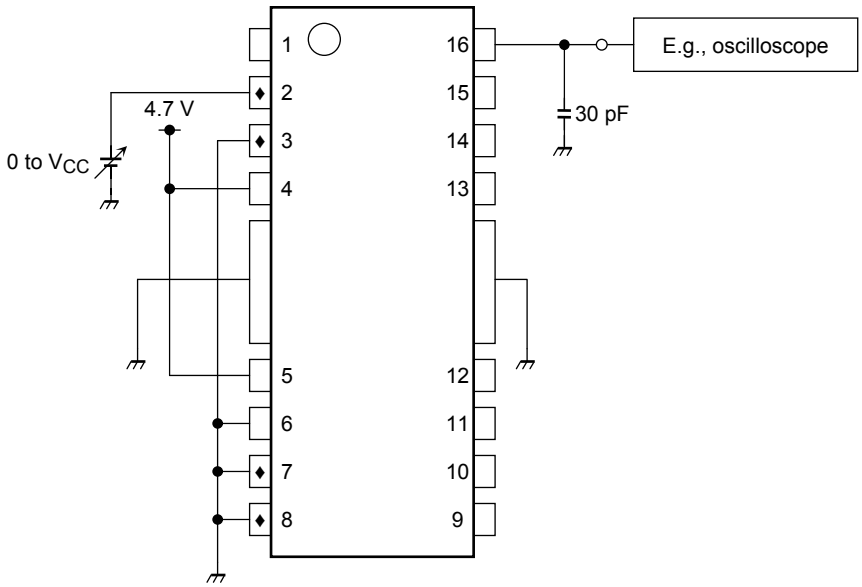
Test Circuit

DC Parameters

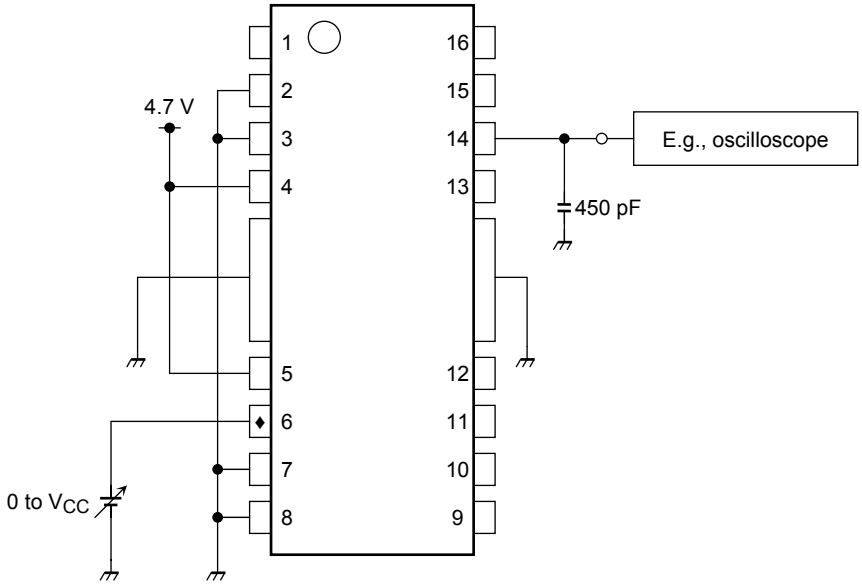
Pins marked with an asterisk (*) are test pins. Ground the input pins that are not being used as test pins so that their logic is determined. Unless otherwise specified, bits of the same type are measured in the same way.

- **V_{IH}/V_{IL}**

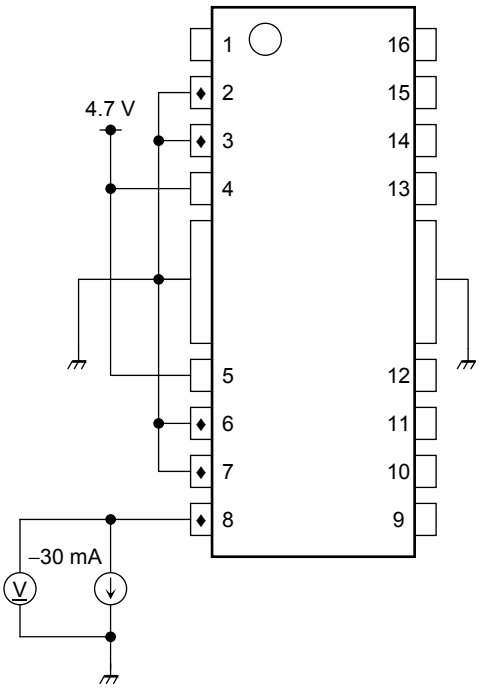
(1) Light-load drive bit



(2) Heavy-load drive bit

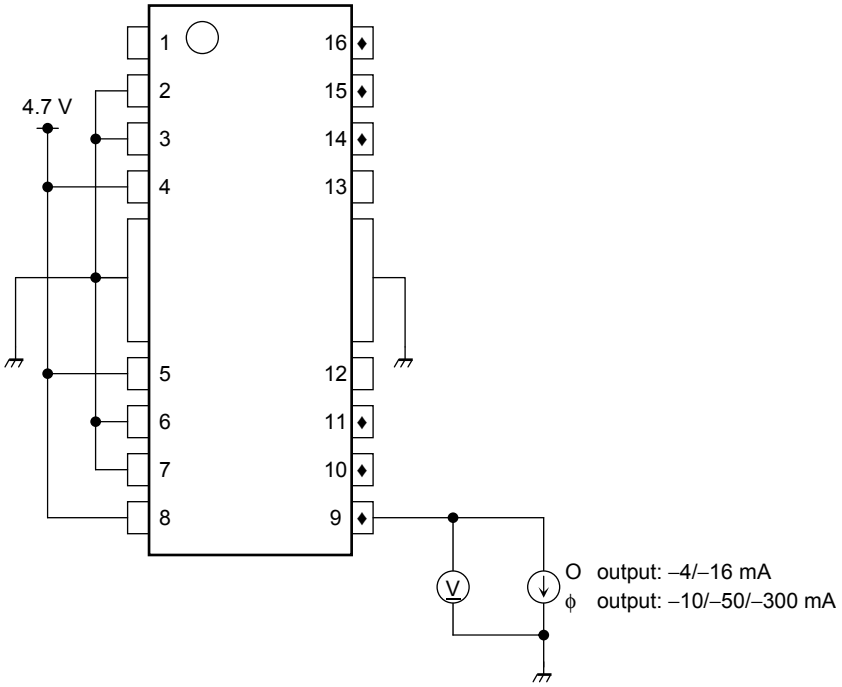


- **V_{IK}**

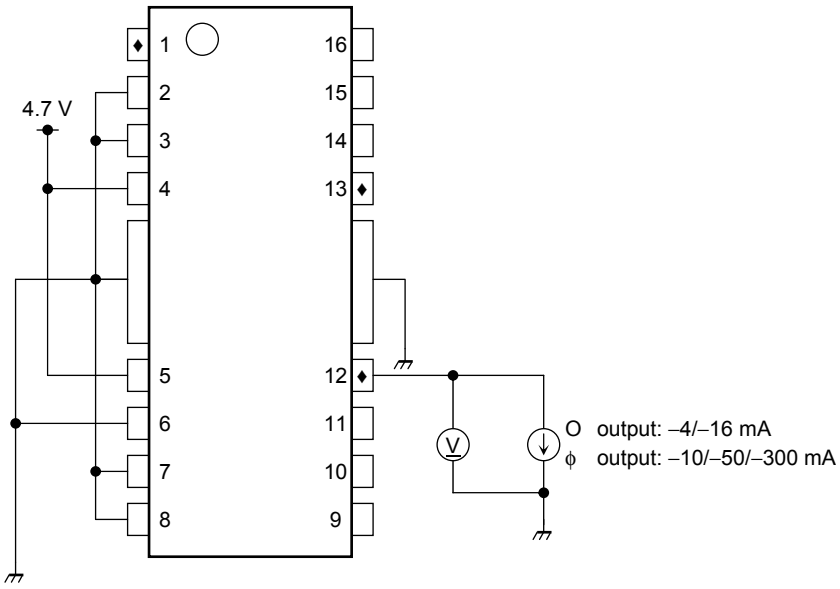


Note 1: When measuring input pins, connect the input pins that are not being measured to GND.

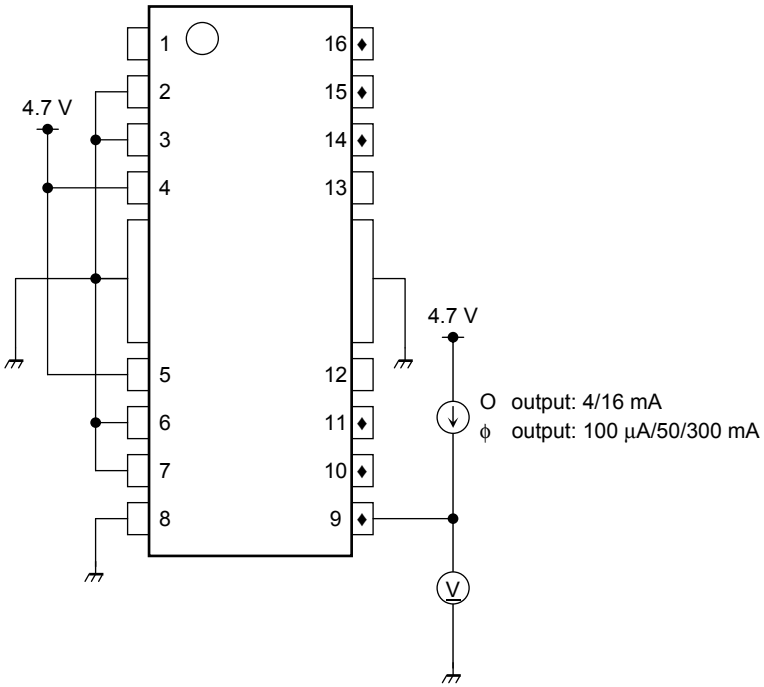
- **V_{OH} (O/ϕ)**



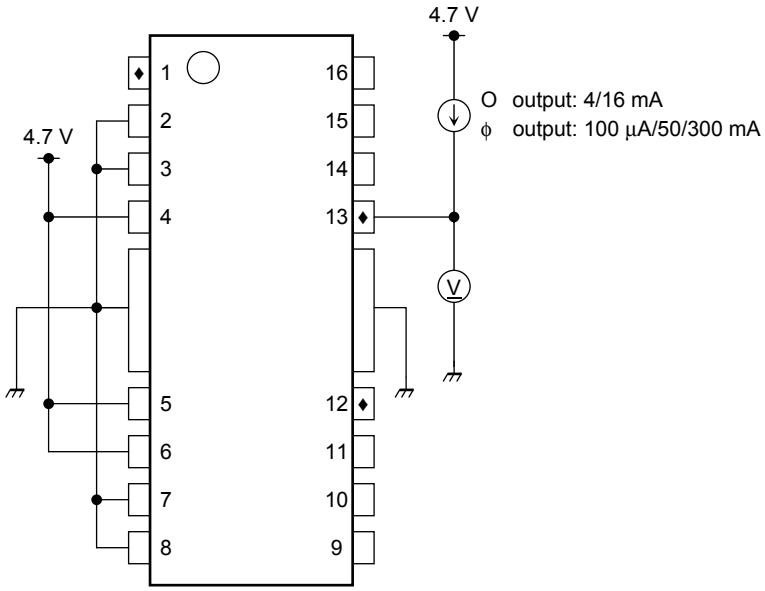
- V_{OH} ($\overline{O}$ / $\overline{\phi}$)



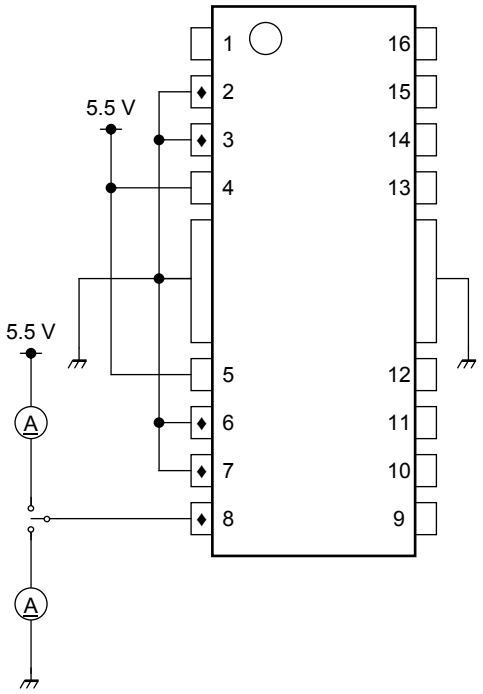
- V_{OL} (O/ϕ)



- V_{OL} ($\overline{o}$ / $\overline{\phi}$)

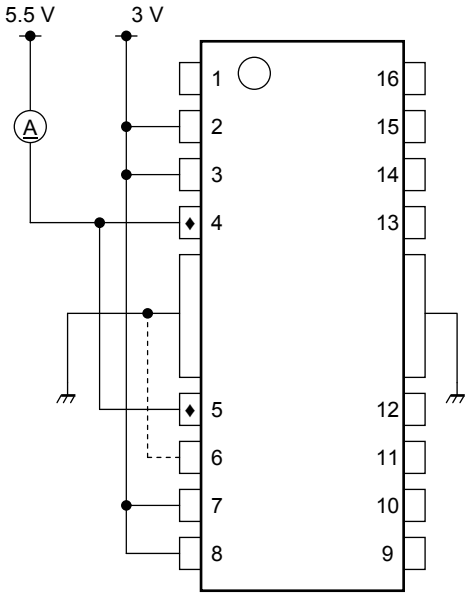


- I_{IN}



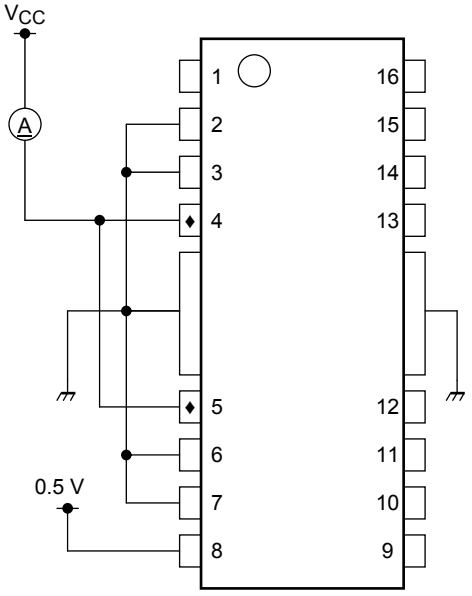
Note: When measuring input pins, connect the input pins that are not being measured to GND.

- I_{CC}



Note 1: The input logic of the heavy-load drive clock input pin (pin 6) is the same for High or Low.

- ΔI_{CC}



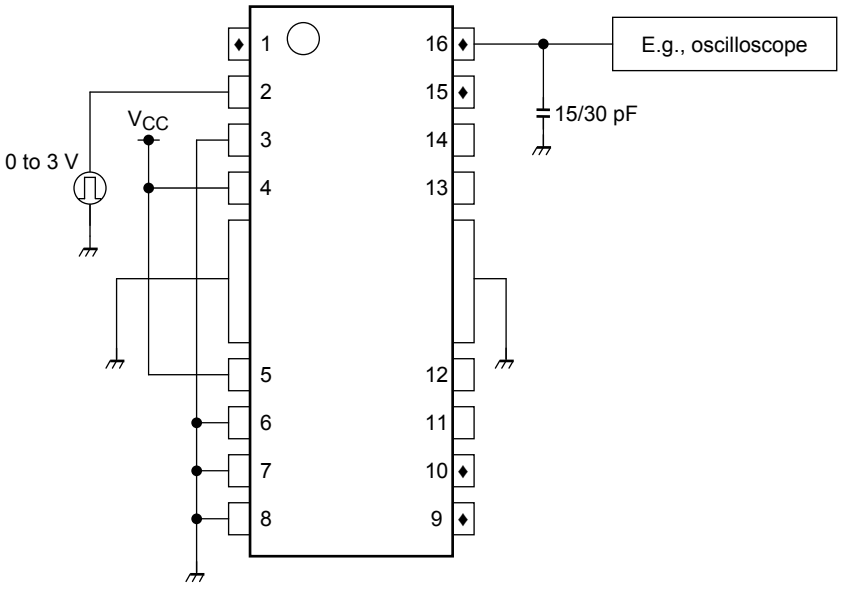
Note 2: When measuring input pins, connect the input pins that are not being measured to GND or power.

AC Parameters

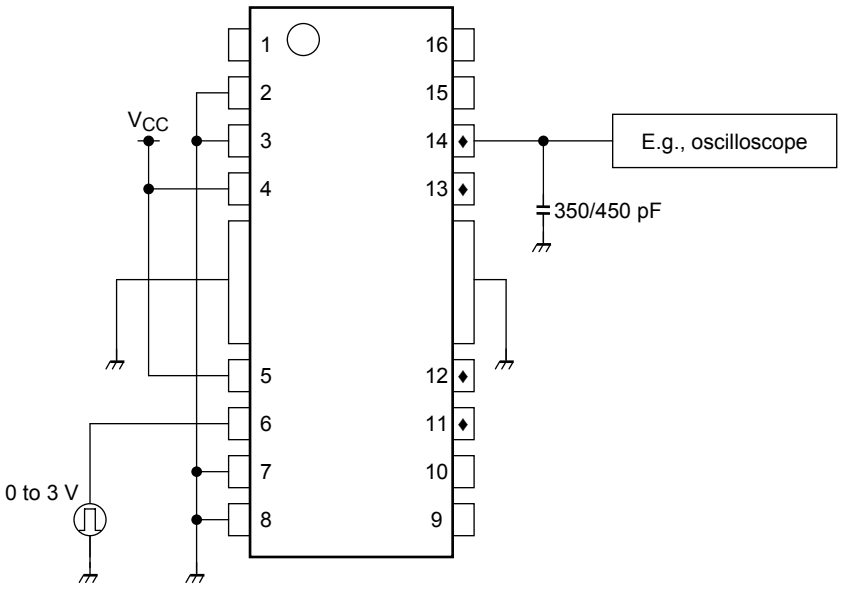
Pins marked with an asterisk (*) are test pins. Ground the input pins that are not being used as test pins so that their logic is determined. Unless otherwise specified, bits of the same type are measured in the same way.

- **Propagation Delay Time**

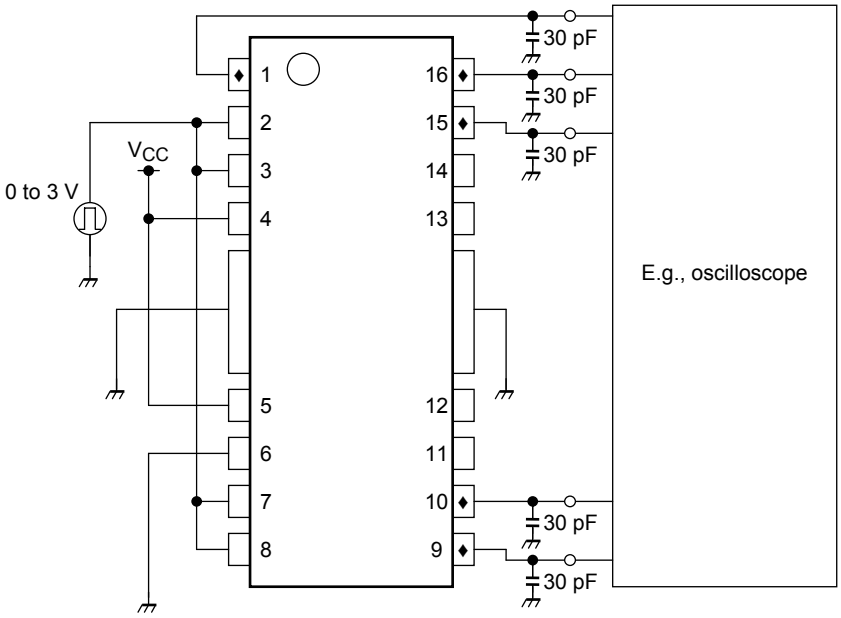
(1) Light-load drive bit



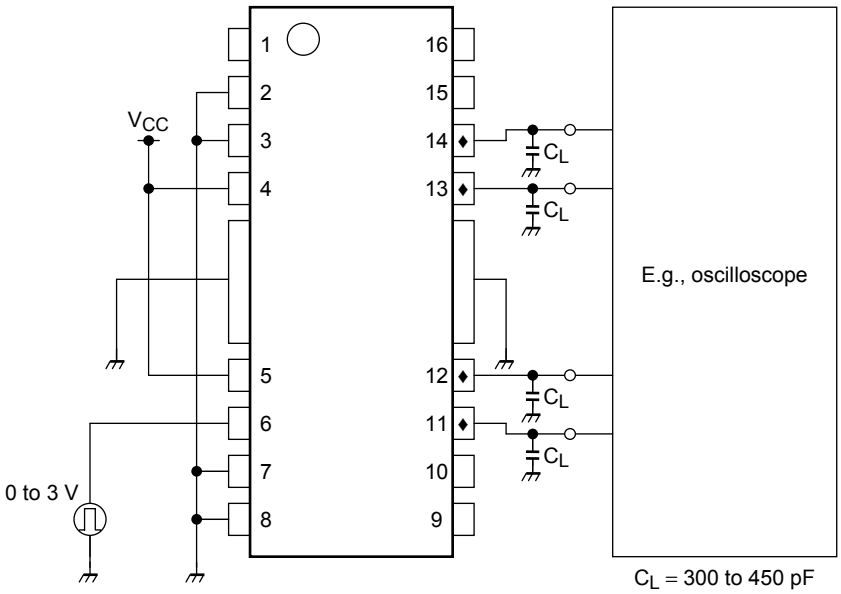
(2) Heavy-load drive bit



- **Light-Load Drive Output Skew**

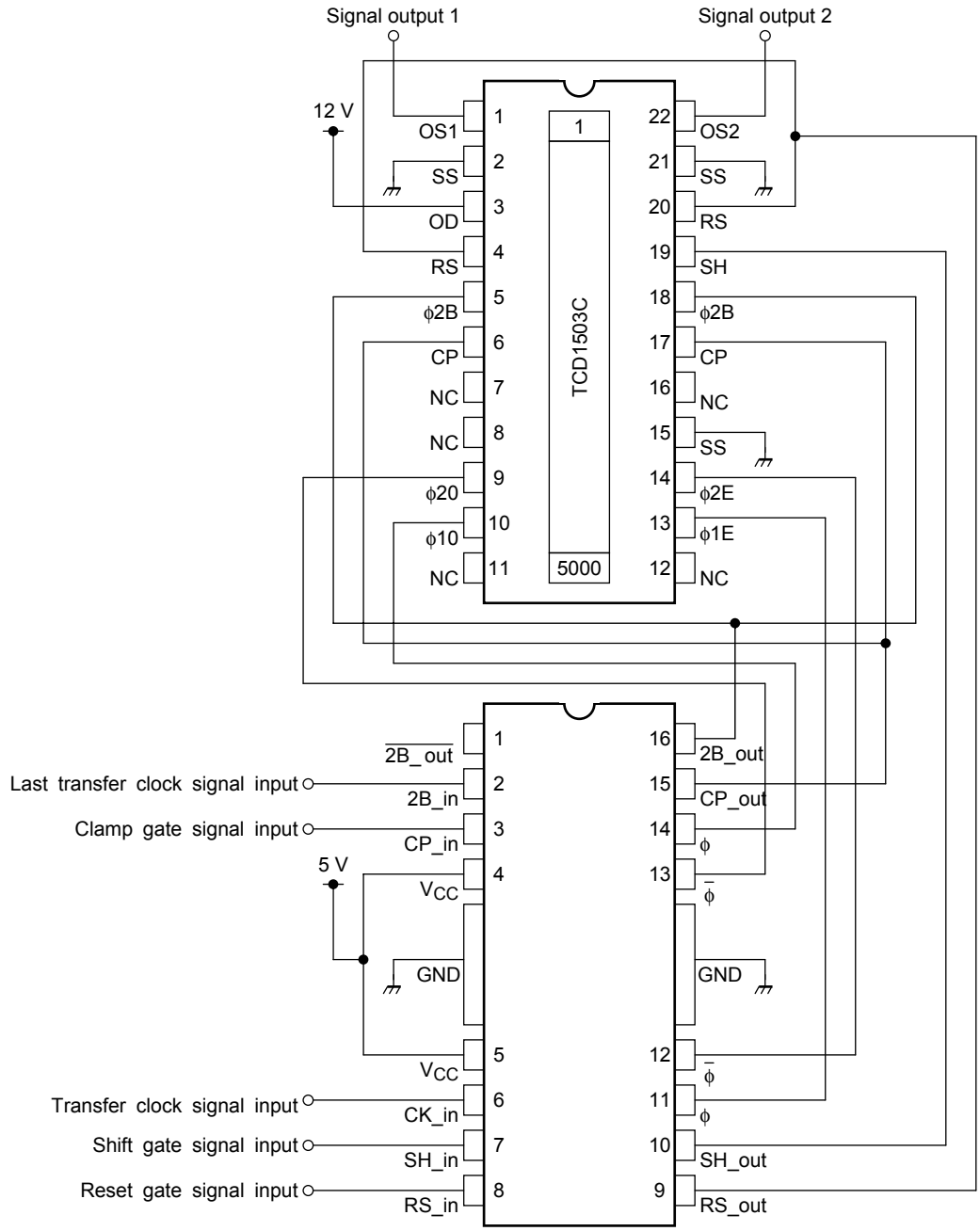


- **Heavy-Load Drive Output Crosspoints**



Example of an Application Circuit

(1) Connection to the TCD1503C



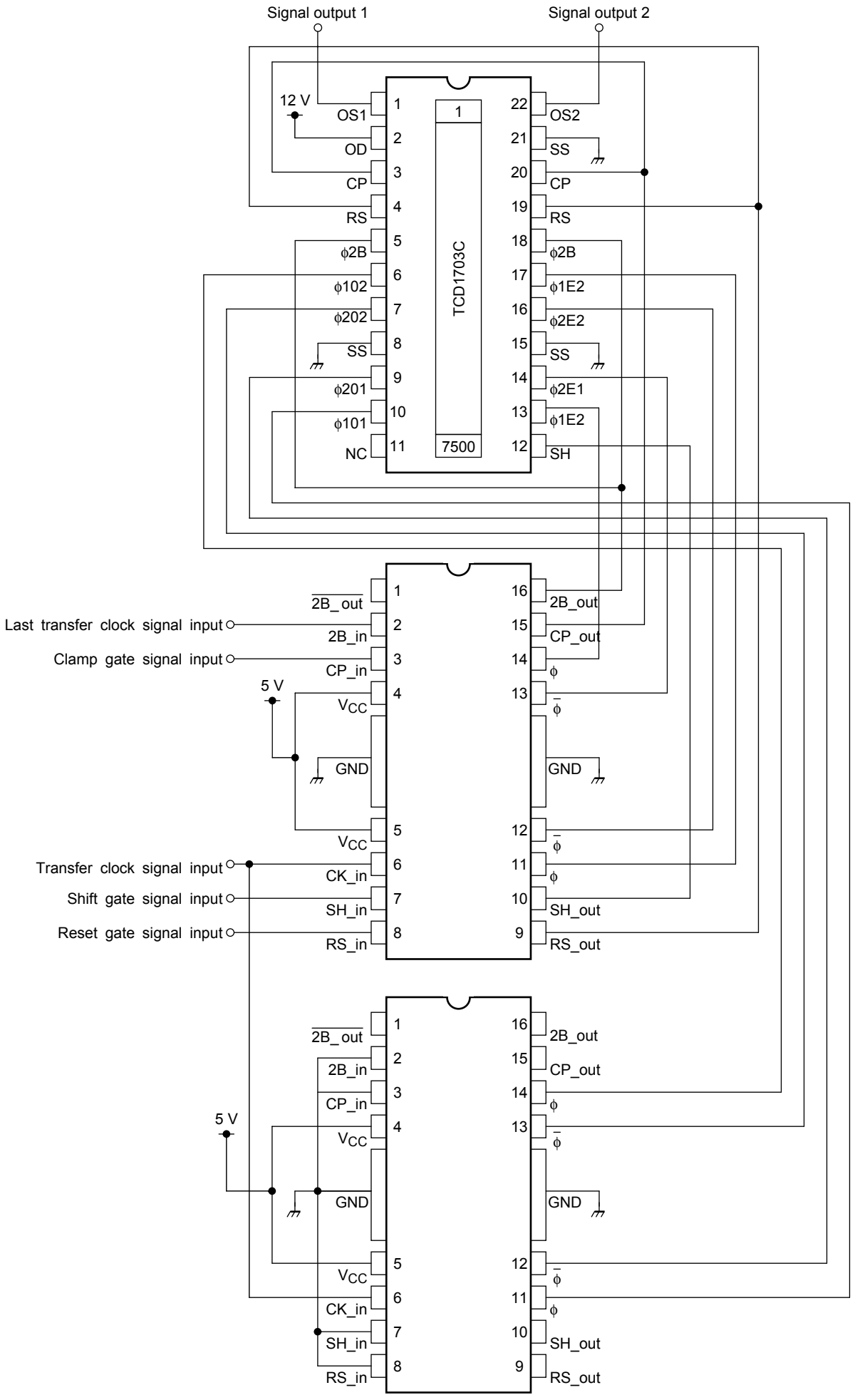
Note: Driving the CCD requires a lot of power. Toshiba recommends using a bypass capacitor connected to the 5 V power supply to stabilize voltage.

Precautions on Use

This IC does not include built-in protection circuits for excess current or overvoltage. If the IC is subjected to excess current or overvoltage, it may be destroyed. Therefore systems incorporating the IC should be designed with the utmost care.

Particular care is necessary in the design of the output, V_{CC} and GND lines since the IC may be destroyed by short circuits between outputs, air contamination faults, or faults due to improper grounding.

(2) Connection to the TCD1703C

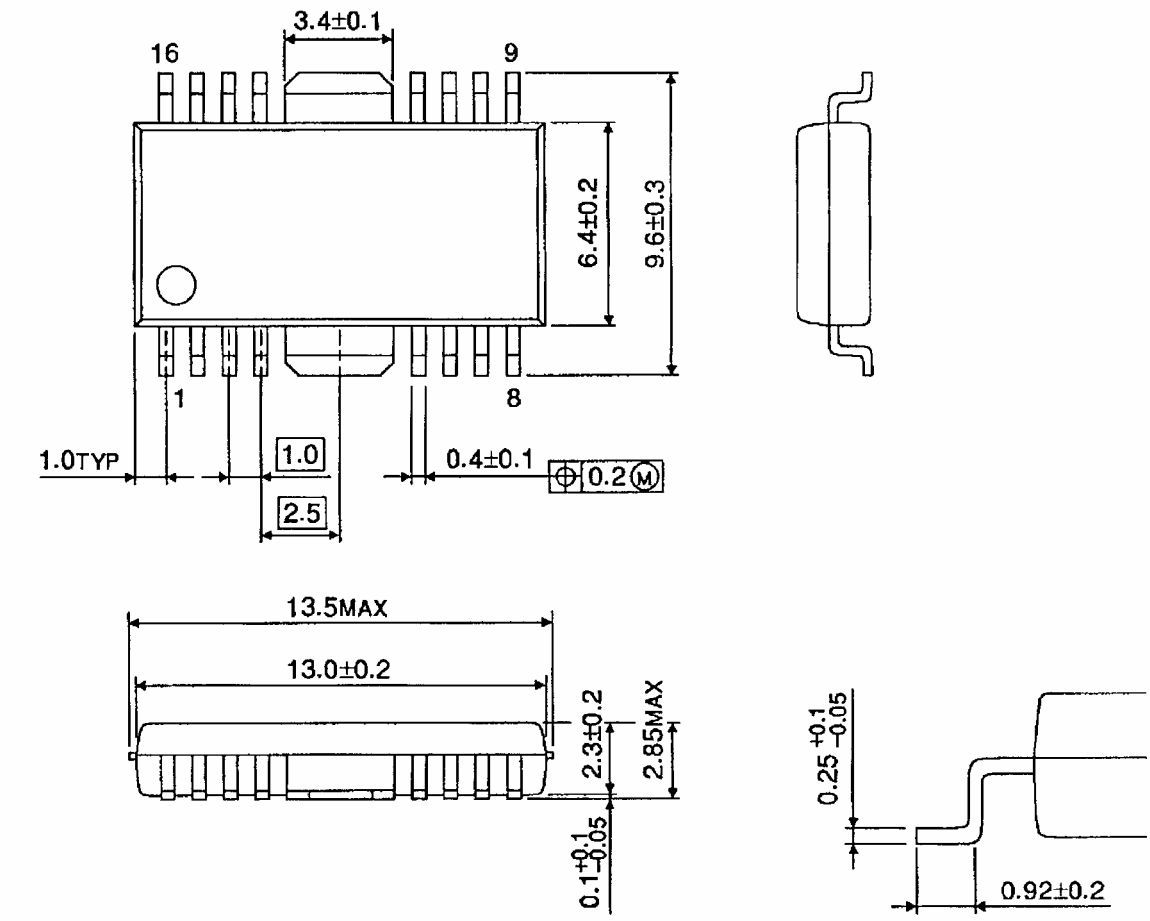


Note: Driving the CCD requires a lot of power. Toshiba recommends the use of a bypass capacitor connected to the 5 V power supply to stabilize voltage.
Two TB62801FGS devices are used in this application: one is used to drive all the control bits and the four transfer clock bits, the other to drive the remaining four transfer clock bits.

Package Dimensions

HSOP16-P-300-1.00

Unit: mm



Weight: 0.5 g (typ.)

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