TOSHIBA Field Effect Transistor Silicon N, P Channel MOS Type

(P Channel U−MOS IV/N Channel U-MOS III)

TPC8405

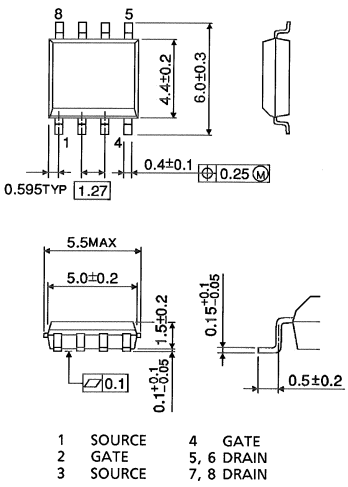
Lithium Ion Secondary Battery Applications

Portable Equipment Applications

Notebook PC Applications

- Low drain-source ON resistance
  : P Channel $R_{DS\ (ON)}$ = 25 mΩ (typ.)
  N Channel $R_{DS\ (ON)}$ = 20 mΩ (typ.)
- High forward transfer admittance
  : P Channel $|Y_{fs}|$ = 12S (typ.)
  N Channel $|Y_{fs}|$ = 14S (typ.)
- Low leakage current
  : P Channel I_{DSS} = −10 μA (V_{DS} = −30 V)
  N Channel I_{DSS} = 10 μA (V_{DS} = 30 V)
- Enhancement-mode
  : P Channel V_{th} = −0.8~ −2.0 V (V_{DS} = −10 V, I_D = −1 mA)
  N Channel V_{th} = 1.3~2.5 V (V_{DS} = 10 V, I_D = 1 mA)

Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	2-6J1E

Weight: 0.080 g (typ.)

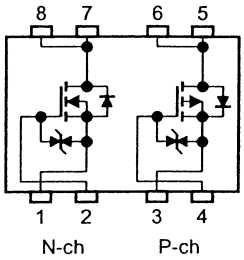
Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating P Channel	Rating N Channel	Unit
Drain-source voltage		V_{DSS}	−30	30	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	−30	30	V
Gate-source voltage		V_{GSS}	±20	±20	V
Drain current	DC (Note 1)	I_D	−4.5	6	A
	Pulse (Note 1)	I_{DP}	−18	24	
Drain power dissipation (t = 10s) (Note 2a)	Single-device operation (Note 3a)	$P_{D\ (1)}$	1.5	1.5	W
	Single-device value at dual operation (Note 3b)	$P_{D\ (2)}$	1.1	1.1	
Drain power dissipation (t = 10s) (Note 2b)	Single-device operation (Note 3a)	$P_{D\ (1)}$	0.75	0.75	
	Single-device value at dual operation (Note 3b)	$P_{D\ (2)}$	0.45	0.45	
Single pulse avalanche energy		E_{AS}	13.2 (Note 4a)	23.4 (Note 4b)	mJ
Avalanche current		I_{AR}	−4.5	6	A
Repetitive avalanche energy Single-device value at operation (Note 2a, 3b, 5)		E_{AR}	0.1		mJ
Channel temperature		T_{ch}	150		°C
Storage temperature range		T_{stg}	−55~150		°C

Note: For Notes 1 to 5, refer to the next page.

This transistor is an electrostatic-sensitive device. Handle with care.

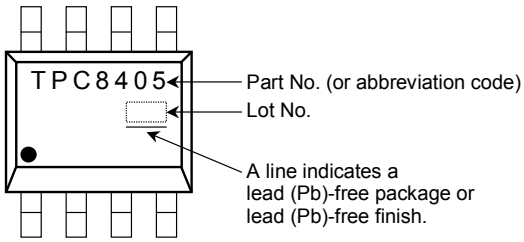
Circuit Configuration



Thermal Characteristics

Characteristics		Symbol	Max	Unit
Thermal resistance, channel to ambient (t = 10s) (Note 2a)	Single-device operation (Note 3a)	$R_{th\ (ch\text{-}a)\ (1)}$	83.3	°C/W
	Single-device value at dual operation (Note 3b)	$R_{th\ (ch\text{-}a)\ (2)}$	114	
Thermal resistance, channel to ambient (t = 10s) (Note 2b)	Single-device operation (Note 3a)	$R_{th\ (ch\text{-}a)\ (1)}$	167	
	Single-device value at dual operation (Note 3b)	$R_{th\ (ch\text{-}a)\ (2)}$	278	

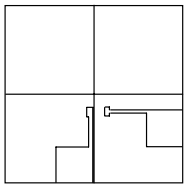
Marking



Note 1: Ensure that the channel temperature does not exceed 150°C.

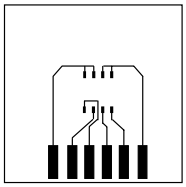
Note 2:

a) Device mounted on a glass-epoxy board (a) b) Device mounted on a glass-epoxy board (b)



FR-4
25.4 × 25.4 × 0.8
(unit: mm)

(a)



FR-4
25.4 × 25.4 × 0.8
(unit: mm)

(b)

Note 3:

a) The power dissipation and thermal resistance values shown are for a single device.
(During single-device operation, power is applied to one device only.)

b) The power dissipation and thermal resistance values shown are for a single device.
(During dual operation, power is evenly applied to both devices.)

Note 4:

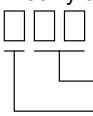
a) V_{DD} = −24 V, T_{ch} = 25°C (initial), L = 0.5 mH, R_G = 25 Ω, I_{AR} = −4.5 A

b) V_{DD} = 24 V, T_{ch} = 25°C (initial), L = 0.5 mH, R_G = 25 Ω, I_{AR} = 6.0 A

Note 5: Repetitive rating: pulse width limited by maximum channel temperature

Note 6: • on the lower left of the marking indicates Pin 1.

※ Weekly code: (Three digits)

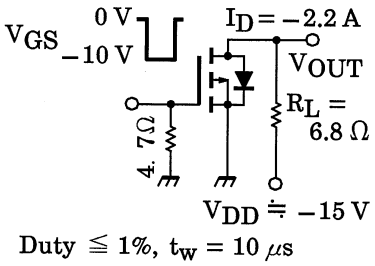


Week of manufacture
(01 for the first week of the year, continuing up to 52 or 53)

Year of manufacture
(the last digit of the calendar year)

P-ch

Electrical Characteristics (Ta = 25°C)

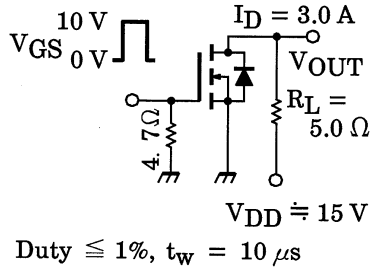
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±10	μA
Drain cut-OFF current		I_{DSS}	V_{DS} = −30 V, V_{GS} = 0 V	—	—	−10	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = −10 mA, V_{GS} = 0 V	−30	—	—	V
		$V_{(BR)\ DSX}$	I_D = −10 mA, V_{GS} = 20 V	−15	—	—	
Gate threshold voltage		V_{th}	V_{DS} = −10 V, I_D = −1 mA	−0.8	—	−2.0	V
Drain-source ON resistance		$R_{DS\ (ON)}$	V_{GS} = −4.5 V, I_D = −2.2 A	—	32	42	mΩ
		$R_{DS\ (ON)}$	V_{GS} = −10 V, I_D = −2.2 A	—	25	33	
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = −10 V, I_D = −2.2 A	6	12	—	S
Input capacitance		C_{iss}	V_{DS} = −10 V, V_{GS} = 0 V, f = 1 MHz	—	1540	—	pF
Reverse transfer capacitance		C_{rss}		—	220	—	
Output capacitance		C_{oss}		—	250	—	
Switching time	Rise time	t_r		—	5.0	—	ns
	Turn-ON time	t_{on}		—	13	—	
	Fall time	t_f		—	35	—	
	Turn-OFF time	t_{off}		—	125	—	
Total gate charge (Gate-source plus gate-drain)		Q_g	V_{DD} ≈ −24 V, V_{GS} = −10 V, I_D = −4.5 A	—	40	—	nC
Gate-source charge 1		Q_{gs1}		—	4.4	—	
Gate-drain ("miller") charge		Q_{gd}		—	8.2	—	

Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain reverse current	Pulse (Note 1)	I_{DRP}	—	—	—	−18	A
Forward voltage (diode)		V_{DSF}	I_{DR} = −4.5 A, V_{GS} = 0 V	—	—	1.2	V

N-ch

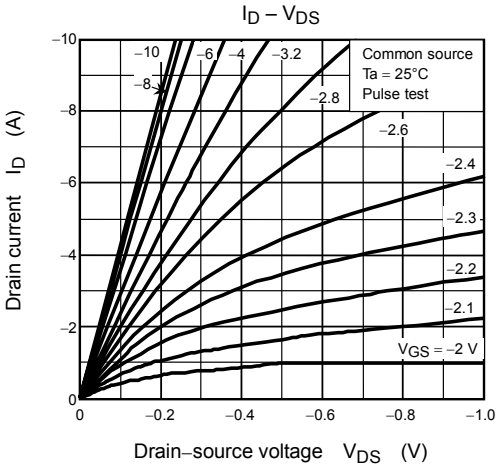
Electrical Characteristics (Ta = 25°C)

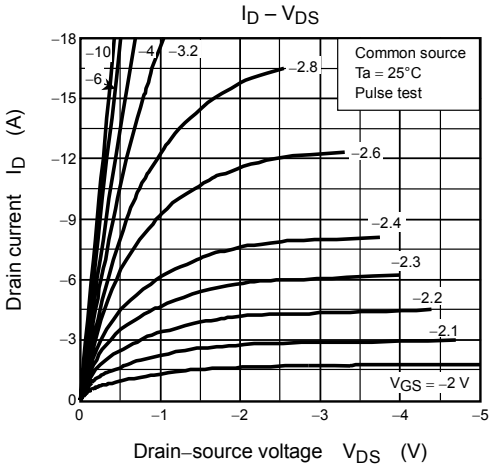
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±10	μA
Drain cut-OFF current		I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V	—	—	10	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	30	—	—	V
		$V_{(BR)\ DSX}$	I_D = 10 mA, V_{GS} = −20 V	15	—	—	
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	1.3	—	2.5	V
Drain-source ON resistance		$R_{DS\ (ON)}$	V_{GS} = 4.5 V, I_D = 3 A	—	25	33	mΩ
		$R_{DS\ (ON)}$	V_{GS} = 10 V, I_D = 3 A	—	20	26	
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 3 A	7	14	—	S
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	1240	—	pF
Reverse transfer capacitance		C_{rss}		—	180	—	
Output capacitance		C_{oss}		—	230	—	
Switching time	Rise time	t_r		—	4.5	—	ns
	Turn-ON time	t_{on}		—	12.5	—	
	Fall time	t_f		—	6.6	—	
	Turn-OFF time	t_{off}		—	33	—	
Total gate charge (Gate-source plus gate-drain)		Q_g	V_{DD} ≈ 24 V, V_{GS} = 10 V, I_D = 6 A	—	27	—	nC
Gate-source charge 1		Q_{gs1}		—	3.9	—	
Gate-drain ("miller") charge		Q_{gd}		—	7.0	—	

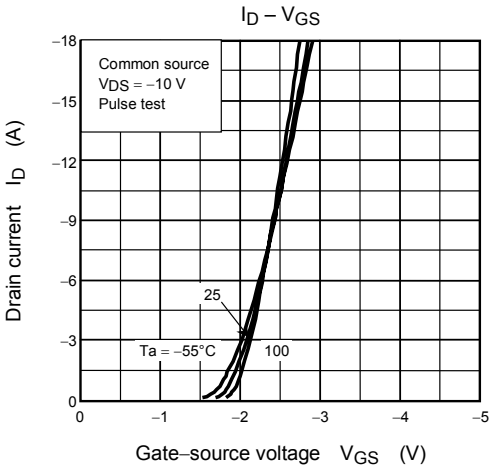
Source-Drain Ratings and Characteristics (Ta = 25°C)

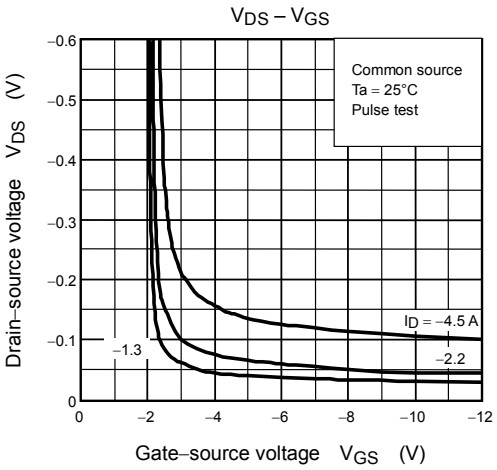
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain reverse current	Pulse (Note 1)	I_{DRP}	—	—	—	24	A
Forward voltage (diode)		V_{DSF}	I_{DR} = 6 A, V_{GS} = 0 V	—	—	−1.2	V

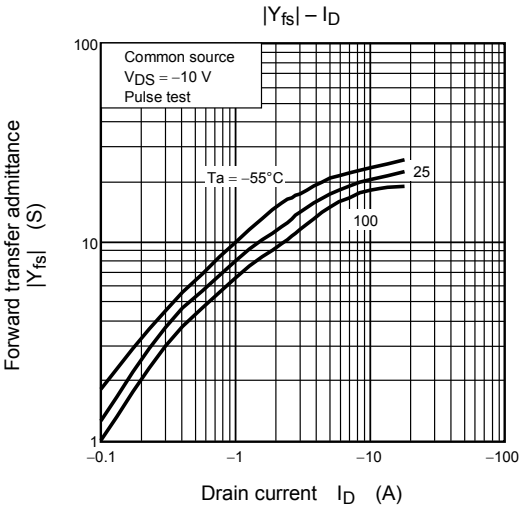
P-ch

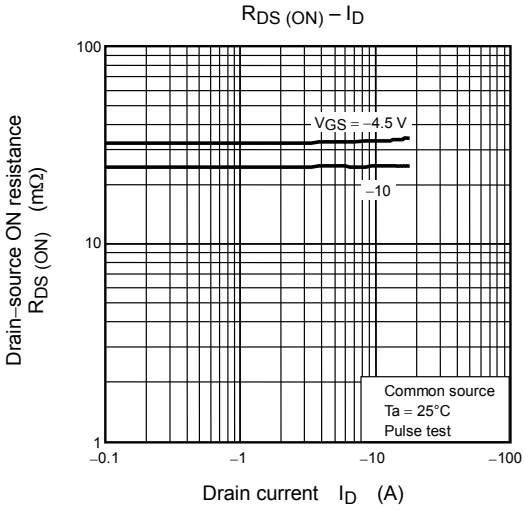

$I_D - V_{DS}$
Common source
Ta = 25°C
Pulse test
−10
−8
−6
−4
−3.2
−2.8
−2.6
−2.4
−2.3
−2.2
−2.1
V_{GS} = −2 V
Drain current I_D (A)
Drain−source voltage V_{DS} (V)


$I_D - V_{DS}$
Common source
Ta = 25°C
Pulse test
−10
−6
−4
−3.2
−2.8
−2.6
−2.4
−2.3
−2.2
−2.1
V_{GS} = −2 V
Drain current I_D (A)
Drain−source voltage V_{DS} (V)

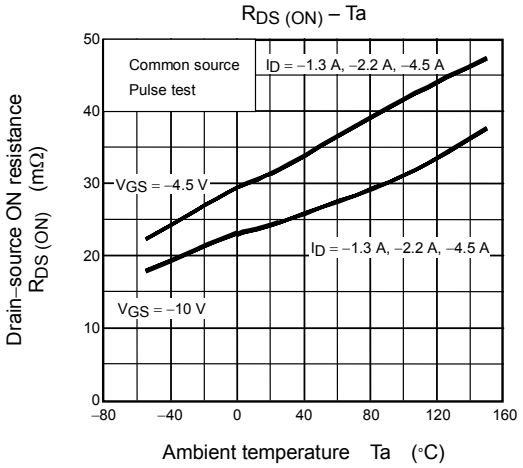

$I_D - V_{GS}$
Common source
V_{DS} = −10 V
Pulse test
25
Ta = −55°C
100
Drain current I_D (A)
Gate−source voltage V_{GS} (V)

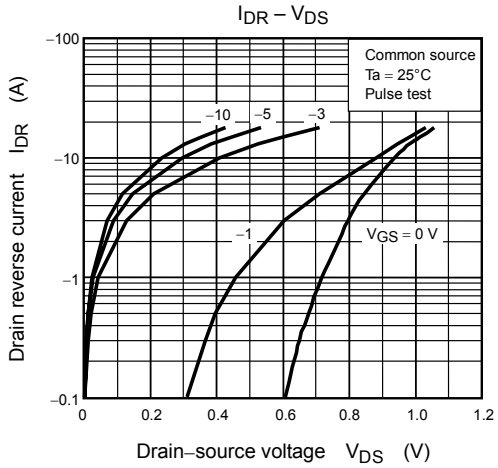

$V_{DS} - V_{GS}$
Common source
Ta = 25°C
Pulse test
I_D = −4.5 A
−2.2
−1.3
Drain−source voltage V_{DS} (V)
Gate−source voltage V_{GS} (V)

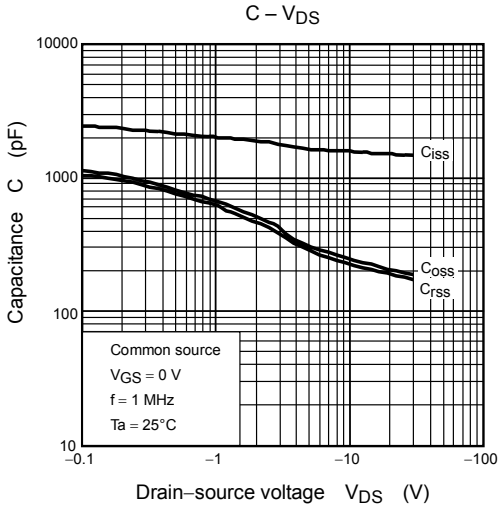

$|Y_{fs}| - I_D$
Common source
V_{DS} = −10 V
Pulse test
Ta = −55°C
25
100
Forward transfer admittance $|Y_{fs}|$ (S)
Drain current I_D (A)

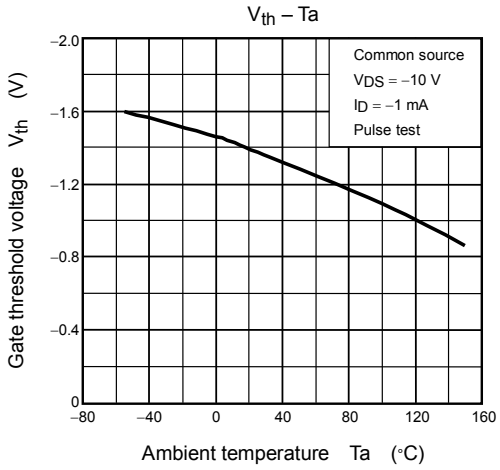

$R_{DS\ (ON)} - I_D$
V_{GS} = −4.5 V
−10
Common source
Ta = 25°C
Pulse test
Drain−source ON resistance $R_{DS\ (ON)}$ (mΩ)
Drain current I_D (A)

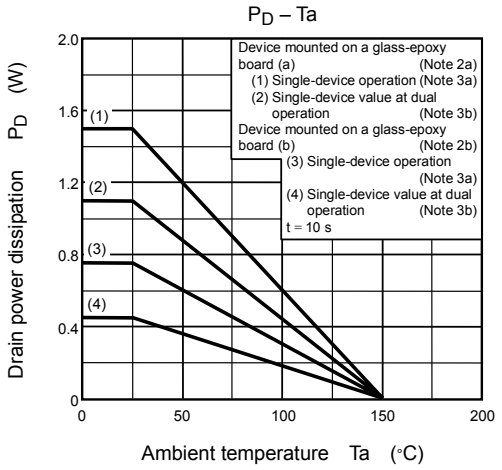
P-ch

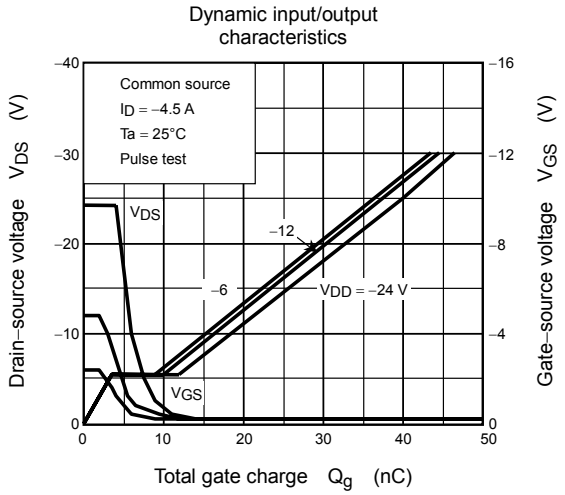

RDS (ON) – Ta
Common source
Pulse test
ID = −1.3 A, −2.2 A, −4.5 A
VGS = −4.5 V
ID = −1.3 A, −2.2 A, −4.5 A
VGS = −10 V
Drain−source ON resistance RDS (ON) (mΩ)
Ambient temperature Ta (°C)


IDR – VDS
Common source
Ta = 25°C
Pulse test
−10
−5
−3
−1
VGS = 0 V
Drain reverse current IDR (A)
Drain−source voltage VDS (V)

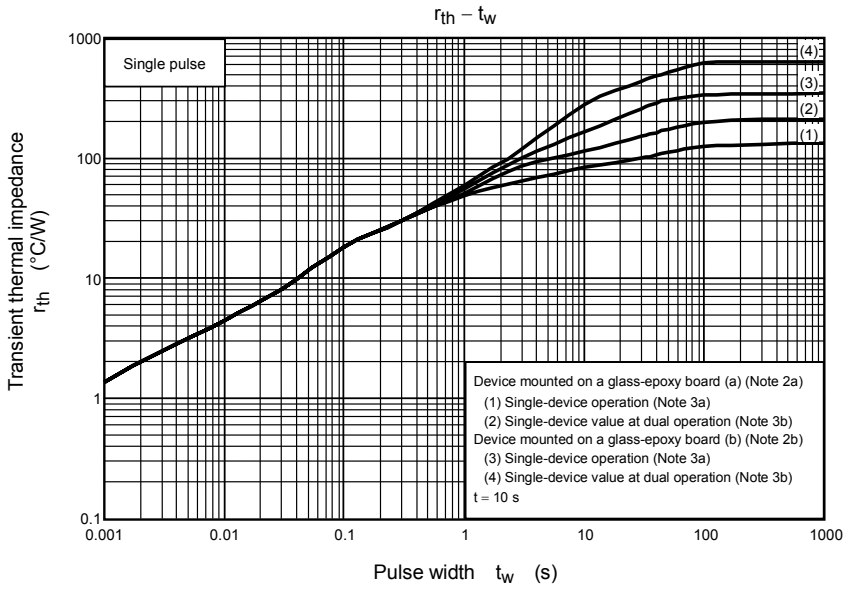

C – VDS
Ciss
Coss
Crss
Common source
VGS = 0 V
f = 1 MHz
Ta = 25°C
Capacitance C (pF)
Drain−source voltage VDS (V)

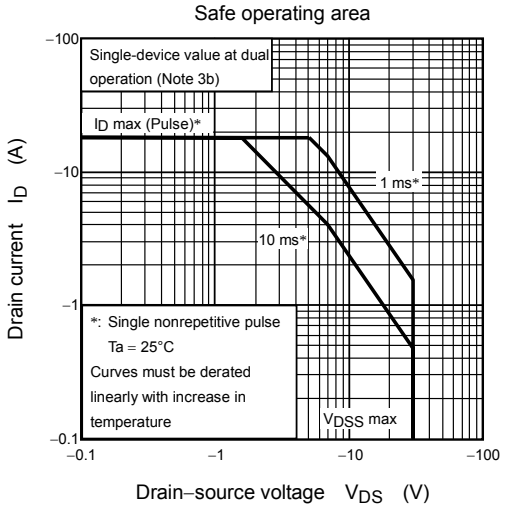

Vth – Ta
Common source
VDS = −10 V
ID = −1 mA
Pulse test
Gate threshold voltage Vth (V)
Ambient temperature Ta (°C)


PD – Ta
Device mounted on a glass-epoxy board (a) (Note 2a)
(1) Single-device operation (Note 3a)
(2) Single-device value at dual operation (Note 3b)
Device mounted on a glass-epoxy board (b) (Note 2b)
(3) Single-device operation (Note 3a)
(4) Single-device value at dual operation (Note 3b)
t = 10 s
(1)
(2)
(3)
(4)
Drain power dissipation PD (W)
Ambient temperature Ta (°C)

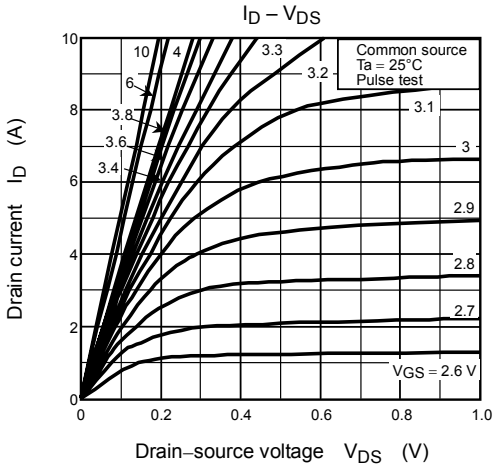

Dynamic input/output characteristics
Common source
ID = −4.5 A
Ta = 25°C
Pulse test
VDS
−12
−6
VDD = −24 V
VGS
Drain−source voltage VDS (V)
Gate−source voltage VGS (V)
Total gate charge Qg (nC)

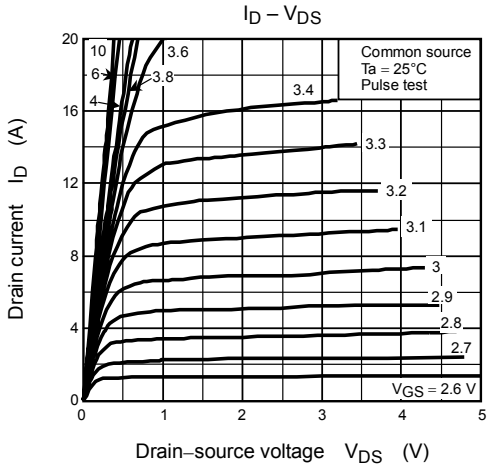
P-ch

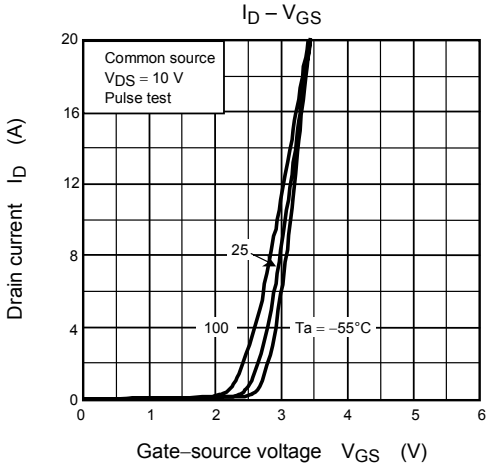

rth – tw
Single pulse
(4)
(3)
(2)
(1)
Transient thermal impedance rth (°C/W)
1000
100
10
1
0.1
0.001
0.01
0.1
1
10
100
1000
Pulse width tw (s)
Device mounted on a glass-epoxy board (a) (Note 2a)
(1) Single-device operation (Note 3a)
(2) Single-device value at dual operation (Note 3b)
Device mounted on a glass-epoxy board (b) (Note 2b)
(3) Single-device operation (Note 3a)
(4) Single-device value at dual operation (Note 3b)
t = 10 s

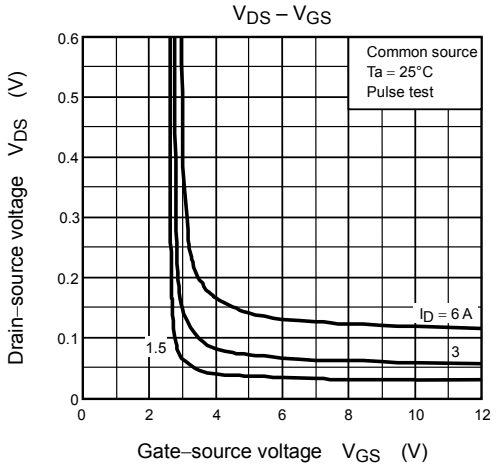

Safe operating area
Single-device value at dual operation (Note 3b)
ID max (Pulse)*
1 ms*
10 ms*
*: Single nonrepetitive pulse
Ta = 25°C
Curves must be derated linearly with increase in temperature
VDSS max
Drain current ID (A)
−100
−10
−1
−0.1
−0.1
−1
−10
−100
Drain−source voltage VDS (V)

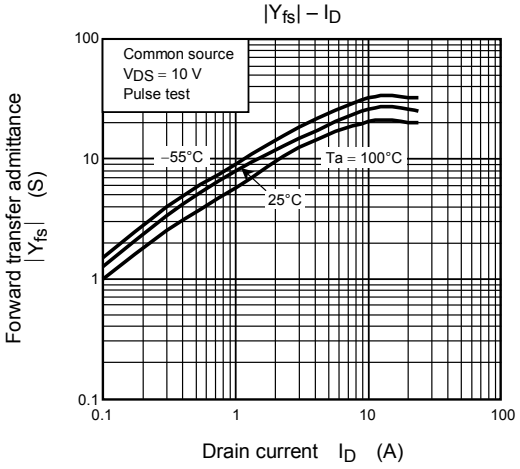
N-ch

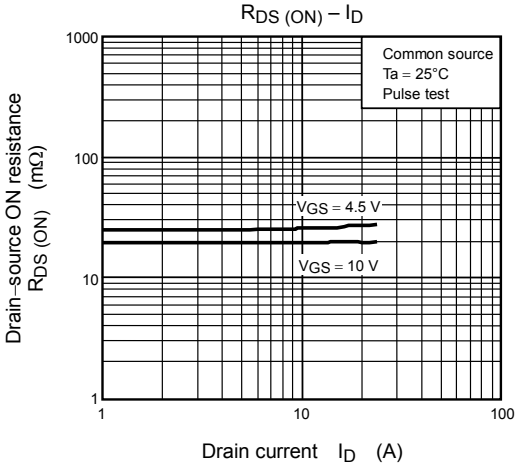

$I_D - V_{DS}$
Common source
Ta = 25°C
Pulse test
10
4
6
3.8
3.6
3.4
3.3
3.2
3.1
3
2.9
2.8
2.7
V_{GS} = 2.6 V
Drain current I_D (A)
Drain−source voltage V_{DS} (V)


$I_D - V_{DS}$
Common source
Ta = 25°C
Pulse test
10
6
4
3.8
3.6
3.4
3.3
3.2
3.1
3
2.9
2.8
2.7
V_{GS} = 2.6 V
Drain current I_D (A)
Drain−source voltage V_{DS} (V)


$I_D - V_{GS}$
Common source
V_{DS} = 10 V
Pulse test
25
100
Ta = −55°C
Drain current I_D (A)
Gate−source voltage V_{GS} (V)

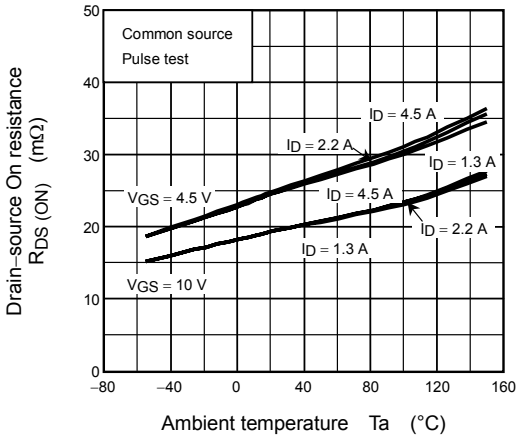

$V_{DS} - V_{GS}$
Common source
Ta = 25°C
Pulse test
I_D = 6 A
3
1.5
Drain−source voltage V_{DS} (V)
Gate−source voltage V_{GS} (V)


$|Y_{fs}| - I_D$
Common source
V_{DS} = 10 V
Pulse test
−55°C
Ta = 100°C
25°C
Forward transfer admittance $|Y_{fs}|$ (S)
Drain current I_D (A)

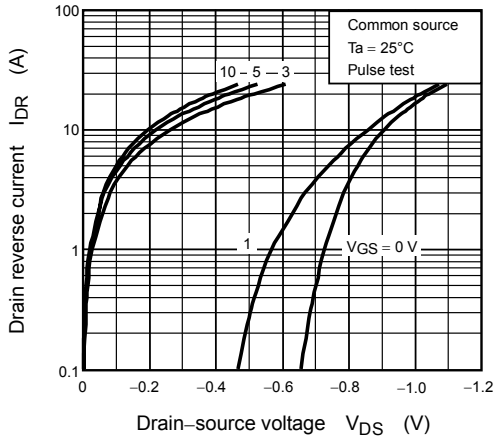

$R_{DS\ (ON)} - I_D$
Common source
Ta = 25°C
Pulse test
V_{GS} = 4.5 V
V_{GS} = 10 V
Drain−source ON resistance $R_{DS\ (ON)}$ (mΩ)
Drain current I_D (A)

N-ch

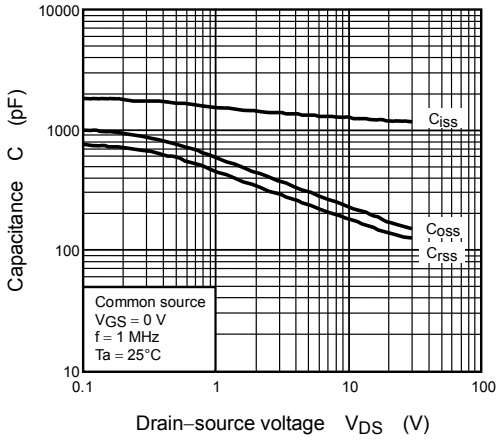
$R_{DS\ (ON)}$ – Ta



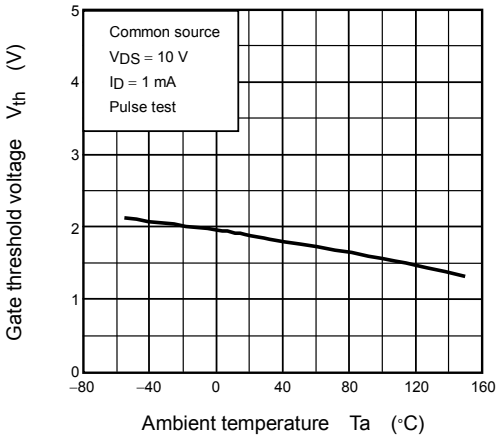
I_{DR} – V_{DS}



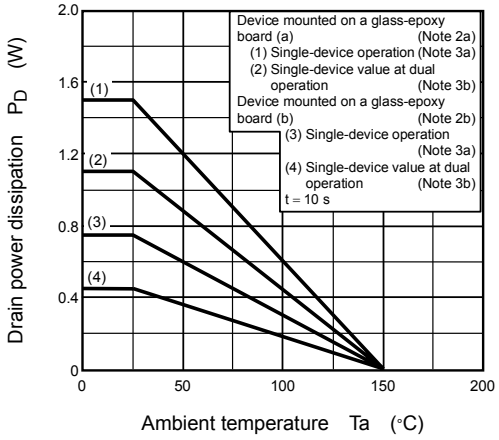
C – V_{DS}



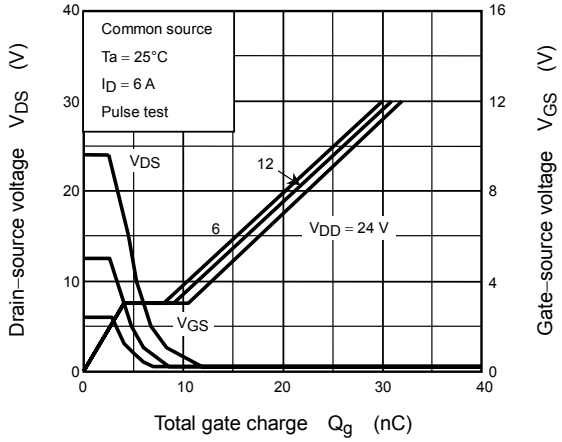
V_{th} – Ta



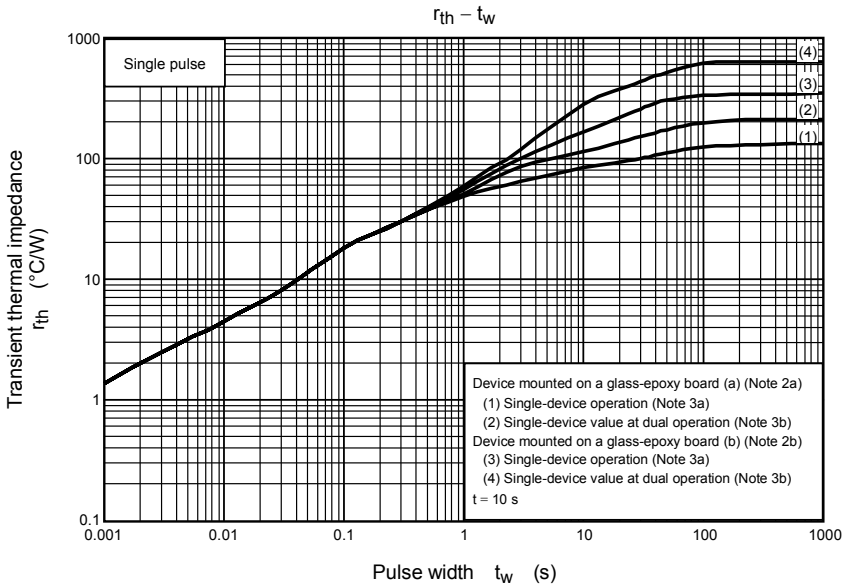
P_D – Ta

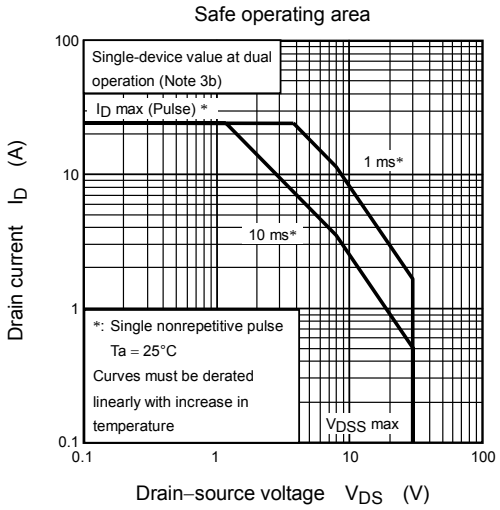


Dynamic input/output characteristics



N-ch


rth – tw
Single pulse
(4)
(3)
(2)
(1)
Transient thermal impedance rth (°C/W)
1000
100
10
1
0.1
0.001
0.01
0.1
1
10
100
1000
Pulse width tw (s)
Device mounted on a glass-epoxy board (a) (Note 2a)
(1) Single-device operation (Note 3a)
(2) Single-device value at dual operation (Note 3b)
Device mounted on a glass-epoxy board (b) (Note 2b)
(3) Single-device operation (Note 3a)
(4) Single-device value at dual operation (Note 3b)
t = 10 s


Safe operating area
Single-device value at dual operation (Note 3b)
ID max (Pulse) *
1 ms*
10 ms*
*: Single nonrepetitive pulse
Ta = 25°C
Curves must be derated linearly with increase in temperature
VDSS max
Drain current ID (A)
100
10
1
0.1
0.1
1
10
100
Drain−source voltage VDS (V)

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