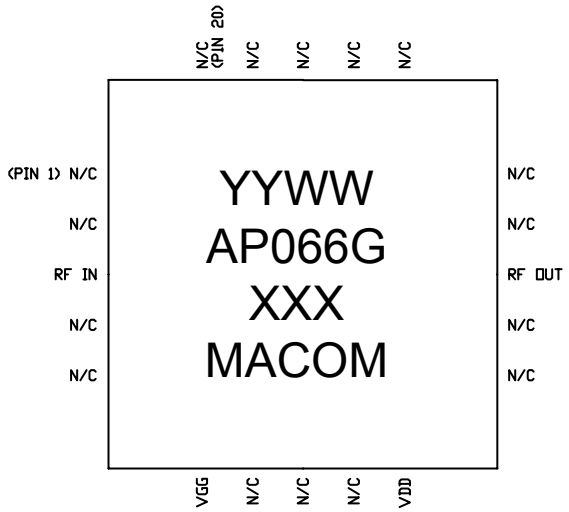
Amplifier, Power, 2.0W 2.5-5.0 GHz

Features

- 2.0 Watt Saturated Output Power Level
- Variable Drain Voltage (6-10V) Operation
- MSAG™ Process
- 5x5 mm 20 Lead PQFN Package



Description

The MAAP-000066-PKG003 is a 4-stage 2.0 W power amplifier with on-chip bias networks in a 20 lead PQFN package, allowing easy assembly. This product is fully matched to 50 ohms on both the input and output. It can be used as a power amplifier stage or as a driver stage in high power applications.

Each device is 100% RF tested to ensure performance compliance. The part is fabricated using M/A-COM's GaAs Multifunction Self-Aligned Gate (MSAG™) Process.

The 5 mm PQFN package has a lead-free lead finish that is RoHS compliant and compatible with a 260°C reflow temperature. The package also features low lead inductance and an excellent thermal path. The MTTF is 1,000,000 hours at 170°C.

Primary Applications

- **Point-to-Point Radios**
- **Point-to-Multipoint Radios**
- **SatCom**
- **Broadband Wireless Access**

Also Available in:

		SAMPLE BOARD
Description	**Die**	**Plastic Package**
Part Number	MAAPGM0066-DIE	MAAP-000066-SMB003

Electrical Characteristics: T_C = 30°C[1], Z_0 = 50Ω, V_{DD} = 8V, I_{DQ} = 660 mA[2], P_{in} = 6dBm, R_G = 150Ω

Parameter	Symbol	Typical	Units
Bandwidth	f	2.5-5.0	GHz
Output Power	P_{OUT}	33.5	dBm
Power Added Efficiency	PAE	30	%
1-dB Compression Point	P1dB	33	dBm
Small Signal Gain	G	28	dB
Input VSWR	VSWR	1.5:1	—
Output VSWR	VSWR	2.5:1	—
Gate Supply Current	I_{GG}	< 10	mA
Drain Supply Current	I_{DD}	< 1	A
Output Third Order Intercept	IP3	42	dBm
3rd Order Intermodulation Distortion, Single Carrier Level = 23 dBm	IM3	-17	dBm

1. **T_C = Case Temperature.**
2. **Adjust V_{GG} between –2.6 to-1.2 to achieve indicated I_{DQ}.**

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Maximum Ratings[3]

Parameter	Symbol	Absolute Maximum	Units
Input Power	P_{IN}	11.0	dBm
Drain Supply Voltage	V_{DD}	+12.0	V
Gate Supply Voltage	V_{GG}	-3.0	V
Quiescent Drain Current (No RF)	I_{DQ}	1.04	A
Quiescent DC Power Dissipated (No RF)	P_{DISS}	10.4	W
Junction Temperature	T_J	170	°C
Storage Temperature	T_{STG}	-55 to +150	°C

3. Operation beyond these limits may result in permanent damage to the part.

Recommended Operating Conditions[4]

Characteristic	Symbol	Min	Typ	Max	Unit
Drain Supply Voltage	V_{DD}	6.0	8.0	10.0	V
Gate Supply Voltage	V_{GG}	-2.6	-1.7	-1.2	V
Input Power	P_{IN}		6	9	dBm
Thermal Resistance	Θ_{JC}		12.8		°C/W
Case Temperature	T_B			Note 5	°C

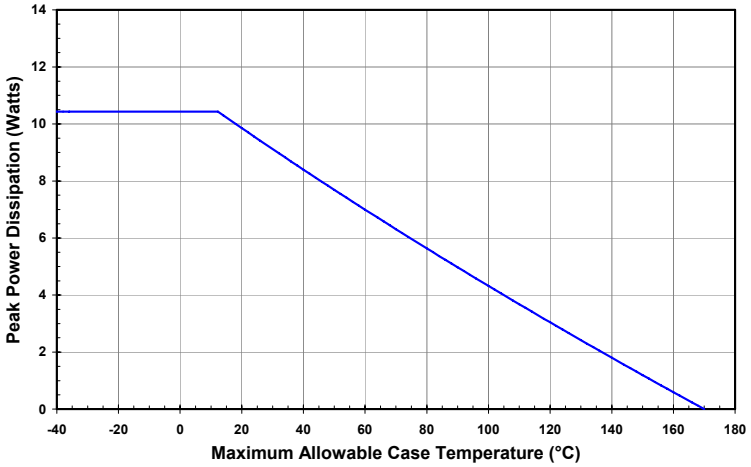
4. Operation outside of these ranges may reduce product reliability.
5. Case Temperature = 170°C — Θ_{JC}* V_{DD} * I_{DQ}

Operating Instructions

This device is static sensitive. Please handle with care.
To operate the device, follow these steps.

1. Apply V_{GG} = -1.7 V, V_{DD}= 0 V.
2. Ramp V_{DD} to desired voltage, typically 8 V.
3. Adjust V_{GG} to set I_{DQ}, (approxmately @ –1.7V).
4. Set RF input.
5. Power down sequence in reverse. Turn gate voltage off last.

Power Derating Curve, Quiescent (No RF)



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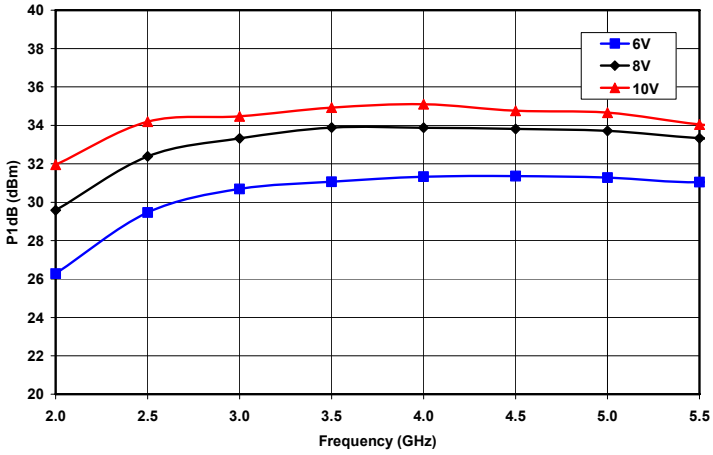

Figure 1. 1 dB Compression Point vs. Frequency and Drain Voltage at IDQ = 660mA

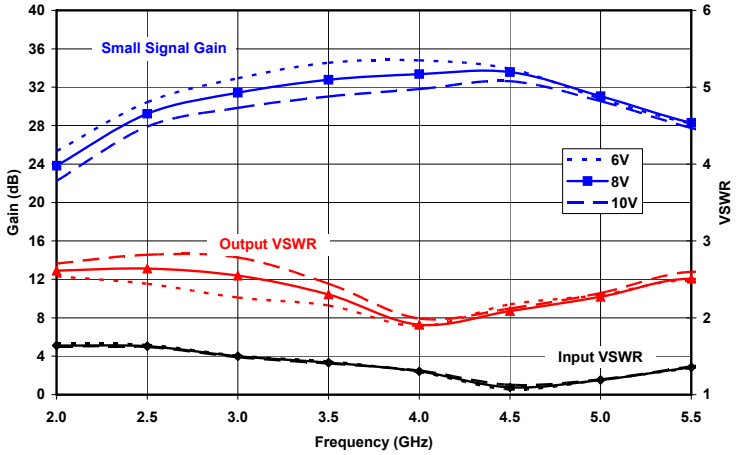

Figure 2. Small Signal Gain and Input & Output VSWR vs. Frequency and Drain Voltage at IDQ = 660mA

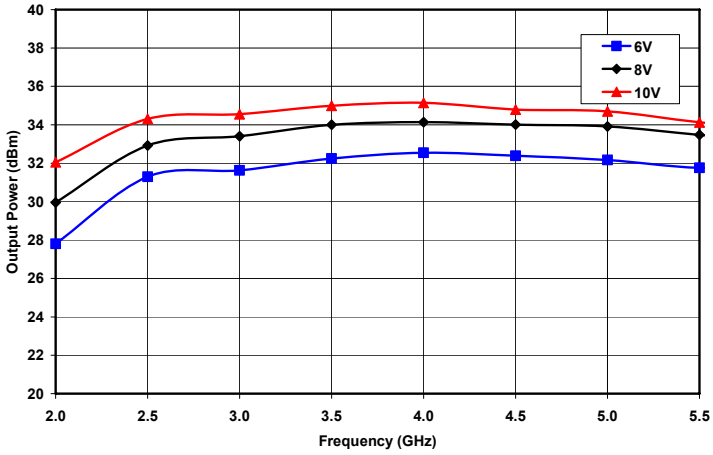

Figure 3. Saturated Output Power vs. Frequency and Drain Voltage at IDQ = 660mA

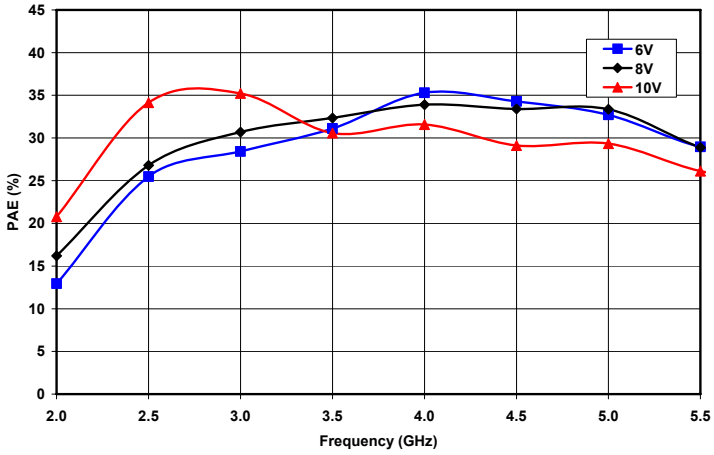

Figure 4. Saturated Power Added Efficiency vs. Frequency and Drain Voltage at IDQ = 660mA

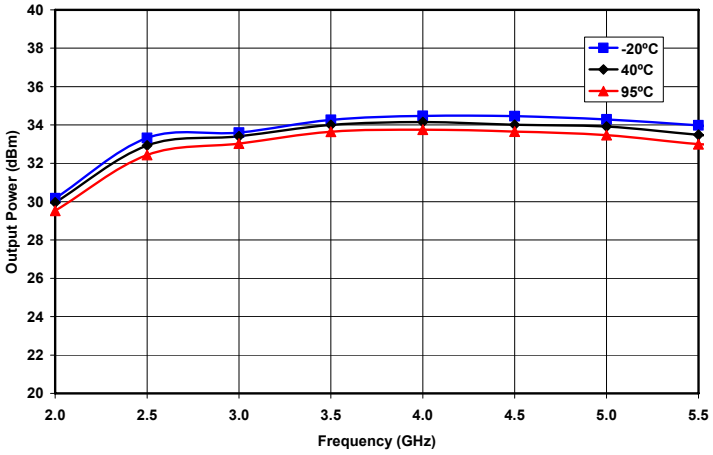

Figure 5. Saturated Output Power vs. Frequency and Case Temperature at VD = 8V and IDQ = 660mA

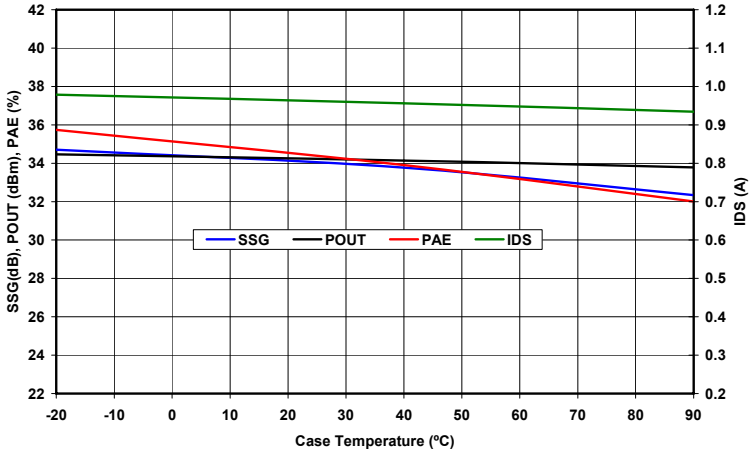

Figure 6. Small Signal Gain & Saturated Output Power, Power Added Efficiency and Drain Current vs. Case Temperature at 4.0 GHZ, VD = 8V and IDQ = 660mA

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VD = 6V

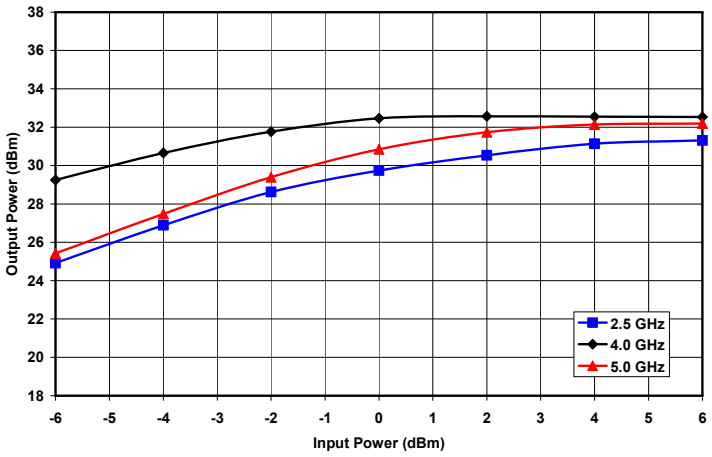

Figure 7. Output Power vs. Input Power and Frequency at VD = 6V and IDQ = 660mA

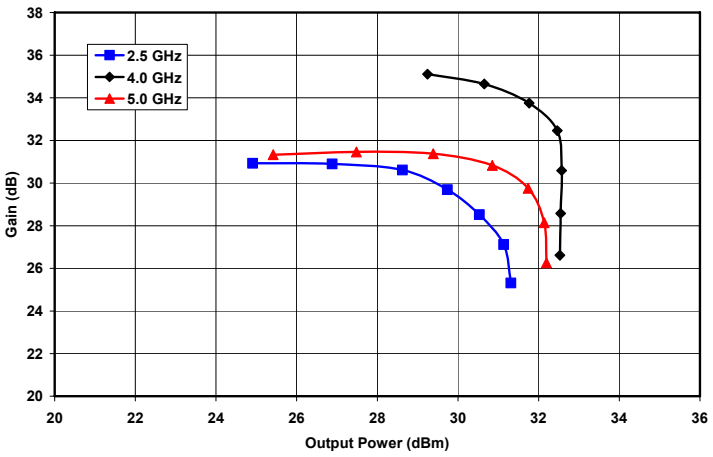

Figure 8. Gain vs. Output Power and Frequency at VD = 6V and IDQ = 660mA

VD = 8V

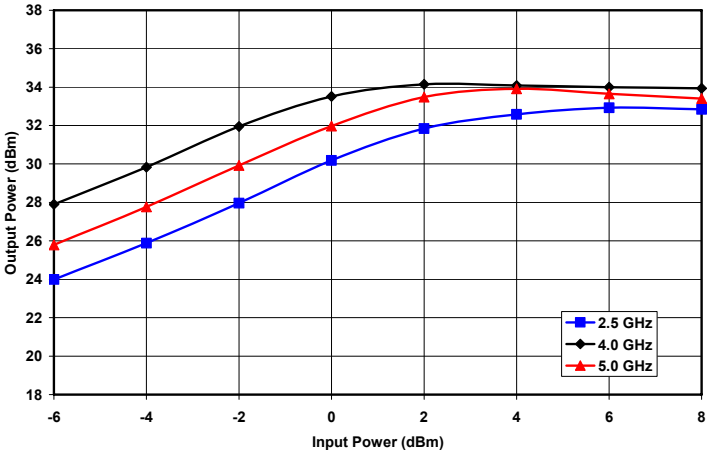

Figure 9. Output Power vs. Input Power and Frequency at VD = 8V and IDQ = 660mA

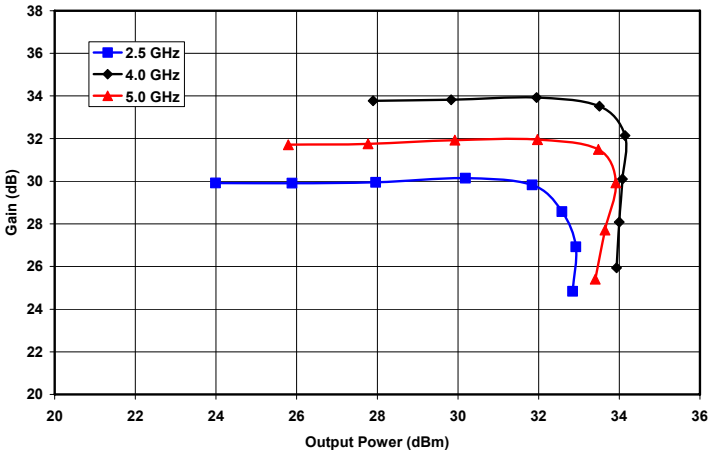

Figure 10. Gain vs. Output Power and Frequency at VD = 8V and IDQ = 660mA

VD = 10V

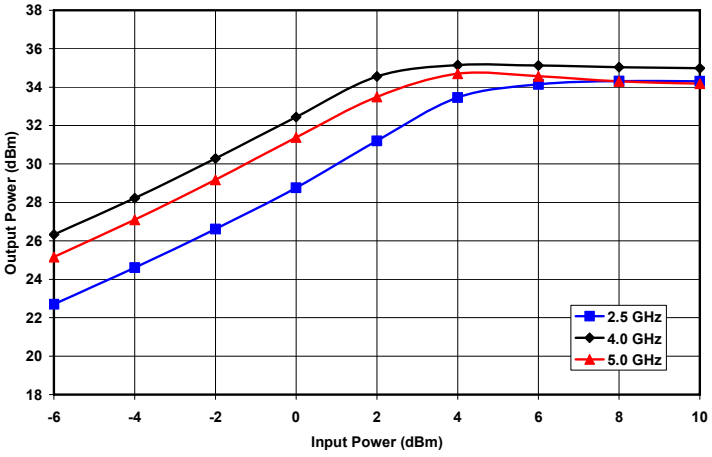

Figure 11. Output Power vs. Input Power and Frequency at VD = 10V and IDQ = 660mA

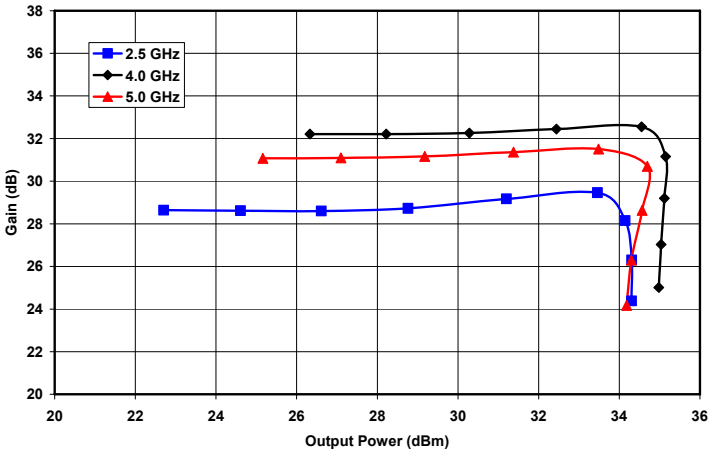

Figure 12. Gain vs. Output Power and Frequencyat VD = 10V and IDQ = 660mA

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VD = 6V

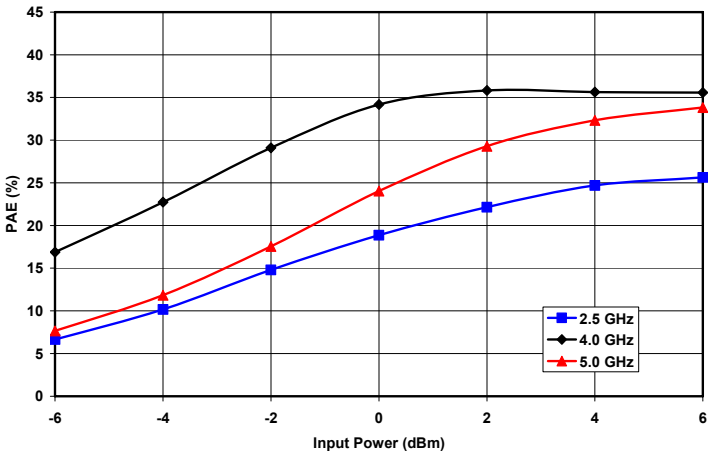

Figure 13. Power Added Efficiency vs. Input Power and Frequency at VD = 6V and IDQ = 660mA

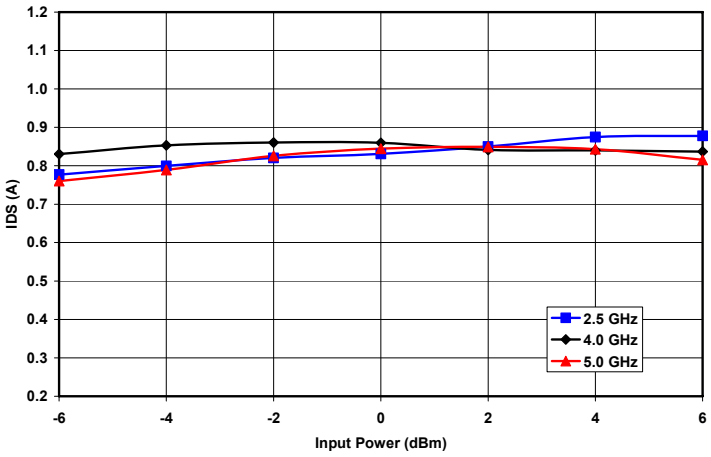

Figure 14. Drain Current vs. Input Power and Frequency at VD = 6V and IDQ = 660mA

VD = 8V

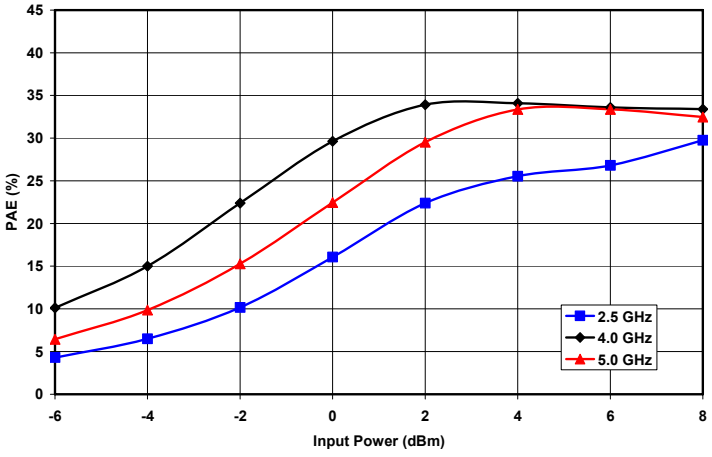

Figure 15. Power Added Efficiency vs. Input Power and Frequency at VD = 8V and IDQ = 660mA

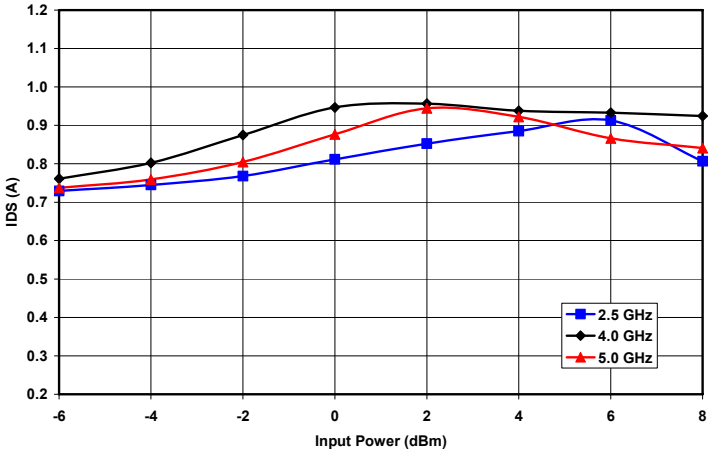

Figure 16. Drain Current vs. Input Power and Frequency at VD = 8V and IDQ = 660mA

VD = 10V

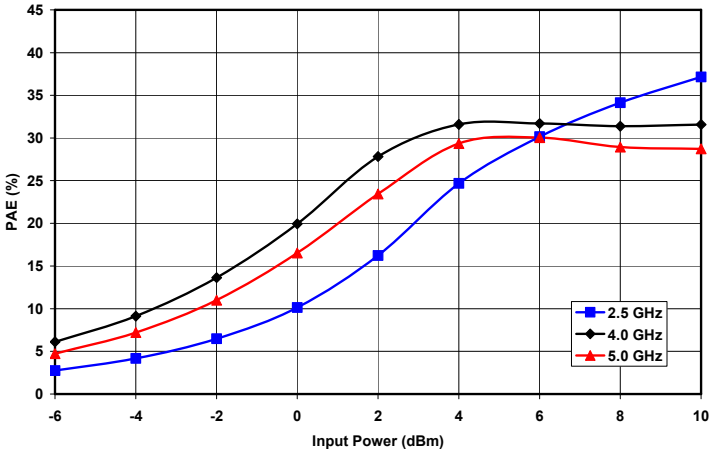

Figure 17. Power Added Efficiency vs. Input Power and Frequency at VD = 10V and IDQ = 660mA

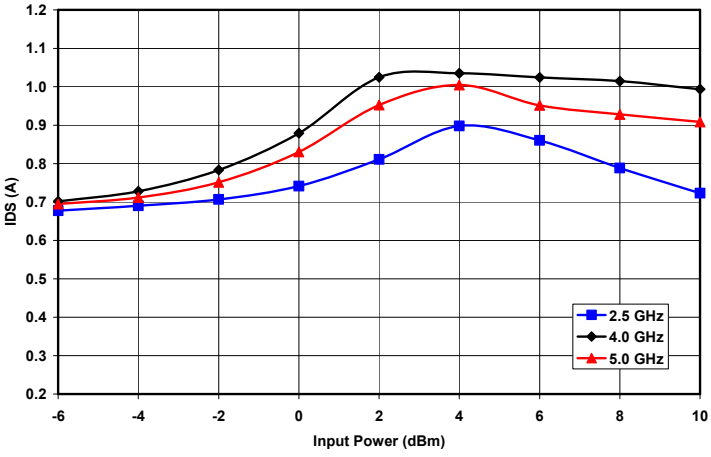

Figure 18. Drain Current vs. Input Power and Frequency at VD = 10V and IDQ = 660mA

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VD = 6V

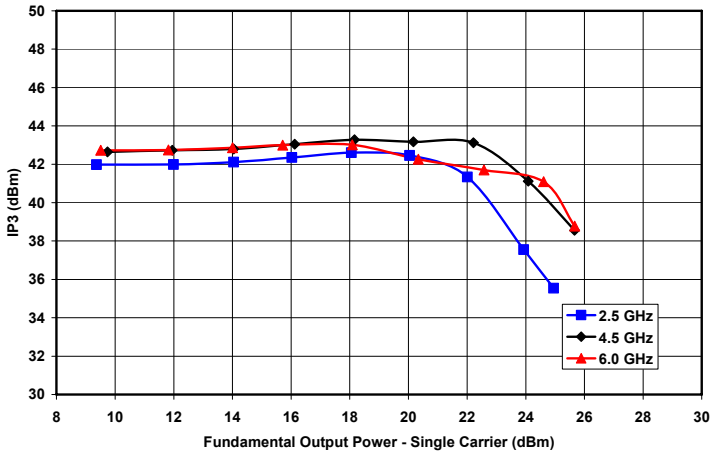

Figure 19. Third Order Intercept vs. Output Power and Frequency at VD = 6V and IDQ =660mA

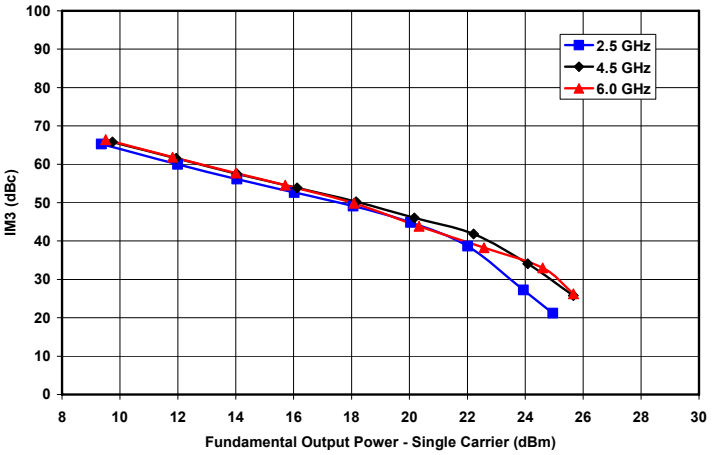

Figure 20. Third Order Intermod vs. Output Power and Frequency at VD = 6V and IDQ =660mA

VD = 8V

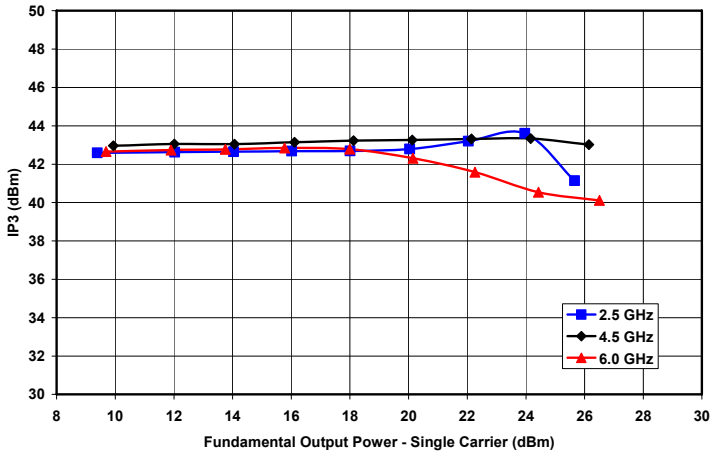

Figure 21. Third Order Intercept vs. Output Power and Frequency at VD = 8V and IDQ =660mA

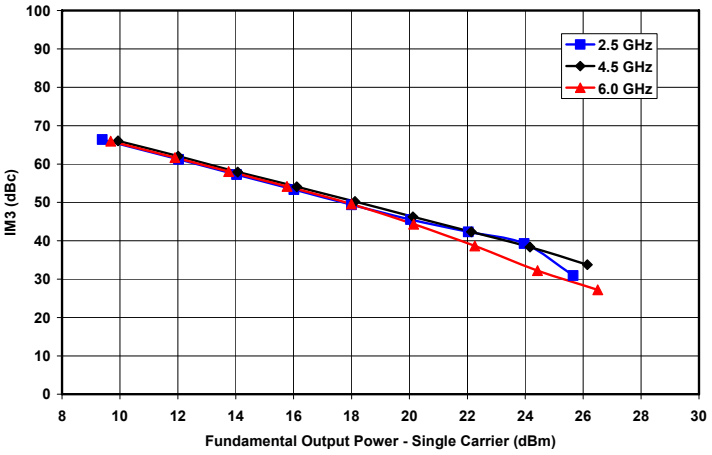

Figure 22. Third Order Intermod vs. Output Power and Frequency at VD = 8V and IDQ =660mA

VD = 10V

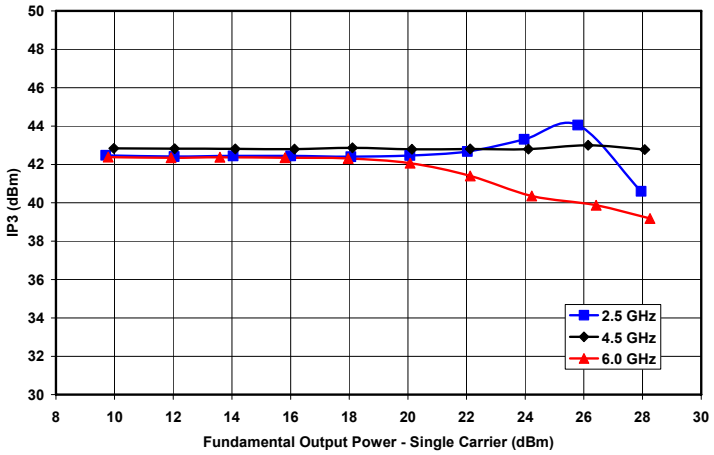

Figure 23. Third Order Intercept vs. Output Power and Frequency at VD = 10V and IDQ =660mA

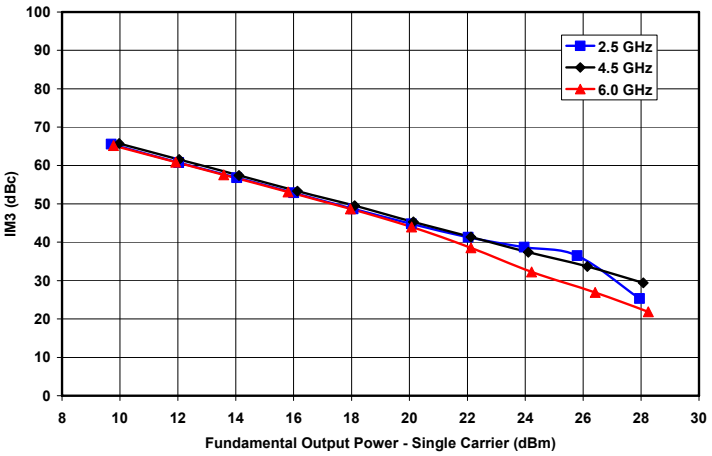

Figure 24. Third Order Intermod vs. Output Power and Frequency at VD = 10V and IDQ =660mA

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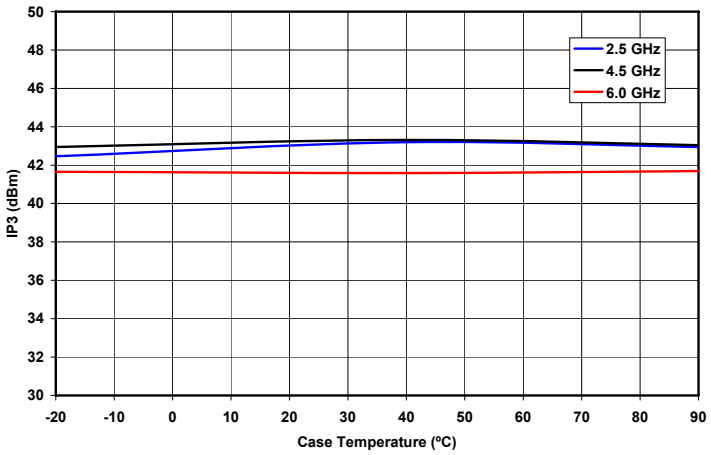

Figure 25. Third Order Intercept vs. Case Temperature and Frequency at Single Carrier Output Power Level = 16 dBm, VD = 8V and IDQ =660mA

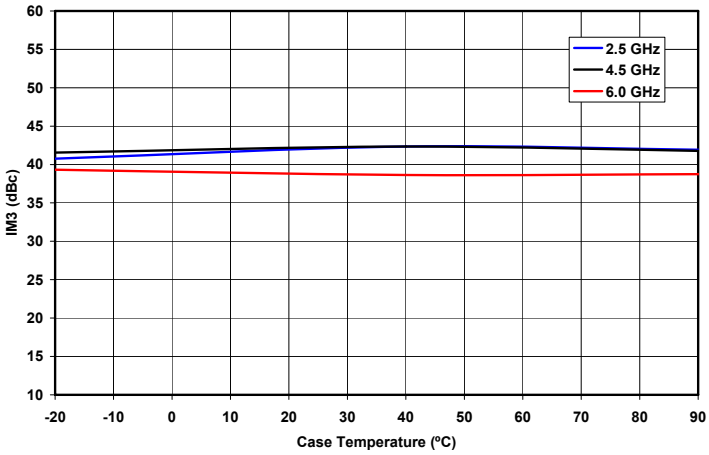

Figure 26. Third Order Intermod vs. Case Temperature and Frequency at Single Carrier Output Power Level = 16 dBm, VD = 8V and IDQ =660mA

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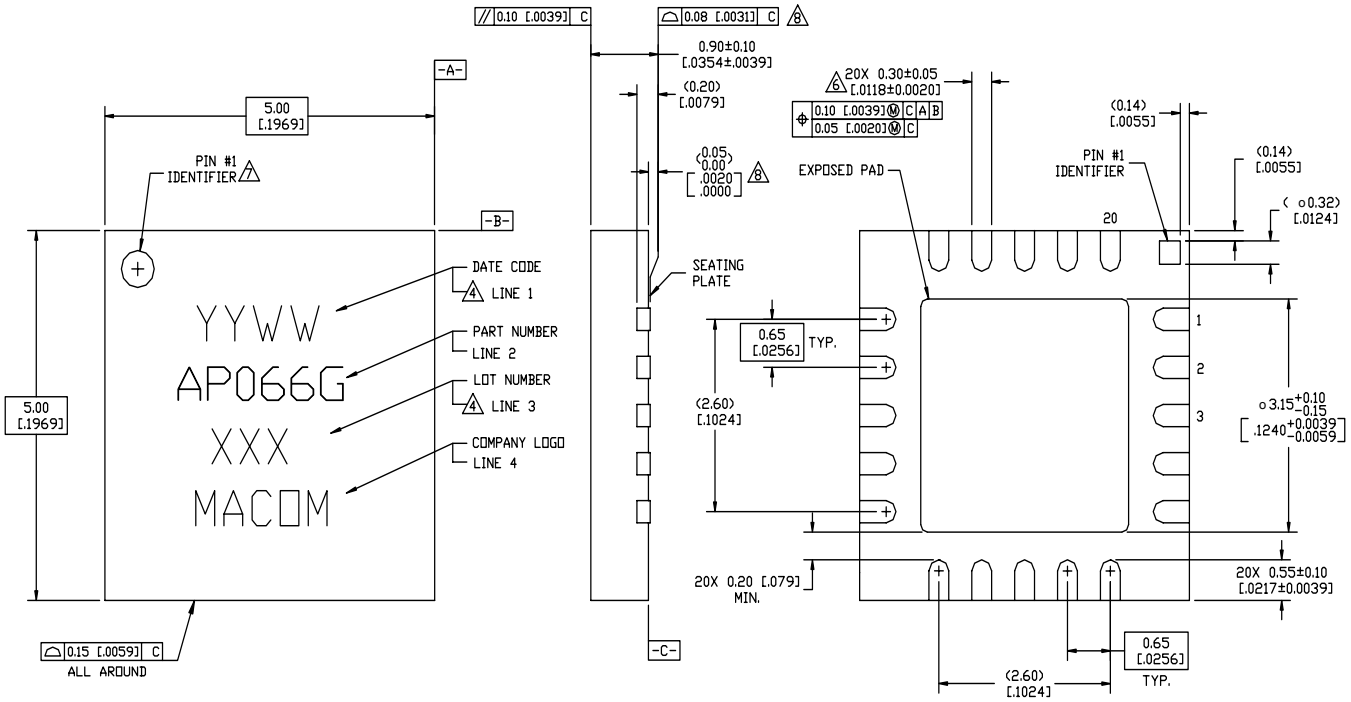

Figure 27. 5x5 mm 20-Lead PQFN.

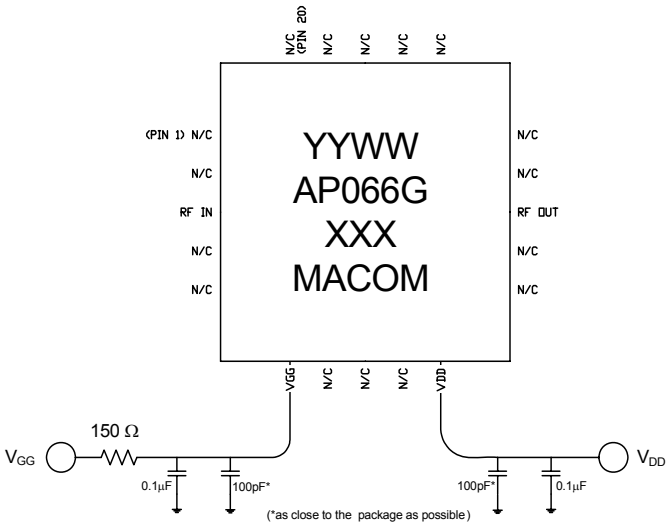

Figure 28. Recommended Bias Configuration.

Note: The exposed pad centered on the package bottom must be connected to RF and dc ground for proper electrical and thermal operation.

Refer to M/A-COM Application Note ***Surface Mounting Instructions for PQFN Packages #S2083**** for assembly guidelines.

Additional Precaution: All parts must receive a bake-out of 125ºC for 24 hours prior to any solder reflow operation.

*Application Notes can be found by going to the Site Search Page of M/A-COM's web page (http://www.macom.com/search/search.jsp) and searching for the required Application Note.

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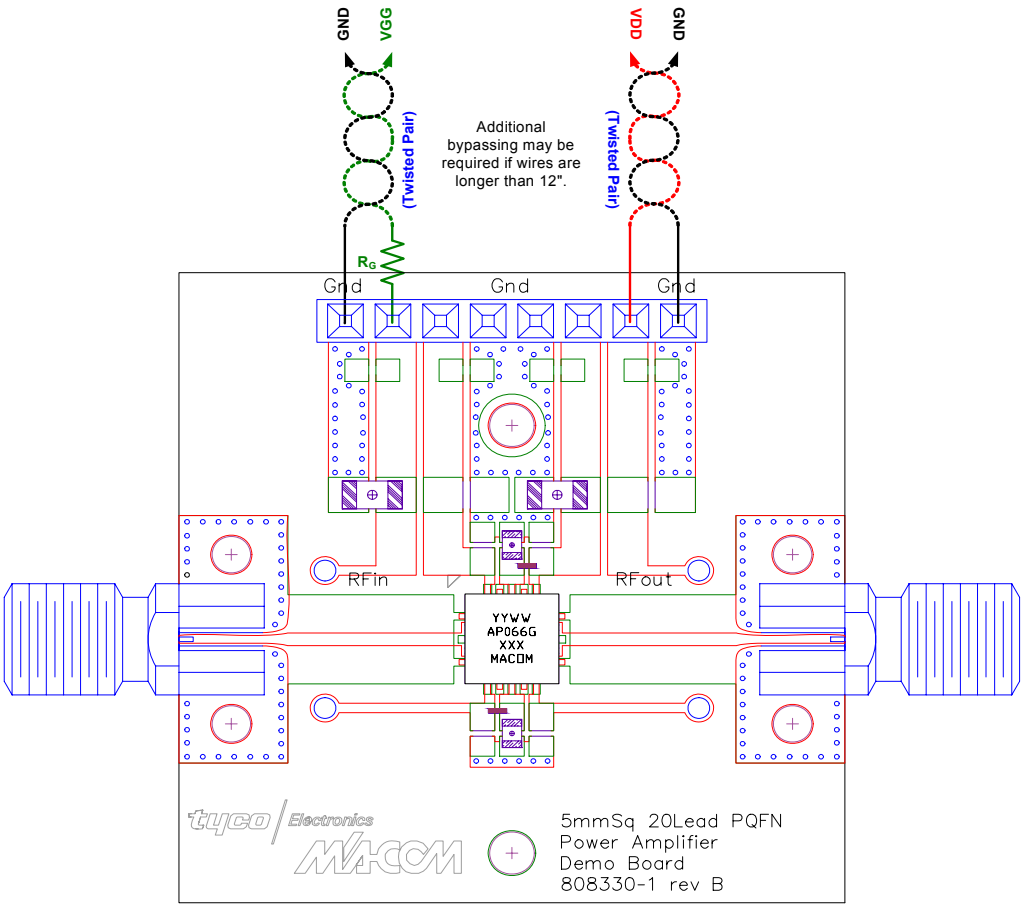

Figure 29. Demonstration Board PN MAAP-000066-SMB003 (available upon request).

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