Electronics

## Features

- Attenuation: 0.5 dB steps to 31.5 dB
- 6 Bit Digital Gain Control
- CMOS Logic
- Serial Logic Interface
- Single Positive Voltage Supply
- 8 mm PBGA Package
- JEDEC MO-151 Footprint
- Single Package Solution for GSM,CDMA,PCS


## Description

The M/A-COM AM55-0024 is a dual channel IF amplifier and digital attenuator packaged in a multilayer multi-chip module (MCM). Gain control is via two separate serial logic interfaces. The part utilizes Plastic Ball Grid Array (PBGA) interconnect technology to achieve high circuit density and superior performance. This device is ideal for GSM/ DCS/PCS digital base station applications where high dynamic range gain control is required.

## Ordering Information ${ }^{1}$

| Part Number | Package |
| :---: | :---: |
| AM55-0024 | Bulk Packaging |
| AM55-0024TR-3000 | 3000 piece reel |

1. Reference Application note M513 for reel size information.

## Functional Block Diagram



## Absolute Maximum Ratings ${ }^{\text {4,5,6}}$

| Parameter | Absolute Maximum |
| :---: | :---: |
| Input Power $^{3}$ | +20 dBm |
| Operating Voltage $^{3}$ | $\mathrm{~V}_{\mathrm{DD}}=+6 \mathrm{~V}$ |
| Operating Temperature $^{\text {Storage Temperature }} 40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |  |
|  | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |

4. Exceeding any one or combination of these limits may cause permanent damage to this device.
5. M/A-COM does not recommend sustained operation near these survivability limits.
6. Ambient Temperature $\left(\mathrm{T}_{\mathrm{A}}\right)=+25^{\circ} \mathrm{C}$.

## Pin Out ${ }^{2,3}$

| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| +5V_A1 | DAT_A | CLK_A | +5V_A2 |  |  |  | RF_OUT_A | A |
|  |  |  |  |  |  |  |  | B |
| RF_IN_A |  |  |  |  |  |  |  | C |
| LE_A |  |  |  |  |  |  |  | D |
| RF_IN_B |  |  |  |  |  |  |  | E |
| LE_B |  |  |  |  |  |  |  | F |
| CLK_B |  |  |  |  |  |  |  | G |
| DAT_B | +5V_B1 |  |  | +5V_B2 |  |  | RF_OUT_B | H |

2. All unmarked positions are ground.
3. Table is oriented to reflect the BGA (bottom view) side of the substrate.

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High Dynamic Range, 2 Channel IF Amplifier with Power Control

Electrical Specifications: $\mathrm{T}_{\mathrm{A}}=\mathbf{2 5}^{\circ} \mathrm{C}, \mathrm{Z}_{\mathbf{0}}=50 \Omega$

| Parameter | Test Conditions | Units | Min. | Typ. | Max. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Gain | $100-400 \mathrm{MHz}$ | dB | 19.5 | 22.5 | 24.9 |
| Gain Control Range | $100-400 \mathrm{MHz}$ | dB | - | 31.5 | - |
| Gain Control Step Size | $100-400 \mathrm{MHz}$ | dB | 0 | 0.5 | - |
| Attenuation Accuracy | 0.5-15.5 dB states | dB | 1.5 dB floating window |  |  |
| Attenuation Accuracy (referenced to the nominal attenuation state) | 16.0-23.5 dB states 24.0-31.5 dB states | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~dB} \end{aligned}$ | $\begin{gathered} \pm(0.3+12 \% \text { of atten. state }) \\ \pm(0.3+15.5 \% \text { of atten. state }) \end{gathered}$ |  |  |
| Return Loss | 100-400 MHz | dB | 10 | 12 | - |
| Output $\mathrm{IP}_{3}$ | 100-400 MHz @ 5 V | dBm | - | 30 | - |
| Supply Voltage | - | V | - | 3/5 | - |
| Supply Current | @ 3 V / @ 5 V | mA | - | 300/400 | - |
| Switching Speed | (50\% TTL to 90\% RF) | nS | - | 50 | - |
| Isolation | - | dB | - | 60 | - |
| P1dB | - | dBm | - | 17.5 | - |
| Noise Figure | $100-400 \mathrm{MHz}$ | dB | - | 4 | - |

## Truth Table ${ }^{7,8}$

| State | $\mathbf{1 6} \mathbf{d B}$ | $\mathbf{8} \mathbf{d B}$ | $\mathbf{4} \mathbf{d B}$ | $\mathbf{2} \mathbf{d B}$ | $\mathbf{1} \mathbf{d B}$ | $\mathbf{0 . 5} \mathbf{~ d B}$ (LSB) | Attenuation |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0.5 |
| 2 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 4 | 0 | 0 | 0 | 1 | 0 | 0 | 2 |
| 8 | 0 | 0 | 1 | 0 | 0 | 0 | 4 |
| 16 | 0 | 1 | 0 | 0 | 0 | 0 | 8 |
| 32 | 1 | 0 | 0 | 0 | 0 | 0 | 16 |
| 63 | 1 | 1 | 1 | 1 | 1 | 1 | 31.5 |

7. Differential voltage, V (state 1 ) -V (state 0$)$, must be +3 V minimum.
8. $0=0 \vee$ to $0.2 \mathrm{~V}, 1=+3 \vee$ to 5 V

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PCB Schematic ${ }^{9,10}$

9. All inductors are 470 nH
10. All capacitors are $10,000 \mathrm{pF}$

## Operating Instructions

The AM55-0024 can operate with voltages between +3 V and +5 V . The amplifier voltages are applied to pins A2, A3, B2 and B3 respectively. A1 and B1 supply the Vdd to the logic circuits and thus must be the same levels as the logic driving the Clock, Latch Enable and Data ports. The amplifiers and logic circuits are independent and need not be the same levels.

Clock Diagram ${ }^{11,12,13,14,15}$

11. Max Clock Speed $=40 \mathrm{MHz}$
12. Ton = Toff
13. Tsu $=>3 n s$
14. Thold $=>7 \mathrm{~ns}$
15. Data clocked in on rising clock edge

## Serial Interface

Each channel in the AM55-0024 is independently controllable with a 3 wire serial interface: Clock, Data, and Latch Enable. These lines can be shared based on application requirements. The attenuator within the device is controlled with a 6 bit word, enabling the selection of 64 possible states. The highest gain state is '000000', and the lowest is '111111'. The sequence for shifting the data is as follows: Present data (Least significant bit first), strobe clock, repeat until 6 bits have been presented and clocked, then strobe the latch enable line, which implements the state change.

## 8 mm PBGA

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## Typical Performance Curves

## Input VSWR



## Attenuation (6 individual bits)



Output VSWR


Gain


Noise Figure


