## 250 mW Linear Power Amplifier and T/R Switch 1.8-2.0 GHz

## Features

- Operates Over Full PCN/PCS/PHS Bands
- Operates Over +3 V to +5 V Supply Voltage
- $+24 \mathrm{dBm} \mathrm{P}_{1 \mathrm{~dB}}$ Typical at PA Out
- $35 \%$ PAE @ $\mathrm{P}_{1 \mathrm{~dB}}$ for Linear Operation
- On-Chip T/R Switch, Linear Operation to +30 dBm
- Low Cost SSOP-28 Plastic Package


## Description

M/A-COM's AM55-0004 power amplifier/switch integrates a power amplifier and transmit/receive switch in a low cost SSOP package. The power amplifier delivers +24 dBm of linear power with high efficiency and can be operated at supply voltages as low as 2.7 V . It is ideally suited for QPSK or other linearly modulated systems in the 1.8 to 2.0 GHz frequency band.

The power amplifier/switch is fully monolithic and requires only one output capacitor for power match. The T/R switch achieves good insertion loss and isolation without degrading the overall linearity.

The AM55-0004 is ideally suited for final stage power amplification in linear TDD systems. The integrated switch is convenient for duplexing. The AM55-0004 can also be used as a driver stage for high power systems. Typical applications include Japanese PHS systems or PCN/PCS transmit chains.

M/A-COM's AM55-0004 is fabricated using a mature 0.5 -micron gate length GaAs process. The process features full passivation for increased performance and reliability.

SSOP-28


Dimensions are inches over millimeters.

## Ordering Information

| Part Number | Description |
| :--- | :--- |
| AM55-0004 | SSOP 28-Lead Plastic Package |
| AM55-0004TR | Forward Tape \& Reel $^{*}$ |
| AM55-0004RTR | Reverse Tape \& Reel $^{*}$ |
| AM55-0004SMB | Designer's Kit |

* If specific reel size is required, consult factory for part number assignment.


## Typical Electrical Specifications

Test conditions: Frequency: $1.9 \mathrm{GHz}, \mathrm{V}_{\mathrm{DD} 1}=\mathrm{V}_{\mathrm{DD} 2}=4.8 \mathrm{~V} \pm 10 \%, \mathrm{~V}_{\mathrm{G} 1}$ adjusted for 30 mA quiescent bias on $\mathrm{V}_{\mathrm{DD} 1}$, $\mathrm{V}_{\mathrm{G} 2}$ adjusted for 65 mA quiescent bias on $\mathrm{V}_{\mathrm{DD} 2}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$

| Parameter | Units | Min. | Typ. | Max. |
| :---: | :---: | :---: | :---: | :---: |
| Power Amplifier |  |  |  |  |
| Linear Gain | dB | 22 | 24 |  |
| Power Output @ $\mathrm{P}_{1 \mathrm{~dB}}$ at PA OUT port | dBm | 22.5 | 24 |  |
| Current From Positive Supply @ $\mathrm{P}_{1 \mathrm{~dB}}$ | mA | 75 | 175 | 275 |
| Input VSWR |  |  | 2.0:1 |  |
| T/R Switch |  |  |  |  |
| Insertion Loss | dB |  | 0.6 | 1.0 |
| Input Match |  |  | 1.5:1 |  |
| Isolation | dB | 15 | 20 |  |

## Absolute Maximum Ratings ${ }^{1}$

| Parameter | Absolute Maximum |
| :--- | :---: |
| Max. Input Power ${ }^{2}$ | +23 dBm |
| Operating Voltages ${ }^{2}$ | $\mathrm{~V}_{\mathrm{DD}}=7 \mathrm{~V}$ |
|  | $\mathrm{~V}_{\mathrm{GG}}=-5 \mathrm{~V}$ |
|  | $\mathrm{~V}_{\mathrm{DD}}-\mathrm{V}_{\mathrm{GG}}=8 \mathrm{~V}$ |
| Operating Temperature | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |
| Storage Temperature | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |

1. Exceeding these limits may cause permanent damage.
2. Ambient temperature $\left(\mathrm{T}_{\mathrm{A}}\right)=+25^{\circ} \mathrm{C}$

## Pin Configuration

| Pin No. | Pin Name | Description |
| :---: | :---: | :---: |
| 1 | GND | DC and RF Ground |
| 2 | $\overline{\text { VSW }}$ | Complimentary T/R Switch Control, -4 V Tx mode/0 V Rx mode |
| 3 | GND | DC and RF Ground |
| 4 | Tx IN | Transmit side of T/R switch |
| 5 | GND | DC and RF Ground |
| 6 | GND | DC and RF Ground |
| 7 | ANT IN/OUT | Common port of T/R switch which is connected to the antenna |
| 8 | GND | DC and RF Ground |
| 9 | Rx OUT | Receive side of $T / R$ switch |
| 10 | GND | DC and RF Ground |
| 11 | GND | DC and RF Ground |
| 12 | $\mathrm{V}_{\mathrm{DD} 1}$ | Positive bias for the first stage of PA, +2.7 to +6.0 volts |
| 13 | SAVE Tx | Sleep mode control of first stage of PA ONLY <br> 0 V - first PA stage on <br> -4 V - first PA stage off |
| 14 | GND | DC and RF Ground |
| 15 | GND | DC and RF Ground |
| 16 | PA IN | RF input of the Power Amplifier |
| 17 | GND | DC and RF Ground |
| 18 | $\mathrm{V}_{\mathrm{G} 1}$ | Negative bias control for the first PA stage, voltage divider is on the MMIC, adjusted to set $\mathrm{V}_{\mathrm{DD} 1}$ quiescent bias current, which is typically 30 mA . Input impedance: $10 \mathrm{k} \Omega$ |
| 19 | GND | DC and RF Ground |
| 20 | $\mathrm{V}_{\mathrm{G} 2}$ | Negative bias control for the second PA stage, adjusted to set $\mathrm{V}_{\mathrm{DD} 2}$ quiescent bias current, which is typically 65 mA . <br> Input impedance: $>1 \mathrm{M} \Omega$ |
| 21 | GND | Second Stage DC and RF Ground |
| 22 | GND | Second Stage DC and RF Ground |
| 23 | GND | Second Stage DC and RF Ground |
| 24 | GND | Second Stage DC and RF Ground |
| 25 | PA OUT | RF output of the Power Amplifier |
| 26 | $\mathrm{V}_{\mathrm{DD} 2}$ | Positive bias for the second stage of the PA, +2.7 to +6.0 volts |
| 27 | VSW | T/R Switch Control, 0 V Tx mode/-4 V Rx mode |
| 28 | GND | DC and RF Ground |

## Truth Table

| Operating Mode | VSW | $\overline{\text { VSW }}$ | SAVE Tx |
| :--- | :---: | :---: | :---: |
| PA Tx | X | X | 0 V |
| PA Sleep | X | X | -4.0 Volts |
| T/R Switch Tx | 0 Volts | -4.0 Volts | X |
| T/R Switch Rx | -4.0 Volts | 0 Volts | X |

X - Don’t Care

Functional Diagram and Pin Configuration


## Power Amplifier Small Signal Performance ${ }^{1}$





Power Amplifier CW Performance at 1.9 GHz¹



GAIN COMPRESSION


1. All data measured at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{G} 1}, \mathrm{~V}_{\mathrm{G} 2}$ adjusted for first stage quiescent current of 30 mA and second stage current of 65 mA , respectively.

## Power Amplifier Temperature Performance ${ }^{1}$





Power Amplifier Spurious Response at Various Supply Voltages ${ }^{1}$


3RD HARMONIC RATIO @ 1.9 GHz


1. All data measured at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{G} 1}, \mathrm{~V}_{\mathrm{G} 2}$ adjusted for first stage quiescent current of 30 mA and second stage current of 65 mA , respectively.

## Power Amplifier Spectral Response Under Modulation Drive <br> ( $\pi / 4$ DQPSK, $\alpha=0.5,384 \mathrm{kB} / \mathrm{sec}, 9$-bit PN code)




## Output Power Under Modulation ${ }^{2}$

| $\mathbf{V}_{\mathbf{D}}$ (volts) | $\mathbf{P}_{\mathbf{O U T}}(\mathbf{d B m})$ |
| :---: | :---: |
| 3 | 20.5 |
| 3.6 | 21.4 |
| 4 | 22.2 |
| 4.8 | 23.4 |
| 6 | 23.7 |

1. Spectral output is tested under the following conditions: Modulation scheme is $\pi / 4$ DQPSK with a bit transfer rate of $384 \mathrm{kB} / \mathrm{sec}$ and a root Nyquist filter with $\alpha=0.5$ per RCR STD-28. The spectrum analyzer settings are as follows:

Resolution bandwidth: 10 kHz
Video bandwidth: 100 kHz
Sweep time: 5 seconds
2. This chart documents the modulated output power delivered for a fixed adjacent channel interference (ACI) rejection of 55 dBc at a $600-\mathrm{kHz}$ offset.

Transmit/Receive Switch Performance




## Recommended PCB Configuration

Layout View


External Circuitry Parts List

| Label | Value | Purpose |
| :--- | :--- | :--- |
| $\mathrm{C} 1-\mathrm{C} 5$ | 1000 pF | Low frequency bypass |
| $\mathrm{C} 6-\mathrm{C} 8$ | 68 pF | RF bypass |
| C 9 | 1.5 pF | Output power tuning |
| C 10 | 15 pF | Reduces low frequency gain |
| R 1 | $2.7 \mathrm{k} \Omega$ | Voltage divider to $\mathrm{V}_{\mathrm{G} 2}$ |
| R 2 | $1.5 \mathrm{k} \Omega$ | Voltage divider to $\mathrm{V}_{\mathrm{G} 2}$ |
| R 3 | $150 \Omega$ | Reduces low frequency gain |
| Tline | 0.250 in. long | Power match |

All off-chip components are low-cost surface mount components obtainable from multiple sources. ( $0.020 \mathrm{in} . \times 0.040 \mathrm{in}$. or $0.030 \mathrm{in} . \times 0.050 \mathrm{in}$.)

## External Circuitry



M/A-COM Inc.

## Designer's Kit (AM55-0004SMB)

The AM55-0004SMB Designer's Kit allows for immediate evaluation of M/A-COM's AM55-0004 integrated Power Amplifier and $\mathrm{T} / \mathrm{R}$ Switch. The evaluation board consists of an AM55-0004, recommended external surface mount circuitry, RF connectors and a DC multipin connector, all mounted to a multi-layer FR-4 PCB. Other items included in the Designer's Kit: a floppy disk (with typical performance data and a .DXF file of the recommended PCB layout) and any additional Application Notes. The AM55-0004SMB PA/Switch evaluation PCB and block diagram are illustrated below with all functional ports labeled.

## P/A Switch Sample Board



Functional Block Diagram


## DC Connector Pinout

| PCB DC <br> Connector | Function | Device Pin <br> Number |
| :---: | :---: | :---: |
| 1 | $\mathrm{~N} / \mathrm{C}$ | $\mathrm{N} / \mathrm{C}$ |
| 2 | $\mathrm{~V}_{\mathrm{DD} 1}(+4.8 \mathrm{~V})$ | 12 |
| 3 | SAVE Tx $(0 \mathrm{~V} /-4 \mathrm{~V})$ | 13 |
| 4 | GND | $\mathrm{N} / \mathrm{C}$ |
| 5 | SAVE Tx $(0 \mathrm{~V} /-4 \mathrm{~V})$ | 13 |
| 6 | $\mathrm{~V}_{\mathrm{G} 1}$ | 18 |
| 7 | $\overline{\mathrm{VSW}}$ | 2 |
| 8 | GND | $\mathrm{N} / \mathrm{C}$ |
| 9 | $\overline{\mathrm{VSW}}$ | 2 |
| 10 | $\mathrm{~V}_{\mathrm{G} 1}$ | 18 |


| PCB DC <br> Connector | Function | Device Pin <br> Number |
| :---: | :---: | :---: |
| 11 | VSW | 27 |
| 12 | $\mathrm{~V}_{\mathrm{G} 1}$ | 18 |
| 13 | VSW | 27 |
| 14 | GND | $\mathrm{N} / \mathrm{C}$ |
| 15 | $\mathrm{~V}_{\mathrm{G} 2}$ | 20 |
| 16 | $\mathrm{~V}_{\mathrm{G} 1}$ | 18 |
| 17 | $\mathrm{~N} / \mathrm{C}$ | $\mathrm{N} / \mathrm{C}$ |
| 18 | $\mathrm{~V}_{\mathrm{G} 2}$ | 20 |
| 19 | $\mathrm{~N} / \mathrm{C}$ | $\mathrm{N} / \mathrm{C}$ |
| 20 | $\mathrm{~V}_{\mathrm{DD} 2}(+4.8 \mathrm{~V})$ | 26 |

## AM55-0004SMB Biasing Procedure

In order to prevent transients which may damage the MMIC, please adhere to the following procedure.

- Turn on all power supplies and set all voltages to 0 volts BEFORE connecting the power supplies to the DC connector.
- Apply - 4.0 volt supply or GND to DC connector pin 9 ( $\overline{\mathrm{VSW}}$, see truth table for desired mode).
- Apply - 4.0 volt supply or GND to DC connector pin 13 (VSW, see truth table for desired mode).
- Apply a -4.0 volt supply to the DC connector pin $16\left(\mathrm{~V}_{\mathrm{G} 1}\right)$.
- Apply a -4.0 volt supply to the DC connector pin $18\left(\mathrm{~V}_{\mathrm{G} 2}\right)$.
- Apply a +4.8 volt supply to the DC connector pin $2\left(\mathrm{~V}_{\mathrm{DD} 1}\right)$.
- Apply a +4.8 volt supply to the DC connector pin $20\left(\mathrm{~V}_{\mathrm{DD} 2}\right)$.
- Apply GND to DC connector pin 5 (Save Tx).
- Adjust $\mathrm{V}_{\mathrm{G} 1}$ supply for desired $\mathrm{V}_{\mathrm{DD} 1}$ quiescent current (typically 30 mA ).
- Adjust $\mathrm{V}_{\mathrm{G} 2}$ supply for desired $\mathrm{V}_{\mathrm{DD} 2}$ quiescent current (typically 65 mA ).
- Change voltage on DC connector pin 5 as required (Save Tx, see truth table for desired mode).
- Apply RF power and test.
- To power off, reverse above procedure

1. Set $\mathrm{V}_{\mathrm{G} 1} \& \mathrm{~V}_{\mathrm{G} 2}$ to -4 V .
2. Set $\mathrm{V}_{\mathrm{DD} 1} \& \mathrm{~V}_{\mathrm{DD} 2}$ to 0 V .
3. Set control voltage supplies to 0 V .
4. Disconnect bias lines from DC connector.
5. Turn off power supplies.

## Evaluation PCB and RF Connector Losses

| Port Reference | Estimated Loss (dB) |
| :---: | :---: |
| PA IN | 0.15 |
| PA OUT | 0.20 |
| Tx IN | 0.20 |
| ANT IN/OUT | 0.20 |
| Rx OUT | 0.20 |

The DC connector on the Designer's Kit PCB allows selection of all the device's operating modes. It is accomplished by one or more of the following methods:

1. A mating female multi-pin connector (Newark Electronics

Stock \# 46F-4658, not included)
2. Wires soldered to the necessary pins (not included)
3. Clip leads (not included)
4. A combination of clip leads or wires and jumpers (jumpers included as required)

