M/A-COM

GaAs MMIC VSAT Power Amplifier, 0.5W 14.0 - 14.5 GHz

Features

- High Linear Gain: 28 dB Typ.
- High Saturated Output Power: +28 dBm Typ.
- High Power Added Efficiency: 22% Typ.
- 50Ω Input/Output Broadband Matched
- High Performance Ceramic Bolt Down Package

Description

M/A-COM's AM42-0041 is a four-stage MMIC linear power amplifier in a ceramic bolt down style hermetic package. The AM42-0041 employs a fully matched chip with internally decoupled Gate and Drain bias networks. The AM42-0041 is designed to be operated from a constant current Drain supply. By varying the Gate bias voltage, the saturated output power performance of this device can be tailored for various applications.

The AM42-0041 is ideally suited for use as an output stage or a driver, in applications for VSAT systems. This design is fully monolithic and requires a minimum of external components.

M/A-COM's AM42-0041 is fabricated using a mature 0.5 micron MBE based GaAs MESFET process. The process features full passivation for increased performance and reliability. This product is 100% RF tested to ensure compliance to performance specifications.

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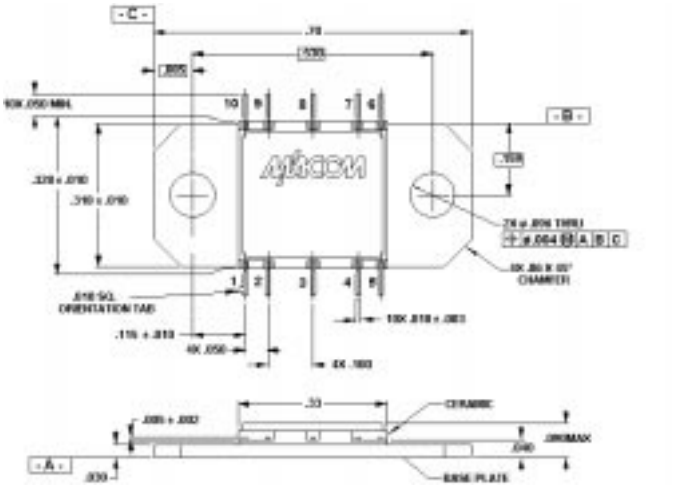

Notes: (unless otherwise specified)
1. Dimensions are in inches.
2. Tolerance: .XXX = ± 0.005
   .XX = ± 0.010

Ordering Information

Part Number	Package
AM42-0041	Ceramic Bolt Down Package

Electrical Specifications: T_A = +25°C, V_{DD} = +8V, V_{GG} adjusted for Ids = 500 mA, Z_0 = 50Ω, F = 14.0 - 14.5 GHz

Parameter	Abbv.	Test Conditions	Units	Min.	Typ.	Max.
Linear Gain	G_L	$P_{IN} \leq$ -10 dBm	dB	27	28	—
Input VSWR	$VSWR_{IN}$	$P_{IN} \leq$ -10 dBm	—	—	2.5:1	2.7:1
Output VSWR	$VSWR_{OUT}$	$P_{IN} \leq$ -10 dBm	—	—	2.5:1	—
Saturated Output Power	P_{SAT}	P_{IN} = +3 dBm, I_{DD}=500 mA Typ.	dBm	27.0	28.0	29.0
Output Power Flatness vs. Frequency	P_{SAT}	P_{IN} = +3 dBm, I_{DD}=500 mA Typ.	dB	—	1.0	1.5
Output Power vs. Temperature (with respect to T_A=+25°C)	P_{SAT}	P_{IN} = +3 dBm, I_{DD}=500 mA Typ. T_A= -40°C to +70°C	dB	—	±0.4	—
Noise Figure	NF	$P_{IN} \leq$ -10 dBm, I_{DD}=500 mA Typ.	dB	—	7	—
Drain Bias Current	I_{DD}	P_{IN} = +3 dBm	mA	400	500	600
Gate Bias Voltage	V_{GG}	P_{IN} = +3 dBm, I_{ds}=500 mA Typ.	V	-2.4	-1.0	-0.4
Gate Bias Current	I_{GG}	P_{IN} = +3 dBm, I_{ds}=500 mA Typ.	mA	—	5	15
Thermal Resistance	θ_{JC}	25°C Heat Sink	°C/W	—	9.5	—
Power Added Efficiency	PAE	P_{IN} = +3 dBm, I_{ds}=500 mA Typ.	%	—	22	—

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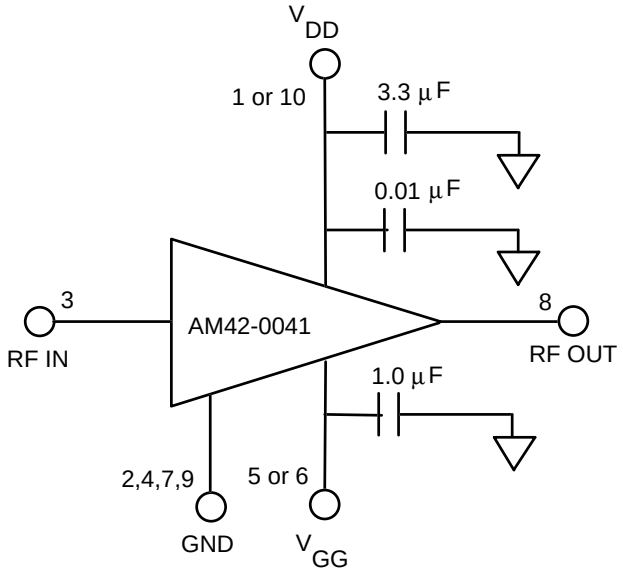
Absolute Maximum Ratings[1,2,3,4]

Parameter	Absolute Maximum
Input Power	+23 dBm
V_{DD}	+12 Volts
V_{GG}	-3 Volts
V_{DD} - V_{GG}	12 Volts
I_{ds}	1000 mA
Channel Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C

1. Operation of this device outside any of these limits may cause permanent damage.
2. Case Temperature (T_C) = +85°C.
3. Nominal bias is obtained by first connecting -2.4 volts to pin 5 or pin 6 (V_{GG}), followed by connecting +8 volts to pin 1 or pin 10 (V_{DD}). Note sequence. Adjust V_{GG} for a drain current of 500 mA typical.
4. RF ground and thermal interface is the flange (case bottom). Adequate heat sinking is required.
5. No dc bias voltage appears at the RF ports.
6. The dc resistance at the input and output ports is a short circuit. No voltage is allowed on these ports.
7. For optimum IP_3 performance, the V_{DD} bypass capacitors should be placed within 0.5 inches of the V_{DD} leads.

Typical Bias Configuration[3,4,7]



Pin Configuration

Pin No.	Pin Name	Description
1	V_{DD}	Drain Supply
2	GND	DC and RF Ground
3	RF In	RF Input
4	GND	DC and RF Ground
5	V_{GG}	Gate Supply
6	V_{GG}	Gate Supply
7	GND	DC and RF Ground
8	RF Out	RF Output
9	GND	DC and RF Ground
10	V_{DD}	Drain Supply

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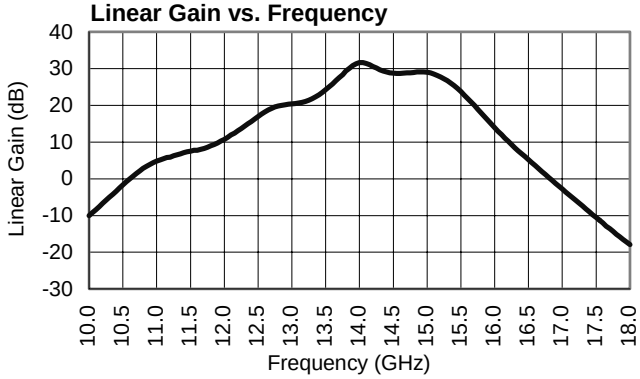
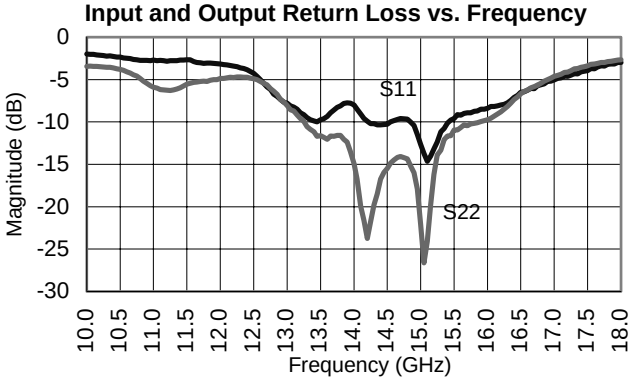
Typical Performance @ +25°C

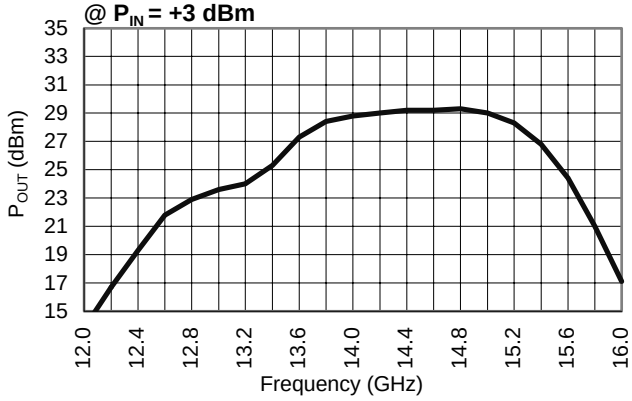
Linear Gain vs. Frequency



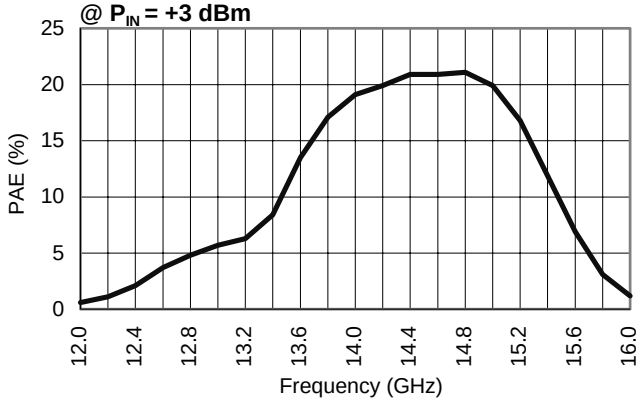
Input and Output Return Loss vs. Frequency



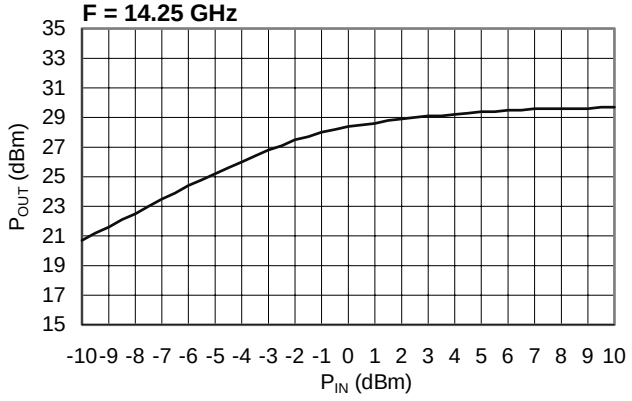
Output Power vs Frequency
@ P_{IN} = +3 dBm



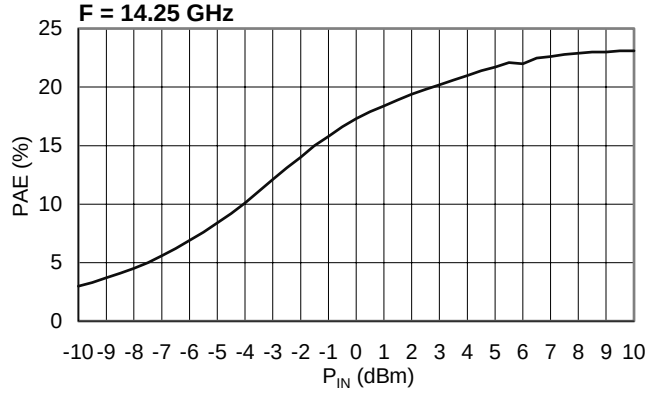
Power Added Efficiency (PAE) vs Frequency
@ P_{IN} = +3 dBm



Output Power vs. Input Power
F = 14.25 GHz



Power Added Efficiency (PAE) vs. Input Power
F = 14.25 GHz



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