

# 1.5 Watt Ku-Band VSAT Power Amplifier 13.75 - 14.5 GHz

# AM42-0042

#### **Features**

- High Linear Gain: 32 dB Typ.
- High Saturated Output Power: +32 dBm Typ.
- High Power Added Efficiency: 25% Typ.
- 50 Ω Input/Output Broadband Matched
- Integrated Output Power Detector

#### Description

M/A-COM's AM42-0042 is a four stage MMIC power amplifier in a bolt down ceramic package, allowing easy assembly. The AM42-0042 employs a fully matched chip with internally decoupled gate and drain bias networks. The AM42-0042 is designed to operate from a constant current drain supply or a constant voltage gate supply. By varying the bias conditions, the saturated output power performance of this device may be tailored for various applications.

The AM42-0042 is ideally suited for use as an output stage or a driver amplifier in VSAT systems. The AM42-0042 includes internal supply line bypassing in the package, minimizing the number of external components required.

M/A-COM's AM42-0042 is fabricated using a mature 0.5 micron MBE based GaAs MESFET process. The process features full passivation for increased performance and reliability. This product is 100% RF tested to ensure compliance to performance specifications.



Notes: (Unless Otherwise Specified) 1. Dimensions are in inches. 2. Tolerance: in .xxx =  $\pm$  .005 .xx =  $\pm$  .010

#### **Ordering Information**

Part Number	Package
AM42-0042	Ceramic Bolt Down Package

#### Electrical Specifications: $V_{DD}$ = +8 V, $V_{GG}$ adjusted for Ids = 750 mA, 13.75 - 14.5 GHz, Zo = 50 $\Omega$ , $T_A$ = +25 °C.

Parameter	Test Conditions	Units	Min.	Тур.	Max.
Linear Gain	Pin = -20 dBm, lds = 750 mA Typ.	dB	29.5	32.0	36.5
Input VSWR	Pin = +3 dBm, Ids = 750 mA Typ.			2.0:1	2.7:1
Output VSWR	Pin = -20 dBm, Ids = 750 mA Typ.			2.0:1	
Output Power	Pin = +3 dBm, lds = 750 mA Typ.	dBm	31.0	32.0	
Output Power vs. Frequency	Pin = +3 dBm, lds = 750 mA Typ.	dB		±0.3	±0.7
Output Power vs. Temperature	$T_A = -40^{\circ}C$ to +85°C, Pin = +3 dBm	dB		±0.5	
Drain Bias Current	Pin = +3 dBm	mA	600	750	900
Gate Bias Voltage	Pin = +3 dBm, lds = 750 mA Typ.	V	-2.0	-1.0	-0.4
Gate Bias Current	Pin = +3 dBm, lds = 750 mA Typ.	mA		10	20
Thermal Resistance ( $\theta_{JC}$ )	25°C Heat Sink	°C/W		8.0	
Second Harmonic	Pin = +3 dBm, lds = 750 mA Typ.	dBc		-35	
Third Harmonic	Pin = +3 dBm, Ids = 750 mA Typ.	= 750 mA Typ. dBc -45			
Detector Voltage	Pin = +3 dBm, lds = 750 mA Typ.	V		2.4	

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### Absolute Maximum Ratings <sup>1, 2</sup>

Parameter	Absolute Maximum		
Input Power	+13 dBm		
V <sub>DD</sub>	+10 volts		
V <sub>GG</sub>	-3 volts		
V <sub>DD</sub> - V <sub>GG</sub>	12 volts		
lds	1000 mA		
Channel Temperature	+150 °C		
Operating Temperature	-40 °C to +85 °C		
Storage Temperature	-65 °C to +150 °C		

1. Exceeding any one or a combination of these limits may cause permanent damage.

2. Adequate heat sinking and grounding required on flange base.

### **Pin Configuration**

Pin No.	Pin Name	Description	
1	VDD	Drain Supply	
2	GND	DC and RF Ground	
3	RF In	RF Input	
4	GND	DC and RF Ground	
5	VGG	Gate Supply	
6	DET	Output Power Detector	
7	GND	DC and RF Ground	
8	RF Out	RF Output	
9	GND	DC and RF Ground	
10	VDD	Drain Supply	



3. Apply -2 volts to pin 5 ( $V_{GG}$ ), prior to applying +8 volts to pins 1 or 10 ( $V_{PG}$ ). Adjust  $V_{QG}$  for twoiced drain current

10 ( $V_{DD}$ ). Adjust  $V_{GG}$  for typical drain current. 4. External DC blocking capacitors required on the RF ports.

5. For optimum IP3 performance,  $V_{DD}$  bypass capacitors should be placed within 0.5 inches of the  $V_{DD}$  leads.

## Typical Bias Configuration<sup>3,4,5</sup>

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