

## Features

- High Speed CMOS Technology
- Single Channel (SWD-109)
- Quad Channel (SWD-119)
- Positive Voltage Control
- Low Power Dissipation
- Low Cost Plastic SOIC Package

## Description

The SWD-109 is a single channel driver used to translate TTL control inputs into gate control voltages for GaAs FET microwave switches and attenuators. High speed analog CMOS technology is utilized to achieve low power dissipation at moderate to high speeds, encompassing most microwave switching applications. The output HIGH level is optionally 0 to +2.0V (relative to GND) to optimize the intermodulation products of the control devices at low frequencies.

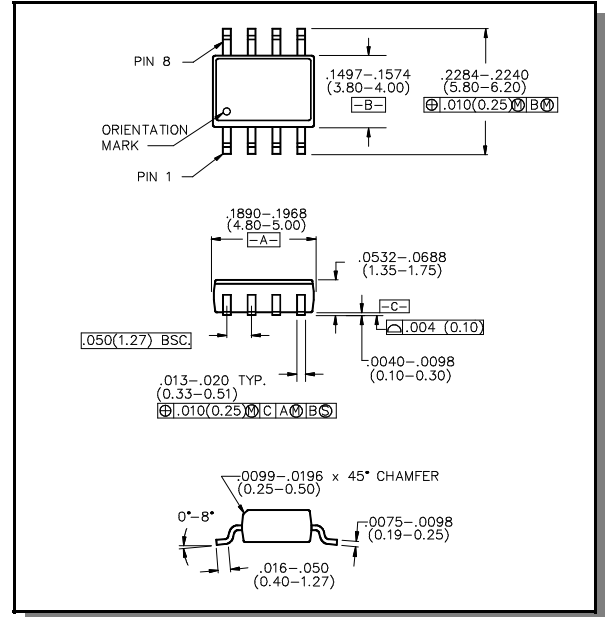
The SWD-119 is a quad channel driver with performance similar to the single channel version.

## Absolute Maximum Ratings

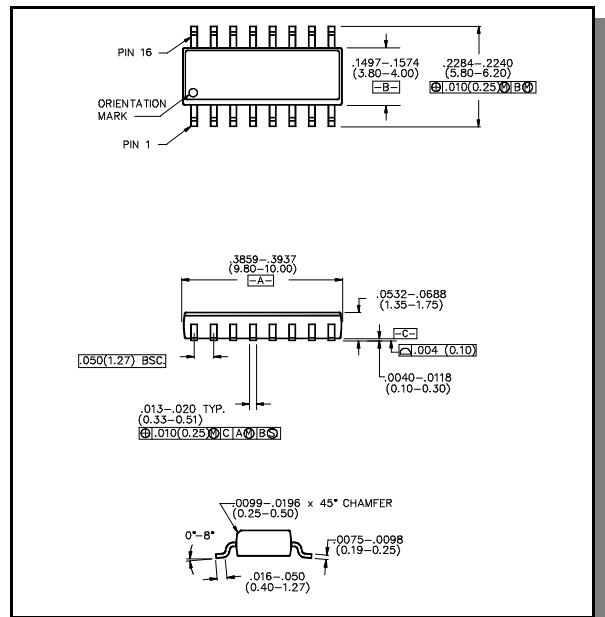
Symbol	Parameter	Min	Max	Unit
$V_{CC}$	Positive DC Supply Voltage	-0.5	5.5	V
$V_{EE}$	Negative DC Supply Voltage	-9.0	0.5	V
$V_{OPT}$	Optional DC Output Supply Voltage	-0.5	2.0	V
$V_{OPT-V_{EE}}$	Output to Negative Supply Voltage Range	-0.5	9.0	V
$V_{CC-V_{EE}}$	Positive to Negative Supply Voltage Range	-0.5	14.5	V
$V_I$	DC Input Voltage	-0.5	$V_{CC} + 0.5$	V
$I_I$	DC Input Current	-25	25	mA
$V_O$	DC Output Voltage	$V_{EE} - 0.5$	$V_{OPT} + 0.5$	V
$V_O$	DC Output Current	-25	25	mA
$T_{STG}$	Storage Temperature	-65	150	°C

All voltages are referenced to GND. All inputs and outputs incorporate latch-up protection structures.

## SO-8 (SWD-109)



## SO-16 (SWD-119)



## Guaranteed Operating Ranges

Symbol	Parameter <sup>1</sup>	Unit	Min.	Typ.	Max.
$V_{CC}$	Positive DC Supply Voltage	V	4.5	5.0	5.5
$V_{EE}$	Negative DC Supply Voltage	V	-8.5	-5.0	-4.5
$V_{OPT}^2$	Optional DC Output Supply Voltage	V	0	1.0	2.0
$V_{OPT}-V_{EE}$	Negative Supply Voltage Range	V	4.5	6.5	8.5
$V_{CC}-V_{EE}$	Positive to negative Supply Range	V	9.0	10.0	14.0
$T_A$	Operating Ambient temperature	°C	-40	+25	+85
$I_{OH}$	DC Output Current - High	mA	—	—	-1.0
$I_{OL}$	DC Output Current - Low	mA	—	—	1.0
$T_{rise}, T_{fall}$	Maximum Input Rise or Fall Time	ns	—	—	500

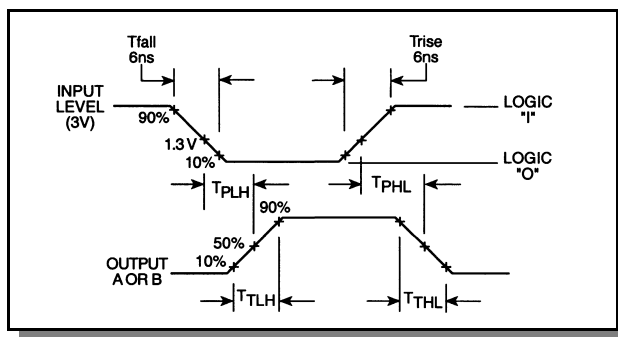
1. All voltages are relative to GND.

2.  $V_{OPT}$  is grounded for most applications. To improve the intermodulation performance and the 1 dB compression point of GaAs control devices at low frequencies,  $V_{OPT}$  can be increased to between 1.0 and 2.0V. The nonlinear characteristics of the GaAs control devices will approximate performance at 500 MHz. It should be noted that the control current is on the GaAs MMICs will increase when positive controls are applied.

## DC Characteristics over Guaranteed Operating Range

Symbol	Parameter	Test Conditions		Units	Min.	Typ.	Max.
$V_{IH}$	Input High Voltage	Guaranteed High Input Voltage		V	2.0	—	—
$V_{IL}$	Input Low Voltage	Guaranteed Low Input Voltage		V	—	—	0.8
$V_{IH}$	Output High Voltage	$I_{OH} = -1$ mA	$V_{EE} = \text{Max}$	V	$V_{OPT} - 0.1$	—	—
$V_{OL}$	Output Low Voltage	$I_{OL} = 1$ mA	$V_{EE} = \text{Max}$	V	—	—	$V_{EE} + 0.1$
$I_{IN}$	Input Leakage Current	$V_{IN} = V_{CC}$ or GND	$V_{EE} = \text{Min}$	$\mu\text{A}$	-1.0	0	1.0
$I_{CC}$	Quiescent Supply Current	$V_{CC} = \text{Max}$ $V_{OPT} = \text{Min}$ or $\text{Max}$	$V_{EE} = \text{Min}$ $V_{IN} = V_{CC}$ or GND	$\mu\text{A}$	—	—	100
$\Delta I_{CC}$	Additional Supply Current, per TTL Input pin	$V_{CC} = \text{Max}$	$V_{IN} = V_{CC} - 2.1\text{V}$	mA	—	—	1.0

## Switching Waveforms

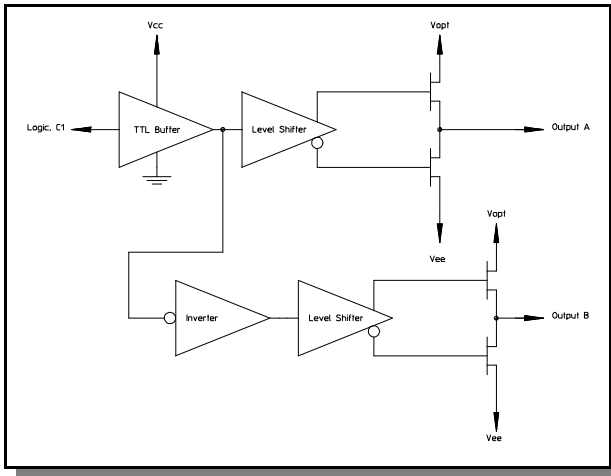


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Visit [www.macom.com](http://www.macom.com) for additional data sheets and product information.

## Functional Schematic (SWD-109)



## Truth Table for Single Driver (SWD-109)

Input	Outputs	
	A	B
Logic "0"	$V_{EE}$	$V_{OPT}$
Logic "1"	$V_{OPT}$	$V_{EE}$

## Pin Configuration

Pin No.	Function	Pin No.	Function
1	Output A	5	Vee
2	GND	6	Vopt
3	Vcc	7	GND
4	C1, Logic	8	Output B

AC Characteristics Over Guaranteed Operating Range<sup>3</sup> (SWD-109)

Symbol	Parameter	$V_{OPT} = V_{EE}$	-55 to +25°C	≤+85°C	≤+125°C	Unit
$T_{PLH}$	Propagation Delay	4.5	45	55	61	ns
		6.5	44	54	59	
		8.5	43	52	57	
$T_{PHL}$	Propagation Delay	4.5	45	55	61	ns
		6.5	43	52	57	
		8.5	41	49	53	
$T_{TLH}$	Output Rising Transition Time	4.5	10.0	10.0	11.0	ns
		6.5	9.0	9.0	9.0	
		8.5	8.0	8.0	8.0	
$T_{THL}$	Output Rising Transition Time	4.5	10.0	10.0	11.0	ns
		6.5	9.0	9.0	9.0	
		8.5	8.0	8.0	8.0	
$T_{skew}$	Delay Skew, Output A to Output B	4.5	8.0	8.5	10.0	ns
		6.5	8.0	8.5	10.0	
		8.5	7.5	8.0	9.5	
$C_{IN}$	Input Capacitance	—	10	10	10	pF
$C_{PDC}$	Power Dissipation Capacitance <sup>4</sup>	—	10	10	10	pF
$C_{PDE}$	Power Dissipation Capacitance <sup>4</sup>	—	140	140	140	pF

3.  $V_{CC} = 4.5V$ ,  $V_{EE} = -4.5V$ ,  $V_{OPT} = 0V$ ,  $C_L = 25$  pF,  $T_{rise}$ ,  $T_{fall} = 6ns$ . These conditions represent the worst case for slow delays.

4. Total Power Dissipation is calculated by the following formula:  $PD = V_{CC}^2 f_{C_{PDC}} + (V_{OPT} - V_{EE})^2 f_{C_{PDE}}$

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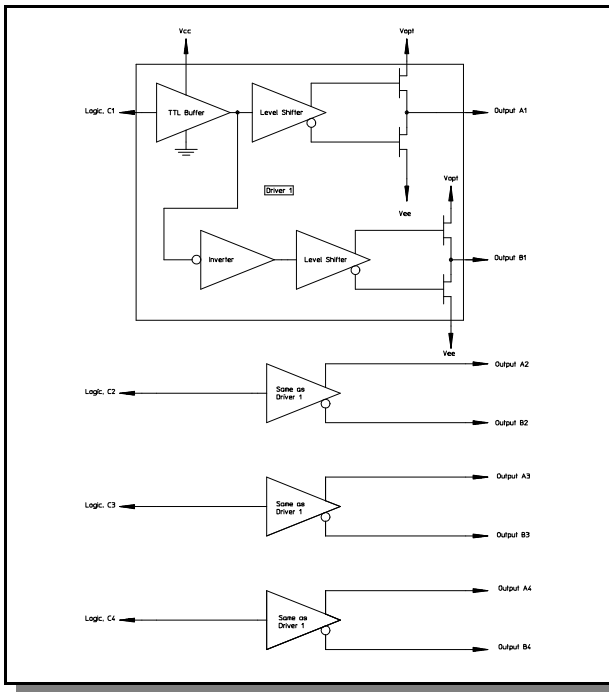
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Functional Schematic (SWD-119)



Truth Table for Quad Driver (SWD-119)

Input	Outputs	
CX	A	B
Logic "0"	$V_{EE}$	$V_{OPT}$
Logic "1"	$V_{OPT}$	$V_{EE}$

Pin Configuration

Pin No.	Function	Pin No.	Function
1	Vee	9	Output A1
2	Vcc	10	Output B1
3	C4	11	Output A2
4	C3	12	Output B2
5	C2	13	Output A3
6	C1	14	Output B3
7	Vopt	15	Output A4
8	GND	16	Output B4

AC Characteristics Over Guaranteed Operating Range <sup>3</sup> (SWD-119)

Symbol	Parameter	$V_{OPT} = V_{EE}$	-55 to +25°C	$\leq +85^\circ\text{C}$	$\leq +125^\circ\text{C}$	Unit
$T_{PLH}$	Propagation Delay	4.5	45	55	61	ns
		6.5	44	54	59	
		8.5	43	52	57	
$T_{PHL}$	Propagation Delay	4.5	45	55	61	ns
		6.5	43	52	57	
		8.5	41	49	53	
$T_{TLH}$	Output Rising Transition Time	4.5	10.5	11.0	12.0	ns
		6.5	10.0	10.0	10.0	
		8.5	9.0	9.0	9.0	
$T_{THL}$	Output Rising Transition Time	4.5	10.0	10.0	11.0	ns
		6.5	9.0	9.0	9.0	
		8.5	8.0	8.0	8.0	
$T_{skew}$	Delay Skew, Output A to Output B	4.5	8.0	8.5	10.0	ns
		6.5	8.0	8.5	10.0	
		8.5	7.5	8.0	9.5	
$C_{IN}$	Input Capacitance	—	10	10	10	pF
$C_{PDC}$	Power Dissipation Capacitance <sup>4</sup>	—	10	10	10	pF
$C_{PDE}$	Power Dissipation Capacitance <sup>4</sup>	—	140	140	140	pF

3.  $V_{CC} = 4.5V$ ,  $V_{EE} = -4.5V$ ,  $V_{OPT} = 0V$ ,  $C_L = 25\text{ pF}$ ,  $Trise, Tfall = 6ns$ . These conditions represent the worst case for slow delays.

4. Total Power Dissipation is calculated by the following formula:  $PD = V_{CC}^2 fC_{PDC} + (V_{OPT} - V_{EE})^2 fC_{PDE}$

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## Ordering Information

Part Number	Package
SWD-109 PIN	SOIC 8 Lead
SWD-109TR	Forward Tape and Reel
SWD-109RTR	Reverse Tape and Reel

Part Number	Package
SWD-119 PIN	SOIC 16 Lead
SWD-119TR	Forward Tape and Reel
SWD-119RTR	Reverse Tape and Reel

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