Features

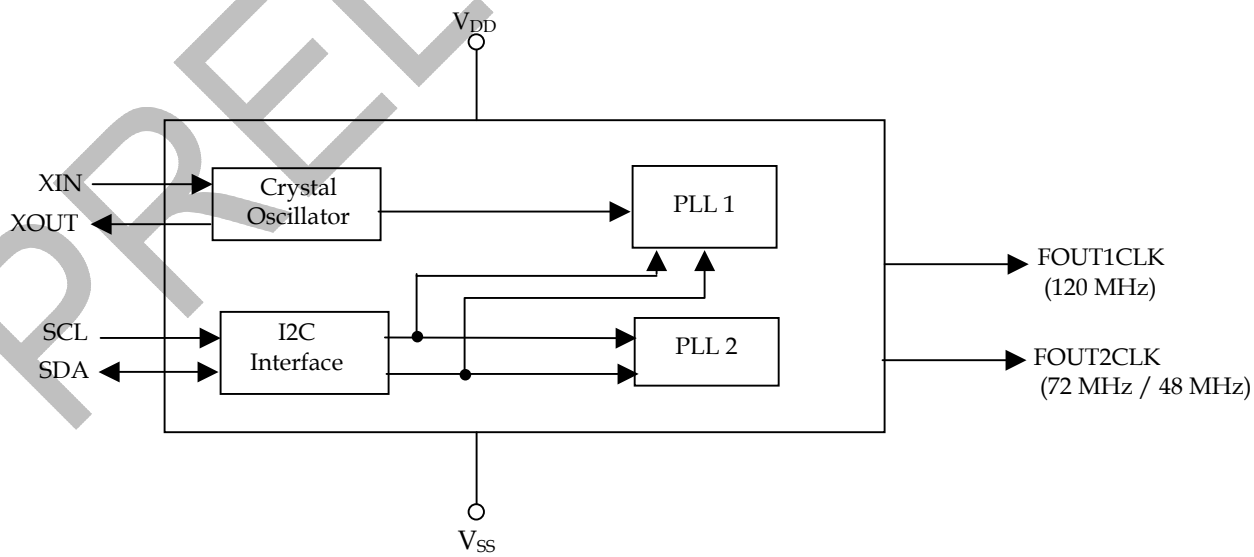
- Generates an EMI optimized clocking signal at output.
- Input frequency – 14.31818 MHz.
- Frequency outputs:
  - 120 MHz (modulated) - default.
  - 72 MHz (modulated) or 48 MHz (modulated) selectable via I2C
- ± 1% Centre spread.
- Modulation rate: 40 KHz.
- Byte Write via I2C
- Supply voltage range 3.3V (± 0.3V).
- Available in 8-pin SOIC package.
- Commercial and Industrial Temperature range.

Product Description

The ASM3P2508A is a versatile spread spectrum frequency modulator. The ASM3P2508A reduces electromagnetic interference (EMI) at the clock source. The ASM3P2508A allows significant system cost savings by reducing the number of circuit board layers and shielding that are required to pass EMI regulations. The ASM3P2508A modulates the output of PLL in order to spread the bandwidth of a synthesized clock, thereby decreasing the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most clock generators. Lowering EMI by increasing a signal's bandwidth is called spread spectrum clock generation.

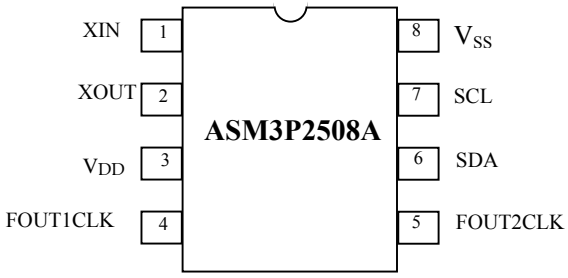
The ASM3P2508A has a feature to power down the 72MHz / 48MHz output by writing data into specific registers in the device via I2C. By writing a '0' into bit 1 of byte 0, the PLL block generating 72 MHz / 48MHz can be powered down. Writing '0' into bit '7' of byte 1 selects an output of 72 MHz on FOUT2CLK while a '1' at the same location selects a 48 MHz clock output. However, the I2C block, crystal oscillator, and the PLL block generating 120MHz would be always running.

Block Diagram



PRELIMINARY

Pin Configuration



Pin Description

Pin Name	Type	Description
XIN	I	Connection to crystal
XOUT	O	Connection to crystal
V_{DD}	P	Power supply for the analog and digital blocks
FOUT1CLK	O	Clock output-1 (120 MHz) - default
FOUT2CLK	O	Clock output-2 (72 MHz / 48 MHz)
SDA	I/O	I2C Data
SCL	I	I2C Clock
V_{SS}	P	Ground to entire chip

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD}	Supply voltage, DC	(V_{SS} – 0.5) to 7	V
V_I	Input voltage, DC	(V_{SS}-0.5) to (V_{DD}+0.5)	V
V_O	Output voltage, DC	(V_{SS}-0.5) to (V_{DD} + 0.5)	V
I_{IK}	Input clamp current (V_I<0 or V_I>V_{DD})	-50 to +50	mA
I_{OK}	Output clamp current (V_I<0 or V_I>V_{DD})	-50 to +50	mA
T_S	Storage temperature	-65 to +125	°C
T_A	Ambient temperature range, under bias	-55 to 125	°C
T_J	Junction temperature	150	°C
	Lead temperature (soldering 10 sec)	260	°C
	Input static discharge voltage protection (MIL –STD 883E, Method 3015.7)	2	kV
Note: These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.			

Operating Conditions

Parameter	Symbol	Condition / Description	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.3V ± 10%	3	3.3	3.6	V
Ambient Operating Temperature Range	T_A		-10		+70	°C
Crystal Resonator Frequency	F_{XIN}			14.31818		MHz
Output Driver Load Capacitance	C_L				15	pF

DC Electrical Characteristics

Parameter	Symbol	Conditions / Description	Min	Typ	Max	Unit
Overall						
Supply Current, Dynamic	I_{DD}	V_{DD}=3.3V, F_{CLK}=14.31818MHz, C_L=15pF		43		mA
Supply Current, Static	I_{DDL}	V_{DD} = 3.3V, Software Power Down		tbd		mA
All input pins						
High-Level Input Voltage	V_{IH}	V_{DD}=3.3V	2.0		V_{DD}+0.3	V
Low-Level Input Voltage	V_{IL}	V_{DD}=3.3V	V_{SS}-0.3		0.8	V
High-Level Input Current	I_{IH}		-1		1	μ A
Low-Level Input Current (pull-up)	I_{IL}		-20	-36	-80	μ A
High-Level Output Source Current	I_{xOH}	V_{DD}=V(XIN) = 3.3V, V_O=0V	10	21	30	mA
Low-Level Output Source Current	I_{xOL}	V_{DD}=3.3V, V(XIN)=V_O=5.5V	-10	-21	-30	mA
Clock Outputs (FOUT1CLK, FOUT2CLK)						
High-Level Output Source Current	I_{OH}	V_O=2.4V		-20		mA
Low-Level Output Sink Current	I_{OL}	V_O=0.4V		23		mA
Output Impedance	Z_{OH}	V_O=0.5V_{DD}; output driving high		29		Ω
	Z_{OL}	Vo=0.5V_{DD}; output driving low		27		

AC Electrical Characteristics

Parameter	Symbol	Conditions/ Description	Min	Typ	Max	Unit
Rise Time	t_r	V_O = 0.3V to 3.0V; CL = 15pF		2.1		ns
Fall Time	t_f	V_O = 3.0V to 0.3V; CL = 15pF		1.9		ns
Clock Duty Cycle		Ratio of pulse width (as measured from rising edge to next falling edge at 2.5V) to one clock period	45		55	%
Jitter, Long Term	$Tj_{(LT)}$	On rising edges 500 uS apart at 2.5 V relative to an ideal clock, PLL B inactive *		45		pS
		On rising edges 500 uS apart at 2.5 V relative to an ideal clock, PLL B active *		165		
Jitter, peak to peak	$Tj_{(\Delta T)}$	From rising edge to next rising edge at 2.5 V, PLL B inactive *		110		pS
		From rising edge to next rising edge at 2.5 V, PLL B active *		390		
Clock Stabilization Time	t_{STB}	Output active from power up, RUN Mode via Software Power Down		125		us
* CL = 15 pF, Fxin = 14.31818 MHz, Fout = 50 MHz						

Crystal Specifications

Fundamental AT cut parallel resonant crystal	
Nominal Frequency	14.31818 MHz
Frequency Tolerance	+/- 50 ppm or better at 25°C
Operating temperature range	-20°C to +85°C
Storage Temperature	-40°C to +85°C
Load Capacitance	18pF
Shunt capacitance	7 pF maximum
ESR	25 Ω

General I2C Serial Interface Information

The information in this section assumes familiarity with I2C programming.

How to Write through I2C:

- Master (host) sends a start bit.
- Master (host) sends the write address XX (H)
- ASM3P2508A device will acknowledge
- Master (host) sends the beginning byte location (=N)
- ASM3P2508A device will acknowledge
- Master (host) sends a dummy byte count
- ASM3P2508A device will acknowledge
- Master (host) starts sending byte N through byte N+X – 1*
- ASM3P2508A device will acknowledge each byte one at a time.
- Master (host) sends a Stop bit

Controller (Host)	ASM3P2508A (slave/receiver)
Start Bit	
Slave Address XX(H)	
	ACK
Beginning byte location (=N)	
	ACK
Dummy byte count	
	ACK
Beginning byte (Byte N)	
	ACK
Next Byte (Byte N+1)	
	ACK

Last Byte (Bye N+X-1)	
	ACK
Stop Bit	

How to Read through I2C:

- Master (host) will send start bit.
- Master (host) sends the write address XX (H)
- ASM3P2508A device will acknowledge
- Master (host) sends the beginning byte location (=N)
- ASM3P2508A device will acknowledge
- Master (host) will send a separate start bit
- Master (host) sends the read address XX (H)
- ASM3P2508A device will acknowledge
- ASM3P2508A device will send the dummy byte count
- Master (host) acknowledges
- ASM3P2508A device sends byte N through byte N+X – 1*
- Master (host) will need to acknowledge each byte
- Master (host) will send a stop bit

(* X is the number of bytes)

Controller (Host)	ASM3P2508A (slave/receiver)
Start Bit	
Slave Address XX(H)	
	ACK
Beginning Byte = N	
	ACK
Repeat start	
Slave address	
	ACK
	Dummy Byte Count
ACK	
	Beginning byte N
ACK	
	Next Byte N+1
ACK	

	Last Byte (Byte N+X-1)
Not Acknowledge	
Stop Bit	

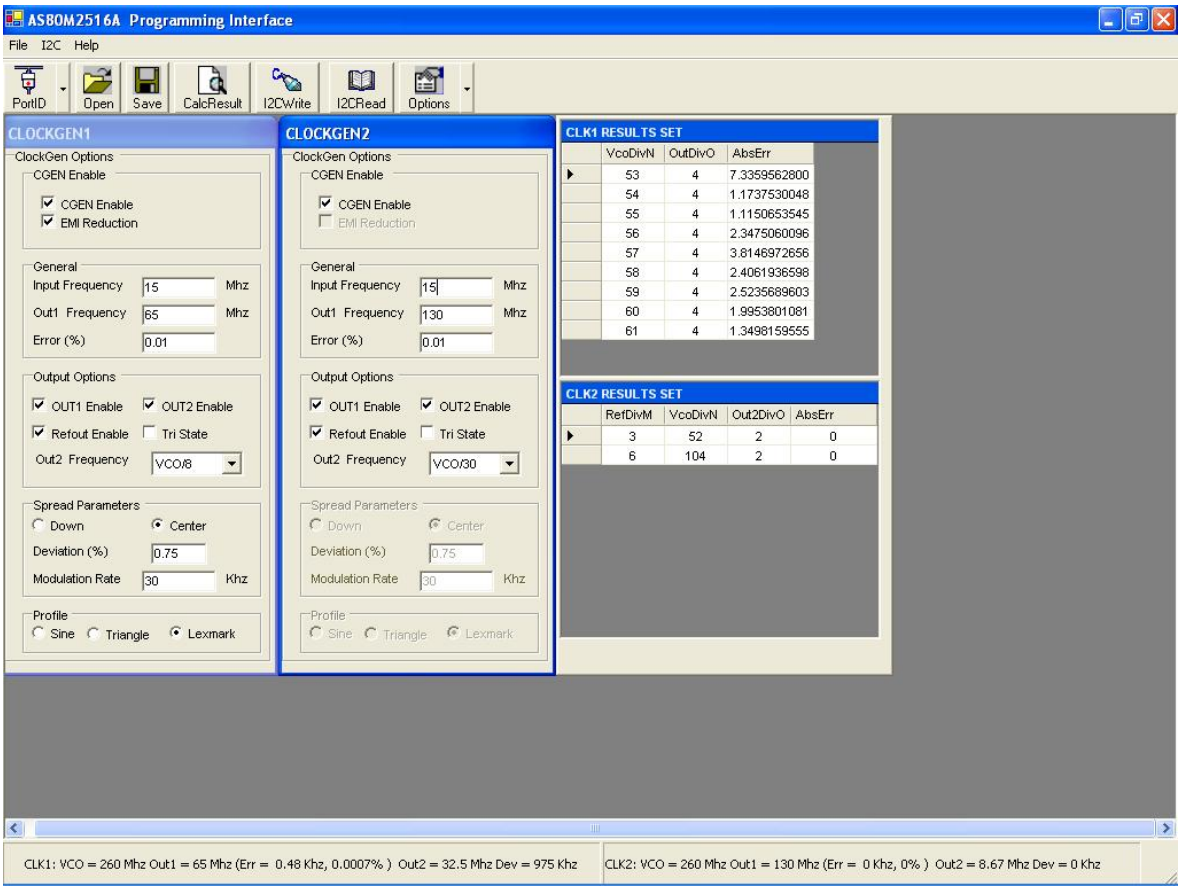
Software

A demonstration board and software is available for the ASM3P2508A.

The software can operate under Windows 95 and Windows NT. The opening screen of the software is shown in figure 2.

By pressing the drop down arrow of **Port ID** toolbar button, any of the three parallel ports (LPT1 LPT2 or LPT3) can be selected. The selected parallel port is used for the I2C data transfer.

Opening Screen



Programming the PLLs:

Select the **CGEN check box** to enable the PLL and the EMI reduction check box to enable the spread spectrum on. Enter the input frequency (in Mhz), output frequency (Mhz) , percentage error and modulation rate (Khz) in the respective input boxes. To enable the OUT1 OUT2 and REFOUT click the respective check box. To tristate all the outputs click the tristate check box. Select the type of the modulation between the center or down and enter the deviation (percentage) in the respective input box. Profile type can be selected between the sine triangular or lexmark.

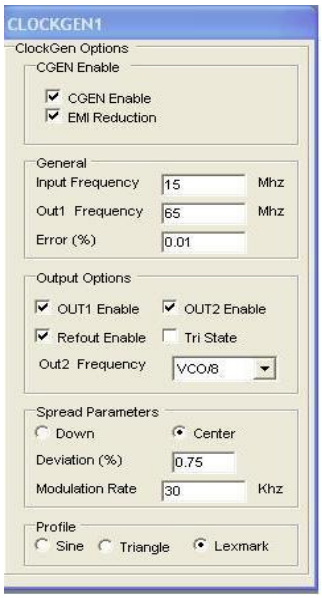
EMI reduction enable/disable option is only available for the PLL1.

Writing the data to the chip:

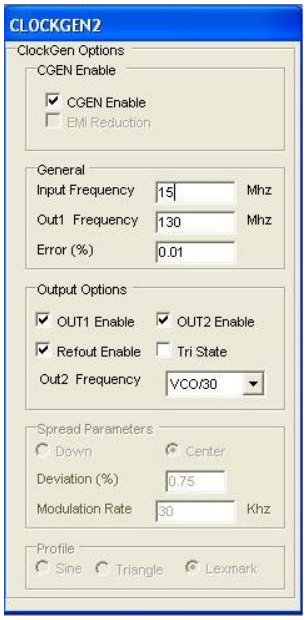
There are two different ways of writing data to the chip.

1. Writing through the file.
2. Enter the required data in the respective forms and calculate and then write.

For Example:

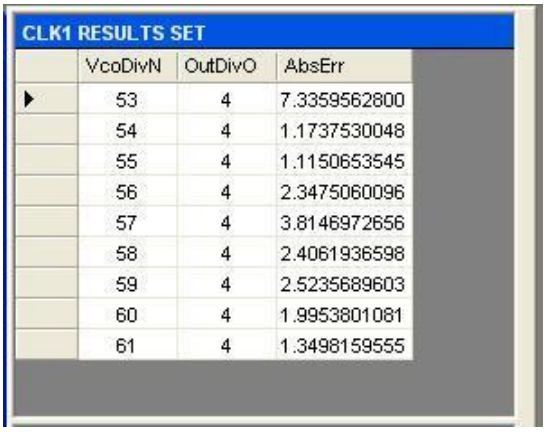


1. Enter the input freq say 15 Mhz, in the **input frequency** box.
2. Enter the required output frequency say 65 Mhz, in the **out1 frequency** box.
3. Enter the percentage error say 0.01 in the **error** box.
4. Enter the modulation rate say 30 khz in the **modulation rate** box.
5. Select the second output frequency by pressing the pull down menu of the out2 frequency.
   The value of OUT2 frequency can be selected as vco/2, vco/3, vco/4, vco/5, vco/6, vco/8, vco/9, vco/10, vco/12, vco/15, vco/18, vco/24 or vco/30.
6. Select the type of the deviation, percentage deviation and type of the profile.
7. Enter the data for PLL2 in a similar manner.



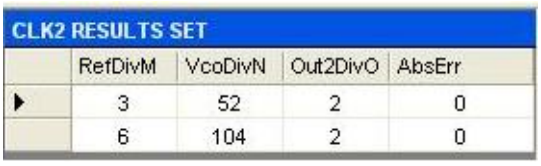
8. Press the **CalcResult** button to load the data in the ROM data panel.
9. To write this data to the chip press the I2CWrite button.

Results Window



CLK1 RESULTS SET

	VcoDivN	OutDivO	AbsErr
▶	53	4	7.3359562800
	54	4	1.1737530048
	55	4	1.1150653545
	56	4	2.3475060096
	57	4	3.8146972656
	58	4	2.4061936598
	59	4	2.5235689603
	60	4	1.9953801081
	61	4	1.3498159555



CLK2 RESULTS SET

	RefDivM	VcoDivN	Out2DivO	AbsErr
▶	3	52	2	0
	6	104	2	0

Reading the data from the Chip

1. To read the data from the chip through I2C, press the **I2CRead** button.
2. The data can be seen in the ROM data field.
3. This data which is read from the chip can be saved in the file by clicking the **Save** button.

An example of a Byte Write via I2C to partially 'power down' the device:

ASM3P2508A can be partially 'powered down' using bit 1 of Byte 0. The organization of the register bits for Byte '0' is given with default values below:

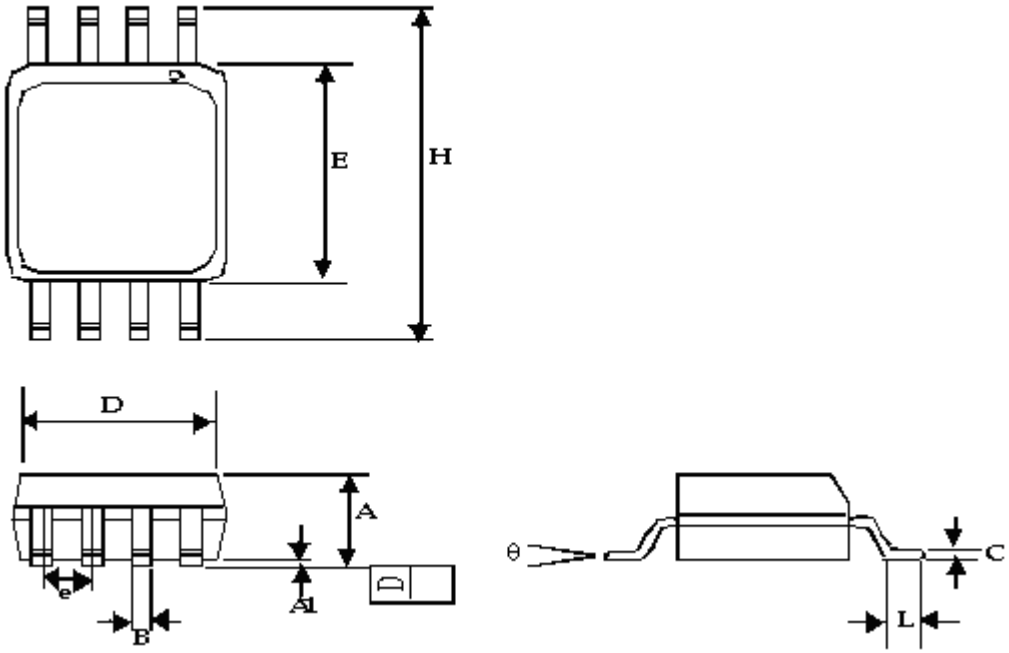
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Resv.	Resv.	Resv.	Resv.	Resv.	Resv.	PLL2 Enable	PLL1 Enable
0	1	0	1	0	1	1	1

The function of partial power down of the device is of interest to us - that is bit 1 of Byte 0. In the default mode this bit is logic '1'. As such, the Byte 0 default value is 57 (H). To put ASM3P 2508A in 'power down' mode, the bit 0 of byte 0 is to be changed to logic '0'. Hence writing a 55 (H) via i2C into byte 0 would put the device in partial 'power down' mode where the PLL block generating 72 MHz / 48 MHz would be powered down while I2C block, crystal oscillator, and the PLL block generating 120 MHz would still be active. The organization of the register bits is as below:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Resv.	Resv.	Resv.	Resv.	Resv.	Resv.	PLL2 Enable	PLL1 Enable
0	1	0	1	0	1	0	1

Package Information

8-Pin SOIC



Symbol	Dimensions in inches		Dimensions in millimeters	
	Min	Max	Min	Max
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.013	0.022	0.33	0.53
C	0.007	0.012	0.18	0.27
D	0.188	0.197	4.78	5.00
E	0.150	0.158	3.80	4.01
H	0.228	0.244	5.80	6.20
e	0.050 BSC		1.27 BSC	
L	0.016	0.035	0.40	0.89
θ	0°	8°	0°	8°

Ordering Codes

Part number	Package Configuration	
ASM3P2508A-08-ST	8-PIN SOIC	TUBE
ASM3P2508A-08-SR	8-PIN SOIC	TAPE AND REEL
ASM3I2508A-08-ST	8-PIN SOIC	TUBE
ASM3I2508A-08-SR	8-PIN SOIC	TAPE AND REEL

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