12 Bit, 500MSPS A/D Converter

Preliminary Technical Data

AD12501

FEATURES

Up to 500 MSPS sample rate
SNR of 63 dBFS @70 MHz
SFDR of 70 dBFS @70 MHz
VSWR of 1:1.5
Wideband ac-coupled input signal conditioning
Enhanced spurious-free dynamic range
Single-ended or differential encode signal
LVDS output levels
Twos complement output data

APPLICATIONS

Communications test equipment
Radar and satellite subsystems
Phased array antennas—digital beam
Multi-channel, multimode receivers
Secure communications
Wireless and wired broadband communications
Wideband carrier frequency systems

GENERAL DESCRIPTION

The AD12501 is a 12-bit analog-to-digital converter (ADC) with a transformer-coupled analog input driving amplifiers providing gain, and digital post-processing for enhanced SFDR. The product operates at up to 500 MSPS conversion rate with outstanding dynamic performance in wideband carrier systems.

The AD12501 requires 3.7 V analog, 3.3 V digital, and 1.5 V digital supplies, and provides a flexible encode signal that can be differential or single-ended. No external reference is required.

The AD12501 package style is an enclosed 2.9" × 2.6" × 0.6" module. Performance is rated over a 0°C to 60°C case temperature range.

FUNCTIONAL BLOCK DIAGRAM

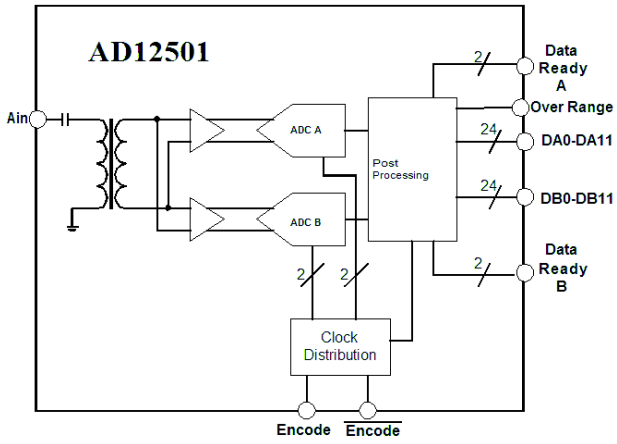

Figure 1.

PRODUCT HIGHLIGHTS

1. Guaranteed sample rate up to 500 MSPS.
2. Input signal conditioning with optimized dynamic performance to 225 MHz.
3. Additional performance options available (sample rates up to 525MSPS or 2nd Nyquist zone operation); contact factory.
4. Proprietary Advanced Filter Bank (AFB™) digital post-processing from V Corp Technologies, Inc.

Rev. PrB

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Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

SPECIFICATIONS

DC SPECIFICATIONS

VA = 3.7V, VC = 3.3 V, VD = 1.5 V, encode = 500 MSPS, 0°C ≤ T_{CASE} ≤ 60°C, unless otherwise noted.

Table 1.

			AD12501-XYZKWS			
Parameter	**Case Temp**	**Test Level**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION				12		Bits
ACCURACY						
No Missing Codes	Full	IV		Guaranteed		
Offset Error	Full	I		TBD		LSB
Gain Error @ 10 MHz	Full	I		TBD		%FS
Differential Nonlinearity (DNL)	60°C	V		TBD		LSB
Integral Nonlinearity (INL)	60°C	V		TBD		LSB
TEMPERATURE DRIFT						
Gain Error	60°C	V		TBD		%/°C
ANALOG INPUT (AIN)						
Full-Scale Input Voltage Range	60°C	V		1.0		V p-p
Frequency Range	Full	IV	1		225	MHz
Flatness (10 MHz to 225 MHz)	Full	IV		0.5	1.5	dB
Input VSWR (50 Ω) (300 KHz to 225 MHz)	60°C	V		1.5		
Analog Input Bandwidth	60°C	V		350		MHz
POWER SUPPLY[1]						
Supply Voltage						
VA	Full	IV	3.6		3.8	V
VC	Full	IV	3.2		3.4	V
VD	Full	IV	1.45		1.55	V
Supply Current						
I_{VA} (VA = 3.7 V)	Full	I		TBD		A
I_{VC} (VC = 3.3 V)	Full	I		TBD		mA
I_{VD} (VD = 1.5 V)	Full	I		TBD		A
Total Power Dissipation	Full	I		5		W
ENCODE INPUTS[2]						
Differential Inputs (ENC, $\overline{ENC}$)						
Input Voltage Range	Full	IV	0.4			V
Input Resistance	60°C	V		100		Ω
Input Capacitance	60°C	V		4		pF
Common-Mode Voltage	60°C	V		±3		V
Single-Ended Inputs (ENC)						
Input Voltage	Full	IV	0.4	2	2.5	V p-p
Input Resistance	60°C	V		50		Ω
LOGIC INPUTS ($\overline{RESET}$)[3]						
Logic 1 Voltage	Full	IV	2.0			V
Logic 0 Voltage	Full	IV			0.8	V
Source I_{IH}	60°C	V		10		µA
Source I_{IL}	60°C	V		1		mA
LOGIC OUTPUTS (DRA, DRB, Output Bits)[4]						
Differential Output Voltage	Full	IV	247		454	mV
Output Drive Current	Full	IV	−4		+4	mA
Output Common-Mode Voltage	Full	IV	1.125		1.375	V
Start-Up Time	Full	IV		600		ms

[1] Tested using input frequency of 70 MHz. See Figure 17

[2] All ac specifications tested by driving ENC single-ended.

[3] Refer to Table 5 for logic convention on all logic inputs.

[4] Digital output logic levels: VC = 3.3 V, C_{LOAD} = 8 pF. 3.3 V LVDS, R1 = 100 Ω.

AC SPECIFICATIONS[1]

VA = 3.7 V, VC = 3.3 V, VD = 1.5 V, encode = 500 MSPS, 0°C ≤ T_{CASE} ≤ 60°C, unless otherwise noted.

Table 2.

Parameter	Case Temp	Test Level	AD12501-500KWS Min	Typ	Max	Unit
DYNAMIC PERFORMANCE[2]						
SNR						
Analog Input 10 MHz	Full	I		64		dBFS
@ −1.0 dBFS 70 MHz	Full	I		63.5		dBFS
128 MHz	Full	I		63		dBFS
225 MHz	Full	I		62.5		dBFS
SINAD[3]						
Analog Input 10 MHz	Full	I		63.5		dBFS
@ −1.0 dBFS 70 MHz	Full	I		63		dBFS
128 MHz	Full	I		62.5		dBFS
225 MHz	Full	I		61		dBFS
Spurious-Free Dynamic Range[3]						
Analog Input 10 MHz	Full	I		80		dBFS
@ −1.0 dBFS 70 MHz	Full	I		84		dBFS
128 MHz	Full	I		76		dBFS
225 MHz	Full	I		71		dBFS
Image Spur[4]						
Analog Input 10 MHz	Full	I		75		dBFS
@ −1.0 dBFS 70 MHz	Full	I		70		dBFS
128 MHz	Full	I		68		dBFS
225 MHz	Full	I		60		dBFS
Offset Spur[4]						
Analog Input @ −1.0 dBFS	60°C	V		65		dBFS
Two-Tone IMD[5]						
F1, F2 @ −6 dBFS	60°C	V		−75		dBc
SWITCHING SPECIFICATIONS						
Conversion Rate[6]	Full	IV	495	500	505	MSPS
Encode Pulse Width High (t_{EH})[1]	60°C	V		1		ns
Encode Pulse Width Low (t_{EL})[1]	60°C	V		1		ns
DIGITAL OUTPUT PARAMETERS						
Valid Time (t_V)	Full	IV		TBD		ns
Propagation Delay (t_{PD})	60°C	V		TBD		ns
Rise Time (t_R) (20% to 80%)	60°C	V		TBD		ns
Fall Time (t_F) (20% to 80%)	60°C	V		TBD		ns
DR Propagation Delay (t_{EDR})	60°C	V		TBD		ns
Data to DR Skew ($t_{EDR} - t_{PD}$)	60°C	V		TBD		ns
Pipeline Latency[7]	Full	IV		TBD		Cycles
Aperture Delay (t_A)	60°C	V		TBD		ns
Aperture Uncertainty (Jitter, t_J)	60°C	V		TBD		ps rms

[1] All ac specifications tested with a single-ended, 2.0 V p-p encode.
[2] Dynamic performance guaranteed for analog input frequencies of 1 MHz to 225 MHz.
[3] Not including image spur.
[4] The image spur is at $f_s/2 - A_{IN}$; the offset spur is at $f_s/2$.
[5] F1 = 70 MHz, F2 = 73 MHz.
[6] Parts are tested with 500 MSPS encode. Device can be clocked at lower encode rates, but specifications are not guaranteed. Specifications are guaranteed by design for encode 500 MSPS ±1%.
[7] Pipeline latency is exactly TBD cycles.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Value
VA to AGND	5 V
VC to DGND	4 V
VD to DGND	1.65 V
Analog Input Voltage	6 V (dc)
Analog Input Power	TBD dBm (ac)
Encode Input Voltage	6 V (dc)
Encode Input Power	12 dBm (ac)
Logic Inputs and Outputs to DGND	5 V
Storage Temperature Range, Ambient	−65°C to +150°C
Operating Temperature	0°C to 60°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

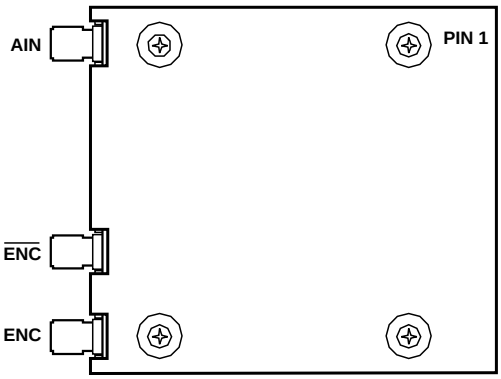
EXPLANATION OF TEST LEVELS

Level	Description
I	100% production tested.
II	100% production tested at 25°C and sample tested at specified temperatures.
III	Sample tested only.
IV	Parameter is guaranteed by design and characterization testing.
V	Parameter is a typical value only.
VI	100% production tested at 25°C; guaranteed by design and characterization testing for industrial temperature range; 100% production tested at temperature extremes for military devices.

ESD CAUTION

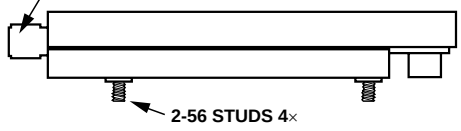
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

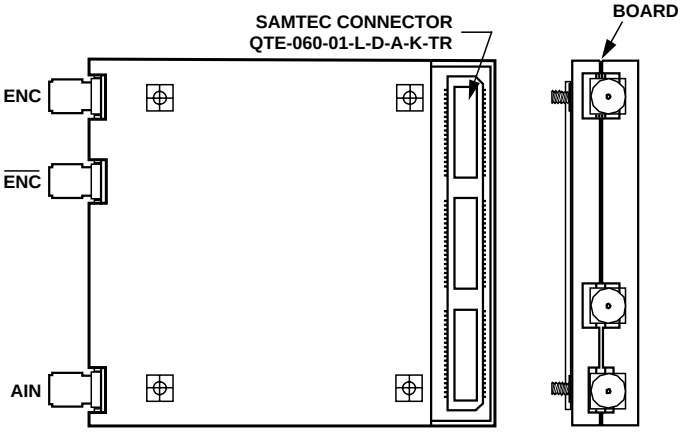


TOP VIEW

JOHNSON SMA-50 OHM CONNECT NO. 142-0711-821

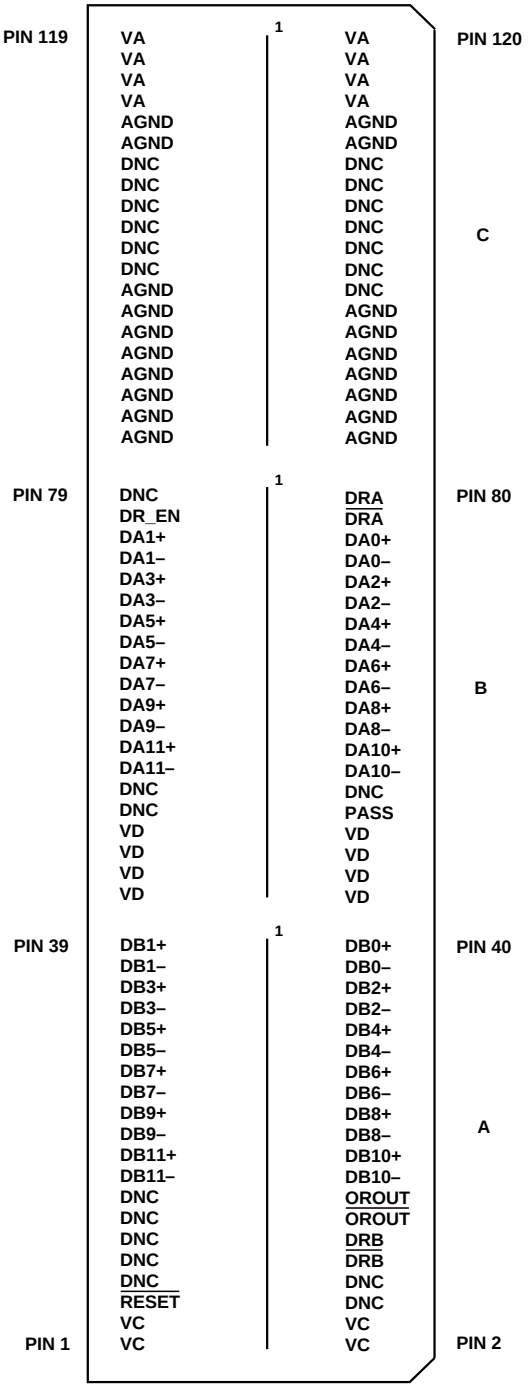


END VIEW



BOTTOM VIEW

LEFT SIDE VIEW



NOTES
1. FOR MATING HALF, USE SAMTEC, INC. PART NO. QSE-60-01-L-D-A-K.

[1]INTEGRAL GROUND PLANE CONNECTIONS.
SECTION A = DGND, PINS 121–124.
SECTION B = DGND, PINS 125–128.
SECTION C = AGND, PINS 129–132.

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 4	VC	Digital Supply, 3.3 V.
5	$\overline{\text{RESET}}$	LVTTL. 0 = device reset. Minimum width = 200 ns. Device resumes operation after 600 ms maximum.
6 to 9, 11, 13 ,15, 49, 51, 79, 95 to 108	DNC	Do Not Connect.
10	$\overline{\text{DRB}}$	Channel B Data Ready. Complement output.
12	DRB	Channel B Data Ready. True output.
14	OROUT-	Over Range. Complement output
16	OROUT	Over Range. True Output 1 = over ranged, 0 = normal operation
17	DB11–	Channel B Data Bit 11. Complement output bit.
18	DB10–	Channel B Data Bit 10. Complement output bit.
19	DB11+	Channel B Data Bit 11. True output bit.
20	DB10+	Channel B Data Bit 10. True output bit.
21	DB9–	Channel B Data Bit 9. Complement output bit.
22	DB8–	Channel B Data Bit 8. Complement output bit.
23	DB9+	Channel B Data Bit 9. True output bit.
24	DB8+	Channel B Data Bit 8. True output bit.
25	DB7–	Channel B Data Bit 7. Complement output bit.
26	DB6–	Channel B Data Bit 6. Complement output bit.
27	DB7+	Channel B Data Bit 7. True output bit.
28	DB6+	Channel B Data Bit 6. True output bit.
29	DB5–	Channel B Data Bit 5. Complement output bit.
30	DB4–	Channel B Data Bit 4. Complement output bit.
31	DB5+	Channel B Data Bit 5. True output bit.
32	DB4+	Channel B Data Bit 4. True output bit.
33	DB3–	Channel B Data Bit 3. Complement output bit.
34	DB2–	Channel B Data Bit 2. Complement output bit.
35	DB3+	Channel B Data Bit 3. True output bit.
36	DB2+	Channel B Data Bit 2. True output bit.
37	DB1–	Channel B Data Bit 1. Complement output bit.
38	DB0–	Channel B Data Bit 0. Complement output bit. DB0 is LSB.
39	DB1+	Channel B Data Bit 1. True output bit.
40	DB0+	Channel B Data Bit 0. True output bit. DB0 is LSB.
41 to 48	VD	Digital Supply, 1.5 V.
50	PASS	LVTTL. Factory use only. (DNC).
52	TC_EN	Enable/disable AFB temperature compensation
53	DA11–	Channel A Data Bit 11. Complement output bit.
54	DA10–	Channel A Data Bit 10. Complement output bit.
55	DA11+	Channel A Data Bit 11. True output bit.
56	DA10+	Channel A Data Bit 10. True output bit.
57	DA9–	Channel A Data Bit 9. Complement output bit.
58	DA8–	Channel A Data Bit 8. Complement output bit.
59	DA9+	Channel A Data Bit 9. True output bit.
60	DA8+	Channel A Data Bit 8. True output bit.
61	DA7–	Channel A Data Bit 7. Complement output bit.
62	DA6–	Channel A Data Bit 6. Complement output bit.
63	DA7+	Channel A Data Bit 7. True output bit.
64	DA6+	Channel A Data Bit 6. True output bit.
65	DA5–	Channel A Data Bit 5. Complement output bit.
66	DA4–	Channel A Data Bit 4. Complement output bit.
67	DA5+	Channel A Data Bit 5. True output bit.
68	DA4+	Channel A Data Bit 4. True output bit.
69	DA3–	Channel A Data Bit 3. Complement output bit.
70	DA2–	Channel A Data Bit 2. Complement output bit.
71	DA3+	Channel A Data Bit 3. True output bit.
72	DA2+	Channel A Data Bit 2. True output bit.
73	DA1–	Channel A Data Bit 1. Complement output bit.
74	DA0–	Channel A Data Bit 0. Complement output bit. DA0 is LSB.
75	DA1+	Channel A Data Bit 1. True output bit.

Pin No.	Mnemonic	Description
76	DA0+	Channel A Data Bit 0. True output bit. DA0 is LSB.
77	DR_EN	Data Ready Enable, Typically DNC. See the DR_EN section.
78	DRA	Channel A Data Ready. Complement output.
80	DRA	Channel A Data Ready. True output.
81 to 94, 109 to 112, 129 to 132[1]	AGND	Analog Ground.
113 to 120	VA	Analog Supply, 3.7 V.
121 to 128[1]	DGND	Digital Ground.

[1] Internal ground plane connections: Section A = DGND, Pins 121 to 124; Section B = DGND, Pins 125 to 128; Section C = AGND, Pins 129 to 132.

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