



32-Channel, 3 V/5 V, Single-Supply, 12-Bit, Voltage Output DAC

AD5383

FEATURES

Guaranteed monotonic
INL error: ± 1 LSB max
On-chip 1.25 V/2.5 V, 10 ppm/ $^{\circ}\text{C}$ reference
Temperature range: -40°C to $+85^{\circ}\text{C}$
Rail-to-rail output amplifier
Power-down mode
Package type: 100-lead LQFP (14 mm \times 14 mm)
User Interfaces:
Parallel
Serial (SPI[®]/QSPI[™]/MICROWIRE[™]/DSP compatible, featuring data readback)
I²C[®] compatible

INTEGRATED FUNCTIONS

Channel monitor
Simultaneous output update via $\overline{\text{LDAC}}$
Clear function to user programmable code
Amplifier boost mode to optimize slew rate
User programmable offset and gain adjust
Toggle mode enables square wave generation
Thermal monitor

APPLICATIONS

Variable optical attenuators (VOA)
Level setting (ATE)
Optical micro-electro-mechanical systems (MEMS)
Control systems
Instrumentation

FUNCTIONAL BLOCK DIAGRAM

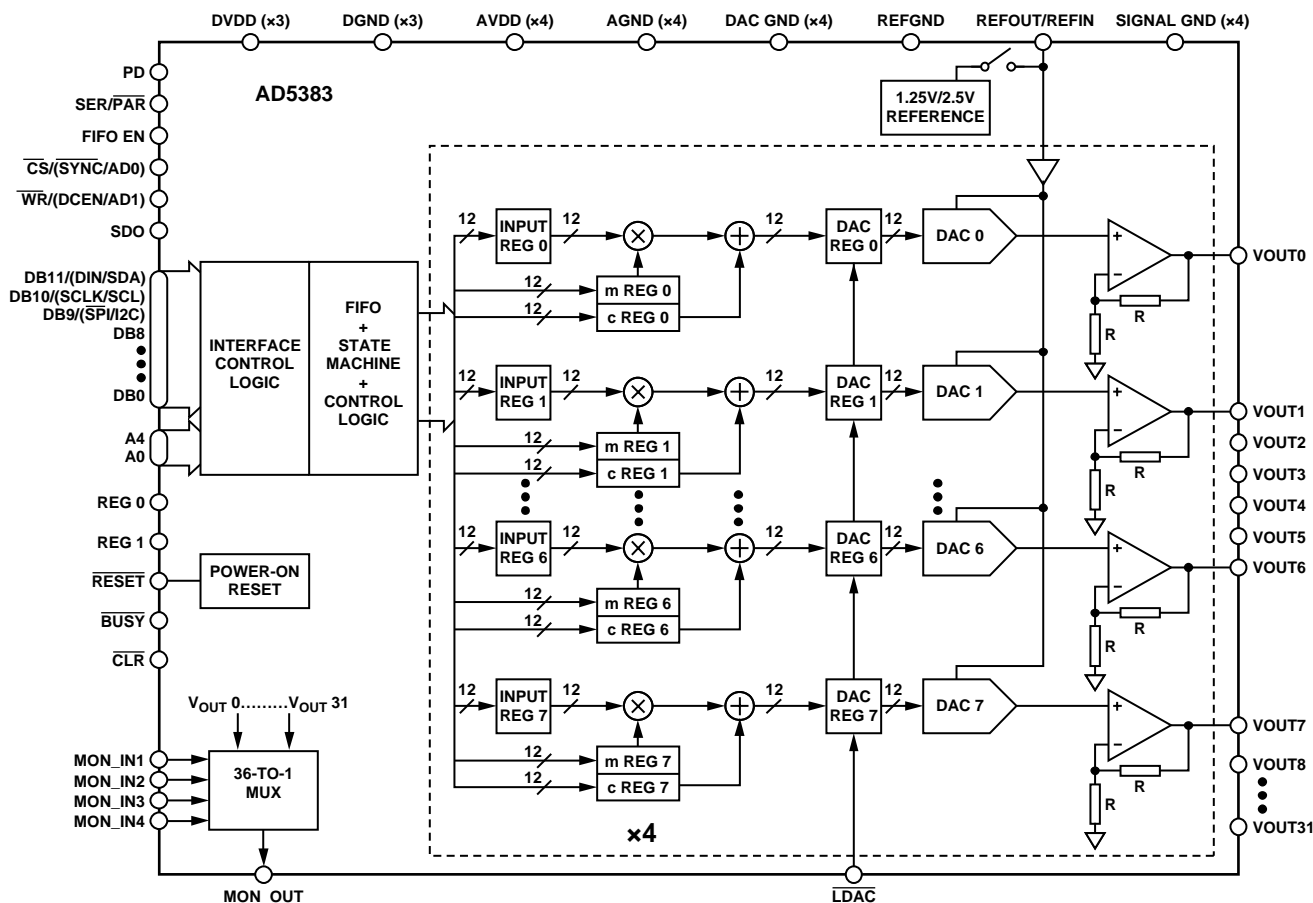


Figure 1.

Rev. 0

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REVISION HISTORY

5/04—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD5383 is a complete, single-supply, 32-channel, 12-bit DAC available in a 100-lead LQFP package. All 32 channels have an on-chip output amplifier with rail-to-rail operation. The AD5383 includes a programmable internal 1.25 V/2.5 V, 10 ppm/°C reference, an on-chip channel monitor function that multiplexes the analog outputs to a common MON_OUT pin for external monitoring, and an output amplifier boost mode that allows optimization of the amplifier slew rate. The AD5383 contains a double-buffered parallel interface that features a 20 ns \overline{WR} pulse width, an SPI/QSPI/MICROWIRE/DSP compatible serial interface with interface speeds in excess of

30 MHz, and an I²C compatible interface that supports a 400 kHz data transfer rate.

An input register followed by a DAC register provides double buffering, allowing the DAC outputs to be updated independently or simultaneously using the LDAC input.

Each channel has a programmable gain and offset adjust register that allows the user to fully calibrate any DAC channel. Power consumption is typically 0.25 mA/channel with boost off.

Table 1. Other High Channel Count, Low Voltage, Single Supply DAC Products in Portfolio

Model	Resolution	AV _{DD} Range	Output Channels	Linearity Error (LSB)	Package Description	Package Option
AD5380BST-5	14 Bits	4.5 V to 5.5 V	40	±4	100-Lead LQFP	ST-100
AD5380BST-3	14 Bits	2.7 V to 3.6 V	40	±4	100-Lead LQFP	ST-100
AD5384BBC-5	14 Bits	4.5 V to 5.5 V	40	±4	100-Lead CSPBGA	BC-100
AD5384BBC-3	14 Bits	2.7 V to 3.6 V	40	±4	100-Lead CSPBGA	BC-100
AD5381BST-5	12 Bits	4.5 V to 5.5 V	40	±1	100-Lead LQFP	ST-100
AD5381BST-3	12 Bits	2.7 V to 3.6 V	40	±1	100-Lead LQFP	ST-100
AD5382BST-5	14 Bits	4.5 V to 5.5 V	32	±4	100-Lead LQFP	ST-100
AD5382BST-3	14 Bits	2.7 V to 3.6 V	32	±4	100-Lead LQFP	ST-100
AD5390BST-5	14 Bits	4.5 V to 5.5 V	16	±3	52-Lead LQFP	ST-52
AD5390BCP-5	14 Bits	4.5 V to 5.5 V	16	±3	64-Lead LFCSP	CP-64
AD5390BST-3	14 Bits	2.7 V to 3.6 V	16	±3	52-Lead LQFP	ST-52
AD5390BCP-3	14 Bits	2.7 V to 3.6 V	16	±3	64-Lead LFCSP	CP-64
AD5391BST-5	12 Bits	4.5 V to 5.5 V	16	±1	52-Lead LQFP	ST-52
AD5391BCP-5	12 Bits	4.5 V to 5.5 V	16	±1	64-Lead LFCSP	CP-64
AD5391BST-3	12 Bits	2.7 V to 3.6 V	16	±1	52-Lead LQFP	ST-52
AD5391BCP-3	12 Bits	2.7 V to 3.6 V	16	±1	64-Lead LFCSP	CP-64
AD5392BST-5	14 Bits	4.5 V to 5.5 V	8	±3	52-Lead LQFP	ST-52
AD5392BCP-5	14 Bits	4.5 V to 5.5 V	8	±3	64-Lead LFCSP	CP-64
AD5392BST-3	14 Bits	2.7 V to 3.6 V	8	±3	52-Lead LQFP	ST-52
AD5392BCP-3	14 Bits	2.7 V to 3.6 V	8	±3	64-Lead LFCSP	CP-64

Table 2. 40-Channel, Bipolar Voltage Output DAC

Model	Resolution	Analog Supplies	Output Channels	Linearity Error (LSB)	Package	Package Option
AD5379ABC	14 Bits	±11.4 V to ±16.5 V	40	±3	108-Lead CSPBGA	BC-108

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SPECIFICATIONS

AD5383-5 SPECIFICATIONS

Table 3. $AV_{DD} = 4.5 \text{ V to } 5.5 \text{ V}$; $DV_{DD} = 2.7 \text{ V to } 5.5 \text{ V}$, $AGND = DGND = 0 \text{ V}$; External $REFIN = 2.5 \text{ V}$;
all specifications T_{MIN} to T_{MAX} , unless otherwise noted

Parameter	AD5383-5 ¹	Unit	Test Conditions/Comments
ACCURACY			
Resolution	12	Bits	
Relative Accuracy ² (INL)	± 1	LSB max	Guaranteed monotonic over temperature
Differential Nonlinearity (DNL)	± 1	LSB max	
Zero-Scale Error	± 4	mV max	
Offset Error	± 4	mV max	Measured at Code 32 in the linear region
Offset Error TC	± 5	$\mu\text{V}/^\circ\text{C}$ typ	
Gain Error	± 0.024	% FSR max	At 25°C
	± 0.06	% FSR max	T_{MIN} to T_{MAX}
Gain Temperature Coefficient ³	2	ppm FSR/ $^\circ\text{C}$ typ	
DC Crosstalk ³	0.5	LSB max	
REFERENCE INPUT/OUTPUT			
Reference Input ³			
Reference Input Voltage	2.5	V	$\pm 1\%$ for specified performance, $AV_{DD} = 2 \times REFIN + 50 \text{ mV}$
DC Input Impedance	1	$\text{M}\Omega$ min	Typically $100 \text{ M}\Omega$
Input Current	± 10	μA max	Typically $\pm 30 \text{ nA}$
Reference Range	1 to $V_{DD}/2$	V min/max	
Reference Output ⁴			Enabled via CR8 in the AD5383 control register. CR10 selects the reference voltage.
Output Voltage	2.495/2.505	V min/max	At ambient. Optimized for 2.5 V operation. CR10 = 1
	1.22/1.28	V min/max	1.25 V reference selected. CR10 = 0
Reference TC	± 10	ppm/ $^\circ\text{C}$ typ	
OUTPUT CHARACTERISTICS ³			
Output Voltage Range ²	$0/AV_{DD}$	V min/max	
Short-Circuit Current	40	mA max	
Load Current	± 1	mA max	
Capacitive Load Stability			
$R_L = \infty$	200	pF max	
$R_L = 5 \text{ k}\Omega$	1000	pF max	
DC Output Impedance	0.5	Ω max	
MONITOR PIN			
Output Impedance	500	Ω typ	
Three-State Leakage Current	100	nA typ	
LOGIC INPUTS (EXCEPT SDA/SCL) ³			$DV_{DD} = 2.7 \text{ V to } 5.5 \text{ V}$
V_{IH} , Input High Voltage	2	V min	
V_{IL} , Input Low Voltage	0.8	V max	
Input Current	± 10	μA max	Total for all pins. $T_A = T_{MIN}$ to T_{MAX}
Pin Capacitance	10	pF max	
LOGIC INPUTS (SDA, SCL ONLY)			
V_{IH} , Input High Voltage	0.7 DV_{DD}	V min	SMBus compatible at $DV_{DD} < 3.6 \text{ V}$
V_{IL} , Input Low Voltage	0.3 DV_{DD}	V max	SMBus compatible at $DV_{DD} < 3.6 \text{ V}$
I_{IN} , Input Leakage Current	± 1	μA max	
V_{HYST} , Input Hysteresis	0.05 DV_{DD}	V min	
C_{IN} , Input Capacitance	8	pF typ	
Glitch Rejection	50	ns max	Input filtering suppresses noise spikes of less than 50 ns

Parameter	AD5383-5 ¹	Unit	Test Conditions/Comments
LOGIC OUTPUTS (BUSY, SDO) ³			
V _{OL} , Output Low Voltage	0.4	V max	DV _{DD} = 5 V ± 10%, sinking 200 μA
V _{OH} , Output High Voltage	DV _{DD} – 1	V min	DV _{DD} = 5 V ± 10%, sourcing 200 μA
V _{OL} , Output Low Voltage	0.4	V max	DV _{DD} = 2.7 V to 3.6 V, sinking 200 μA
V _{OH} , Output High Voltage	DV _{DD} – 0.5	V min	DV _{DD} = 2.7 V to 3.6 V, sourcing 200 μA
High Impedance Leakage Current	±1	μA max	SDO only
High Impedance Output Capacitance	5	pF typ	SDO only
LOGIC OUTPUT (SDA) ³			
V _{OL} , Output Low Voltage	0.4	V max	I _{SINK} = 3 mA
	0.6	V max	I _{SINK} = 6 mA
Three-State Leakage Current	±1	μA max	
Three-State Output Capacitance	8	pF typ	
POWER REQUIREMENTS			
AV _{DD}	4.5/5.5	V min/max	
DV _{DD}	2.7/5.5	V min/max	
Power Supply Sensitivity ³			
ΔMidscale/ΔAV _{DD}	–85	dB typ	
AI _{DD}	0.375	mA/channel max	Outputs unloaded, Boost off. 0.25 mA/channel typ
	0.475	mA/channel max	Outputs unloaded, Boost on. 0.325 mA/channel typ
DI _{DD}	1	mA max	V _{IH} = DV _{DD} , V _{IL} = DGND.
AI _{DD} (Power-Down)	2	μA max	Typically 200 nA
DI _{DD} (Power-Down)	20	μA max	Typically 3 μA
Power Dissipation	65	mW max	Outputs unloaded, Boost off, AV _{DD} = DV _{DD} = 5 V

¹ AD5383-5 is calibrated using an external 2.5 V reference. Temperature range for all versions: –40°C to +85°C.

² Accuracy guaranteed from V_{OUT} = 10 mV to AV_{DD} – 50 mV.

³ Guaranteed by characterization, not production tested.

⁴ Default on the AD5383-5 is 2.5 V. Programmable to 1.25 V via CR10 in the AD5383 control register; operating the AD5383-5 with a 1.25 V reference will lead to degraded accuracy specifications.

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AD5383-3 SPECIFICATIONS

Table 4. $AV_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$; $DV_{DD} = 2.7 \text{ V to } 5.5 \text{ V}$, $AGND = DGND = 0 \text{ V}$; external $REFIN = 1.25 \text{ V}$;

all specifications T_{MIN} to T_{MAX} , unless otherwise noted

Parameter	AD5383-3 ¹	Unit	Test Conditions/Comments
ACCURACY			
Resolution	12	Bits	
Relative Accuracy ² (INL)	± 1	LSB max	
Differential Nonlinearity (DNL)	± 1	LSB max	Guaranteed monotonic over temperature
Zero-Scale Error	± 4	mV max	
Offset Error	± 4	mV max	Measured at Code 64 in the linear region
Offset Error TC	± 5	$\mu\text{V}/^\circ\text{C}$ typ	
Gain Error	± 0.024	% FSR max	At 25°C
	± 0.06	% FSR max	T_{MIN} to T_{MAX}
Gain Temperature Coefficient ³	2	ppm FSR/ $^\circ\text{C}$ typ	
DC Crosstalk ³	0.5	LSB max	
REFERENCE INPUT/OUTPUT			
Reference Input ³			
Reference Input Voltage	1.25	V	$\pm 1\%$ for specified performance
DC Input Impedance	1	M Ω min	Typically 100 M Ω
Input Current	± 10	μA max	Typically $\pm 30 \text{ nA}$
Reference Range	1 to $AV_{DD}/2$	V min/max	
Reference Output ⁴			Enabled via CR8 in the AD5383 control register. CR10 selects the reference voltage.
Output Voltage	1.247/1.253	V min/max	At ambient. Optimized for 1.25 V operation. CR10 = 0
	2.43/2.57	V min/max	2.5 V reference enabled. CR10 = 1
Reference TC	± 10	ppm/ $^\circ\text{C}$ typ	
OUTPUT CHARACTERISTICS ³			
Output Voltage Range ²	0/ AV_{DD}	V min/max	
Short-Circuit Current	40	mA max	
Load Current	± 1	mA max	
Capacitive Load Stability			
$R_L = \infty$	200	pF max	
$R_L = 5 \text{ k}\Omega$	1000	pF max	
DC Output Impedance	0.5	Ω max	
MONITOR PIN			
Output Impedance	500	Ω typ	
Three-State Leakage Current	100	nA typ	
LOGIC INPUTS (EXCEPT SDA/SCL) ³			$DV_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$
V_{IH} , Input High Voltage	2	V min	
V_{IL} , Input Low Voltage	0.8	V max	
Input Current	± 10	μA max	Total for all pins. $T_A = T_{MIN}$ to T_{MAX}
Pin Capacitance	10	pF max	
LOGIC INPUTS (SDA, SCL ONLY)			
V_{IH} , Input High Voltage	0.7 DV_{DD}	V min	SMBus compatible at $DV_{DD} < 3.6 \text{ V}$
V_{IL} , Input Low Voltage	0.3 DV_{DD}	V max	SMBus compatible at $DV_{DD} < 3.6 \text{ V}$
I_{IN} , Input Leakage Current	± 1	μA max	
V_{HYST} , Input Hysteresis	0.05 DV_{DD}	V min	
C_{IN} , Input Capacitance	8	pF typ	
Glitch Rejection	50	ns max	Input filtering suppresses noise spikes of less than 50 ns

Parameter	AD5383-3 ¹	Unit	Test Conditions/Comments
LOGIC OUTPUTS (BUSY, SDO) ³			
V _{OL} , Output Low Voltage	0.4	V max	Sinking 200 μ A
V _{OH} , Output High Voltage	DV _{DD} – 0.5	V min	Sourcing 200 μ A
High Impedance Leakage Current	± 1	μ A max	SDO only
High Impedance Output Capacitance	5	pF typ	SDO only
LOGIC OUTPUT (SDA) ³			
V _{OL} , Output Low Voltage	0.4	V max	I _{SINK} = 3 mA
	0.6	V max	I _{SINK} = 6 mA
Three-State Leakage Current	± 1	μ A max	
Three-State Output Capacitance	8	pF typ	
POWER REQUIREMENTS			
AV _{DD}	2.7/3.6	V min/max	
DV _{DD}	2.7/5.5	V min/max	
Power Supply Sensitivity ³			
Δ Midscale/ Δ AV _{DD}	–85	dB typ	
AI _{DD}	0.375	mA/channel max	Outputs unloaded, Boost off. 0.25 mA/channel typ
	0.475	mA/channel max	Outputs unloaded, Boost on. 0.325 mA/channel typ
DI _{DD}	1	mA max	V _{IH} = DV _{DD} , V _{IL} = DGND.
AI _{DD} (Power-Down)	2	μ A max	Typically 200 nA
DI _{DD} (Power-Down)	20	μ A max	Typically 3 μ A
Power Dissipation	39	mW max	Outputs unloaded, Boost off, AV _{DD} = DV _{DD} = 3 V

¹ AD5383-3 is calibrated using an external 1.25 V reference. Temperature range is –40°C to +85°C.

² Accuracy guaranteed from V_{OUT} = 10 mV to AV_{DD} – 50 mV.

³ Guaranteed by characterization, not production tested.

⁴ Default on the AD5383-3 is 1.25 V. Programmable to 2.5 V via CR10 in the AD5383 control register; operating the AD5383-3 with a 2.5 V reference will lead to degraded accuracy specifications and limited input code range.

AC CHARACTERISTICS¹

Table 5. AV_{DD} = 4.5 V to 5.5 V; DV_{DD} = 2.7 V to 5.5 V; AGND = DGND = 0 V

Parameter	All	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Output Voltage Settling Time ²			1/4 scale to 3/4 scale change settling to ± 1 LSB.
	6	μ s typ	
	8	μ s max	
Slew Rate ²	2	V/ μ s typ	Boost mode off, CR9 = 0
	3	V/ μ s typ	Boost mode on, CR9 = 1
Digital-to-Analog Glitch Energy	12	nV-s typ	
Glitch Impulse Peak Amplitude	15	mV typ	
Channel-to-Channel Isolation	100	dB typ	See Terminology section
DAC-to-DAC Crosstalk	1	nV-s typ	See Terminology section
Digital Crosstalk	0.8	nV-s typ	
Digital Feedthrough	0.1	nV-s typ	Effect of input bus activity on DAC output under test
Output Noise 0.1 Hz to 10 Hz	15	μ V p-p typ	External reference, midscale loaded to DAC
	40	μ V p-p typ	Internal reference, midscale loaded to DAC
Output Noise Spectral Density			
@ 1 kHz	150	nV/ $\sqrt{\text{Hz}}$ typ	
@ 10 kHz	100	nV/ $\sqrt{\text{Hz}}$ typ	

¹ Guaranteed by design and characterization, not production tested.

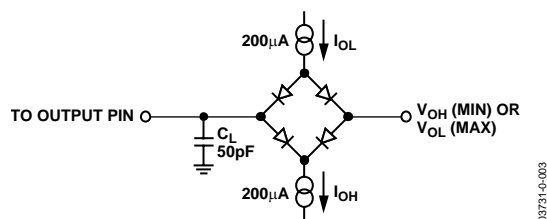
² The slew rate can be programmed via the current boost control bit (CR9) in the AD5383 control register.

TIMING CHARACTERISTICS

SERIAL INTERFACE TIMING

Table 6. $DV_{DD} = 2.7\text{ V to }5.5\text{ V}$; $AV_{DD} = 4.5\text{ V to }5.5\text{ V or }2.7\text{ V to }3.6\text{ V}$; $AGND = DGND = 0\text{ V}$; all specifications T_{MIN} to T_{MAX} , unless otherwise noted

Parameter ^{1, 2, 3}	Limit at T_{MIN} , T_{MAX}	Unit	Description
t_1	33	ns min	SCLK cycle time
t_2	13	ns min	SCLK high time
t_3	13	ns min	SCLK low time
t_4	13	ns min	\overline{SYNC} falling edge to SCLK falling edge setup time
t_5^4	13	ns min	24th SCLK falling edge to \overline{SYNC} falling edge
t_6^4	33	ns min	Minimum \overline{SYNC} low time
t_7	10	ns min	Minimum \overline{SYNC} high time
t_{7A}	50	ns min	Minimum \overline{SYNC} high time in Readback mode
t_8	5	ns min	Data setup time
t_9	4.5	ns min	Data hold time
t_{10}^4	30	ns max	24th SCLK falling edge to \overline{BUSY} falling edge
t_{11}	670	ns max	\overline{BUSY} pulse width low (single channel update)
t_{12}^4	20	ns min	24th SCLK falling edge to \overline{LDAC} falling edge
t_{13}	20	ns min	\overline{LDAC} pulse width low
t_{14}	100	ns max	\overline{BUSY} rising edge to DAC output response time
t_{15}	0	ns min	\overline{BUSY} rising edge to \overline{LDAC} falling edge
t_{16}	100	ns min	\overline{LDAC} falling edge to DAC output response time
t_{17}	8	$\mu\text{s typ}$	DAC output settling time, Boost mode off
t_{18}	20	ns min	\overline{CLR} pulse width low
t_{19}	35	$\mu\text{s max}$	\overline{CLR} pulse activation time
t_{20}^5	20	ns max	SCLK rising edge to SDO valid
t_{21}^5	5	ns min	SCLK falling edge to \overline{SYNC} rising edge
t_{22}^5	8	ns min	\overline{SYNC} rising edge to SCLK rising edge
t_{23}	20	ns min	\overline{SYNC} rising edge to \overline{LDAC} falling edge

¹ Guaranteed by design and characterization, not production tested.² All input signals are specified with $t_r = t_f = 5\text{ ns}$ (10% to 90% of V_{CC}) and are timed from a voltage level of 1.2 V.³ See Figure 2, Figure 3, Figure 4, and Figure 5.⁴ Standalone mode only.⁵ Daisy-chain mode only.Figure 2. Load Circuit for SDO Timing Diagram
(Serial Interface, Daisy-Chain Mode)

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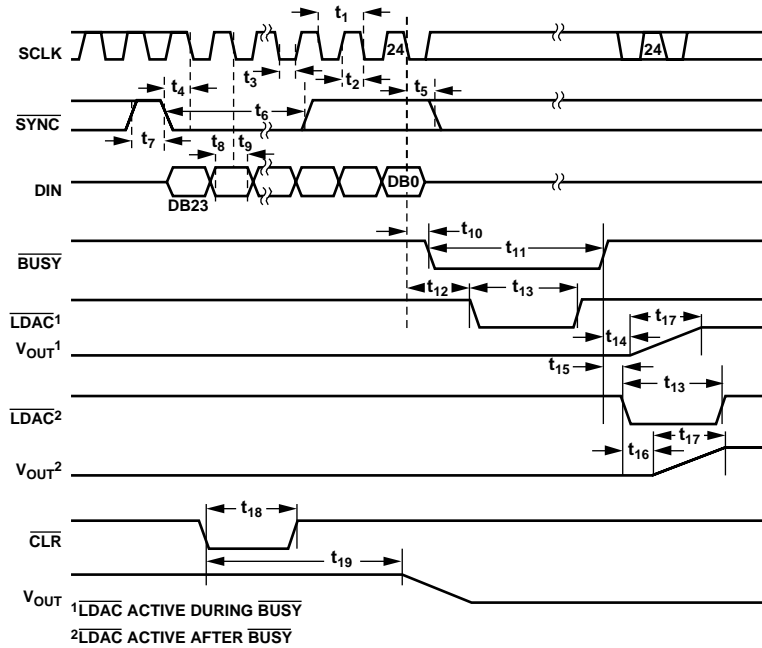


Figure 3. Serial Interface Timing Diagram (Standalone Mode)

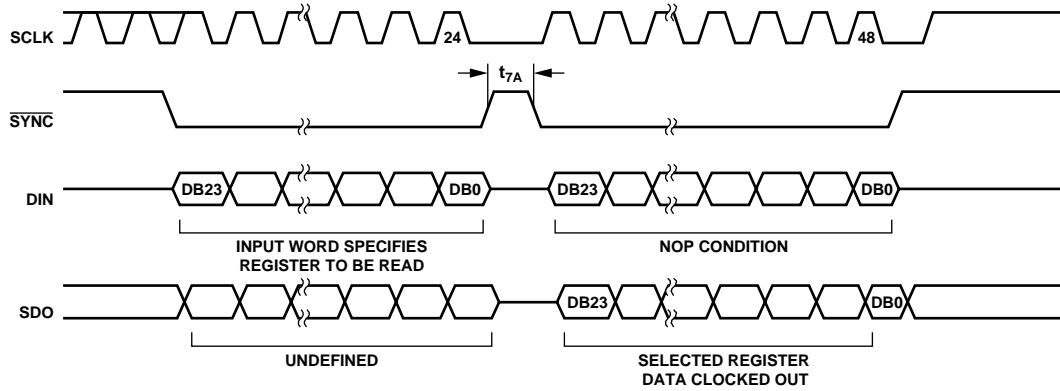


Figure 4. Serial Interface Timing Diagram (Data Readback Mode)

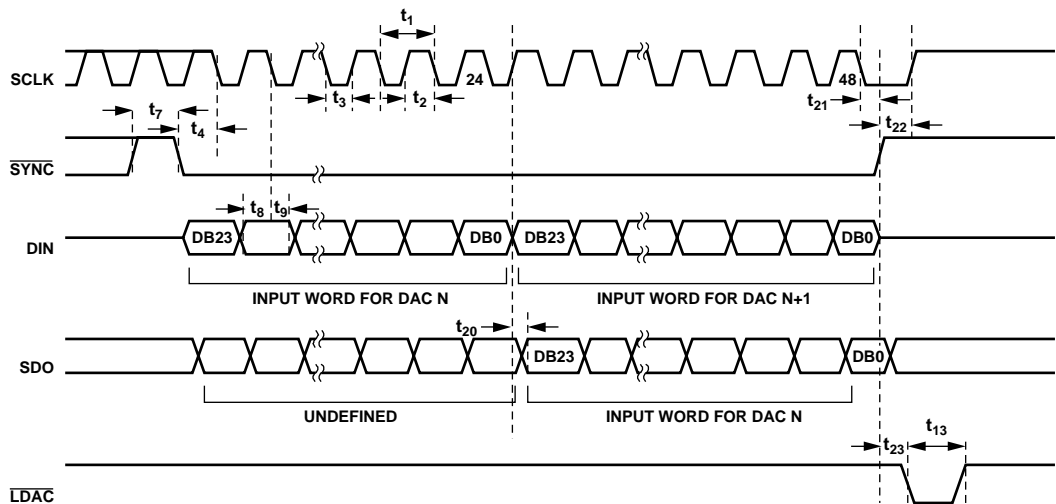


Figure 5. Serial Interface Timing Diagram (Daisy-Chain Mode)

I²C SERIAL INTERFACE TIMING

Table 7. $DV_{DD} = 2.7\text{ V to }5.5\text{ V}$; $AV_{DD} = 4.5\text{ V to }5.5\text{ V or }2.7\text{ V to }3.6\text{ V}$; $AGND = DGND = 0\text{ V}$; all specifications

T_{MIN} to T_{MAX} , unless otherwise noted

Parameter ^{1,2}	Limit at T_{MIN} , T_{MAX}	Unit	Description
F_{SCL}	400	kHz max	SCL clock frequency
t_1	2.5	$\mu\text{s min}$	SCL cycle time
t_2	0.6	$\mu\text{s min}$	t_{HIGH} , SCL high time
t_3	1.3	$\mu\text{s min}$	t_{LOW} , SCL low time
t_4	0.6	$\mu\text{s min}$	$t_{HD,STA}$, start/repeated start condition hold time
t_5	100	ns min	$t_{SU,DAT}$, data setup time
t_6^3	0.9	$\mu\text{s max}$	$t_{HD,DAT}$, data hold time
	0	$\mu\text{s min}$	$t_{HD,DAT}$, data hold time
t_7	0.6	$\mu\text{s min}$	$t_{SU,STA}$, setup time for repeated start
t_8	0.6	$\mu\text{s min}$	$t_{SU,STO}$, stop condition setup time
t_9	1.3	$\mu\text{s min}$	t_{BUF} , bus free time between a STOP and a START condition
t_{10}	300	ns max	t_R , rise time of SCL and SDA when receiving
	0	ns min	t_R , rise time of SCL and SDA when receiving (CMOS compatible)
t_{11}	300	ns max	t_F , fall time of SDA when transmitting
	0	ns min	t_F , fall time of SDA when receiving (CMOS compatible)
	300	ns max	t_F , fall time of SCL and SDA when receiving
	$20 + 0.1C_b^4$	ns min	t_F , fall time of SCL and SDA when transmitting
C_b	400	pF max	Capacitive load for each bus line

¹ Guaranteed by design and characterization, not production tested.

² See Figure 6.

³ A master device must provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} min of the SCL signal) in order to bridge the undefined region of SCL's falling edge.

⁴ C_b is the total capacitance, in pF, of one bus line. t_R and t_F are measured between $0.3DV_{DD}$ and $0.7DV_{DD}$.

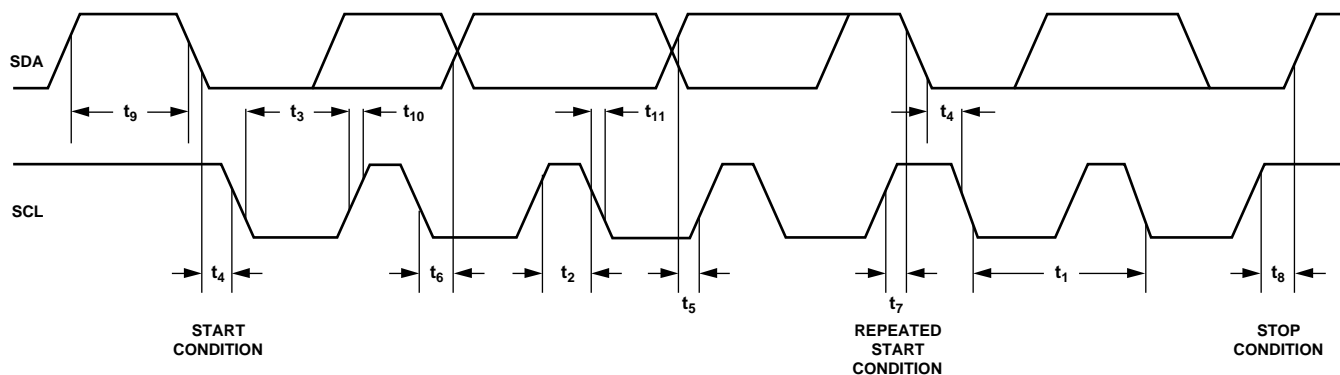


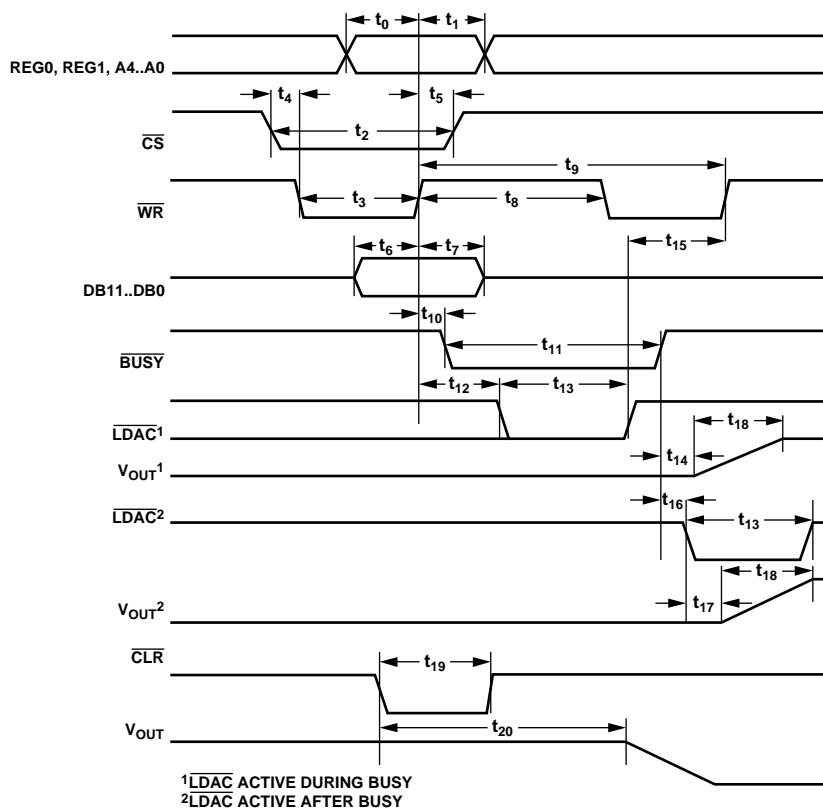
Figure 6. I²C Compatible Serial Interface Timing Diagram

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PARALLEL INTERFACE TIMING**Table 8.** $DV_{DD} = 2.7\text{ V to }5.5\text{ V}$; $AV_{DD} = 4.5\text{ V to }5.5\text{ V or }2.7\text{ V to }3.6\text{ V}$; $AGND = DGND = 0\text{ V}$; all specifications T_{MIN} to T_{MAX} , unless otherwise noted

Parameter ^{1,2,3}	Limit at T_{MIN} , T_{MAX}	Unit	Description
t_0	4.5	ns min	REG0, REG1, address to \overline{WR} rising edge setup time
t_1	4.5	ns min	REG0, REG1, address to \overline{WR} rising edge hold time
t_2	20	ns min	\overline{CS} pulse width low
t_3	20	ns min	\overline{WR} pulse width low
t_4	0	ns min	\overline{CS} to \overline{WR} falling edge setup time
t_5	0	ns min	\overline{WR} to \overline{CS} rising edge hold time
t_6	4.5	ns min	Data to \overline{WR} rising edge setup time
t_7	4.5	ns min	Data to \overline{WR} rising edge hold time
t_8	20	ns min	\overline{WR} pulse width high
t_9^4	700	ns min	Minimum \overline{WR} cycle time (single-channel write)
t_{10}^4	30	ns max	\overline{WR} rising edge to \overline{BUSY} falling edge
$t_{11}^{4,5}$	670	ns max	\overline{BUSY} pulse width low (single-channel update)
t_{12}	30	ns min	\overline{WR} rising edge to \overline{LDAC} falling edge
t_{13}	20	ns min	\overline{LDAC} pulse width low
t_{14}	100	ns max	\overline{BUSY} rising edge to DAC output response time
t_{15}	20	ns min	\overline{LDAC} rising edge to \overline{WR} rising edge
t_{16}	0	ns min	\overline{BUSY} rising edge to \overline{LDAC} falling edge
t_{17}	100	ns min	\overline{LDAC} falling edge to DAC output response time
t_{18}	8	$\mu\text{s max}$	DAC output settling time
t_{19}	20	ns min	\overline{CLR} pulse width low
t_{20}	35	$\mu\text{s max}$	\overline{CLR} pulse activation time

¹ Guaranteed by design and characterization, not production tested.² All input signals are specified with $t_R = t_F = 5\text{ ns}$ (10% to 90% of DV_{DD}) and timed from a voltage level of 1.2 V.³ See Figure 7.⁴ See Figure 29.⁵ Measured with the load circuit of Figure 2.



03731-0-008

Figure 7. Parallel Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 9. $T_A = 25^\circ\text{C}$, unless otherwise noted¹

Parameter	Rating
AV_{DD} to AGND	$-0.3\text{ V to }+7\text{ V}$
DV_{DD} to DGND	$-0.3\text{ V to }+7\text{ V}$
Digital Inputs to DGND	$-0.3\text{ V to }DV_{DD} + 0.3\text{ V}$
SDA/SCL to DGND	$-0.3\text{ V to }+7\text{ V}$
Digital Outputs to DGND	$-0.3\text{ V to }DV_{DD} + 0.3\text{ V}$
REFIN/REFOUT to AGND	$-0.3\text{ V to }AV_{DD} + 0.3\text{ V}$
AGND to DGND	$-0.3\text{ V to }+0.3\text{ V}$
VOU _T x to AGND	$-0.3\text{ V to }AV_{DD} + 0.3\text{ V}$
Analog Inputs to AGND	$-0.3\text{ V to }AV_{DD} + 0.3\text{ V}$
MON_IN Inputs to AGND	$-0.3\text{ V to }AV_{DD} + 0.3\text{ V}$
MON_OUT to AGND	$-0.3\text{ V to }AV_{DD} + 0.3\text{ V}$
Operating Temperature Range	
Commercial (B Version)	$-40^\circ\text{C to }+85^\circ\text{C}$
Storage Temperature Range	$-65^\circ\text{C to }+150^\circ\text{C}$
Junction Temperature (T_J Max)	150°C
100-lead LQFP Package	
θ_{JA} Thermal Impedance	44°C/W
Reflow Soldering	
Peak Temperature	230°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

¹ Transient currents of up to 100 mA will not cause SCR latch-up

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

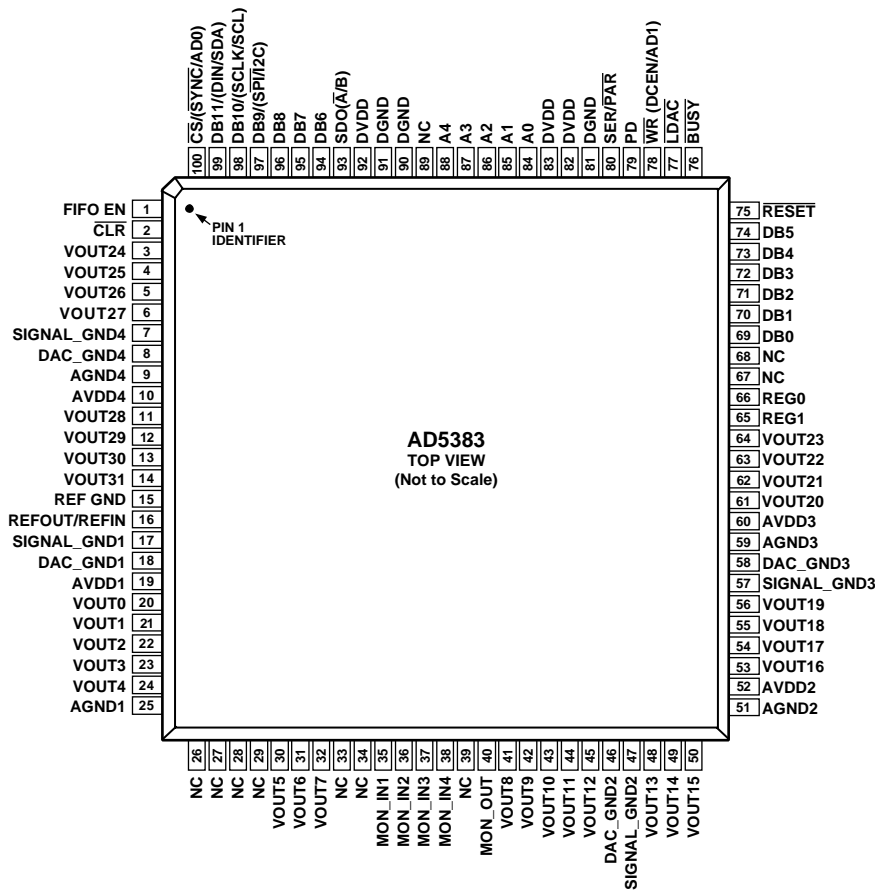


Figure 8. 100-Lead LQFP Pin Configuration

Table 10. Pin Function Descriptions

Mnemonic	Function
VOUTx	Buffered Analog Outputs for Channel x. Each analog output is driven by a rail-to-rail output amplifier operating at a gain of 2. Each output is capable of driving an output load of 5 k Ω to ground. Typical output impedance is 0.5 Ω .
SIGNAL_GND(1–4)	Analog Ground Reference Points for Each Group of Eight Output Channels. All SIGNAL_GND pins are tied together internally and should be connected to the AGND plane as close as possible to the AD5383.
DAC_GND(1–4)	Each group of eight channels contains a DAC_GND pin. This is the ground reference point for the internal 12-bit DAC. These pins should be connected to the AGND plane.
AGND(1–4)	Analog Ground Reference Point. Each group of eight channels contains an AGND pin. All AGND pins should be connected externally to the AGND plane.
AVDD(1–4)	Analog Supply Pins. Each group of eight channels has a separate AVDD pin. These pins are connected together internally and should be decoupled with a 0.1 μ F ceramic capacitor and a 10 μ F tantalum capacitor. Operating range for the AD5383-5 is 4.5 V to 5.5 V; operating range for the AD5383-3 is 2.7 V to 3.6 V.
DGND	Ground for All Digital Circuitry.
DVDD	Logic Power Supply. Guaranteed operating range is 2.7 V to 5.5 V. It is recommended that these pins be decoupled with 0.1 μ F ceramic and 10 μ F tantalum capacitors to DGND.
REFGND	Ground Reference Point for the Internal Reference.
REFOUT/REFIN	The AD5383 contains a common REFOUT/REFIN pin. When the internal reference is selected, this pin is the reference output. If the application requires an external reference, it can be applied to this pin and the internal reference can be disabled via the control register. The default for this pin is a reference input.

Mnemonic	Function
MON_OUT	When the monitor function is enabled, this output acts as the output of a 36-to-1 channel multiplexer that can be programmed to multiplex one of Channels 0 to 31 or any of the monitor input pins (MON_IN1 to MON_IN4) to the MON_OUT pin. The MON_OUT pin's output impedance is typically 500 Ω , and is intended to drive a high input impedance like that exhibited by SAR ADC inputs.
MON_INx	MON_IN Monitor Input Pins. The AD5383 contains four monitor input pins that allow the user to connect input signals within the maximum ratings of the device to these pins for monitoring purposes. Any of the signals applied to the MON_IN pins along with the 32 output channels can be switched to the MON_OUT pin via software. An external ADC for example can be used to monitor these signals.
SER/ $\overline{\text{PAR}}$	Interface Select Input. This pin allows the user to select whether the serial or parallel interface will be used. If it is tied high, the serial interface mode is selected and Pin 97 ($\overline{\text{SPI/I2C}}$) is used to determine if the interface mode is SPI or I ² C. Parallel interface mode is selected when SER/ $\overline{\text{PAR}}$ is low.
$\overline{\text{CS}}/(\overline{\text{SYNC}}/\text{AD0})$	In parallel interface mode, this pin acts as chip select input (level sensitive, active low). When low, the AD5383 is selected. Serial Interface Mode. This is the frame synchronization input signal for the serial clocks before the addressed register is updated.
$\overline{\text{WR}}/(\text{DCEN}/\text{AD1})$	I ² C Mode. This pin acts as a hardware address pin used in conjunction with AD1 to determine the software address for the device on the I ² C bus. Multifunction Pin. In parallel interface mode, this pin acts as write enable. In serial interface mode, this pin acts as a daisy-chain enable in SPI mode and as a hardware address pin in I ² C mode. Parallel Interface Write Input (edge sensitive). The rising edge of $\overline{\text{WR}}$ is used in conjunction with $\overline{\text{CS}}$ low and the address bus inputs to write to the selected device registers. Serial Interface. Daisy-chain select input (level sensitive, active high). When high, this signal is used in conjunction with SER/ $\overline{\text{PAR}}$ high to enable the SPI serial interface Daisy-Chain mode. I ² C Mode. This pin acts as a hardware address pin used in conjunction with AD0 to determine the software address for this device on the I ² C bus.
DB11–DB0	Parallel Data Bus. DB11 is the MSB and DB0 is the LSB of the input data-word on the AD5383.
A4–A0	Parallel Address Inputs. A5 to A0 are decoded to address one of the AD5383's 40 input channels. Used in conjunction with the REG1 and REG0 pins to determine the destination register for the input data.
REG1, REG0	In parallel interface mode REG1 and REG0 are used in decoding the destination registers for the input data. REG1 and REG0 are decoded to address the input data register, offset register, or gain register for the selected channel and are also used to decide the special function registers.
SDO/ $(\overline{\text{A}}/\text{B})$	Serial Data Output in Serial Interface Mode. Three-stateable CMOS output. SDO can be used for daisy-chaining a number of devices together. Data is clocked out on SDO on the rising edge of SCLK, and is valid on the falling edge of SCLK. When operating in parallel interface mode, this pin acts as the A or B data register select when writing data to the AD5383's data registers with toggle mode selected (see the Toggle Mode Function section). In toggle mode, the LDAC is used to switch the output between the data contained in the A and B data registers. All DAC channels contain two data registers. In normal mode, Data Register A is the default for data transfers.
$\overline{\text{BUSY}}$	Digital CMOS Output. $\overline{\text{BUSY}}$ goes low during internal calculations of the data (x2) loaded to the DAC data register. During this time, the user can continue writing new data to the x1, c, and m registers in parallel mode (these are stored in a FIFO), but no further updates to the DAC registers and DAC outputs can take place. If $\overline{\text{LDAC}}$ is taken low while $\overline{\text{BUSY}}$ is low, this event is stored. $\overline{\text{BUSY}}$ also goes low during power-on reset, and when the $\overline{\text{BUSY}}$ pin is low. During this time, the interface is disabled and any events on $\overline{\text{LDAC}}$ are ignored. A CLR operation also brings $\overline{\text{BUSY}}$ low.
$\overline{\text{LDAC}}$	Load DAC Logic Input (Active Low). If $\overline{\text{LDAC}}$ is taken low while $\overline{\text{BUSY}}$ is inactive (high), the contents of the input registers are transferred to the DAC registers and the DAC outputs are updated. If $\overline{\text{LDAC}}$ is taken low while $\overline{\text{BUSY}}$ is active and internal calculations are taking place, the $\overline{\text{LDAC}}$ event is stored and the DAC registers are updated when $\overline{\text{BUSY}}$ goes inactive. However any events on $\overline{\text{LDAC}}$ during power-on reset or on $\overline{\text{RESET}}$ are ignored.
$\overline{\text{CLR}}$	Asynchronous Clear Input. The $\overline{\text{CLR}}$ input is falling edge sensitive. When $\overline{\text{CLR}}$ is activated, all channels are updated with the data contained in the $\overline{\text{CLR}}$ code register. $\overline{\text{BUSY}}$ is low for a duration of 35 μs while all channels are being updated with the $\overline{\text{CLR}}$ code.
$\overline{\text{RESET}}$	Asynchronous Digital Reset Input (Falling Edge Sensitive). The function of this pin is equivalent to that of the power-on reset generator. When this pin is taken low, the state machine initiates a reset sequence to digitally reset the x1, m, c, and x2 registers to their default power-on values. This sequence typically takes 270 μs . The falling edge of $\overline{\text{RESET}}$ initiates the $\overline{\text{RESET}}$ process and $\overline{\text{BUSY}}$ goes low for the duration, returning high when $\overline{\text{RESET}}$ is complete. While $\overline{\text{BUSY}}$ is low, all interfaces are disabled and all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{BUSY}}$ returns high, the part resumes normal operation and the status of the $\overline{\text{RESET}}$ pin is ignored until the next falling edge is detected.

AD5383

Mnemonic	Function
PD	Power Down (Level Sensitive, Active High). PD is used to place the device in low power mode where the device consumes 2 μ A analog supply current and 20 μ A digital supply current. In power-down mode, all internal analog circuitry is placed in low power mode, and the analog output will be configured as a high impedance output or will provide a 100 k Ω load to ground, depending on how the power-down mode is configured. The serial interface remains active during power-down.
FIFOEN	FIFO Enable (Level Sensitive, Active High). When connected to DVDD, the internal FIFO is enabled, allowing the user to write to the device at full speed. FIFO is only available in parallel interface mode. The status of the FIFO_EN pin is sampled on power-up, and also following a CLEAR or RESET, to determine if the FIFO is enabled. In either serial or I ² C interface modes, the FIFO_EN pin should be tied low.
DB9 ($\overline{\text{SPI/I2C}}$)	Multifunction Input Pin. In parallel interface mode, this pin acts as DB9 of the parallel input data-word. In serial interface mode, this pin acts as serial interface mode select. When serial interface mode is selected (SER/PAR = 1) and this input is low, SPI mode is selected. In SPI mode, DB12 is the serial clock (SCLK) input and DB11 is the serial data (DIN) input. When serial interface mode is selected (SER/ $\overline{\text{PAR}}$ = 1) and this input is high I2C Mode is selected.
DB10 (SCLK/SCL)	In this mode, DB12 is the serial clock (SCL) input and DB11 is the serial data (SDA) input. Multifunction Input Pin. In parallel interface mode, this pin acts as DB10 of the parallel input data-word. In serial interface mode, this pin acts as a serial clock input. Serial Interface Mode. In serial interface mode, data is clocked into the shift register on the falling edge of SCLK. This operates at clock speeds up to 50 MHz.
DB11/(DIN/SDA)	I ² C Mode. In I ² C mode, this pin performs the SCL function, clocking data into the device. The data transfer rate in I ² C mode is compatible with both 100 kHz and 400 kHz operating modes. Multifunction Data Input Pin. In parallel interface mode, this pin acts as DB11 of the parallel input data-word. Serial Interface Mode. In serial interface mode, this pin acts as the serial data input. Data must be valid on the falling edge of SCLK.
NC	I ² C Mode. In I ² C mode, this pin is the serial data pin (SDA) operating as an open-drain input/output. No Connect. The user is advised not to connect any signal to these pins.

TERMINOLOGY

Relative Accuracy

Relative accuracy or endpoint linearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero-scale error and full-scale error, and is expressed in LSB.

Differential Nonlinearity

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB maximum ensures monotonicity.

Zero-Scale Error

Zero-scale error is the error in the DAC output voltage when all 0s are loaded into the DAC register. Ideally, with all 0s loaded to the DAC and $m = \text{all } 1\text{s}$, $c = 2^{n-1}$

$$V_{OUT}(\text{Zero-Scale}) = 0 \text{ V}$$

Zero-scale error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal), expressed in mV. It is mainly due to offsets in the output amplifier.

Offset Error

Offset error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal) in the linear region of the transfer function, expressed in mV. Offset error is measured on the AD5383-5 with Code 32 loaded into the DAC register, and on the AD5383-3 with Code 64.

Gain Error

Gain Error is specified in the linear region of the output range between $V_{OUT} = 10 \text{ mV}$ and $V_{OUT} = AV_{DD} - 50 \text{ mV}$. It is the deviation in slope of the DAC transfer characteristic from the ideal and is expressed in %FSR with the DAC output unloaded.

DC Crosstalk

This is the dc change in the output level of one DAC at midscale in response to a full-scale code (all 0s to all 1s, and vice versa) and output change of all other DACs. It is expressed in LSB.

DC Output Impedance

This is the effective output source resistance. It is dominated by package lead resistance.

Output Voltage Settling Time

This is the amount of time it takes for the output of a DAC to settle to a specified level for a $\frac{1}{4}$ to $\frac{3}{4}$ full-scale input change, and is measured from the BUSY rising edge.

Digital-to-Analog Glitch Energy

This is the amount of energy injected into the analog output at the major code transition. It is specified as the area of the glitch in nV-s. It is measured by toggling the DAC register data between 0x1FFF and 0x2000.

DAC-to-DAC Crosstalk

DAC-to-DAC crosstalk is the glitch impulse that appears at the output of one DAC due to both the digital change and to the subsequent analog output change at another DAC. The victim channel is loaded with midscale. DAC-to-DAC crosstalk is specified in nV-s.

Digital Crosstalk

The glitch impulse transferred to the output of one converter due to a change in the DAC register code of another converter is defined as the digital crosstalk and is specified in nV-s.

Digital Feedthrough

When the device is not selected, high frequency logic activity on the device's digital inputs can be capacitively coupled both across and through the device to show up as noise on the V_{OUT} pins. It can also be coupled along the supply and ground lines. This noise is digital feedthrough.

Output Noise Spectral Density

This is a measure of internally generated random noise. Random noise is characterized as a spectral density (voltage per $\sqrt{\text{Hertz}}$). It is measured by loading all DACs to midscale and measuring noise at the output. It is measured in nV/ $\sqrt{\text{Hz}}$ in a 1 Hz bandwidth at 10 kHz.

TYPICAL PERFORMANCE CHARACTERISTICS

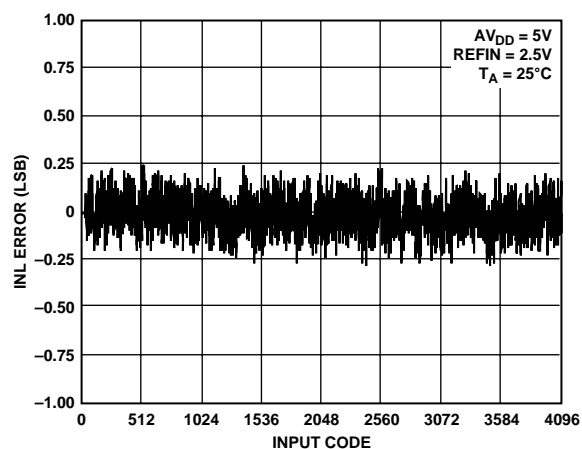


Figure 9. Typical AD5383-5 INL Plot

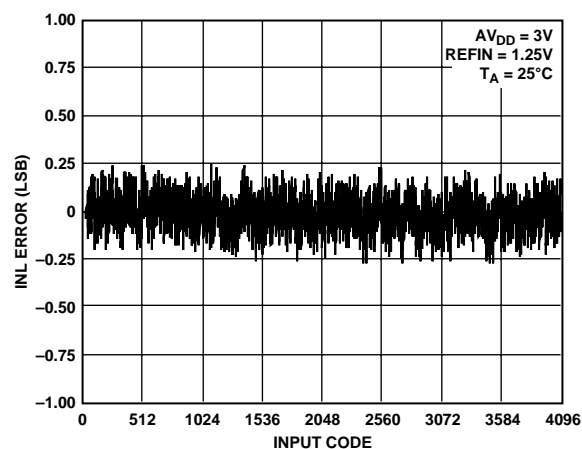


Figure 12. Typical AD5383-3 INL Plot

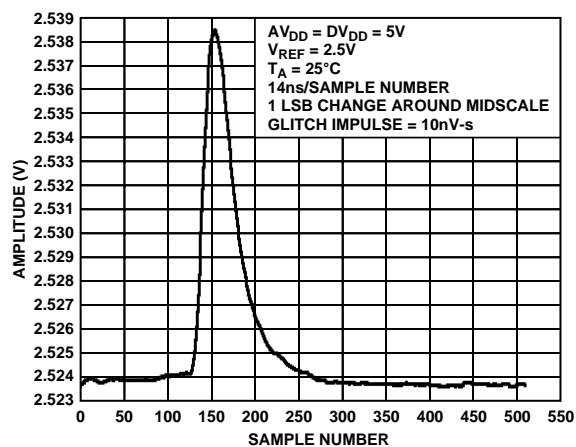


Figure 10. AD5383-5 Glitch Impulse

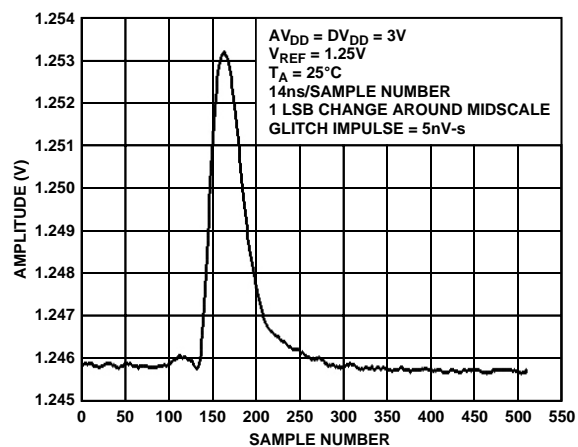


Figure 13. AD5383-3 Glitch Impulse

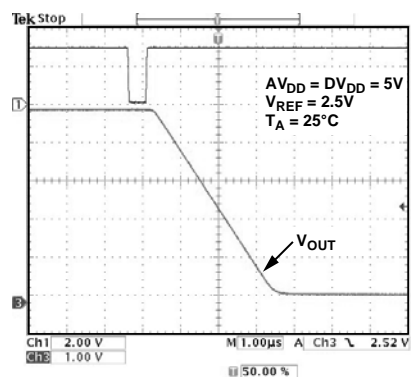


Figure 11. Slew Rate with Boost Off

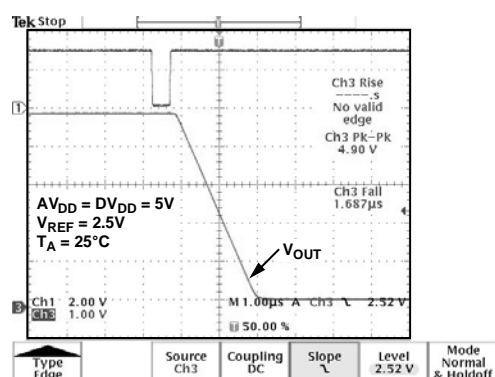


Figure 14. Slew Rate with Boost On

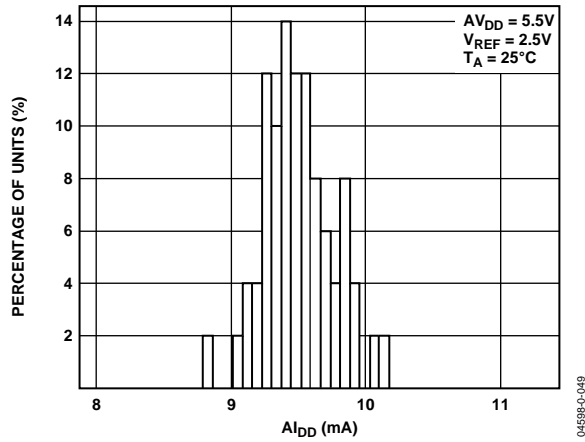


Figure 15. $A_{I_{DD}}$ Histogram

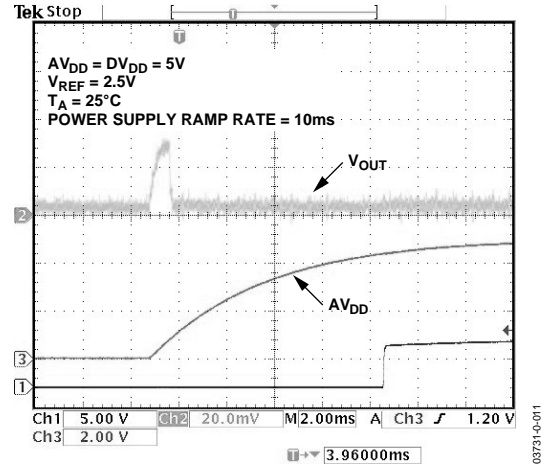


Figure 18. AD5383 Power-Up Transient

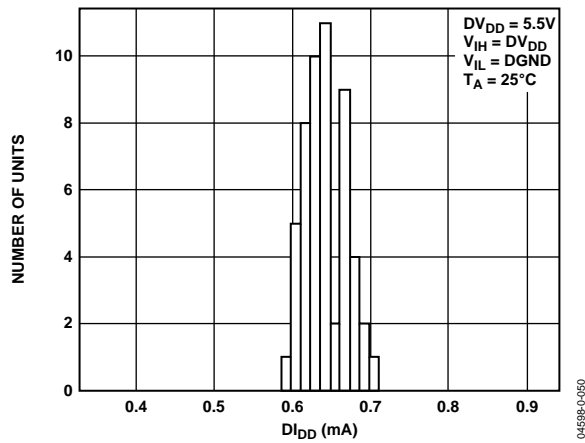


Figure 16. $D_{I_{DD}}$ Histogram

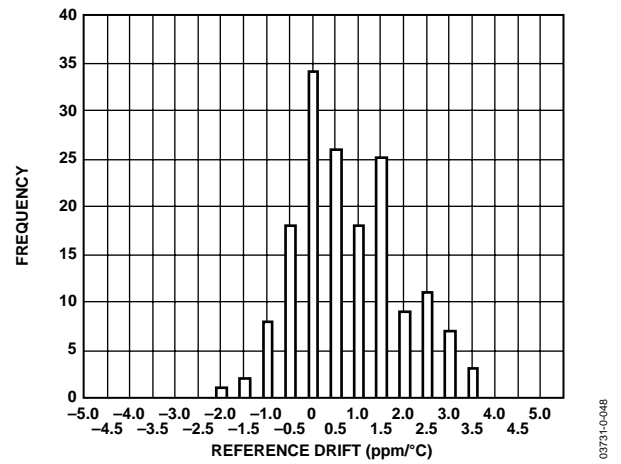


Figure 19. AD5383 $REFOUT$ Temperature Coefficient

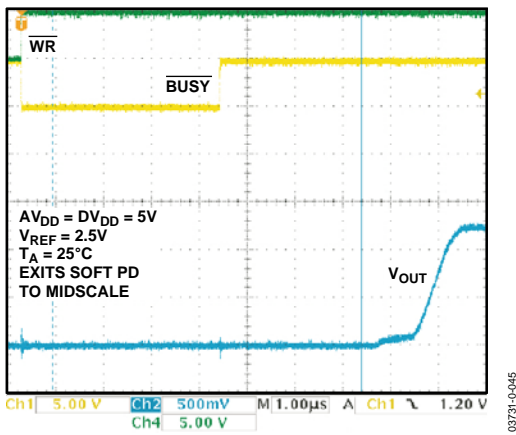


Figure 17. Exiting Soft Power-Down

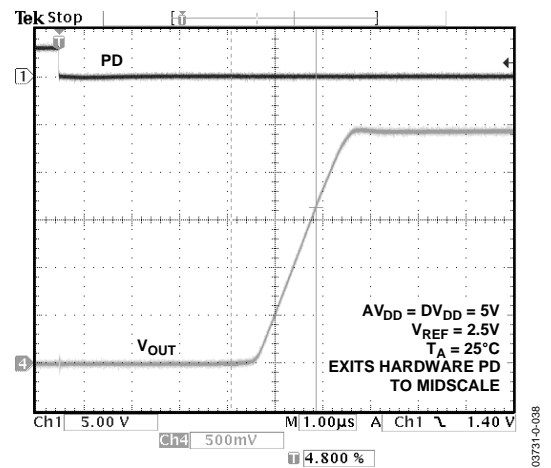


Figure 20. Exiting Hardware Power-Down

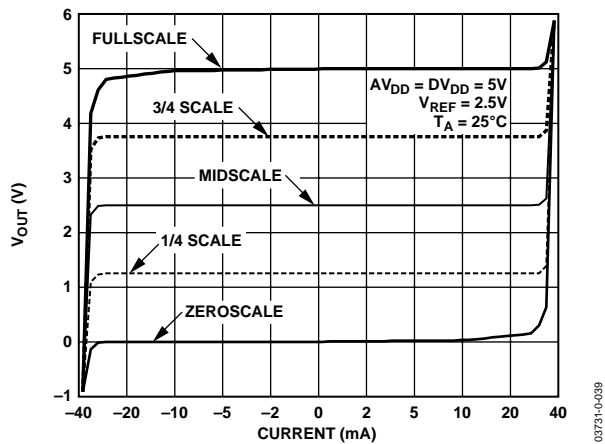


Figure 21. AD5383-5 Output Amplifier Source and Sink Capability

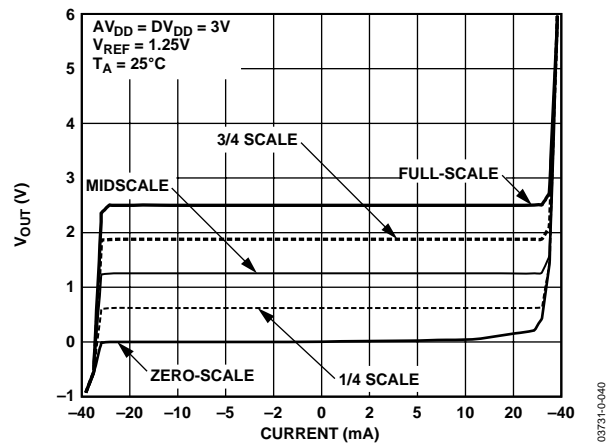


Figure 24. AD5383-3 Output Amplifier Source and Sink Capability

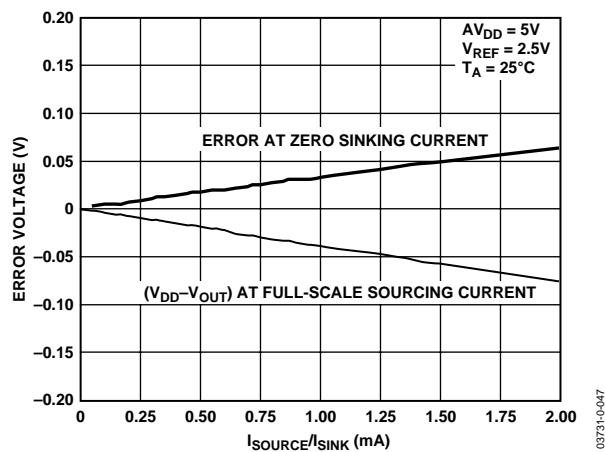


Figure 22. Headroom at Rails vs. Source/Sink Current

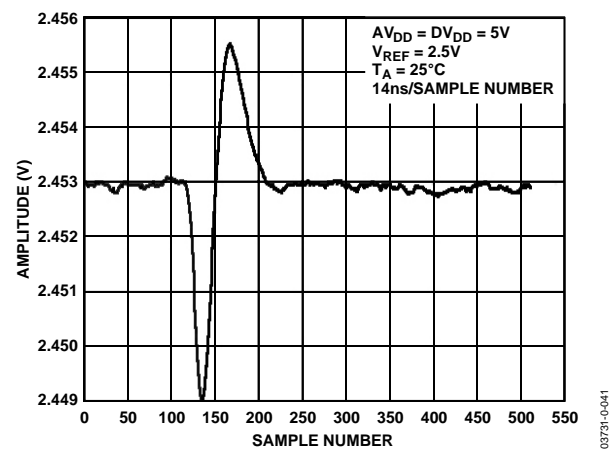


Figure 25. Adjacent Channel DAC-to-DAC Crosstalk

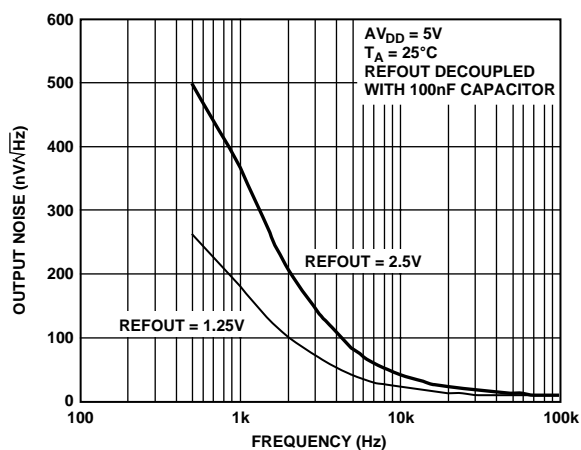


Figure 23. REFOUT Noise Spectral Density

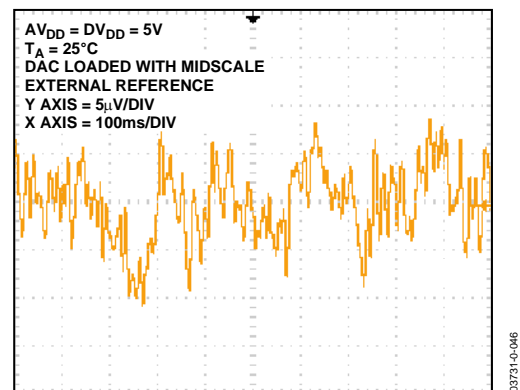


Figure 26. 0.1 Hz to 10 Hz Noise Plot

FUNCTIONAL DESCRIPTION

DAC ARCHITECTURE—GENERAL

The AD5383 is a complete, single-supply, 32-channel voltage output DAC that offers 12-bit resolution. The part is available in a 100-lead LQFP package and features both a parallel and a serial interface. This product includes an internal, software selectable, 1.25 V/2.5 V, 10 ppm/°C reference that can be used to drive the buffered reference inputs; alternatively, an external reference can be used to drive these inputs. Internal/external reference selection is via the CR8 bit in the control register; CR10 selects the reference magnitude if the internal reference is selected. All channels have an on-chip output amplifier with rail-to-rail output capable of driving 5 kΩ in parallel with a 200 pF load.

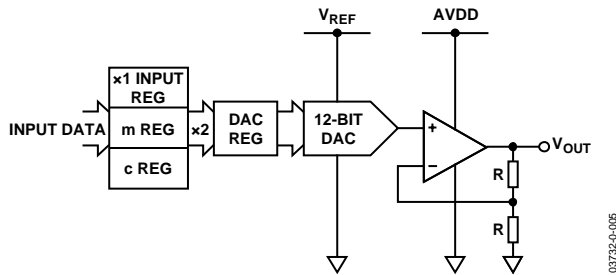


Figure 27. Single-Channel Architecture

The architecture of a single DAC channel consists of a 12-bit resistor-string DAC followed by an output buffer amplifier operating at a gain of 2. This resistor-string architecture guarantees DAC monotonicity. The 12-bit binary digital code loaded to the DAC register determines at what node on the string the voltage is tapped off before being fed to the output amplifier. Each channel on these devices contains independent offset and gain control registers that allow the user to digitally trim offset and gain. These registers give the user the ability to calibrate out errors in the complete signal chain, including the DAC, using the internal m and c registers, which hold the correction factors. All channels are double buffered, allowing synchronous updating of all channels using the LDAC pin. Figure 27 shows a block diagram of a single channel on the AD5383. The digital input transfer function for each DAC can be represented as

$$x2 = [(m + 2)/2^n \times x1] + (c - 2^{n-1})$$

where:

$x2$ = the data-word loaded to the resistor string DAC.

$x1$ = the 12-bit data-word written to the DAC input register.

m = the gain coefficient (default is 0xFFE). The gain coefficient is written to the 11 most significant bits (DB11 to DB1) and the LSB (DB0) is 0.

n = DAC resolution ($n = 12$ for AD5383).

c is the 12-bit offset coefficient (default is 0x800).

The complete transfer function for these devices can be represented as

$$V_{OUT} = 2 \times V_{REF} \times x2/2^n$$

$x2$ is the data-word loaded to the resistor string DAC. V_{REF} is the internal reference voltage or the reference voltage externally applied to the DAC REFOUT/REFIN pin. For specified performance, an external reference voltage of 2.5 V is recommended for the AD5380-5 and 1.25 V for the AD5380-3.

DATA DECODING

The AD5383 contains a 12-bit data bus, DB11–DB0. Depending on the value of REG1 and REG0 (see Table 11), this data is loaded into the addressed DAC input registers, offset (c) registers, or gain (m) registers. The format data, offset (c), and gain (m) register contents are shown in Table 12 to Table 14.

Table 11. Register Selection

REG1	REG0	Register Selected
1	1	Input Data Register (x1)
1	0	Offset Register (c)
0	1	Gain Register (m)
0	0	Special Function Registers (SFRs)

Table 12. DAC Data Format (REG1 = 1, REG0 = 1)

DB11 to DB0			DAC Output (V)
1111	1111	1111	$2 V_{REF} \times (4095/4096)$
1111	1111	1110	$2 V_{REF} \times (4094/4096)$
1000	0000	0001	$2 V_{REF} \times (2049/4096)$
1000	0000	0000	$2 V_{REF} \times (2048/4096)$
0111	1111	1111	$2 V_{REF} \times (2047/4096)$
0000	0000	0001	$2 V_{REF} \times (1/4096)$
0000	0000	0000	0

Table 13. Offset Data Format (REG1 = 1, REG0 = 0)

DB11 to DB0			Offset (LSB)
1111	1111	1111	+2048
1111	1111	1110	+2047
1000	0000	0001	+1
1000	0000	0000	0
0111	1111	1111	-1
0000	0000	0001	-2047
0000	0000	0000	-2048

Table 14. Gain Data Format (REG1 = 0, REG0 = 1)

DB11 to DB1			Gain Factor
1111	1111	1110	1
1011	1111	1110	0.75
0111	1111	1110	0.5
0011	1111	1110	0.25
0000	0000	0000	0

ON-CHIP SPECIAL FUNCTION REGISTERS (SFR)

The AD5383 contains a number of special function registers (SFRs), as outlined in Table 15. SFRs are addressed with $REG1 = REG0 = 0$ and are decoded using address bits A4 to A0.

Table 15. SFR Register Functions ($REG1 = 0$, $REG0 = 0$)

R/W	A4	A3	A2	A1	A0	Function
X	0	0	0	0	0	NOP (No Operation)
0	0	0	0	0	1	Write CLR Code
0	0	0	0	1	0	Soft CLR
0	0	1	0	0	0	Soft Power-Down
0	0	1	0	0	1	Soft Power-Up
0	0	1	1	0	0	Control Register Write
1	0	1	1	0	0	Control Register Read
0	0	1	0	1	0	Monitor Channel
0	0	1	1	1	1	Soft Reset

SFR COMMANDS

NOP (No Operation)

$REG1 = REG0 = 0$, A4–A0 = 00000

Performs no operation but is useful in serial readback mode to clock out data on D_{OUT} for diagnostic purposes. $BUSY$ pulses low during a NOP operation.

Write CLR Code

$REG1 = REG0 = 0$, A4–A0 = 00001
DB11–DB0 = Contain the CLR data

Bringing the \overline{CLR} line low or exercising the soft clear function will load the contents of the DAC registers with the data contained in the user configurable CLR register, and will set $VOUT0$ to $VOUT31$ accordingly. This can be very useful for setting up a specific output voltage in a clear condition. It is also beneficial for calibration purposes; the user can load full scale or zero scale to the clear code register and then issue a hardware or software clear to load this code to all DACs, removing the need for individual writes to each DAC. Default on power-up is all zeros.

Soft CLR

$REG1 = REG0 = 0$, A4–A0 = 00010
DB11–DB0 = Don't Care

Executing this instruction performs the CLR, which is functionally the same as that provided by the external \overline{CLR} pin. The DAC outputs are loaded with the data in the CLR code register. It takes 35 μs to fully execute the SOFT CLR, as indicated by the $BUSY$ low time.

Soft Power-Down

$REG1 = REG0 = 0$, A4–A0 = 01000
DB11–DB0 = Don't Care

Executing this instruction performs a global power-down feature that puts all channels into a low power mode that reduces the analog supply current to 2 μA max, and the digital current to 20 μA . In power-down mode, the output amplifier can be configured as a high impedance output or provide a 100 k Ω load to ground. The contents of all internal registers are retained in power-down mode. No register can be written to while in power-down.

Soft Power-Up

$REG1 = REG0 = 0$, A4–A0 = 01001
DB11–DB0 = Don't Care

This instruction is used to power up the output amplifiers and the internal reference. The time to exit power-down is 8 μs . The hardware power-down and software function are internally combined in a digital OR function.

Soft RESET

$REG1 = REG0 = 0$, A4–A0 = 01111
DB11–DB0 = Don't Care

This instruction is used to implement a software reset. All internal registers are reset to their default values, which correspond to m at full scale and c at zero. The contents of the DAC registers are cleared, setting all analog outputs to 0 V. The soft reset activation time is 135 μs .

Table 16. Control Register Contents

MSB											LSB
CR11	CR10	CR9	CR8	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0

Control Register Write/Read

REG1 = REG0 = 0, A4–A0 = 01100, $\overline{R/\overline{W}}$ status determines if the operation is a write ($\overline{R/\overline{W}} = 0$) or a read ($\overline{R/\overline{W}} = 1$). DB11 to DB0 contains the control register data.

Control Register Contents

CR11: Power-Down Status. This bit is used to configure the output amplifier state in power down.

CR11 = 1: Amplifier output is high impedance (default on power-up).

CR11 = 0: Amplifier output is 100 kΩ to ground.

CR10: REF Select. This bit selects the operating internal reference for the AD5383. CR12 is programmed as follows:

CR10 = 1: Internal reference is 2.5 V (AD5383-5 default), the recommended operating reference for AD5383-5.

CR10 = 0: Internal reference is 1.25 V (AD5383-3 default), the recommended operating reference for AD5383-3.

CR9: Current Boost Control. This bit is used to boost the current in the output amplifier, thereby altering its slew rate. This bit is configured as follows:

CR9 = 1: Boost Mode On. This maximizes the bias current in the output amplifier, optimizing its slew rate but increasing the power dissipation.

CR9 = 0: Boost Mode Off (default on power-up). This reduces the bias current in the output amplifier and reduces the overall power consumption.

CR8: Internal/External Reference. This bit determines if the DAC uses its internal reference or an externally applied reference.

CR8 = 1: Internal Reference Enabled. The reference output depends on data loaded to CR10.

CR8 = 0: External Reference Selected (default on power up).

CR7: Channel Monitor Enable (see Channel Monitor Function)

CR7 = 1: Monitor Enabled. This enables the channel monitor function. After a write to the monitor channel in the SFR register, the selected channel output is routed to the MON_OUT pin.

CR7 = 0: Monitor Disabled (default on power-up). When the monitor is disabled, the MON_OUT pin is tristated.

CR6: Thermal Monitor Function. This function is used to monitor the AD5383's internal die temperature when enabled. The thermal monitor powers down the output amplifiers when the temperature exceeds 130°C. This function can be used to protect the device in cases where power dissipation may be exceeded if a number of output channels are simultaneously short-circuited. A soft power-up will re-enable the output amplifiers if the die temperature has dropped below 130°C.

CR6 = 1: Thermal Monitor Enabled.

CR6 = 0: Thermal Monitor Disabled (default on power-up).

CR5 and CR4: Don't Care.

CR3 to CR0: Toggle Function Enable. This function allows the user to toggle the output between two codes loaded to the A and B register for each DAC. Control register bits CR3 to CR0 are used to enable individual groups of eight channels for operation in toggle mode. A Logic 1 written to any bit enables a group of channels; a Logic 0 disables a group. LDAC is used to toggle between the two registers. Logic 1 enables a group of channels; Logic 0 disables a group of channels.

Table 17.

CR Bit	Group	Channels
CR3	3	24–31
CR2	2	16–23
CR1	1	8–15
CR0	0	0–7

Channel Monitor Function

REG1 = REG0 = 0, A4–A0 = 01010

DB11–DB6 = Contain data to address the monitored channel.

A channel monitor function is provided on the AD5383. This feature, which consists of a multiplexer addressed via the interface, allows any channel output or signals connected to the MON_IN pins to be routed to the MON_OUT pin for monitoring using an external ADC. The channel monitor function must be enabled in the control register before any channels are routed to MON_OUT. On the AD5383, DB11 to DB6 contain the channel address for the monitored channel. Selecting channel address 63 three-states MON_OUT.

AD5383

Table 18. AD5383 Channel Monitor Decoding

REG1	REG0	A4	A3	A2	A1	A0	DB11	DB10	DB9	DB8	DB7	DB6	DB5-DB0	MON_OUT
0	0	0	1	0	1	0	0	0	0	0	0	0	X	VOUT0
0	0	0	1	0	1	0	0	0	0	0	0	1	X	VOUT1
0	0	0	1	0	1	0	0	0	0	0	1	0	X	VOUT2
0	0	0	1	0	1	0	0	0	0	0	1	1	X	VOUT3
0	0	0	1	0	1	0	0	0	0	1	0	0	X	VOUT4
0	0	0	1	0	1	0	0	0	0	1	0	1	X	VOUT5
0	0	0	1	0	1	0	0	0	0	1	1	0	X	VOUT6
0	0	0	1	0	1	0	0	0	0	1	1	1	X	VOUT7
0	0	0	1	0	1	0	0	0	1	0	0	0	X	VOUT8
0	0	0	1	0	1	0	0	0	1	0	0	1	X	VOUT9
0	0	0	1	0	1	0	0	0	1	0	1	0	X	VOUT10
0	0	0	1	0	1	0	0	0	1	0	1	1	X	VOUT11
0	0	0	1	0	1	0	0	0	1	1	0	0	X	VOUT12
0	0	0	1	0	1	0	0	0	1	1	0	1	X	VOUT13
0	0	0	1	0	1	0	0	0	1	1	1	0	X	VOUT14
0	0	0	1	0	1	0	0	0	1	1	1	1	X	VOUT15
0	0	0	1	0	1	0	0	1	0	0	0	0	X	VOUT16
0	0	0	1	0	1	0	0	1	0	0	0	1	X	VOUT17
0	0	0	1	0	1	0	0	1	0	0	1	0	X	VOUT18
0	0	0	1	0	1	0	0	1	0	0	1	1	X	VOUT19
0	0	0	1	0	1	0	0	1	0	1	0	0	X	VOUT20
0	0	0	1	0	1	0	0	1	0	1	0	1	X	VOUT21
0	0	0	1	0	1	0	0	1	0	1	1	0	X	VOUT22
0	0	0	1	0	1	0	0	1	0	1	1	1	X	VOUT23
0	0	0	1	0	1	0	0	1	1	0	0	0	X	VOUT24
0	0	0	1	0	1	0	0	1	1	0	0	1	X	VOUT25
0	0	0	1	0	1	0	0	1	1	0	1	0	X	VOUT26
0	0	0	1	0	1	0	0	1	1	0	1	1	X	VOUT27
0	0	0	1	0	1	0	0	1	1	1	0	0	X	VOUT28
0	0	0	1	0	1	0	0	1	1	1	0	1	X	VOUT29
0	0	0	1	0	1	0	0	1	1	1	1	0	X	VOUT30
0	0	0	1	0	1	0	0	1	1	1	1	1	X	VOUT31
0	0	0	1	0	1	0	1	0	0	0	0	0	X	MON_IN1
0	0	0	1	0	1	0	1	0	0	0	0	1	X	MON_IN2
0	0	0	1	0	1	0	1	0	0	1	0	0	X	MON_IN3
0	0	0	1	0	1	0	1	0	0	0	1	1	X	MON_IN4
0	0	0	1	0	1	0	1	0	0	1	0	0	X	Undefined
0	0	0	1	0	1	0	1	0	0	1	0	1	X	Undefined
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
0	0	0	1	0	1	0	1	1	1	1	1	0	X	Undefined
0	0	0	1	0	1	0	1	1	1	1	1	1	X	Three-State

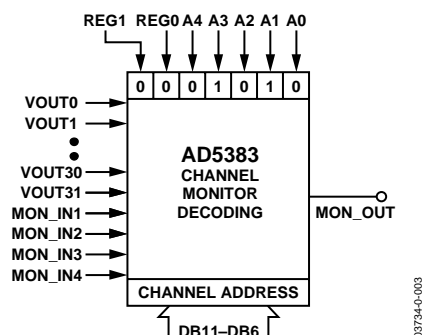


Figure 28. Channel Monitor Decoding

HARDWARE FUNCTIONS

RESET FUNCTION

Bringing the $\overline{\text{RESET}}$ line low resets the contents of all internal registers to their power-on reset state. Reset is a negative edge-sensitive input. The default corresponds to m at full scale and to c at zero. The contents of the DAC registers are cleared, setting VOUT 0 to VOUT 31 to 0 V. This sequence takes 270 μs max. The falling edge of $\overline{\text{RESET}}$ initiates the reset process; $\overline{\text{BUSY}}$ goes low for the duration, returning high when $\overline{\text{RESET}}$ is complete. While $\overline{\text{BUSY}}$ is low, all interfaces are disabled and all LDAC pulses are ignored. When $\overline{\text{BUSY}}$ returns high, the part resumes normal operation and the status of the $\overline{\text{RESET}}$ pin is ignored until the next falling edge is detected.

ASYNCHRONOUS CLEAR FUNCTION

Bringing the $\overline{\text{CLR}}$ line low clears the contents of the DAC registers to the data contained in the user configurable CLR register and sets VOUT 0 to VOUT 31 accordingly. This function can be used in system calibration to load zero scale and full scale to all channels. The execution time for a CLR is 32 μs .

BUSY AND LDAC FUNCTIONS

$\overline{\text{BUSY}}$ is a digital CMOS output that indicates the status of the AD5383. The value of x2, the internal data loaded to the DAC data register, is calculated each time the user writes new data to the corresponding x1, c, or m registers. During the calculation of x2, the $\overline{\text{BUSY}}$ output goes low. While $\overline{\text{BUSY}}$ is low, the user can continue writing new data to the x1, m, or c registers, but no DAC output updates can take place. The DAC outputs are updated by taking the $\overline{\text{LDAC}}$ input low. If $\overline{\text{LDAC}}$ goes low while $\overline{\text{BUSY}}$ is active, the $\overline{\text{LDAC}}$ event is stored and the DAC outputs update immediately after $\overline{\text{BUSY}}$ goes high. The user may hold the $\overline{\text{LDAC}}$ input permanently low, in which case the DAC outputs update immediately after $\overline{\text{BUSY}}$ goes high. $\overline{\text{BUSY}}$ also goes low during power-on reset and when a falling edge is detected on the $\overline{\text{RESET}}$ pin. During this time, all interfaces are disabled and any events on $\overline{\text{LDAC}}$ are ignored. The AD5383 contains an extra feature whereby a DAC register is not updated unless its x2 register has been written to since the last time $\overline{\text{LDAC}}$ was brought low. Normally, when $\overline{\text{LDAC}}$ is brought low, the DAC registers are filled with the contents of the x2 registers. However, the AD5383 will only update the DAC register if the x2 data has changed, thereby removing unnecessary digital crosstalk.

FIFO OPERATION IN PARALLEL MODE

The AD5383 contains a FIFO to optimize operation when operating in parallel interface mode. The FIFO Enable (level sensitive, active high) is used to enable the internal FIFO. When connected to DVDD, the internal FIFO is enabled, allowing the user to write to the device at full speed. FIFO is only available in parallel interface mode. The status of the FIFO_EN pin is sampled on power-up, and after a CLR or RESET, to determine if the FIFO is enabled. In either serial or I²C interface modes, FIFO_EN should be tied low. Up to 128 successive instructions can be written to the FIFO at maximum speed in parallel mode. When the FIFO is full, any further writes to the device are ignored. Figure 29 shows a comparison between FIFO mode and non-FIFO mode in terms of channel update time. Figure 29 also outlines digital loading time.

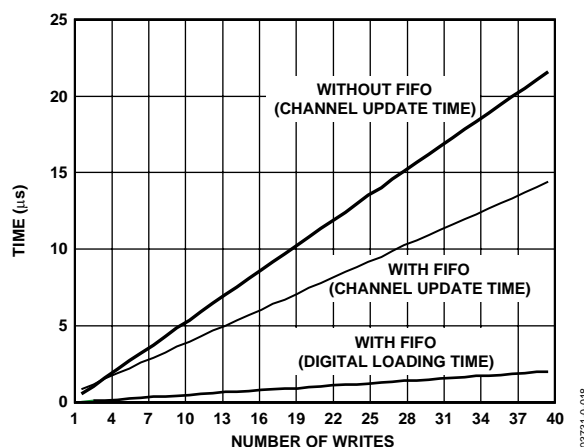


Figure 29. Channel Update Rate (FIFO vs. NON-FIFO)

POWER-ON RESET

The AD5383 contains a power-on reset generator and state machine. The power-on reset resets all registers to a predefined state and configures the analog outputs as high impedance. The $\overline{\text{BUSY}}$ pin goes low during the power-on reset sequencing, preventing data writes to the device.

POWER-DOWN

The AD5383 contains a global power-down feature that puts all channels into a low power mode and reduces the analog power consumption to 2 μA max and digital power consumption to 20 μA max. In power-down mode, the output amplifier can be configured as a high impedance output or provide a 100 k Ω load to ground. The contents of all internal registers are retained in power-down mode. When exiting power-down, the settling time of the amplifier will elapse before the outputs settle to their correct values.

AD5383 INTERFACES

The AD5383 contains both parallel and serial interfaces. Furthermore, the serial interface can be programmed to be either SPI, DSP, MICROWIRE, or I²C compatible. The $\overline{\text{SER/PAR}}$ pin selects parallel and serial interface modes. In serial mode, the $\overline{\text{SPI/I2C}}$ pin is used to select DSP, SPI, MICROWIRE, or I²C interface mode.

The devices use an internal FIFO memory to allow high speed successive writes in parallel interface mode. The user can continue writing new data to the device while write instructions are being executed. The $\overline{\text{BUSY}}$ signal indicates the current status of the device, going low while instructions in the FIFO are being executed. In parallel mode, up to 128 successive instructions can be written to the FIFO at maximum speed. When the FIFO is full, any further writes to the device are ignored.

To minimize both the power consumption of the device and the on-chip digital noise, the active interface only powers up fully when the device is being written to, i.e., on the falling edge of $\overline{\text{WR}}$ or the falling edge of $\overline{\text{SYNC}}$.

DSP, SPI, MICROWIRE COMPATIBLE SERIAL INTERFACES

The serial interface can be operated with a minimum of three wires in standalone mode or four wires in daisy-chain mode. Daisy chaining allows many devices to be cascaded together to increase system channel count. The $\overline{\text{SER/PAR}}$ pin must be tied high and the $\overline{\text{SPI/I2C}}$ pin (Pin 97) should be tied low to enable the DSP/SPI/MICROWIRE compatible serial interface. In serial interface mode, the user does not need to drive the parallel input data pins. The serial interface's control pins are

$\overline{\text{SYNC}}$, $\overline{\text{DIN}}$, $\overline{\text{SCLK}}$ —Standard 3-Wire Interface Pins.

$\overline{\text{DCEN}}$ —Selects Standalone Mode or Daisy-Chain Mode.

$\overline{\text{SDO}}$ —Data Out Pin for Daisy-Chain Mode.

Figure 3 and Figure 5 show timing diagrams for a serial write to the AD5383 in standalone and daisy-chain modes. The 24-bit data-word format for the serial interface is shown in Table 19

$\overline{\text{A/B}}$. When toggle mode is enabled, this pin selects whether the data write is to the A or B register. With toggle disabled, this bit should be set to zero to select the A data register.

$\overline{\text{R/W}}$ is the read or write control bit.

A4–A0 are used to address the input channels.

REG1 and REG0 select the register to which data is written, as shown in Table 11.

DB11–DB0 contain the input data-word.

X is a don't care condition.

Standalone Mode

By connecting the $\overline{\text{DCEN}}$ (Daisy-Chain Enable) pin low, standalone mode is enabled. The serial interface works with both a continuous and a noncontinuous serial clock. The first falling edge of $\overline{\text{SYNC}}$ starts the write cycle and resets a counter that counts the number of serial clocks to ensure that the correct number of bits are shifted into the serial shift register. Any further edges on $\overline{\text{SYNC}}$ except for a falling edge are ignored until 24 bits are clocked in. Once 24 bits have been shifted in, the $\overline{\text{SCLK}}$ is ignored. In order for another serial transfer to take place, the counter must be reset by the falling edge of $\overline{\text{SYNC}}$.

Table 19. 40-Channel, 12-bit DAC Serial Input Register Configuration

MSB																								LSB	
$\overline{\text{A/B}}$	$\overline{\text{R/W}}$	0	A4	A3	A2	A1	A0	REG1	REG0	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	X	X		

Daisy-Chain Mode

For systems that contain several devices, the SDO pin may be used to daisy-chain several devices together. This daisy-chain mode can be useful in system diagnostics and in reducing the number of serial interface lines.

By connecting the DCEN (Daisy-Chain Enable) pin high, daisy-chain mode is enabled. The first falling edge of $\overline{\text{SYNC}}$ starts the write cycle. The SCLK is continuously applied to the input shift register when $\overline{\text{SYNC}}$ is low. If more than 24 clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. This data is clocked out on the rising edge of SCLK and is valid on the falling edge. By connecting the SDO of the first device to the DIN input on the next device in the chain, a multidevice interface is constructed. Twenty-four clock pulses are required for each device in the system. Therefore, the total number of clock cycles must equal $24N$, where N is the total number of AD5383x devices in the chain.

When the serial transfer to all devices is complete, $\overline{\text{SYNC}}$ is taken high. This latches the input data in each device in the daisy-chain and prevents any further data from being clocked into the input shift register.

If the $\overline{\text{SYNC}}$ is taken high before 24 clocks are clocked into the part, this is considered a bad frame and the data is discarded.

The serial clock may be either a continuous or a gated clock. A continuous SCLK source can only be used if it can be arranged that $\overline{\text{SYNC}}$ is held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used and $\overline{\text{SYNC}}$ must be taken high after the final clock to latch the data.

Readback Mode

Readback mode is invoked by setting the $\overline{\text{R/W}}$ bit = 1 in the serial input register write. With $\overline{\text{R/W}} = 1$, Bits A4 to A0, in association with Bits REG1 and REG0, select the register to be read. The remaining data bits in the write sequence are don't cares. During the next SPI write, the data appearing on the SDO output will contain the data from the previously addressed register. For a read of a single register, the NOP command can be used in clocking out the data from the selected register on SDO. Figure 30 shows the readback sequence. For example, to read back the M register of Channel 0 on the AD5383, the following sequence should be implemented. First, write 0x404XXX to the AD5383 input register. This configures the AD5383 for read mode with the m register of Channel 0 selected. Note that data bits DB11 to DB0 are don't cares. Follow this with a second write, a NOP condition, 0x000000. During this write, the data from the m register is clocked out on the DOUT line, i.e., data clocked out will contain the data from the m register in Bits DB11 to DB0, and the top 10 bits contain the address information as previously written. In readback mode, the $\overline{\text{SYNC}}$ signal must frame the data. Data is clocked out on the rising edge of SCLK and is valid on the falling edge of the SCLK signal. If the SCLK idles high between the write and read operations of a readback operation, the first bit of data is clocked out on the falling edge of $\overline{\text{SYNC}}$.

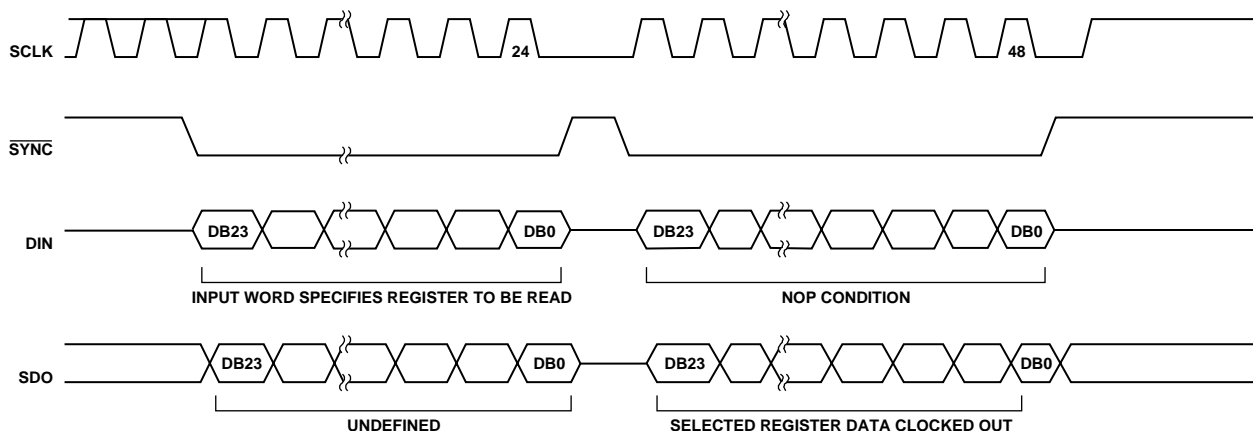


Figure 30. Serial Readback Operation

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I²C SERIAL INTERFACE

The AD5383 features an I²C compatible 2-wire interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate communication between the AD5383 and the master at rates up to 400 kHz. Figure 6 shows the 2-wire interface timing diagrams that incorporate three different modes of operation. In selecting the I²C operating mode, first configure serial operating mode (SER/PAR = 1) and then select I²C mode by configuring the $\overline{\text{SPI/I2C}}$ pin to a Logic 1. The device is connected to the I²C bus as a slave device (i.e., no clock is generated by the AD5383). The AD5383 has a 7-bit slave address 1010 1(AD1)(AD0). The 5 MSB are hard-coded and the 2 LSB are determined by the state of the AD1 and AD0 pins. The facility to hardware configure AD1 and AD0 allows four of these devices to be configured on the bus.

I²C Data Transfer

One data bit is transferred during each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high are control signals that configure START and STOP conditions. Both SDA and SCL are pulled high by the external pull-up resistors when the I²C bus is not busy.

START and STOP Conditions

A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high. A START condition from the master signals the beginning of a transmission to the AD5383. The STOP condition frees the bus. If a repeated START condition (Sr) is generated instead of a STOP condition, the bus remains active.

Repeated START Conditions

A repeated START (Sr) condition may indicate a change of data direction on the bus. Sr may be used when the bus master is writing to several I²C devices and wants to maintain control of the bus.

Acknowledge Bit (ACK)

The acknowledge bit (ACK) is the ninth bit attached to any 8-bit data-word. ACK is always generated by the receiving device. The AD5383 devices generate an ACK when receiving an address or data by pulling SDA low during the ninth clock period. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication.

AD5383 Slave Addresses

A bus master initiates communication with a slave device by issuing a START condition followed by the 7-bit slave address. When idle, the AD5383 waits for a START condition followed by its slave address. The LSB of the address word is the Read/Write (R/W) bit. The AD5383 is a receive only device; when communicating with the AD5383, $\overline{\text{R/W}} = 0$. After receiving the proper address 10101 (AD1) (AD0), the AD5383 issues an ACK by pulling SDA low for one clock cycle.

The AD5383 has four different user programmable addresses determined by the AD1 and AD0 bits.

Write Operation

There are three specific modes in which data can be written to the AD5383 DAC.

4-Byte Mode

When writing to the AD5383 DACs, the user must begin with an address byte ($\overline{\text{R/W}} = 0$) after which the DAC will acknowledge that it is prepared to receive data by pulling SDA low. The address byte is followed by the pointer byte; this addresses the specific channel in the DAC to be addressed and is also acknowledged by the DAC. Two bytes of data are then written to the DAC, as shown in Figure 31. A STOP condition follows. This allows the user to update a single channel within the AD5383 at any time and requires four bytes of data to be transferred from the master.

3-Byte Mode

In 3-byte mode, the user can update more than one channel in a write sequence without having to write the device address byte each time. The device address byte is only required once; subsequent channel updates require the pointer byte and the data bytes. In 3-byte mode, the user begins with an address byte ($\overline{\text{R/W}} = 0$), after which the DAC will acknowledge that it is prepared to receive data by pulling SDA low. The address byte is followed by the pointer byte. This addresses the specific channel in the DAC to be addressed and is also acknowledged by the DAC. This is then followed by the two data bytes. REG1 and REG0 determine the register to be updated.

If a STOP condition does not follow the data bytes, another channel can be updated by sending a new pointer byte followed by the data bytes. This mode only requires three bytes to be sent to update any channel once the device has been initially addressed, and reduces the software overhead in updating the AD5383 channels. A STOP condition at any time exits this mode. Figure 32 shows a typical configuration.

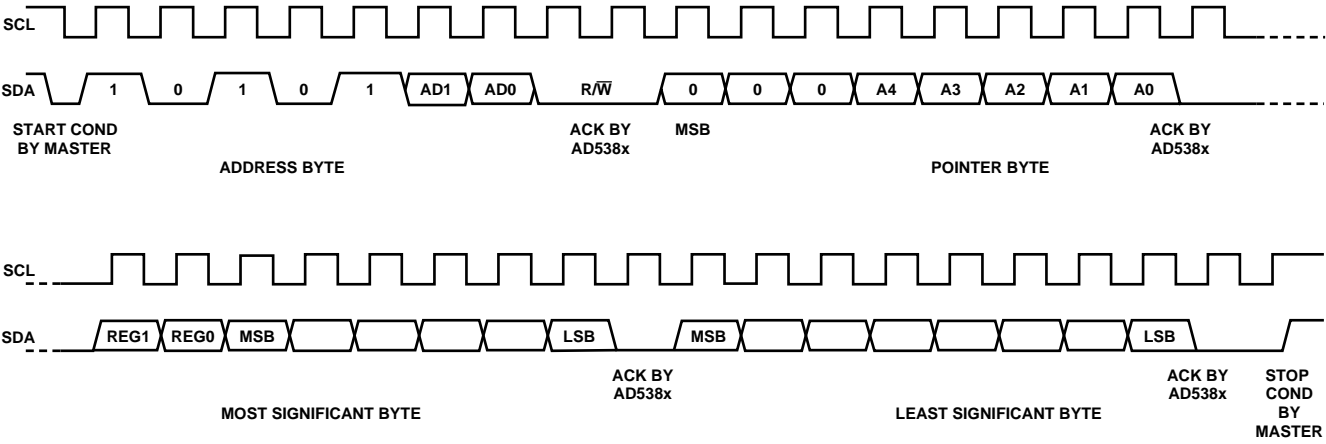


Figure 31. 4-Byte AD5383, I²C Write Operation

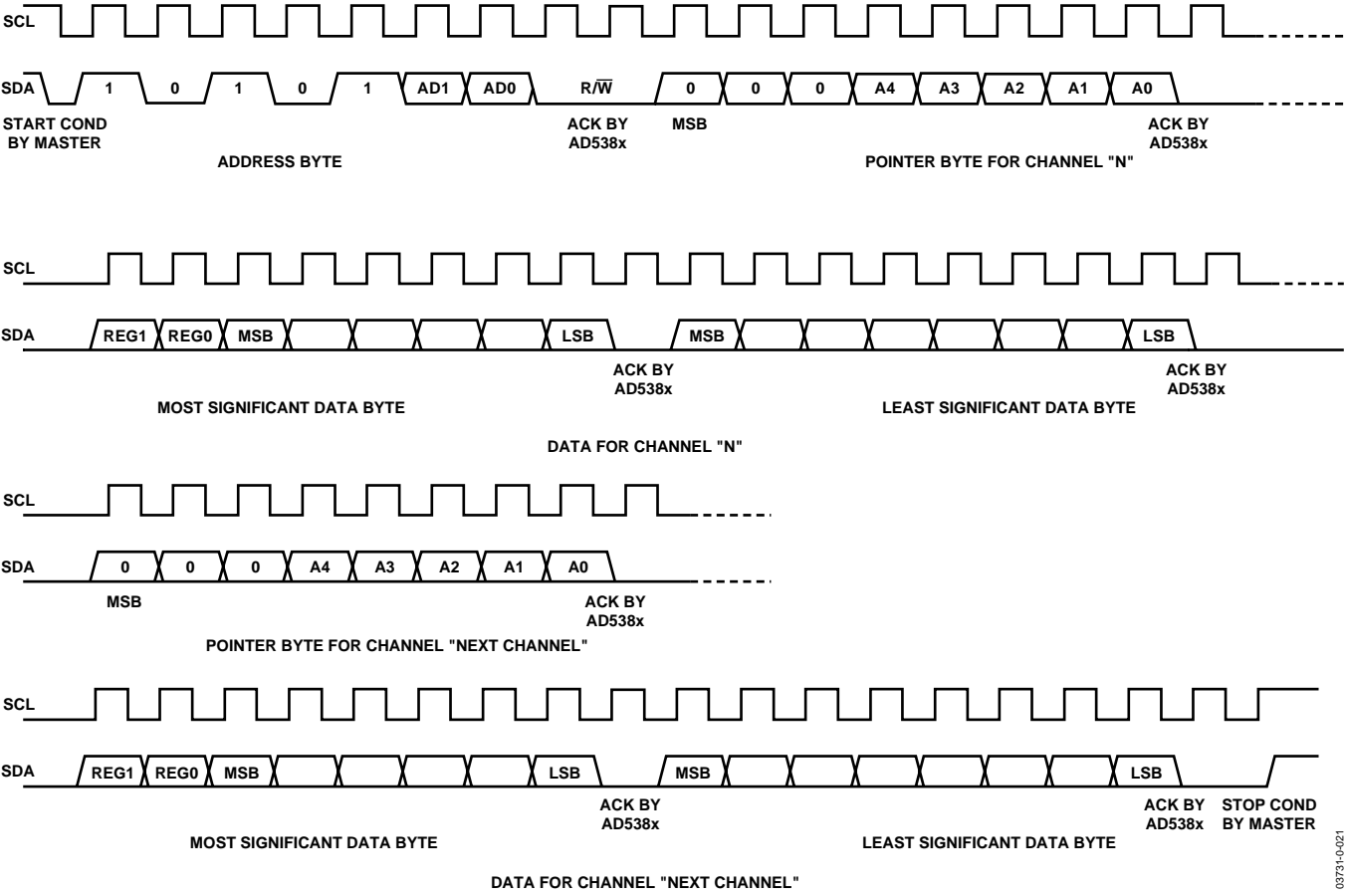


Figure 32. 3-Byte AD5383, I²C Write Operation

2-Byte Mode

Following initialization of 2-byte mode, the user can update channels sequentially. The device address byte is only required once and the pointer address pointer is configured for auto-increment or burst mode.

The user must begin with an address byte ($R/\overline{W} = 0$), after which the DAC will acknowledge that it is prepared to receive data by pulling SDA low. The address byte is followed by a specific pointer byte (0xFF) that initiates the burst mode of operation. The address pointer initializes to Channel 0, the data following the pointer is loaded to channel 0, and the address pointer automatically increments to the next address.

The REG0 and REG1 bits in the data byte determine which register will be updated. In this mode, following the initialization, only the two data bytes are required to update a channel. The channel address automatically increments from Address 0 to Channel 31 and then returns to the normal 3-byte mode of operation. This mode allows transmission of data to all channels in one block and reduces the software overhead in configuring all channels. A STOP condition at any time exits this mode. Toggle mode is not supported in 2-byte mode. Figure 33 shows a typical configuration.

PARALLEL INTERFACE

The $\overline{SER}/\overline{PAR}$ pin must be tied low to enable the parallel interface and disable the serial interfaces. Figure 7 shows the timing diagram for a parallel write. The parallel interface is controlled by the following pins:

\overline{CS} Pin

Active Low Device Select Pin.

\overline{WR} Pin

On the rising edge of \overline{WR} , with \overline{CS} low, the addresses on Pins A4 to A0 are latched; data present on the data bus is loaded into the selected input registers.

REG0, REG1 Pins

The REG0 and REG1 pins determine the destination register of the data being written to the AD5383. See Table 11.

Pins A4 to A0

Each of the 32 DAC channels can be addressed individually.

Pins DB11 to DB0

The AD5383 accepts a straight 12-bit parallel word on DB11 to DB0, where DB11 is the MSB and DB0 is the LSB.

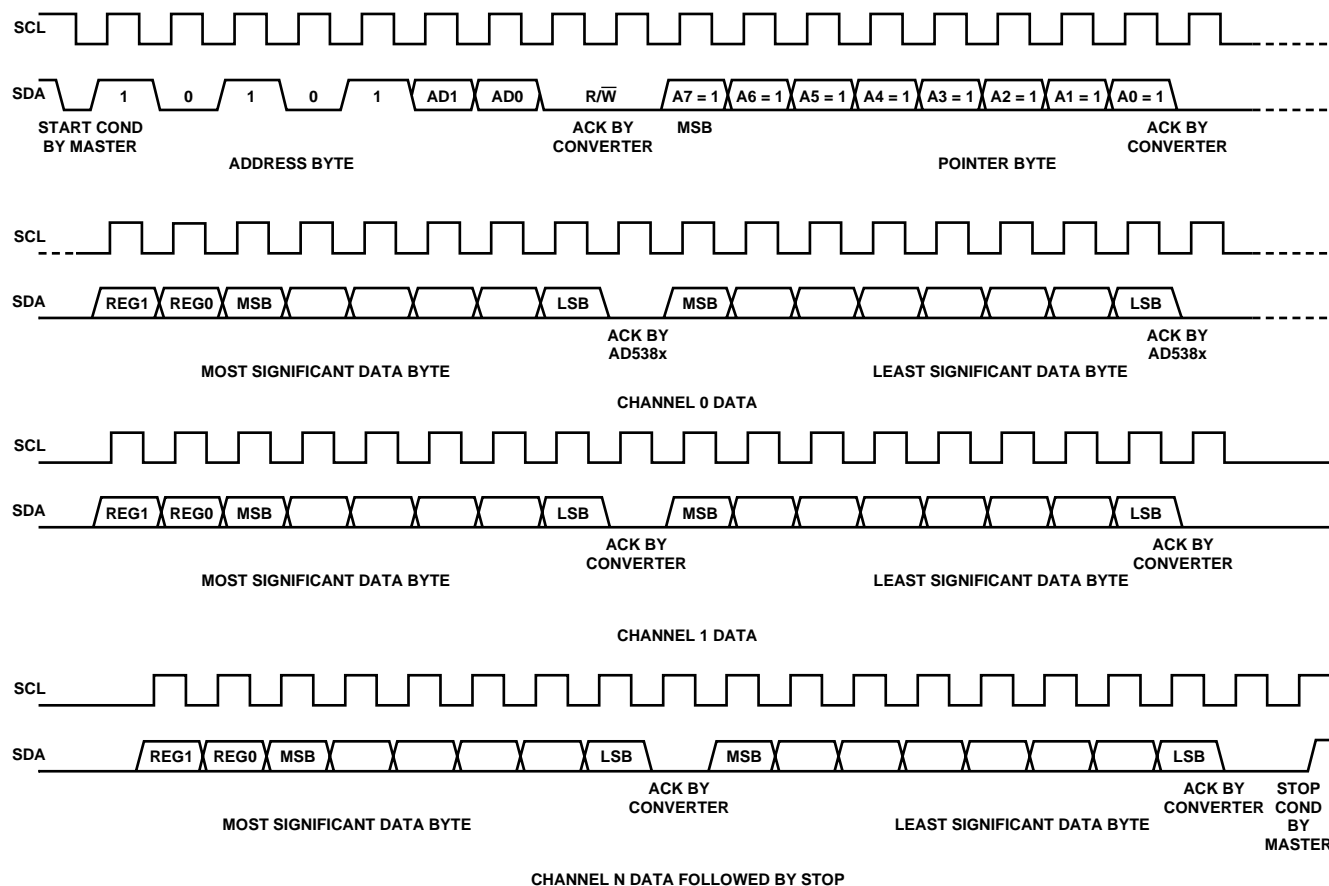


Figure 33. 2-Byte, I²C Write Operation

MICROPROCESSOR INTERFACING

Parallel Interface

The AD5383 can be interfaced to a variety of 16-bit microcontrollers or DSP processors. Figure 35 shows the AD5383 family interfaced to a generic 16-bit microcontroller/DSP processor. The lower address lines from the processor are connected to A0–A4 on the AD5383. The upper address lines are decoded to provide a $\overline{\text{CS}}$, $\overline{\text{LDAC}}$ signal for the AD5383. The fast interface timing of the AD5383 allows direct interface to a wide variety of microcontrollers and DSPs, as shown in Figure 35.

AD5383 to MC68HC11

The serial peripheral interface (SPI) on the MC68HC11 is configured for Master Mode (MSTR = 1), Clock Polarity bit (CPOL) = 0, and the Clock Phase bit (CPHA) = 1. The SPI is configured by writing to the SPI control register (SPCR)—see the 68HC11 User Manual. SCK of the 68HC11 drives the SCLK of the AD5383, the MOSI output drives the serial data line (D_{IN}) of the AD5383, and the MISO input is driven from D_{OUT} . The SYNC signal is derived from a port line (PC7). When data is

being transmitted to the AD5383, the SYNC line is taken low (PC7). Data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle.

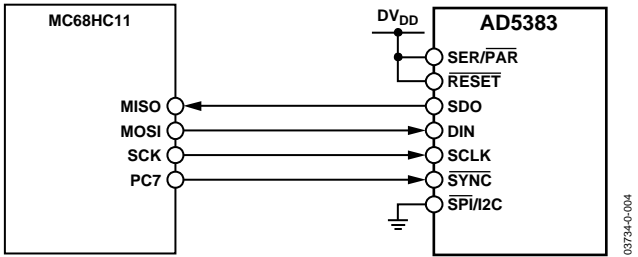
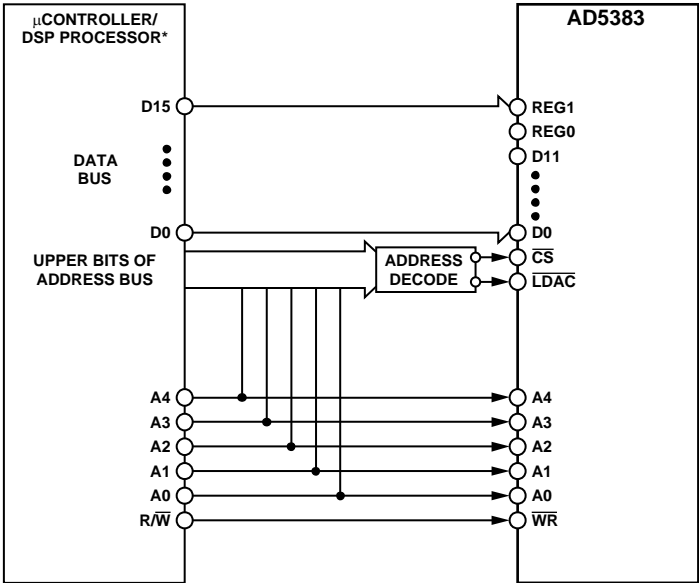


Figure 34. AD5383-to-MC68HC11 Interface



*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 35. AD5383-to-Parallel Interface

AD5383

AD5383 to PIC16C6x/7x

The PIC16C6x/7x synchronous serial port (SSP) is configured as an SPI master with the Clock Polarity bit = 0. This is done by writing to the synchronous serial port control register (SSPCON). See the PIC16/17 Microcontroller User Manual. In this example I/O, port RA1 is being used to pulse SYNC and enable the serial port of the AD5383. This microcontroller transfers only eight bits of data during each serial transfer operation; therefore, three consecutive read/write operations may be needed depending on the mode. Figure 36 shows the connection diagram.

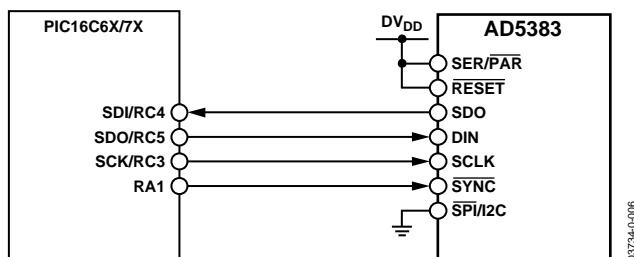


Figure 36. AD5383-to-PIC16C6x/7x Interface

AD5383 to 8051

The AD5383 requires a clock synchronized to the serial data. The 8051 serial interface must therefore be operated in Mode 0. In this mode, serial data enters and exits through RxD, and a shift clock is output on TxD. Figure 37 shows how the 8051 is connected to the AD5383. Because the AD5383 shifts data out on the rising edge of the shift clock and latches data in on the falling edge, the shift clock must be inverted. The AD5383 requires its data to be MSB first. Since the 8051 outputs the LSB first, the transmit routine must take this into account.

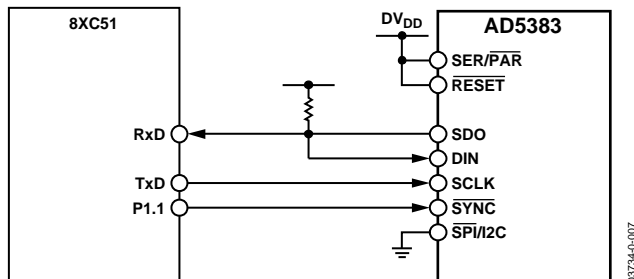


Figure 37. AD5383-to-8051 Interface

AD5383 to ADSP-2101/ADSP-2103

Figure 38 shows a serial interface between the AD5383 and the ADSP-2101/ADSP-2103. The ADSP-2101/ADSP-2103 should be set up to operate in SPORT transmit alternate framing mode. The ADSP-2101/ADSP-2103 SPORT is programmed through the SPORT control register and should be configured as follows: internal clock operation, active low framing, and 16-bit word length. Transmission is initiated by writing a word to the Tx register after the SPORT has been enabled.

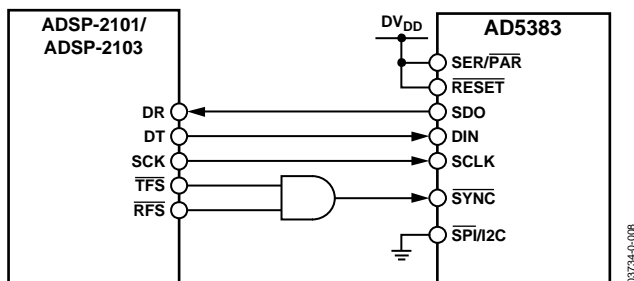


Figure 38. AD5383-to-ADSP-2101/ADSP-2103 Interface

APPLICATION INFORMATION

POWER SUPPLY DECOUPLING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5383 is mounted should be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the AD5383 is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only, a star ground point established as close to the device as possible.

For supplies with multiple pins (AV_{DD} , DV_{DD}), these pins should be tied together. The AD5383 should have ample supply bypassing of 10 μF in parallel with 0.1 μF on each supply, located as close to the package as possible and ideally right up against the device. The 10 μF capacitors are the tantalum bead type. The 0.1 μF capacitor should have low effective series resistance (ESR) and effective series inductance (ESI), like the common ceramic types that provide a low impedance path to ground at high frequencies, to handle transient currents due to internal logic switching.

The power supply lines of the AD5383 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other parts of the board, and should never be run near the reference inputs. A ground line routed between the D_{IN} and SCLK lines will help reduce crosstalk between them (this is not required on a multilayer board because there will be a separate ground plane, but separating the lines will help). It is essential to minimize noise on the V_{IN} and REFIN lines.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A micro-strip technique is by far the best, but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to the ground plane while signal traces are placed on the solder side.

TYPICAL CONFIGURATION CIRCUIT

Figure 39 shows a typical configuration for the AD5383-5 when configured for use with an external reference. In the circuit shown, all AGND, SIGNAL_GND, and DAC_GND pins are tied together to a common AGND. AGND and DGND are connected together at the AD5383 device. On power-up, the AD5383 defaults to external reference operation. All AV_{DD} lines are connected together and driven from the same 5 V source. It is recommended to decouple close to the device with a 0.1 μF ceramic and a 10 μF tantalum capacitor. In this application, the reference for the AD5383-5 is provided externally from either

an ADR421 or ADR431 2.5 V reference. Suitable external references for the AD5383-3 include the ADR280 1.2 V reference. The reference should be decoupled at the REFOUT/REFIN pin of the device with a 0.1 μF capacitor.

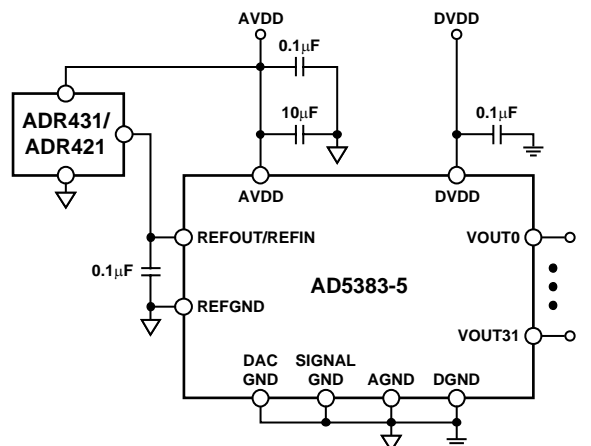


Figure 39. Typical Configuration with External Reference

Figure 40 shows a typical configuration when using the internal reference. On power-up, the AD5383 defaults to an external reference; therefore, the internal reference needs to be configured and turned on via a write to the AD5383 control register. Control Register Bit CR10 allows the user choose the reference value; Bit CR 8 is used to select the internal reference. It is recommended to use the 2.5 V reference when $AV_{DD} = 5\text{ V}$, and the 1.25 V reference when $AV_{DD} = 3\text{ V}$.

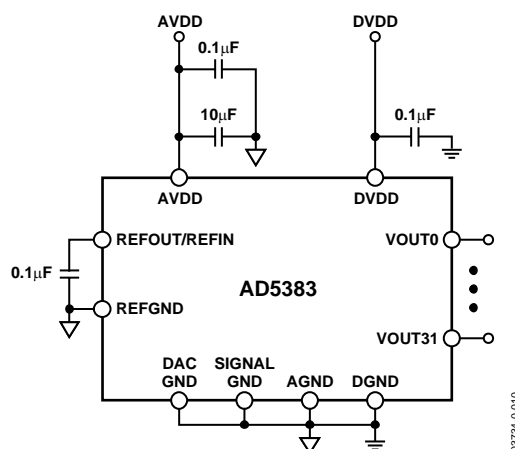


Figure 40. Typical Configuration with Internal Reference

Digital connections have been omitted for clarity. The AD5383 contains an internal power-on reset circuit with a 10 ms brownout time. If the power supply ramp rate exceeds 10 ms, the user should reset the AD5383 as part of the initialization process to ensure the calibration data gets loaded correctly into the device.

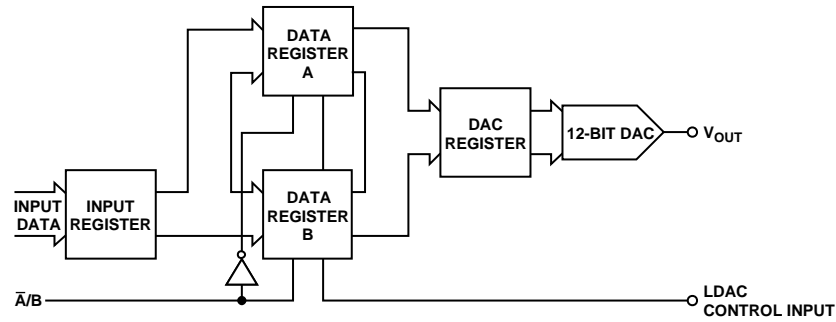


Figure 42. Toggle Mode Function

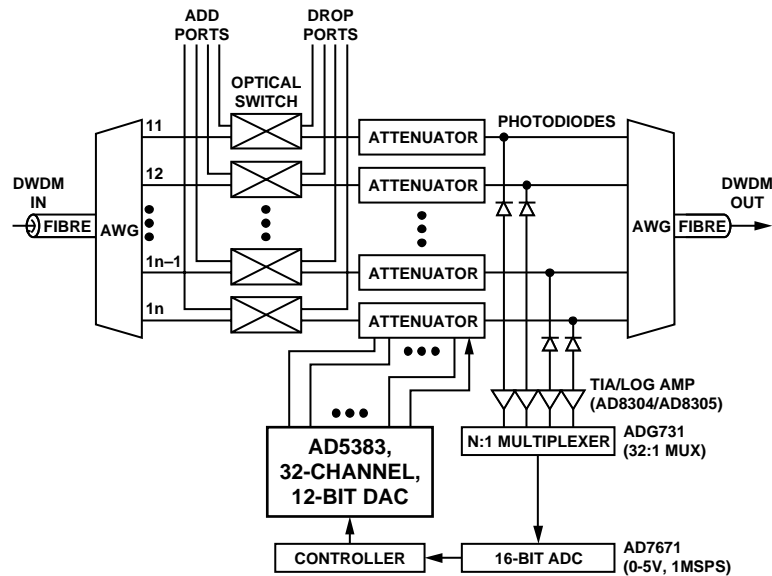


Figure 43. OADM Using the AD5383 as Part of an Optical Attenuator

OPTICAL ATTENUATORS

Based on its high channel count, high resolution, monotonic behavior, and high level of integration, the AD5383 is ideally targeted at optical attenuation applications used in dynamic gain equalizers, variable optical attenuators (VOA), and optical add-drop multiplexers (OADM). In these applications, each wavelength is individually extracted using an arrayed wave

guide; its power is monitored using a photodiode, transimpedance amplifier and ADC in a closed-loop control system. The AD5383 controls the optical attenuator for each wavelength, ensuring that the power is equalized in all wavelengths before being multiplexed onto the fiber. This prevents information loss and saturation from occurring at amplification stages further along the fiber.

UTILIZING THE AD5383 FIFO

The AD5383 FIFO mode optimizes total system update rates in applications where a large number of channels need to be updated. FIFO mode is only available when parallel interface mode is selected. The FIFO_EN pin is used to enable the FIFO. The status of FIFO_EN is sampled during the initialization sequence. Therefore, the FIFO status can only be changed by resetting the device. In a telescope that provides for the cancellation of atmospheric distortion, for example, a large number of channels need to be updated in a short period of time. In such

systems, as many as 320 channels need to be updated within 25 μ s to 30 μ s. Three-hundred-twenty channels require the use of 10 AD5383s. With FIFO mode enabled, the data write cycle time is 40 ns; therefore each group consisting of 32 channels can be fully loaded in 1.28 μ s. In FIFO mode, a complete group of 32 channels updates in 11.5 μ s. The time taken to update all 320 channels is 11.5 μ s + 9 \times 1.28 μ s = 23 μ s. Figure 44 shows the FIFO operation scheme.

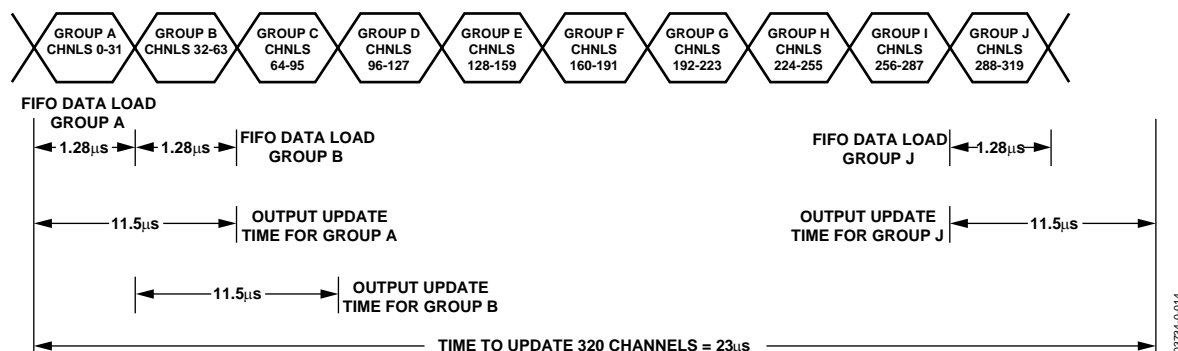


Figure 44. Using FIFO Mode 320 Channels Updated in under 25 μ s

Figure 45. 100-Lead Leaded Quad Flatpack [LQFP]
(ST-100)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Resolution	Temperature Range	AV _{DD} Range	Output Channels	Linearity Error	Package Description	Package Option
AD5383BST-3	12 Bits	−40°C to +85°C	2.7 V to 3.6 V	32	±1 LSB	100-Lead LQFP	ST-100
AD5383BST-3-REEL	12 Bits	−40°C to +85°C	2.7 V to 3.6 V	32	±1 LSB	100-Lead LQFP	ST-100
AD5383BST-5	12 Bits	−40°C to +85°C	4.5 V to 5.5 V	32	±1 LSB	100-Lead LQFP	ST-100
AD5383BST-5-REEL	12 Bits	−40°C to +85°C	4.5 V to 5.5 V	32	±1 LSB	100-Lead LQFP	ST-100
EVAL-AD5383EB						Evaluation Kit	

AD5383

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AD5383

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