ANALOG DEVICES

Precision Sample-and-Hold with 16-Channel Multiplexer

AD362

FEATURES

- 16 Single-Ended or 8 Differential Channels with Switchable Mode Control
- True 12-Bit Precision: Nonlinearity ≤±0.005%
- High Speed: 10μs Acquisition Time to 0.01%
- Complete and Calibrated: No Additional Parts Required
- Small, Reliable: 32 Pin Hermetic Metal DIP
- Versatile: Simple Interface to Popular Analog to Digital Converters
- High Differential Input Impedance ($10^{10}\Omega$) and Common Mode Rejection (80dB)
- Fully Protected Multiplexer Inputs

PRODUCT DESCRIPTION

The AD362 is a complete, precision 16-channel data acquisition system analog input section in hybrid integrated circuit form. Large-scale linear integrated circuitry, thick- and thin-film technology and active laser trimming gives the AD362 extensive applications versatility along with full 12-bit accuracy.

The AD362 contains two 9-channel multiplexers, a differential amplifier, a sample-and-hold with high-speed output amplifier, a channel address latch and control logic. The multiplexers may be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A unique feature of the AD362 is an internal user-controllable analog switch that connects the multiplexers in either a single-ended or differential mode. This allows a single device to perform in either mode without hard-wire programming and permits a mixture of single-ended and differential sources to be interfaced by dynamically switching the input mode control.

The sample-and-hold mode control is designed to connect directly to the "Status" output of an analog to digital converter so that a convert command to the ADC will automatically put the sample-and-hold into the "Hold" mode. A precision hold capacitor is included with each AD362. The AD362 output amplifier is capable of driving the unbuffered analog input of most high-speed, 12-bit successive-approximation ADCs. Interface is thereby reduced to two simple connections with no additional components required.

When used with a 12-bit, 25-microsecond ADC such as the AD572, AD574 or AD ADC80, system throughput rate is as high as 30kHz at full rated accuracy. The AD362KD is specified for operation over a 0 to +70°C temperature range while the AD362SD operates to specification from −55°C to +125°C. Processing to MIL-STD-883, Class B is available for the AD362SD. Both grades are packaged in a hermetic, electrostatically shielded 32 pin metal dual-in-line package.

PRODUCT HIGHLIGHTS

1. The AD362, when used with a precision analog to digital converter, forms a complete, accurate, high-speed data acquisition system.
2. The 16-input channels may be configured in single-ended, differential or a mixture of both modes. Mode switching is provided by a user-controllable internal analog switch.
3. Multiplexers, differential amplifier, sample-and-hold and high-speed output buffer provide complete analog interfacing capabilities.
4. Internal channel address latches are provided to facilitate interfacing the AD362 to data, address or control buses.
5. All grades of the AD362 are hermetically sealed in rugged metal DIP packages.
6. A precision hold capacitor is provided with each AD362.
7. The AD362SD is specified over the entire military temperature range, −55°C to +125°C. Processing to MIL-STD-883, Class B is available.

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SPECIFICATIONS (typical @ +25°C, ±15V and +5V with 2000pF hold capacitor as provided unless otherwise noted)

MODEL	AD362KD	AD362SD/AD362SD-883B[1]
ANALOG INPUTS		
Number of Inputs	16 Single-Ended or 8 Differential (Electronically Selectable)	*
Input Voltage Range, Linear		
T_{min} to T_{max}	±10V min	*
Input (Bias) Current, Per Channel	±50nA max	*
Input Impedance		
On Channel	$10^{10}\Omega$, 100pF	*
Off Channel	$10^{10}\Omega$, 10pF	*
Input Fault Current (Power Off or On)	20mA, max, Internally Limited	*
Common Mode Rejection		
Differential Mode	70dB min (80dB typ) @ 1kHz, 20V p-p	*
Mux Crosstalk (Interchannel, Any Off Channel to Any On Channel)	-80dB max (-90dB typ) @ 1kHz, 20V p-p	*
Offset, Channel to Channel	±2.5mV max	*
ACCURACY		
Gain Error, T_{min} to T_{max}	±0.02% FSR, max	*
Offset Error, T_{min} to T_{max}	±4mV	*
Linearity Error	±0.005% max	*
T_{min} to T_{max}	±0.01% max	*
Noise Error	1mV p-p, 0.1 to 1MHz, max	*
T_{min} to T_{max}	2mV p-p, 0.1 to 1MHz, max	*
TEMPERATURE COEFFICIENTS		
Gain, T_{min} to T_{max}	±4ppm/°C max	±2ppm/°C max
Offset, ±10V Range, T_{min} to T_{max}	±2ppm/°C max	±1.5ppm/°C max
SAMPLE AND HOLD DYNAMICS		
Aperture Delay	100ns max (50ns typ)	*
Aperture Uncertainty	500ps max (100ps typ)	*
Acquisition Time, for 20V Step to ±0.01% of Final Value	18μs max (10μs typ)	*
Feedthrough	-70dB max (-80dB typ) @ 1kHz	*
Droop Rate	2mV/ms max (1mV/ms typ)	*
DIGITAL INPUT SIGNALS[2]		
Input Channel Select (Pins 28-31)	4-Bit Binary, Channel Address	*
	1LS TTL Load	*
Channel Select Latch (Pin 32)	"1": Latch Transparent	*
	"0": Latched	*
	8LS TTL Loads	*
Single Ended/Differential Mode Select (Pin 1)	"0": Single-Ended Mode	*
	"1": Differential Mode	*
	3TTL Loads	*
Sample and Hold Command (Pin 13)	"0": Sample Mode	*
	"1": Hold Mode	*
	1TTL Load	*
POWER REQUIREMENTS		
Supply Voltages/Currents	+15V, ±5% @ 30mA max	*
	-15V, ±5% @ 30mA max	*
	+5V, ±5% @ 40mA max	*
Total Power Dissipation	1.1 Watts max	*
TEMPERATURE RANGE		
Specification	0 to +70°C	-55°C to +125°C
Storage	-55°C to +85°C[3]	-55°C to +150°C

NOTES:
[1] The AD362 is available fully processed and screened to the requirements of MIL-STD-883, Class B. A complete list of tests is given on page 3. When ordering, specify "AD362SD/883B".
[2] One TTL Load is defined as $I_{IL} = -1.6mA$ max @ $V_{IL} = 0.4V$, $I_{IH} = 40\mu A$ max @ $V_{IH} = 2.4V$.
One LS TTL Load is defined as $I_{IL} = -0.36mA$ max @ $V_{IL} = 0.4V$, $I_{IH} = 20\mu A$ max @ $V_{IH} = 2.7V$.
[3] AD362KD External Hold Capacitor is limited to +85°C; AD362 device itself may be stored at up to +150°C.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (ALL MODELS)

+V, Digital Supply	+5.5V
+V, Analog Supply	+16V
−V, Analog Supply	−16V
V_{IN}, Signal	±V, Analog Supply
V_{IN}, Digital	0 to +V, Digital Supply
A_{GND} to D_{GND}	±1V

PROCESSING FOR HIGH RELIABILITY

STANDARD PROCESSING

As part of the standard manufacturing procedure, all models of the AD362 receive the following processing:

PROCESS	CONDITIONS
1) 100% pre-cap Visual Inspection	Inhouse Criteria
2) Stabilization Bake	24 hours @ +150°C
3) Seal Test, Gross Leak	Method 1014 Test Condition C
4) Operating Burn-In	24 hours @ +125°C

PROCESSING TO MIL-STD-883

All models of AD362 ordered to the requirements of MIL-STD-883. Method 5008 are identified with a /883B suffix and receive the following processing:

PROCESS	CONDITIONS
1) 100% pre-cap Visual Inspection	2017.1
2) Stabilization Bake	1008, 24 hours @ +150°C
3) Temperature Cycle	1010, Test Condition C, 10 cycles, −65°C to +150°C
4) Constant Acceleration	2001, Y1 Plane, 1000G
5) Visual Inspection	Visable Damage
6) Operating Burn-In	1015, Test Condition B 160 hours @ +125°C
7) Seal Test: Fine Leak	1014, Test Condition A, 5 x 10^{-7} std cc/sec
Gross Leak	1014, Condition C
8) Final Electrical Test	Per Data Sheet
9) External Visual Inspection	2009

AD362 PIN FUNCTION DESCRIPTION

Pin Number	Function
1	Single-End/Differential Mode Select "0": Single-Ended Mode "1": Differential Mode
2	Digital Ground
3	Positive Digital Power Supply, +5V
4	"High" Analog Input, Channel 7
5	"High" Analog Input, Channel 6
6	"High" Analog Input, Channel 5
7	"High" Analog Input, Channel 4
8	"High" Analog Input, Channel 3
9	"High" Analog Input, Channel 2
10	"High" Analog Input, Channel 1
11	"High" Analog Input, Channel 0
12	Hold Capacitor (Provided)
13	Sample-Hold Command "0": Sample Mode "1": Hold Mode Normally Connected to ADC Status
14	Offset Adjust (See Figure 5)
15	Offset Adjust (See Figure 5)
16	Analog Output Normally Connected to ADC "Analog In"
17	Analog Ground
18	"High" ("Low") Analog Input, Channel 15 (7)
19	"High" ("Low") Analog Input, Channel 14 (6)
20	Negative Analog Power Supply, −15V
21	Positive Analog Power Supply, +15V
22	"High" ("Low") Analog Input, Channel 13 (5)
23	"High" ("Low") Analog Input, Channel 12 (4)
24	"High" ("Low") Analog Input, Channel 11 (3)
25	"High" ("Low") Analog Input, Channel 10 (2)
26	"High" ("Low") Analog Input, Channel 9 (1)
27	"High" ("Low") Analog Input, Channel 8 (0)
28	Input Channel Select, Address Bit AE
29	Input Channel Select, Address Bit A0
30	Input Channel Select, Address Bit A1
31	Input Channel Select, Address Bit A2
32	Input Channel Select Latch "0": Latched "1": Latch Transparent

AD362 ORDERING GUIDE

Model	Specification Temp Range	Max Gain TC	Prices (1−24)	(25−99)	(100+)
AD362KD	0 to +70°C	±4ppm/°C	$160.00	$139.50	$119.50
AD362SD	−55°C to +125°C	±2ppm/°C	$295.00	$270.00	$230.00
AD362SD/883B	−55°C to +125°C	±2ppm/°C	$365.00	$330.00	$280.00

NOTE: D Suffix = Dual-In-Line package designator.

AD362 DESIGN

The AD362 consists of two 8-channel multiplexers, a differential amplifier, a sample-and-hold with high-speed output buffer, channel address latches and control logic as shown in Figure 1. The multiplexers can be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A unique feature of the AD362 is an internal analog switch controlled by a digital input that performs switching between single-ended and differential modes. This feature allows a single AD362 to perform in either mode without external hard-wire interconnections. Of more significance is the ability to serve a mixture of both single-ended and differential sources with a single AD362 by dynamically switching the input mode control.

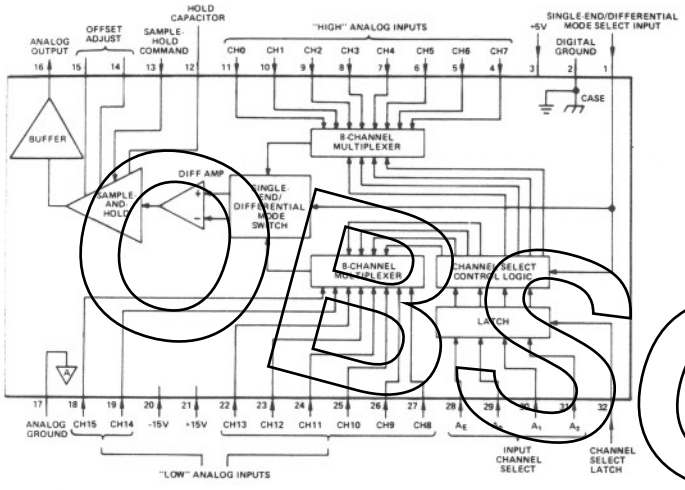


Figure 1. AD362 Analog Input Section Functional Block Diagram and Pinout

Multiplexer channel address inputs are interfaced through a level-triggered ("transparent") input register. With a Logic "1" at the Channel Select Latch input, the address signals feed through the register to directly select the appropriate input channel. This address information can be held in the register by placing a Logic "0" on the Channel Select Latch input. Internal logic monitors the status of the Single-Ended/Differential Mode input and addresses the multiplexers accordingly.

A differential amplifier buffers the multiplexer outputs while providing high input impedance in both differential and single-ended modes. Amplifier gain and common mode rejection are actively laser-trimmed.

The sample-and-hold is a high speed monolithic device that can also function as a gated operational amplifier. Its uncommitted differential inputs allow it to serve a second role as the output subtractor in the differential amplifier. This eliminates one amplifier and decreases drift, settling time and power consumption. A Logic "1" on the Sample-and-Hold Command input will cause the sample-and-hold to "freeze" the analog signal while the ADC performs the conversion. Normally the Sample-and-Hold Command is connected to the ADC Status output which is at Logic "1" during conversion and Logic "0" between conversions. For slowly-changing inputs, throughput speed may be increased by grounding the Sample-and-Hold Command input instead of connecting it to the ADC status.

A Polystyrene hold capacitor is provided with each commercial temperature range device (AD362KD) while a Teflon capacitor is provided with units intended for operation at temperatures up to 125°C (AD362SD). Use of an external capacitor allows the user to make his own speed/accuracy tradeoff; a smaller capacitor will allow faster sample-and-hold response but will decrease accuracy while a larger capacitor will increase accuracy at slower conversion rates.

The output buffer is a high speed amplifier whose output impedance remains low and constant at high frequencies. Therefore, the AD362 may drive a fast, unbuffered, precision ADC without loss of accuracy.

The AD362 is constructed on a substrate that includes thick-film resistors for non-critical applications such as input protection and biasing. A separately-mounted laser-trimmed thin-film resistor network is used to establish accurate gain and high common-mode rejection. The metal package affords electromagnetic and electrostatic shielding and is hermetically welded at low temperatures. Welding eliminates the possibility of contamination from solder particles or flux while low temperature sealing maintains the accuracy of the laser-trimmed thin-film resistors.

THEORY OF OPERATION

Concept

The AD362 is intended to be used in conjunction with a high-speed precision analog-to-digital converter to form a complete data acquisition system (DAS) in microcircuit form. Figure 2 shows a general AD362-with-ADC DAS application.

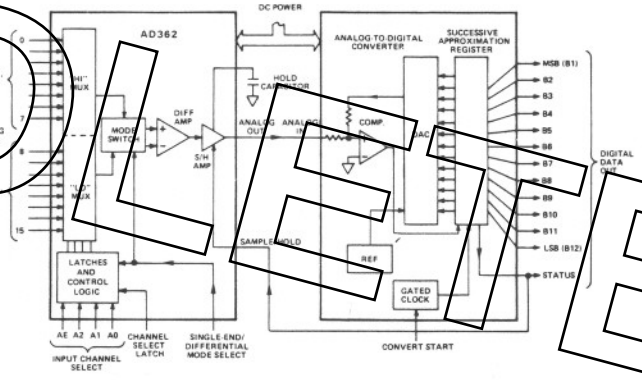


Figure 2. AD362 with ADC as a Complete Data Acquisition System

By dividing the data acquisition task into two sections, several important advantages are realized. Performance of each design is optimized for its specific function. Production yields are increased thus decreasing costs. Furthermore, the standard configuration packages plug into standard sockets and are easier to handle than larger packages with higher pin counts.

System Timing

Figure 3 is a timing diagram for the AD362 connected as shown in Figure 2 and operating at maximum conversion rate. The ADC is assumed to be a conventional 12 bit type such as the AD572 or AD ADC80.

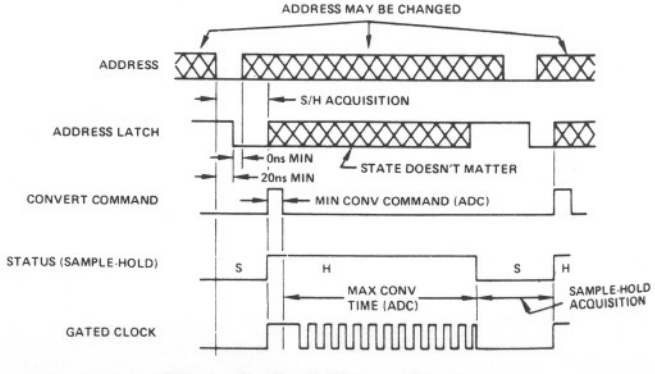


Figure 3. DAS Timing Diagram

The normal sequence of events is as follows:

1. The appropriate Channel Select Address is latched into the address register. Time is allowed for the multiplexers to settle.
2. A Convert Start command is issued to the ADC which, in response, indicates that it is "busy" by placing a Logic "1" on its Status line.
3. The ADC Status controls the sample-and-hold. When the ADC is "busy", the sample-and-hold is in the Hold mode.
4. The ADC goes into its conversion routine. Since the sample-and-hold is holding the proper analog value, the address may be updated during conversion. Thus multiplexer settling time can coincide with conversion and need not affect throughput rate.
5. The ADC indicates completion of its conversion by returning Status to Logic "0". The sample-and-hold returns to the Sample mode.
6. If the input signal has changed full-scale (different channels may have widely-varying data) the sample-and-hold will typically require 10 microseconds to "acquire" the next input to sufficient accuracy for 12-bit conversion.

After allowing a suitable interval for the sample-and-hold to stabilize at its new value, another Convert Start command may be issued to the ADC.

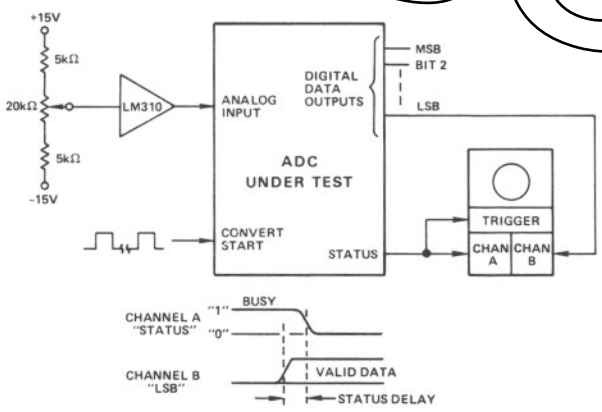


Figure 4. ADC Status Valid Test

NOTE:

Valid Output Data

Not all ADCs have all data bits available when Status indicates that the conversion is complete. Successive approximation ADCs based on the 2502/3/4 type of register must have a Status delay built in or the final data bit will lag Status by approximately 50ns. This will result in two problems:

1. The sample-and-hold will return to Sample, disturbing the analog input to the ADC as it is attempting to convert the least significant bit. This may result in an error.
2. If the falling edge of Status is being used to load the data into a register, the least significant bit will not be valid when loaded.

An external 100ns delay or use of an ADC with a valid Status output is necessary to prevent this problem. The applications shown in this data sheet ensure that all data bits will be valid.

The following test may be made to determine if the ADC Status timing is correct:

1. Connect the ADC under test as shown in Figure 4.
2. Trigger the oscilloscope on Status. Delay the display such that Status is mid-screen.
3. Observe the LSB data output of the ADC.
4. Vary the analog input control to confirm that the LSB transition precedes the Status transition.

Single-Ended/Differential Mode Control

The AD362 features an internal analog switch that configures the Analog Input Section in either a 16-channel single-ended or 8-channel differential mode. This switch is controlled by a TTL logic input applied to pin 1 of the Analog Input Section:

"0": Single-Ended (16 channels)
"1": Differential (8 channels)

When in the differential mode, a differential source may be applied between corresponding "High" and "Low" analog input channels.

It is possible to mix SE and DIFF inputs by using the mode control to command the appropriate mode. In this case, four microseconds must be allowed for the output of the Analog Input Section to settle to within ±0.01% of its final value, but if the mode is switched concurrent with changing the channel address, no significant additional delay is introduced. The effect of this delay may be eliminated by changing modes while a conversion is in progress (with the sample-and-hold in the "Hold" mode). When SE and DIFF signals are being processed concurrently, the DIFF signals must be applied between corresponding "High" and "Low" analog input channels. Another application of this feature is the capability of measuring 16 sources individually and/or measuring differences between pairs of those sources.

Input Channel Addressing

Table 1 is the truth table for input channel addressing in both the single-ended and differential modes. The 16 single-ended channels may be addressed by applying the corresponding digital number to the four Input Channel Select address bits, AE, A0, A1, A2 (pins 28–31). In the differential mode, the eight channels are addressed by applying the appropriate digital code to A0, A1 and A2; AE must be enabled with a Logic "1". Internal logic monitors the status of the SE/DIFF Mode input and addresses the multiplexers singularly or in pairs as required.

ADDRESS				ON CHANNEL (Pin Number)		
					Differential	
AE	A2	A1	A0	Single Ended	"Hi"	"Lo"
0	0	0	0	0 (11)	None	
0	0	0	1	1 (10)	None	
0	0	1	0	2 (9)	None	
0	0	1	1	3 (8)	None	
0	1	0	0	4 (7)	None	
0	1	0	1	5 (6)	None	
0	1	1	0	6 (5)	None	
0	1	1	1	7 (4)	None	
1	0	0	0	8 (27)	0 (11)	0 (27)
1	0	0	1	9 (26)	1 (10)	1 (26)
1	0	1	0	10 (25)	2 (9)	2 (25)
1	0	1	1	11 (24)	3 (8)	3 (24)
1	1	0	0	12 (23)	4 (7)	5 (23)
1	1	0	1	13 (22)	5 (6)	5 (22)
1	1	1	0	14 (19)	6 (5)	6 (19)
1	1	1	1	15 (18)	7 (4)	7 (18)

Table 1. Input Channel Addressing Truth Table

When the channel address is changed, six microseconds must be allowed for the Analog Input Section to settle to within ±0.01% of its final output (including settling times of all elements in the signal path). The effect of this delay may be eliminated by performing the address change while a conversion is in progress (with the sample-and-hold in the "Hold" mode).

Input Channel Address Latch

The AD362 is equipped with a latch for the Input Channel Select address bits. If the Latch Control pin (pin 32) is at Logic "1", input channel select address information is passed through to the multiplexers. A Logic "0" "freezes" the input channel address present at the inputs at the "1"-to-"0" transition (level-triggered).

This feature is useful when input channel address information is provided from an address, data or control bus that may be required to service many devices. The ability to latch an address is helpful whenever the user has no control of when address information may change.

Sample-and-Hold Mode Control

The Sample-and-Hold Mode Control input (pin 13) is normally connected to the Status output (pin 20) from an analog to digital converter. When a conversion is initiated by applying a Convert Start command to the ADC, Status goes to Logic "1", putting the sample-and-hold into the "Hold" mode. This "freezes" the information to be digitized for the period of conversion. When the conversion is complete, Status returns to Logic "0" and the sample-and-hold returns to the "Sample" mode. Eighteen microseconds must be allowed for the sample-and-hold to acquire ("catch up" to) the analog input to within ±0.01% of the final value before a new Convert Start command is issued.

The purpose of a sample-and-hold is to "stop" fast changing input signals long enough to be converted. In this application, it also allows the user to change channels and/or SE/ DIFF mode while a conversion is in progress thus eliminating the effects of multiplexer, analog switch and differential amplifier settling times. If maximum throughput rate is required for slowly changing signals, the Sample-and-Hold Mode Control may be wired to ground (Logic "0") rather than to ADC Status thus leaving the sample-and-hold in a continuous Sample mode.

Hold Capacitor

A 2000pF capacitor is provided with each AD362. One side of this capacitor is wired to pin 12, the other to analog ground as close to pin 17 as possible. The capacitor provided with the AD362KD is Polystyrene while the wider operating temperature range of the AD362SD requires a Teflon capacitor (supplied).

Smaller capacitors will allow slightly faster operation, but only with increased noise and decreased precision. 1000pF will typically allow acquisition to 0.1% in four microseconds.

Larger capacitors may be substituted to reduce noise, and sample-to-hold offset, but acquisition time of the sample-and-hold will be extended. If less than 12 bits of accuracy is required, a smaller capacitor may be used. This will shorten the S/H acquisition time. In all cases, the proper capacitor dielectric must be used; i.e., Polystyrene (AD326KD only) or Teflon (AD362KD or SD). Other types of capacitors may have higher dielectric absorption (memory) and will cause errors. CAUTION: Polystyrene capacitors will be destroyed if subjected to temperatures above +85°C. No capacitor is required if the sample-and-hold is not used.

Analog Input Section Offset Adjust Circuit

Although the offset voltage of the AD362 may be adjusted, that adjustment is normally performed at the ADC. In some special applications, however, it may be helpful to adjust the offset of the Analog Input Section. An example of such a case would be if the input signals were small (<10mV) relative to AD362 voltage offset and gain was to be inserted between the AD362 and the ADC. To adjust the offset of the AD362, the circuit shown in Figure 5 is recommended.

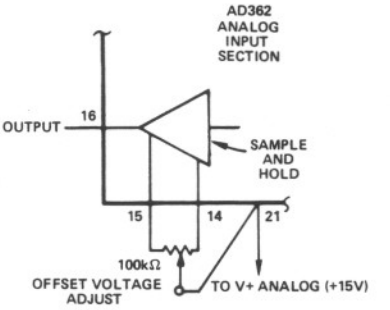


Figure 5. AD362 Offset Voltage Adjustment

Under normal conditions, all calibration is performed at the ADC Section.

Other Considerations

Grounding: Analog and digital signal grounds should be kept separate where possible to prevent digital signals from flowing in the analog ground circuit and inducing spurious analog signal noise. Analog Ground (pin 17) and Digital Ground (pin 2) are not connected internally; these pins must be connected externally for the system to operate properly. Preferably, this connection is made at only one point, as close to the AD362 as possible. The case is connected internally to Digital Ground to provide good electrostatic shielding. If the grounds are not tied common on the same card with the AD362, the digital and analog grounds should be connected locally with back-to-back general-purpose diodes as shown in Figure 6. This will protect the AD362 from possible damage caused by voltages in excess of ±1 volt between the ground systems which could occur if the key grounding card should be removed from the overall system. The device will operate properly with as much as ±200mV between grounds, however this difference will be reflected directly as an input offset voltage.

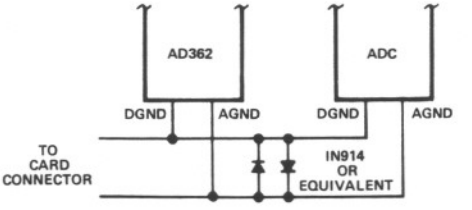


Figure 6. Ground-Fault Protection Diodes

Power Supply Bypassing: The ±15V and +5V power leads should be capacitively bypassed to Analog Ground and Digital Ground respectively for optimum device performance. 1μF tantalum types are recommended; these capacitors should be located close to the system. It is not necessary to shunt these capacitors with disc capacitors to provide additional high frequency power supply decoupling since each power lead is bypassed internally with a 0.039μF ceramic capacitor.

Interfacing to Popular Analog to Digital Converters

The AD362 has been designed to interface directly to most analog to digital converters; often no additional components are required and only two interconnections must be made. The direct interface requirements for the ADC are as follows:

1. The ADC Status output must be positive-true Logic ("1" during conversion).
2. Transition from "0" to "1" must occur at least 200ns before the most significant bit decision is made (successive approximation ADC) or before input integration starts (integrating type ADC).
3. Status must not return to "0" before the LSB decision is made (see page 5).
4. If Status is being used to latch output data, it must not return to Logic "0" until all output data bits are valid and available.

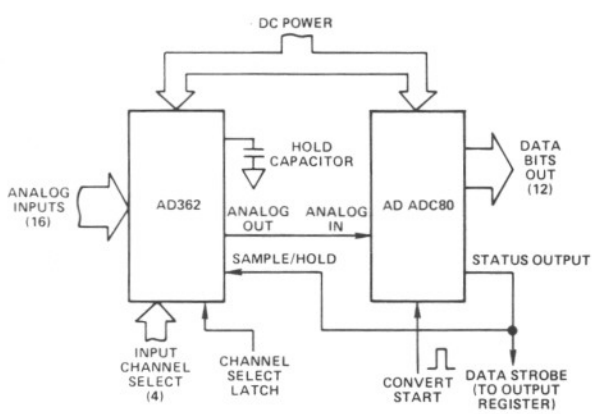
Complete system throughput performance is determined by combining the worst-case specifications of the AD362 and the ADC. If guaranteed system performance is required, the AD363 and AD364 are recommended. The AD363 includes an AD362 and an AD572 12-bit, 25-microsecond precision ADC. The AD364 consists of an AD362 and an AD574 12-bit, microprocessor-compatible, low cost ADC. Each is specified as a complete, two-package system; data sheets are available upon request.

Figure 7a shows the AD362 driving an AD ADC80. The AD ADC80 is a 12-bit, 25-microsecond, low-cost ADC that meets all of the requirements listed above. Throughput rate is typically 30kHz with no missing codes over the operating temperature range.

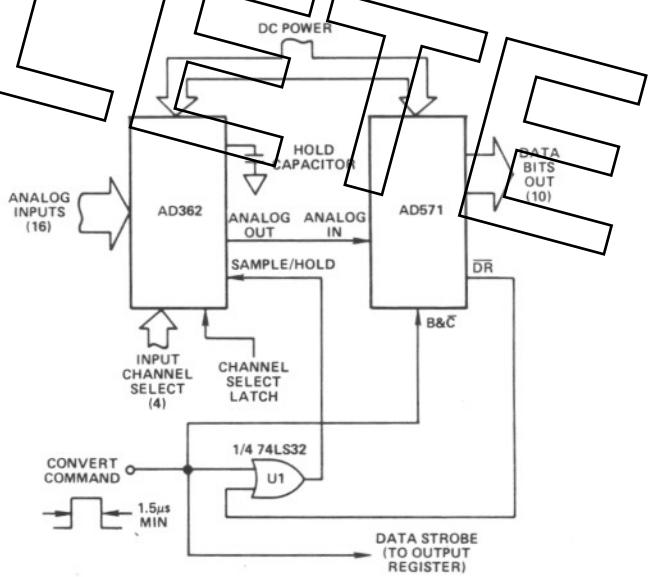
Figure 7b shows a 10-bit application based on the AD362 and the AD571, a complete low cost 10-bit, 25-microsecond ADC. In this case, two of the above requirements are not met:

1. $\overline{DR}$ ($\overline{DATA\ READY}$), as Status, is positive-true but. . .
2. $\overline{DR}$ does not indicate that a conversion is in progress until 1.5μs after conversion starts.
3. $\overline{DR}$ does indicate conversion complete after the LSB decision is made, but. . .
4. $\overline{DR}$ precedes the enabling of the AD571 output 3-state gates by 500ns.

The gating provided by U1 allows the applied convert command (CC) to initiate input hold at the AD362. CC must last for more than 1.5μs so that $\overline{DR}$ may then assume control of Hold. If conversion is continuous (consistent with multichannel operation), the next convert command can be used to load the previously-converted data into an output register. For single conversion operation, a 1μs delay of the falling edge of $\overline{DR}$ may be used to signify valid data.



a. 12-Bit DAS Using AD362 and AD ADC80



b. 10-Bit DAS Using AD362 and AD571

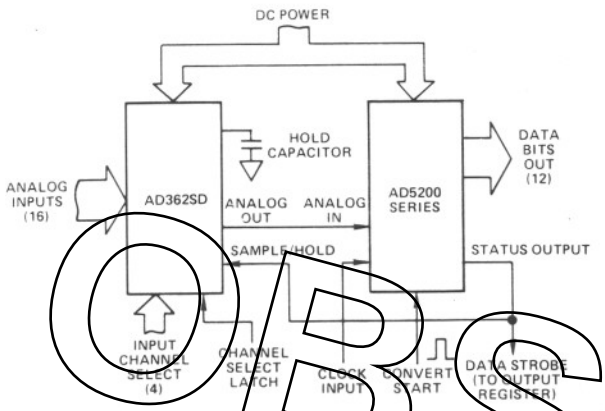
Figure 7. Data Acquisition Systems Based on the AD362 and Popular ADC's

Interfacing to Special Purpose ADCs

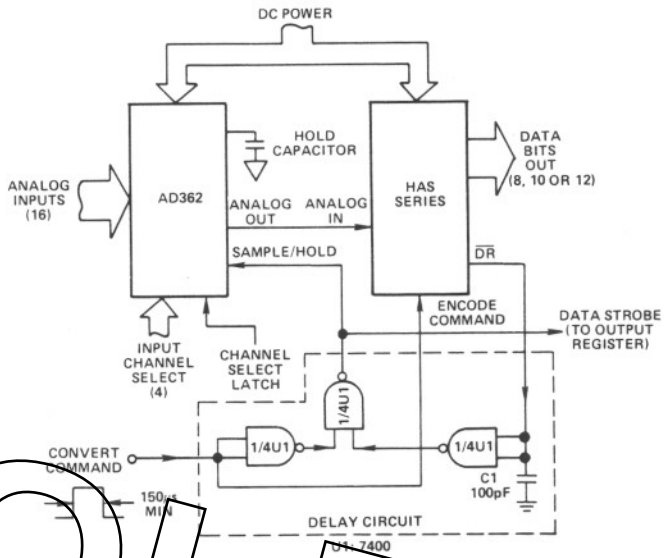
The AD5200 series of ADCs perform a 12-bit conversion in 50 microseconds and feature totally adjustment-free operation, high accuracy, and a small hermetically-sealed 24-pin package.

These ADCs are often used in high-reliability applications and, like the AD362SD (which operates over the -55°C to +125°C temperature range) are available processed to MIL-STD-883, Class B. The AD5200 series meets all of the interfacing requirements for direct connection to the AD362 as shown in Figure 8a. System throughput rate is typically 16kHz.

The HAS series of ultra-fast ADCs are 8-bit (HAS0801), 10-bit (HAS1001) and 12-bit (HAS1202) devices that convert in 1.5, 1.7, and 2.8 microseconds (maximum) respectively. These devices are hybrid IC's, packaged in 32-pin DIPs. Since the Data Ready signal from the HAS precedes the LSB decision, $\overline{DR}$ must be delayed. Figure 8b shows the appropriate circuitry to provide that delay. Throughput rate for the 12-bit system is typically 80kHz.



a. 12-Bit High Accuracy and Reliability DAS Using AD362 and AD5200



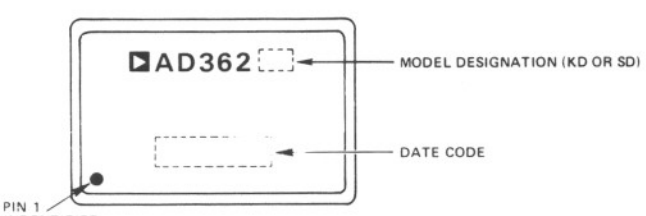
b. High-Speed DAS Using AD362 and HAS

Figure 8. Data Acquisition Systems Based on the AD362 and Purpose ADCs

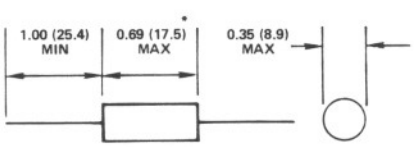
OUTLINE DIMENSIONS
PACKAGE SPECIFICATIONS

Dimensions shown in inches and (mm).

"D" PACKAGE

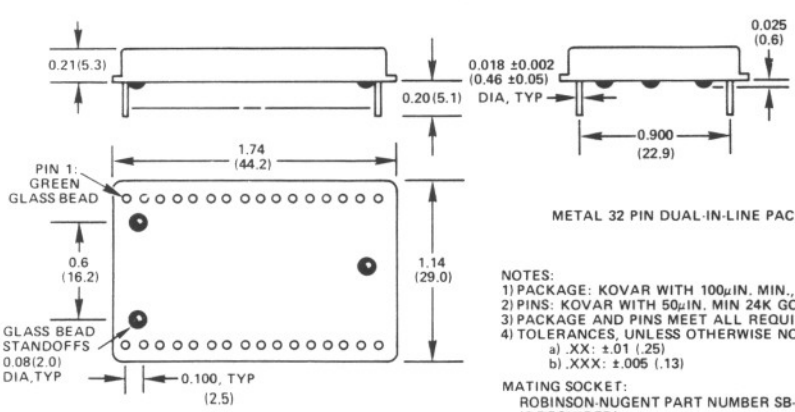


HOLD CAPACITOR



*THIS DIMENSION IS FOR POLYSTYRENE CAPACITOR SUPPLIED WITH AD362KD

MAX BODY LENGTH OF TEFLON CAPACITOR SUPPLIED WITH AD362SD IS 1.00".



METAL 32 PIN DUAL-IN-LINE PACKAGE

NOTES:
1) PACKAGE: KOVAR WITH 100μIN. MIN., NICKEL PLATE
2) PINS: KOVAR WITH 50μIN. MIN 24K GOLD PLATE
3) PACKAGE AND PINS MEET ALL REQUIREMENTS OF MIL-STD-883
4) TOLERANCES, UNLESS OTHERWISE NOTED:
   a) .XX: ±.01 (.25)
   b) .XXX: ±.005 (.13)

MATING SOCKET:
ROBINSON-NUGENT PART NUMBER SB-16-G
(2 REQUIRED)

ROBINSON-NUGENT, INC.
800 EAST EIGHTH STREET
NEW ALBANY, IN 47150
(812) 945-0211

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