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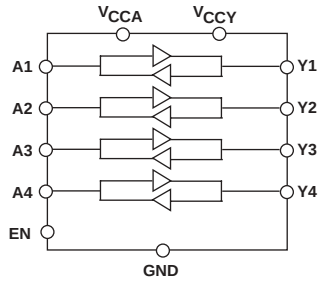
Low Voltage 1.2 V to 5.5 V, Bidirectional, Logic Level Translators

Preliminary Technical Data — ADG3304

FEATURES
Bidirectional Level Translation
Operates from 1.2 V to 5.5 V
12 Bump WLCSP package and 14-lead TSSOP
Low Quiescent Current <5μA

APPLICATIONS
SPI™, Microwire™ and I²C™ Translation
Low Voltage ASIC level Translation
Smart Card Readers
Cell Phones & Cell-Phone Cradles
Portable Communication Devices
Telecommunicatons Equipment
Network Switches and Routers
Storage Systems (SAN/NAS)
Computing/Server Applications
GPS
Portable POS Systems
Low Cost Serial Interfaces

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADG3304 is a 4-Channel bidirectional level translator. Its function is to provide level shifting in a multi-voltage system. The voltage applied to V_{CCA} sets up the logic levels on the A side of the device, while V_{CCY} sets the levels on the Y side. In this way, signals applied to the V_{CCA} side of the device appear as V_{CCY} compatible logic on the other side of the device and vice versa as the device is designed to handle bidirectional signals. The device is guaranteed for operation over the supply range 1.2 V to 5.5 V.

These devices are suited to applications like data transfer between a low voltage DSP/Controller and a higher voltage device. Other applications include high end consumer products where constant changes to the chipset desgins result in multiple supply levels in the application.

V_{CCY} operates from +1.65 to 5.5 V while V_{CCA} from +1.2 to V_{CCY}. V_{CCA} must always operate from a supply that is lower than V_{CCY}. When the device Enable pin (EN) is pulled low, the Ax and Yx inputs/outputs are tri-stated. The EN pin is driven high for normal operation. EN pin is referred to V_{CCA} voltage.

PRODUCT HIGHLIGHTS

1. Bidirectional Level Translation.
2. The ADG3304 is fully guaranteed from 1.2 V to 5.5 V supply range.
3. 14 lead TSSOP and 12 lead WLCSP package.

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ADG3304–SPECIFICATIONS[1]

(V_{CCY} = +1.65 to 5.5 V, V_{CCA} = +1.1 to V_{CCY}, GND = 0 V, All specifications T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ[2]	Max	Units
LOGIC INPUTS/OUTPUTS						
Input High Voltage	V_{IH}		V_{CCY} -0.4			V
			V_{CCA} -0.4			V
Input Low Voltage	V_{IL}				0.4	V
					0.4	V
Output High Voltage	V_{OH}	I_{OH} = 20 µA,	V_{CCY} -0.4			V
		I_{OH} = 20 µA,	V_{CCA} -0.4			V
Output Low Voltage	V_{OL}	I_{OL} = 20 µA,			0.4	V
		I_{OL} = 20 µA,			0.4	V
Input Leakage Current	I_I	$0 \le V_{IN} \le 3.6$ V			±1	µA
Output Leakage Current	I_O	$0 \le V_{IN} \le 3.6$ V			±1	µA
Input Capacitance[3]	C_{IN}	f = 1 MHz, $V_{A/Y}$ = $V_{CCA/Y}$ or GND		5		pF
Output Capacitance[3]	C_O	f = 1 MHz, $V_{A/Y}$ = $V_{CCY/A}$ or GND		5		pF
SWITCHING CHARACTERISTICS[3]						
3.3V ± 0.3V ≤ V_{CCA} ≤ V_{CCY} ≤ 5V ± 0.5V						
Propagation Delay, t_{PD}	Y - A	R_S = 50Ω, C_A = 15 pF			5	ns
	A - Y	R_S = 50Ω, C_Y = 50 pF			5	ns
Rise Time	t_{R_Y}	R_S = 50Ω, C_Y = 50 pF			5	ns
Fall Time	t_{F_Y}	R_S = 50Ω, C_Y = 50 pF			5	ns
Rise Time	t_{R_A}	R_S = 50Ω, C_A = 15 pF			5	ns
Fall Time	t_{F_A}	R_S = 50Ω, C_A = 15 pF			5	ns
Maximum Data Rate		R_S = 50Ω, C_Y = 50 pF, C_A = 15 pF	40			Mbps
Channel To Channel Skew	t_{SKEW}	R_S = 50Ω, C_Y = 50 pF, C_A = 15 pF			tbd	ns
Part To Part Skew	t_{PPSKEW}	R_S = 50Ω, C_Y = 50 pF, C_A = 15 pF			tbd	ns
1.8V ± 0.15V ≤ V_{CCA} ≤ V_{CCY} ≤ 3.3V ±0.3V						
Propagation Delay, t_{PD}	Y - A	R_S = 50Ω, C_A = 15 pF			10	ns
	A - Y	R_S = 50Ω, C_Y = 50 pF			15	ns
Rise Time	t_{R_Y}	R_S = 50Ω, C_Y = 50 pF			10	ns
Fall Time	t_{F_Y}	R_S = 50Ω, C_Y = 50 pF			10	ns
Rise Time	t_{R_A}	R_S = 50Ω, C_A = 15 pF			10	ns
Fall Time	t_{F_A}	R_S = 50Ω, C_A = 15 pF			10	ns
Maximum Data Rate		R_S = 50Ω, C_Y = 50 pF, C_A = 15 pF	35			Mbps
Channel To Channel Skew	t_{SKEW}	R_S = 50Ω, C_Y = 50 pF, C_A = 15 pF			5	ns
1.2V ± 0.1 V ≤ V_{CCA} ≤ V_{CCY} ≤ 3.3 ± 0.3 V						
Propagation Delay, t_{PD}	Y - A	R_S = 50Ω, C_A = 15 pF			20	ns
	A - Y	R_S = 50Ω, C_Y = 50 pF			20	ns
Rise Time	t_{R_Y}	R_S = 50Ω, C_Y = 50 pF			15	ns
Fall Time	t_{F_Y}	R_S = 50Ω, C_Y = 50 pF			15	ns
Rise Time	t_{R_A}	R_S = 50Ω, C_A = 15 pF			15	ns
Fall Time	t_{F_A}	R_S = 50Ω, C_A = 15 pF			15	ns
Maximum Data Rate		R_S = 50Ω, C_Y = 50 pF, C_A = 15 pF		20		Mbps
Channel To Channel Skew	t_{SKEW}	R_S = 50Ω, C_Y = 50 pF, C_A = 15 pF			5	ns
2.5V ± 0.2V ≤ V_{CCA} ≤ V_{CCY} ≤ 3.3V ± 0.3V						
Propagation Delay, t_{PD}	Y - A	R_S = 50Ω, C_A = 15 pF			8.5	ns
	A - Y	R_S = 50Ω, C_Y = 50 pF			8.5	ns
Rise Time	t_{R_Y}	R_S = 50Ω, C_Y = 50 pF			8.5	ns
Fall Time	t_{F_Y}	R_S = 50Ω, C_Y = 50 pF			8.5	ns
Rise Time	t_{R_A}	R_S = 50Ω, C_A = 15 pF			8.5	ns
Fall Time	t_{F_A}	R_S = 50Ω, C_A = 15 pF			8.5	ns
Maximum Data Rate		R_S = 50Ω, C_Y = 50 pF, C_A = 15 pF	40			Mbps
Channel To Channel Skew	t_{SKEW}	R_S = 50Ω, C_Y = 50 pF, C_A = 15 pF			10	ns
POWER REQUIREMENTS						
Power Supply Voltages	V_{CCY}		1.65		5.5	V
	V_{CCA}		1.1		5.5	V
Quiescent Power Supply Current	I_{CCY}	Digital Inputs = 0 V or V_{CCY}			5	µA
	I_{CCA}	Digital Inputs = 0 V or V_{CCA}			5	µA

NOTES

[1]Temperature range is as follows: B Version: –40°C to +85°C.

[2] All typical vlaues are at T_A = +25°C unless otherwise stated.

[3] Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

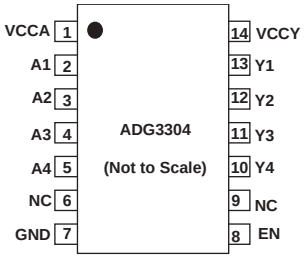
(T_A = 25°C unless otherwise noted)

V_{CCY} to GND .....-0.3 V to +7 V
V_{CCA} to GND .....-0.3 V to +7 V
Digtal Inputs (A) .....-0.3 V to (V_{CCA} +0.3V)
Digtal Inputs (Y) .....-0.3 V to (V_{CCY} +0.3V)
EN to GND .....-0.3 V to +7 V
Operating Temperature Range
Industrial (B Version) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... 150°C
14 Lead TSSOP
θ_{JA} Thermal Impedance ..... 150°C/W
Lead Temperature, Soldering (10seconds) ..... 300°C
IR Reflow, Peak Temperature (<20 seconds) ... +235°C

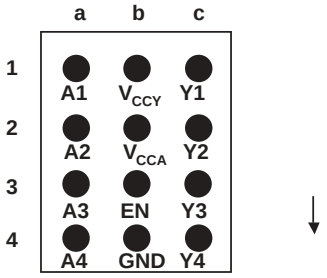
NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specifcation is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

Pin Configuration
14 Lead TSSOP (RU-14)



12 Lead WLCSP (CB-12)



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG3304BRU	–40°C to +85°C	TSSOP	RU-14
ADG3304BCB	–40°C to +85°C	WLCSP	CB-12

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG3304 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

GENERAL DESCRIPTION

The ADG3304 level translator allows the required level shifting necessary for data transfer in a system where multiple voltages are used. The device requires two supplies, V_{CCA} and V_{CCY}. These supplies set the logic levels on each side of the device. The device translates data present on the V_A side of the device to the higher voltage level at the V_Y side of the device. Similarly, as the device is capable of bidirectional translation, data applied to the V_Y side will be translated to the voltage referenced to V_A.

Level Translator Architecture

The forward channel consists of a string of inverters and a level translator, while the reverse channel consists simply of inverters. A level translator is not required in the reverse path (Y-A) as the supply voltage V_{CCY} must always be greater than or equal to V_{CCA}. A current limiting resistor is used in series with each channel to prevent any contention issues, see figure 1.

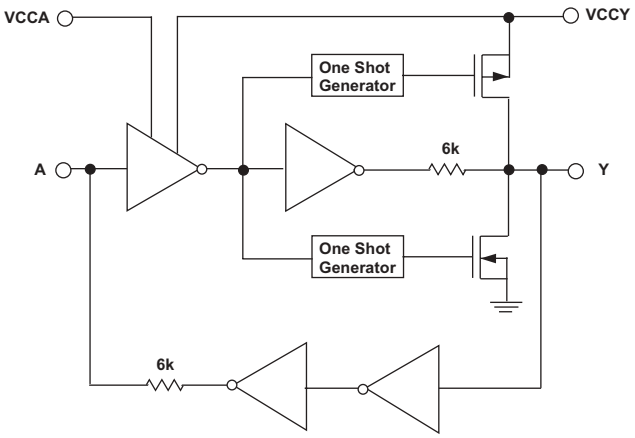


Figure 1. Simplified Functional Diagram of one channel.

As the driven side has to drive a load capacitance through this 6k resistance, one shot generators are used to drive large mos devices in the output stage to help speed up the rate of switching. The output stage is inactive and three state except when transistions are present on either side of the translator. When this happens the one shot fires turning on the output stage and driving the load capacitance faster than if it were driven through the resistor. As the device is bi-directional, both input stages will be active during this period. While this design gives maximum speed from the device, it can result in some current driving back into the source driving the input of the translator.

To ensure correct operation, the input driver should meet the following requirements - 50 Ω maximum output impedance with minimum of 20mA output current when driving 20Mbps.

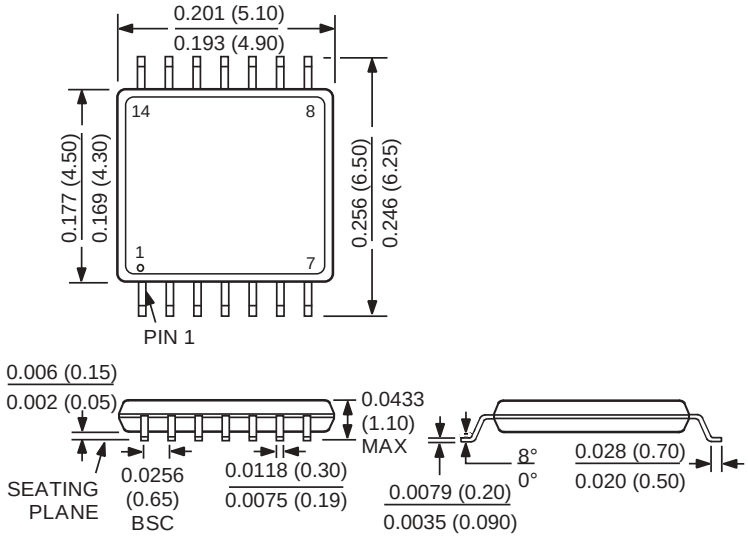
Enable Operation

When pulled low, the EN input allows the user to tri-state both sides (A and Y) of the level translator. EN pin is referred to V_{CCA} voltage.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

14-Lead TSSOP
(RU-14)



12-Lead WLCSP
(CB-12)