4-Channel, 12-/10-/8-Bit ADC with I²C-Compatible Interface in 8-Lead SOT23

Preliminary Technical Data

AD7991/AD7995/AD7999

FEATURES

- 12-/10-/8-bit ADC with fast conversion time: 2 µs typ
- 4 Channel / 3 Channel with Reference input
- Specified for V_{DD} of 2.7 V to 5.5 V
- Sequencer operation
- Temperature Range: -40 °C to 125 °C
- I²C®-compatible serial interface supports standard, fast, and High-speed modes
- 2 versions allow 2 I²C addresses
- Low power consumption
  - Shutdown mode: 1 µA max
- 8-lead SOT23 package

APPLICATIONS

- System Monitoring
- Battery Powered Systems
- Data Acquisition
- Medical Instruments

FUNCTIONAL BLOCK DIAGRAM

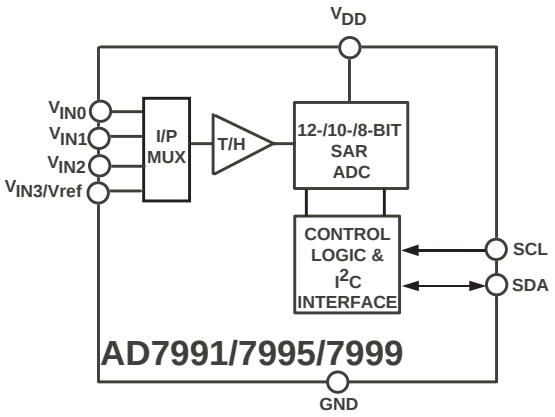


Figure 1.

GENERAL DESCRIPTION

The AD7991/AD7995/AD7999 are 12-/10-/8-bit, low power, successive approximation ADCs with an I²C-compatible interface. The parts operate from a single 2.7 V to 5.5 V power supply and feature a 2 µs conversion time. The part contains a 4-channel multiplexer and track-and-hold amplifier that can handle input frequencies up to 11 MHz.

The AD7991/AD7995/AD7999 provides a 2-wire serial interface compatible with I²C interfaces. The parts come in two versions with each part having an individual I²C address. This will allow two of the same devices be connected to the same I²C bus. Both parts support standard, fast and high-speed I²C interface modes

The AD7991/AD7995/AD7999 normally remain in a shutdown state while not converting, and power up only for conversions. The conversion process is controlled by a command mode, where every time an I²C read operation is executed on the AD7991/AD7995/AD7999, a conversion is performed and the result is returned on the I²C bus.

The reference for the part is taken from V_{DD}, this allows the widest dynamic input range to the ADC. Thus the analog input range to the ADC is 0V to V_{DD}. An external reference may also be used with this part. The external reference may be applied through the Ain3 input.

PRODUCT HIGHLIGHTS

1. 4 single ended analog input channels, with the option of having 3 single ended analog input channels and 1 reference input channel.
2. I²C compatible serial Interface. Standard, Fast and Hs-Modes
3. Automatic shutdown.
4. Reference derived from the power supply or external reference.
5. 8-lead SOT23 Package.

Table 1 Related Devices

Device Number	Resolution	Input Channels
AD7998	12	8
AD7997	10	8
AD7994	12	4
AD7993	10	4
AD7992	12	2

Rev. PrB

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

PrB/Sept 06—Revision 0: Initial Version

AD7991 SPECIFICATIONS

Temperature range is as follows: B version −40°C to +85°C, Y version -40°C to +125°C. Unless otherwise noted, V_{DD} = 2.7 V to 5.5 V; f_{SCL} = 3.4 Mhz Unless otherwise noted; $T_A = T_{MIN}$ to T_{MAX}.

Table 2.

Parameter	B Version	Y Version	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE[1]				F_{IN} = 10 kHz sine wave for f_{SCL} from 1.7 MHz to 3.4 MHz F_{IN} = 1 kHz sine wave for f_{SCL} up to 400 kHz
Signal-to-Noise + Distortion (SINAD)[2]	70.5	70.5	dB min	
Signal-to-Noise Ratio (SNR)[2]	71	71	dB min	
Total Harmonic Distortion (THD)[2]	−78	−78	dB max	
Peak Harmonic or Spurious Noise (SFDR)[2]	−79	−79	dB max	
Intermodulation Distortion (IMD)[2]				fa = 10.1 kHz, fb = 9.9 kHz for f_{SCL} from 1.7 MHz to 3.4 MHz fa = 1.1 kHz, fb = 0.9 kHz for f_{SCL} up to 400 kHz
Second Order Terms	−90	−90	dB typ	
Third Order Terms	−90	−90	dB typ	
Channel-to-Channel Isolation[2]	-90	-90	dB typ	F_{IN} = 108 Hz; see the Terminology Section
Full Power Bandwidth[2]	11	11	MHz typ	@ 3 dB
	2	2	MHz typ	@ 0.1 dB
DC ACCURACY				
Resolution	12	12	Bits	
Integral Nonlinearity[1, 2]	±1	±1	LSB max	
	±0.2	±0.2	LSB typ	
Differential Nonlinearity[1, 2]	+1/−0.9	+1/−0.9	LSB max	Guaranteed no missed codes to 12 bits
	±0.2	±0.2	LSB typ	
Offset Error[2]	±4	±4	LSB max	
Offset Error Matching	±0.5	±0.5	LSB max	
Offset Temperature drift	TBD	TBD	ppm/°C typ	
Gain Error[2]	±2	±2	LSB max	
Gain Error Matching	±0.5	±0.5	LSB max	
Gain Temperature drift	TBD	TBD	ppm/°C typ	
ANALOG INPUT				
Input Voltage Range	0 to REF_{IN}	0 to REF_{IN}	V	
DC Leakage Current	±1	±1	µA max	
Input Capacitance	30	30	pF typ	
REFERENCE INPUT				
REF_{IN} Input Voltage Range	1.2 to V_{DD}	1.2 to V_{DD}	V min/V max	
DC Leakage Current	±1	±1	µA max	
REF_{IN} Input Capacitance	30	pF typ		
Input Impedance	69	69	kΩ typ	
LOGIC INPUTS (SDA, SCL)				
Input High Voltage, V_{INH}	0.7 (V_{DD})	0.7 (V_{DD})	V min	
Input Low Voltage, V_{INL}	0.3 (V_{DD})	0.3 (V_{DD})	V max	
Input Leakage Current, I_{IN}	±1	±1	µA max	V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[3]	10	10	pF max	

Parameter	B Version	Y Version	Unit	Test Conditions/Comments
Input Hysteresis, V_{HYST}	0.1 (V_{DD})	0.1 (V_{DD})	V min	
LOGIC OUTPUTS (OPEN DRAIN)				
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 3 mA
	0.6	0.6	V max	I_{SINK} = 6 mA
Floating-State Leakage Current	±1	±1	µA max	
Floating-State Output Capacitance[3]	10	10	pF max	
Output Coding	Straight (Natural) Binary			
THROUGHPUT RATE	18 * (1/f_{SCL})		us max	See the Serial Interface section
POWER REQUIREMENTS				
V_{DD}	2.7/5.5	2.7/5.5	V min/max	
I_{DD}				Digital inputs = 0 V or V_{DD}
ADC Operating, Interface Active	0.06/0.1	0.06/0.1	mA max	V_{DD} = 3.3 V/5.5 V, 400 kHz f_{SCL}
	0.3/0.6	0.3/0.6	mA max	V_{DD} = 3.3 V/5.5 V, 3.4 MHz f_{SCL}
Power Down, Interface Active	TBD	TBD	mA max	V_{DD} = 3.3 V/5.5 V, 400 kHz f_{SCL}
	TBD	TBD	mA max	V_{DD} = 3.3 V/5.5 V, 3.4 MHz f_{SCL}
Power-Down , Interface Inactive	1/2	1/2	µA max	V_{DD} = 3.3 V/5.5 V
Power Dissipation				
Fully Operational			mW max	V_{DD} = 3.3 V/5.5 V, 400 kHz f_{SCL}
			mW max	V_{DD} = 3.3 V/5.5 V, 3.4 MHz f_{SCL}
ADC Operating, Interface Active	0.495/2.2	0.495/2.2	mW max	V_{DD} = 3.3 V/5.5 V, 400 kHz f_{SCL}
	1.98/6.05	1.98/6.05	mW max	V_{DD} = 3.3 V/5.5 V, 3.4 MHz f_{SCL}
Power Down, Interface Inactive	3.3/11	3.3/11	µW max	V_{DD} = 3.3 V/5.5 V

[1] Max/min AC dynamic performance, INL and DNL specifications are typical specifications when operating in Mode 2 with I^2C Hs-mode SCL frequencies. Specifications outlined for Mode 2 apply to Mode 3 also. Sample delay and bit trial delay enabled.
[2] See the terminology section
[3] Guaranteed by Initial Characterization.

AD7995 SPECIFICATIONS

Temperature range for Y version is −40°C to +125°C. Unless otherwise noted, V_{DD} = 2.7 V to 5.5 V; f_{SCL} = 3.4 Mhz Unless otherwise noted; $T_A = T_{MIN}$ to T_{MAX}.

Table 3.

Parameter	Y Version	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE[1]			F_{IN} = 10 kHz sine wave for f_{SCL} from 1.7 MHz to 3.4 MHz F_{IN} = 1 kHz sine wave for f_{SCL} up to 400 kHz
Signal-to-Noise + Distortion (SINAD)[2]	61	dB min	
Total Harmonic Distortion (THD)[2]	−75	dB max	
Peak Harmonic or Spurious Noise (SFDR)[2]	−76	dB max	
Intermodulation Distortion (IMD)[2]			fa = 10.1 kHz, fb = 9.9 kHz for f_{SCL} from 1.7 MHz to 3.4 MHz fa = 1.1 kHz, fb = 0.9 kHz for f_{SCL} up to 400 kHz
Second Order Terms	−86	dB typ	
Third Order Terms	−86	dB typ	
Channel-to-Channel Isolation[2]	-90	dB typ	F_{IN} = 108 Hz; see the Terminology Section
Full Power Bandwidth[2]	11	MHz typ	@ 3 dB
	2	MHz typ	@ 0.1 dB
DC ACCURACY			
Resolution	10	Bits	
Integral Nonlinearity[1, 2]	±0.5	LSB max	
Differential Nonlinearity[1, 2]	±0.5	LSB max	Guaranteed no missed codes to 10 bits
Offset Error[2]	±2	LSB max	
Offset Error Matching	±0.5	LSB max	
Offset Temperature drift	TBD	ppm/°C typ	
Gain Error[2]	±1.5	LSB max	
Gain Error Matching	±0.5	LSB max	
Gain Temperature drift	TBD	ppm/°C typ	
ANALOG INPUT			
Input Voltage Range	0 to REF_{IN}	V	When Vin3/VREF = VIN3, Vref = VDD
DC Leakage Current	±1	µA max	
Input Capacitance	30	pF typ	
REFERENCE INPUT			
REF_{IN} Input Voltage Range	1.2 to V_{DD}	V min/V max	
DC Leakage Current	±1	µA max	
REF_{IN} Input Capacitance	30	pF typ	
Input Impedance	69	kΩ typ	
LOGIC INPUTS (SDA, SCL)			
Input High Voltage, V_{INH}	0.7 (V_{DD})	V min	
Input Low Voltage, V_{INL}	0.3 (V_{DD})	V max	
Input Leakage Current, I_{IN}	±1	µA max	V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[3]	10	pF max	
Input Hysteresis, V_{HYST}	0.1 (V_{DD})	V min	
LOGIC OUTPUTS (OPEN DRAIN)			
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 3 mA
	0.6	V max	I_{SINK} = 6 mA
Floating-State Leakage Current	±1	µA max	
Floating-State Output Capacitance[3]	10	pF max	
Output Coding	Straight (Natural) Binary		
THROUGHPUT RATE			See the Serial Interface section
	18 * (1/f_{SCL})	us max	

Parameter	Y Version	Unit	Test Conditions/Comments
POWER REQUIREMENTS			
V_{DD}	2.7/5.5	V min/max	
I_{DD}			Digital inputs = 0 V or V_{DD}
ADC Operating, Interface Active	0.06/0.1	mA max	V_{DD} = 3.3 V/5.5 V, 400 kHz f_{SCL}
	0.3/0.6	mA max	V_{DD} = 3.3 V/5.5 V, 3.4 MHz f_{SCL}
Power Down, Interface Active	TBD	mA max	V_{DD} = 3.3 V/5.5 V, 400 kHz f_{SCL}
	TBD	mA max	V_{DD} = 3.3 V/5.5 V, 3.4 MHz f_{SCL}
Power-Down , Interface InActive	1/2	µA max	V_{DD} = 3.3 V/5.5 V
Power Dissipation			
Fully Operational		mW max	V_{DD} = 3.3 V/5.5 V, 400 kHz f_{SCL}
		mW max	V_{DD} = 3.3 V/5.5 V, 3.4 MHz f_{SCL}
ADC Operating, Interface Active	0.495/2.2	mW max	V_{DD} = 3.3 V/5.5 V, 400 kHz f_{SCL}
	1.98/6.05	mW max	V_{DD} = 3.3 V/5.5 V, 3.4 MHz f_{SCL}
Power Down, Interface Inactive	3.3/11	µW max	V_{DD} = 3.3 V/5.5 V

[1] Max/min AC dynamic performance, INL and DNL specifications are typical specifications when operating in Mode 2 with I^2C Hs-mode SCL frequencies. Specifications outlined for Mode 2 apply to Mode 3 also. Sample delay and bit trial delay enabled.
[2] See the Terminology section
[3] Guaranteed by Initial Characterization.

AD7999 SPECIFICATIONS

Temperature range for Y version is −40°C to +125°C. Unless otherwise noted, V_{DD} = 2.7 V to 5.5 V; f_{SCL} = 3.4 Mhz Unless otherwise noted; $T_A = T_{MIN}$ to T_{MAX}.

Table 4.

Parameter	Y Version	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE[1]			F_{IN} = 10 kHz sine wave for f_{SCL} from 1.7 MHz to 3.4 MHz F_{IN} = 1 kHz sine wave for f_{SCL} up to 400 kHz
Signal-to-Noise + Distortion (SINAD)[2]	49	dB min	
Total Harmonic Distortion (THD)[2]	–65	dB max	
Peak Harmonic or Spurious Noise (SFDR)[2]	–65	dB max	
Intermodulation Distortion (IMD)[2]			fa = 10.1 kHz, fb = 9.9 kHz for f_{SCL} from 1.7 MHz to 3.4 MHz fa = 1.1 kHz, fb = 0.9 kHz for f_{SCL} up to 400 kHz
Second Order Terms	–76	dB typ	
Third Order Terms	–76	dB typ	
Channel-to-Channel Isolation[2]	-90	dB typ	F_{IN} = 108 Hz; see the Terminology section
Full Power Bandwidth[2]	11	MHz typ	@ 3 dB
	2	MHz typ	@ 0.1 dB
DC ACCURACY			
Resolution	8	Bits	
Integral Nonlinearity[1, 2]	±0.3	LSB max	
Differential Nonlinearity[1, 2]	±0.3	LSB max	Guaranteed no missed codes to 8 bits
Offset Error[2]	±0.5	LSB max	
Offset Error Matching	±0.3	LSB max	
Offset Temperature drift	TBD	ppm/°C typ	
Gain Error[2]	±0.3	LSB max	
Gain Error Matching	±0.3	LSB max	
Gain Temperature drift	TBD	ppm/°C typ	
ANALOG INPUT			
Input Voltage Range	0 to REF_{IN}	V	When Vin3/VREF = VIN3, Vref = VDD
DC Leakage Current	±1	µA max	
Input Capacitance	30	pF typ	
REFERENCE INPUT			
REF_{IN} Input Voltage Range	1.2 to V_{DD}	V min/V max	
DC Leakage Current	±1	µA max	
REF_{IN} Input Capacitance	30	pF typ	
Input Impedance	69	kΩ typ	
LOGIC INPUTS (SDA, SCL)			
Input High Voltage, V_{INH}	0.7 (V_{DD})	V min	
Input Low Voltage, V_{INL}	0.3 (V_{DD})	V max	
Input Leakage Current, I_{IN}	±1	µA max	V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[3]	10	pF max	
Input Hysteresis, V_{HYST}	0.1 (V_{DD})	V min	
LOGIC OUTPUTS (OPEN DRAIN)			
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 3 mA
	0.6	V max	I_{SINK} = 6 mA
Floating-State Leakage Current	±1	µA max	
Floating-State Output Capacitance[3]	10	pF max	
Output Coding	Straight (Natural) Binary		
THROUGHPUT RATE			See the Serial Interface section
	18 * (1/f_{SCL})	us max	

Parameter	Y Version	Unit	Test Conditions/Comments
POWER REQUIREMENTS			
V_{DD}	2.7/5.5	V min/max	
I_{DD}			Digital inputs = 0 V or V_{DD}
ADC Operating, Interface Active	0.06/0.1	mA max	V_{DD} = 3.3 V/5.5 V, 400 kHz f_{SCL}
	0.3/0.6	mA max	V_{DD} = 3.3 V/5.5 V, 3.4 MHz f_{SCL}
Power Down, Interface Active	TBD	mA max	V_{DD} = 3.3 V/5.5 V, 400 kHz f_{SCL}
	TBD	mA max	V_{DD} = 3.3 V/5.5 V, 3.4 MHz f_{SCL}
Power-Down , Interface Inactive	1/2	µA max	V_{DD} = 3.3 V/5.5 V
Power Dissipation			
Fully Operational		mW max	V_{DD} = 3.3 V/5.5 V, 400 kHz f_{SCL}
		mW max	V_{DD} = 3.3 V/5.5 V, 3.4 MHz f_{SCL}
ADC Operating, Interface Active	0.495/2.2	mW max	V_{DD} = 3.3 V/5.5 V, 400 kHz f_{SCL}
	1.98/6.05	mW max	V_{DD} = 3.3 V/5.5 V, 3.4 MHz f_{SCL}
Power Down, Interface Inactive	3.3/11	µW max	V_{DD} = 3.3 V/5.5 V

[1] Max/min AC dynamic performance, INL and DNL specifications are typical specifications when operating in Mode 2 with I^2C Hs-mode SCL frequencies. Specifications outlined for Mode 2 apply to Mode 3 also. Sample delay and bit trial delay enabled.
[2] See the Terminology section
[3] Guaranteed by Initial Characterization.

I²C TIMING SPECIFICATIONS

Guaranteed by initial characterization. All values measured with the input filtering enabled. C_B refers to the capacitive load on the bus line. t_r and t_f measured between 0.3 V_{DD} and 0.7 V_{DD}.

Standard, Fast and High speed mode timing specifications apply to the AD7991/AD7995/AD7999-1. See Figure 2.Unless otherwise noted, V_{DD} = 2.7 V to 5.5 V; T_A = T_{MIN} to T_{MAX}.

Table 5.

		Limit at T_{MIN}, T_{MAX}			
Parameter	**Conditions**	**Min**	**Max**	**Unit**	**Description**
f_{SCL}	Standard mode		100	kHz	Serial clock frequency
	Fast mode		400	kHz	
	High speed mode				
	C_B = 100 pF max		3.4	MHz	
	C_B = 400 pF max		1.7	MHz	
t_1	Standard mode	4		µs	t_{HIGH}, SCL high time
	Fast mode	0.6		µs	
	High speed mode				
	C_B = 100 pF max	60		ns	
	C_B = 400 pF max	120		ns	
t_2	Standard mode	4.7		µs	t_{LOW}, SCL low time
	Fast mode	1.3		µs	
	High speed mode				
	C_B = 100 pF max	160		ns	
	C_B = 400 pF max	320		ns	
t_3	Standard mode	250		ns	$t_{SU;DAT}$, data setup time
	Fast mode	100		ns	
	High speed mode	10		ns	
t_4[1]	Standard mode	0	3.45	µs	$t_{HD;DAT}$, data hold time
	Fast mode	0	0.9	µs	
	High Speed mode				
	C_B = 100 pF max	0	70[2]	ns	
	C_B = 400 pF max	0	150	ns	
t_5	Standard mode	4.7		µs	$t_{SU;STA}$, setup time for a repeated START condition
	Fast mode	0.6		µs	
	High Speed mode	160		ns	
t_6	Standard mode	4		µs	$t_{HD;STA}$, hold time for a repeated START condition
	Fast mode	0.6		µs	
	High speed mode	160		ns	
t_7	Standard mode	4.7		µs	t_{BUF}, bus free time between a STOP and a START condition
	Fast mode	1.3		µs	
t_8	Standard mode	4		µs	$t_{SU;STO}$, setup time for STOP condition
	Fast mode	0.6		µs	
	High speed mode	160		ns	
t_9	Standard mode		1000	ns	t_{RDA}, rise time of SDA signal
	Fast mode	20 + 0.1 C_B	300	ns	
	High speed mode				
	C_B = 100 pF max	10	80	ns	
	C_B = 400 pF max	20	160	ns	

Parameter	Conditions	Limit at T_{MIN}, T_{MAX}			Description
		Min	Max	Unit	
t_{10}	Standard mode		300	ns	t_{FDA}, fall time of SDA signal
	Fast mode	20 + 0.1 C_B	300	ns	
	High speed mode				
	C_B = 100 pF max	10	80	ns	
	C_B = 400 pF max	20	160	ns	
t_{11}	Standard mode		1000	ns	t_{RCL}, rise time of SCL signal
	Fast mode	20 + 0.1 C_B	300	ns	
	High speed mode				
	C_B = 100 pF max	10	40	ns	
	C_B = 400 pF max	20	80	ns	
t_{11A}	Standard mode		1000	ns	t_{RCL1}, rise time of SCL signal after a repeated START condition and after an acknowledge bit
	Fast mode	20 + 0.1 C_B	300	ns	
	High speed mode				
	C_B = 100 pF max	10	80	ns	
	C_B = 400 pF max	20	160	ns	
t_{12}	Standard mode		300	ns	t_{FCL}, fall time of SCL signal
	Fast mode	20 + 0.1 C_B	300	ns	
	High speed mode				
	C_B = 100 pF max	10	40	ns	
	C_B = 400 pF max	20	80	ns	
t_{SP}	Fast mode	0	50	ns	Pulse width of suppressed spike
	High speed mode	0	10	ns	
$t_{POWER-UP}$		1		µs typ	Power-up time

[1] A device must provide a data hold time for SDA in order to bridge the undefined region of the SCL falling edge.
[2] For 3 V supplies, the maximum hold time with C_B = 100 pF max is 100 ns max.

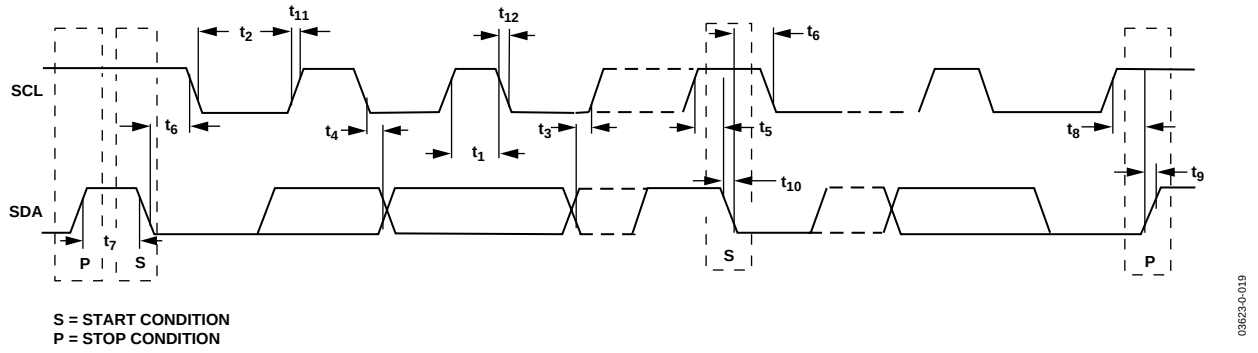


Figure 2. Two-Wire Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to GND	−0.3 V to 7 V
Analog Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Reference Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to +7 V
Digital Output Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	
Commercial (B Version)	−40°C to +85°C
Industrial (Y Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°
Junction Temperature	150°C
8-Lead SOT-23 Package	
θ_{JA} Thermal Impedance	TBD °C/W
θ_{JC} Thermal Impedance	TBD °C/W
Pb/SN Temperature, Soldering	
Reflow (10 sec to 30 sec)	TBD °C
Pb-Free Temperature, Soldering Reflow	TBD °C
ESD	TBD kV

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

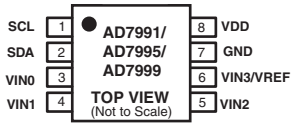


Figure 3.AD7991/AD7995/AD7999 Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	SCL	Digital Input. Serial bus clock. External pull-up resistor required.
2	SDA	Digital I/O. Serial bus bidirectional data. Open-drain output. External pull-up resistor required.
3	V_{IN0}	Analog Input 1. Single-ended analog input channel. The input range is 0 V to V_{ref}.
4	V_{IN1}	Analog Input 2. Single-ended analog input channel. The input range is 0 V to V_{ref}.
5	V_{IN2}	Analog Input 3. Single-ended analog input channel. The input range is 0 V to V_{ref}.
6	V_{IN3}/V_{REF}	Analog Input 4. Single-ended analog input channel. The input range is 0 V to V_{ref}. Can also be used to input an external Vref signal.
7	GND	Analog Ground. Ground reference point for all circuitry on the AD7991/AD7995/AD7999. All analog input signals should be referred to this AGND voltage.
8	V_{DD}	Power Supply Input. The V_{DD} range for the AD7991/AD7995/AD7999 is from 2.7 V to 5.5 V.

Table 8. I^2C Address Selection

Part Number	I^2C Address
AD7991 -0	010 1000
AD7991-1	010 1001
AD7995-0	010 1000
AD7995-1	010 1001
AD7999-0	010 1000
AD7999-1	010 1001

TYPICAL PERFORMANCE CHARACTERISTICS

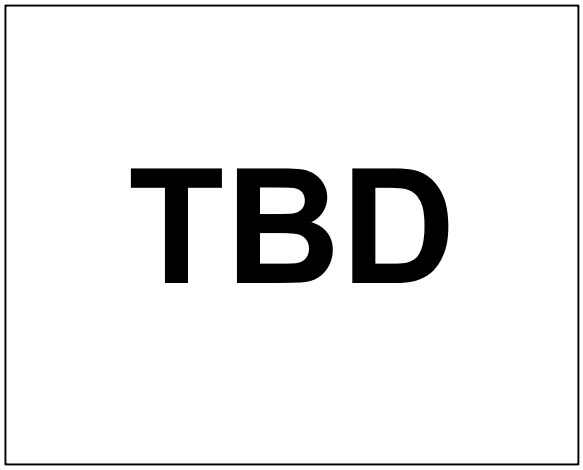


Figure 4

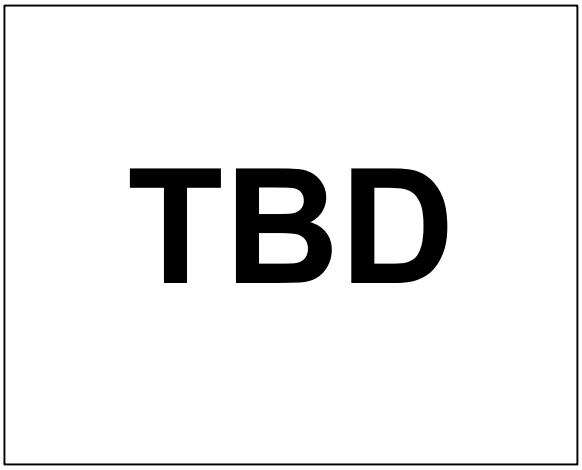


Figure 7

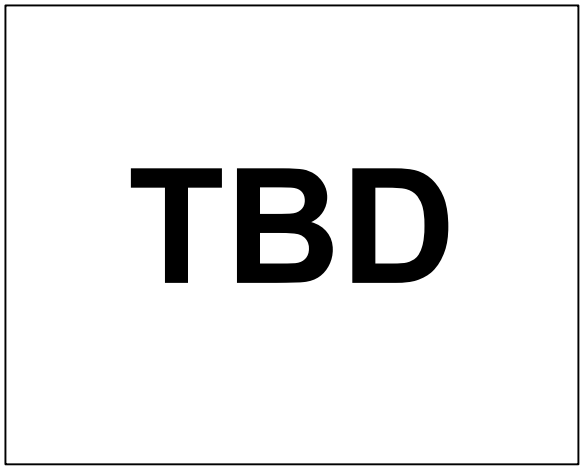


Figure 5

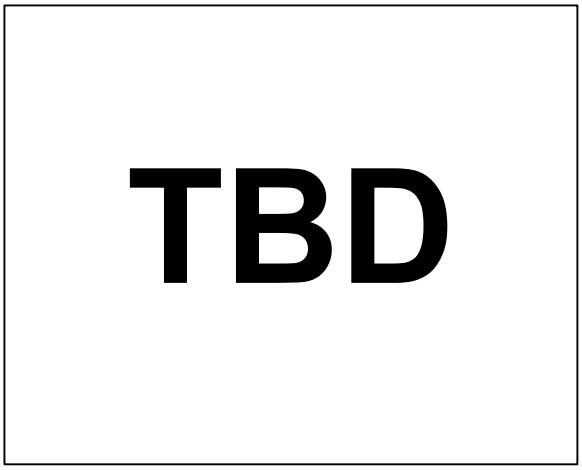


Figure 8

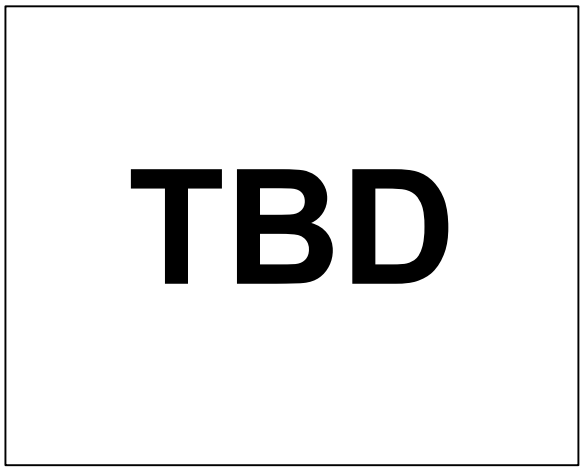


Figure 6

TERMINOLOGY

Signal-to-Noise and Distortion Ratio (SINAD)
The measured ratio of signal-to-noise and distortion at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-noise and distortion ratio for an ideal N-bit converter with a sine wave input is given by

$$Signal\text{-}to\text{-}(Noise + Distortion) = (6.02\ N + 1.76)\ \text{dB}$$

Thus, the SINAD is 49.92 dB for an 8-bit converter, 61.96 dB for a 10-bit converter and 74 dB for a 12-bit converter.

Total Harmonic Distortion (THD)
The ratio of the rms sum of harmonics to the fundamental. For the AD7991/AD7995/AD7999, it is defined as

$$THD\ (\text{dB}) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through sixth harmonics.

Peak Harmonic or Spurious Noise
The ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Typically, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n equal zero. For example, second-order terms include (fa + fb) and (fa − fb), while third-order terms include (2fa + fb), (2fa − fb),(fa + 2fb) and (fa − 2fb).

The AD7993/AD7994 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves while the third-order terms are usually at a frequency close to the input frequencies. As a result, the second and third-order terms are specified separately. The calculation of intermodulation distortion is, like the THD specification, the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals, expressed in dB.

Channel-to-Channel Isolation
A measure of the level of crosstalk between channels, taken by applying a full-scale sine wave signal to the unselected input channels, and determining how much the 108 Hz signal is attenuated in the selected channel. The sine wave signal applied to the unselected channels is then varied from 1 kHz up to 2 MHz, each time determining how much the 108 Hz signal in the selected channel is attenuated. This figure represents the worst-case level across all channels.

Full-Power Bandwidth
The input frequency at which the amplitude of the reconstructed fundamental is reduced by 0.1 dB or 3 dB for a full-scale input.

Integral Nonlinearity
The maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints are zero scale, a point 1 LSB below the first code transition, and full scale, a point 1 LSB above the last code transition.

Differential Nonlinearity
The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
The deviation of the first code transition (00…000) to (00…001) from the ideal—that is, AGND + 1 LSB.

Offset Error Match
The difference in offset error between any two channels.

Gain Error
The deviation of the last code transition (111…110) to (111…111) from the ideal (that is, REF_{IN} − 1 LSB) after the offset error has been adjusted out.

Gain Error Match
The difference in gain error between any two channels.

THEORY OF OPERATION

The AD7991/AD7995/AD7999 are low power, 12-/10-/8-bit, single-supply, 4-channel A/D converters. The parts can be operated from a 2.35 V to 5.5 V supply.

The AD7991/AD7995/AD7999 provides the user with a 4-channel multiplexer, an on-chip track-and-hold, an A/D converter, and an I²C-compatible serial interface, all housed in a 8-lead SOT23 package that offers the user considerable space saving advantages over alternative solutions.

The AD7991/AD7995/AD7999 normally remains in a power-down state while not converting. When supplies are first applied, the part comes up in a power-down state. Power-up is initiated prior to a conversion, and the device returns to power-down upon completion of the conversion. This automatic power-down feature allows power saving between conversions. This means any read or write operations across the I²C interface can occur while the device is in power-down.

CONVERTER OPERATION

The AD7991/AD7995/AD7999 is a successive approximation, analog-to-digital converter based around a capacitive DAC. Figure 9 and Figure 10 show simplified schematics of the ADC during its acquisition and conversion phases, respectively. Figure 9 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in position A, the comparator is held in a balanced condition, and the sampling capacitor acquires the signal on V_{IN}.

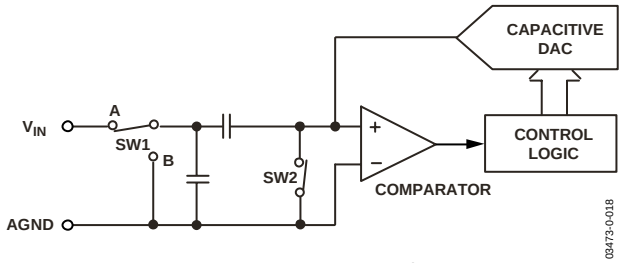


Figure 9. ADC Acquisition Phase

When the ADC starts a conversion, as shown in Figure 10, SW2 opens and SW1 moves to position B, causing the comparator to become unbalanced. The input is disconnected once the conversion begins. The control logic and the capacitive DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. Figure 11 shows the ADC transfer function.

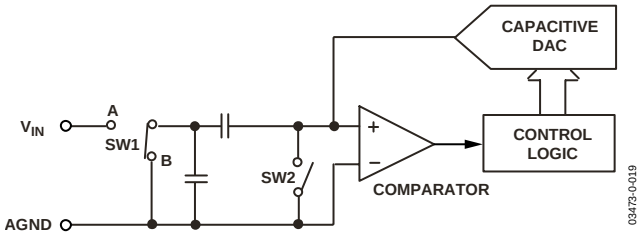


Figure 10. ADC Conversion Phase

ADC Transfer Function

The output coding of the AD7991/AD7995/AD7999 is straight binary. The designed code transitions occur at successive integer LSB values (i.e., 1 LSB, 2 LSB, and so on). The LSB size for the AD7991/AD7995/AD7999 is $REF_{IN}/4096$. Figure 11 shows the ideal transfer characteristic for the AD7991/AD7995/AD7999.

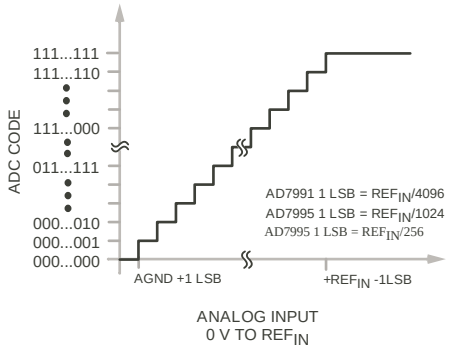


Figure 11. AD7991/AD7995/AD7999 Transfer Characteristic

TYPICAL CONNECTION DIAGRAM

Figure 13 shows the typical connection diagram for the AD7991/AD7995/AD7999.

The reference voltage can be taken from the supply voltage V_{DD}. However, the AD7991/AD7995/AD7999 can be configured to be a three-channel device with the reference voltage applied to the $V_{IN}3/REF_{IN}$ pin.

SDA and SCL form the 2-wire I^2C compatible interface. External pull-up resisters are required for both SDA and SCL lines.

The AD7991/AD7995/AD7999-0 and the AD7991/AD7995/AD7999-1 both support the standard, fast and high speed I^2C interface modes. Both the -0 and the -1 device will have an independent I^2C address. This will allow both device to connect to the same I^2C bus without any contention issues.

Wake up from power-down prior to a conversion is approximately 1 µs, and conversion time is approximately 2 µs. The AD7991/AD7995/AD7999 enters shutdown mode again after each conversion, which is useful in applications where power consumption is a concern.

ANALOG INPUT

Figure 12 shows an equivalent circuit of the AD7991/AD7995/AD7999 analog input structure. The two diodes, D1 and D2, provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal does not exceed the supply rails by more than 300 mV. This causes these diodes to become forward-biased and start conducting current into the substrate. These diodes can conduct a maximum current of 10 mA without causing irreversible damage to the part.

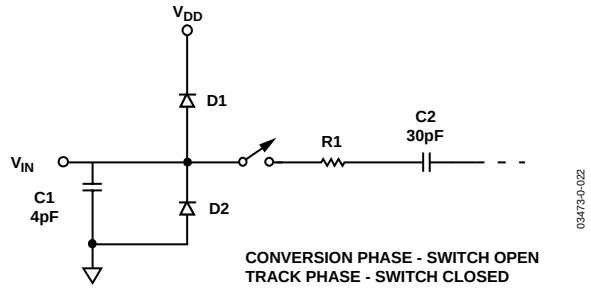


Figure 12. Equivalent Analog Input Circuit

Capacitor C1 in Figure 12 is typically about 4 pF and can primarily be attributed to pin capacitance. Resistor R1 is a lumped component made up of the on resistance (R_{ON}) of a track-and-hold switch, and also the R_{ON} of the input multiplexer. The total resistor is typically about 400 Ω. C2, the ADC sampling capacitor, has a typical capacitance of 30 pF.

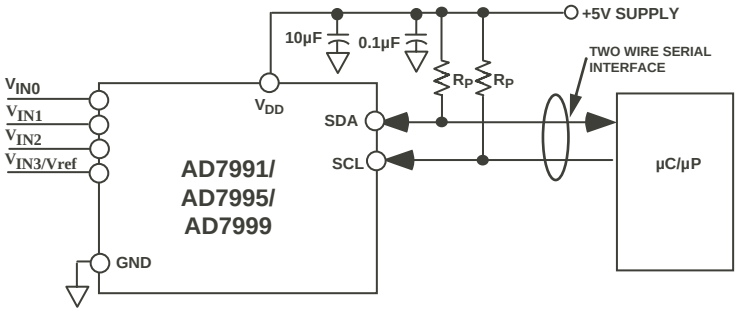


Figure 13. AD7991/AD7995/AD7999 Typical Connection Diagram

For ac applications, removing high frequency components from the analog input signal is recommended by use of an RC band-pass filter on the relevant analog input pin. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the op amp is a function of the particular application.

When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance depends on the amount of total harmonic distortion (THD) that can be tolerated. THD increases as the source impedance increases, and performance degrades. Figure 14 and Figure 15 shows the THD vs. the analog input signal frequency for different source impedances. at 3V and 5V respectively.

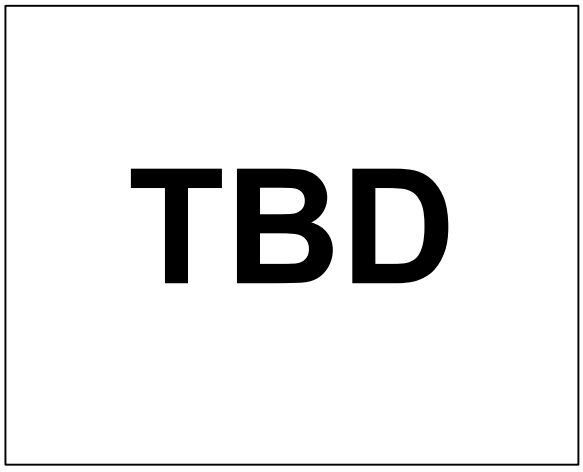


Figure 14. THD vs Analog Input Frequency for various source Impedances for VDD = 3V

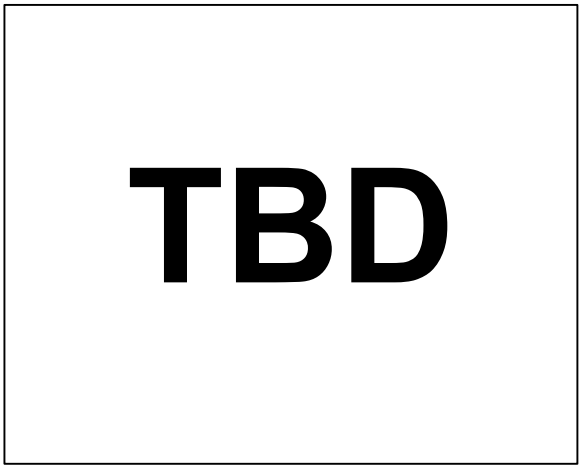


Figure 15. THD vs Analog Input Frequency for various source Impedances for VDD = 5V

INTERNAL REGISTER STRUCTURE

CONFIGURATION REGISTER

The configuration register is an 8-bit write only register that is used to set the operating modes of the AD7991/AD7995/AD7995. The bit functions are outlined in Table 9. A single-byte write is necessary when writing to the configuration register. D7 is the MSB. When the master writes to the AD7991/AD799/AD7999, the first byte is written to the status register.

Table 9. Configuration Register Bit Function Descriptions and * shows the default Settings at Power-Up

D7	D6	D5	D4	D3	D2	D1	D0
CH3	CH2	CH1	CH0	REF_SEL	FLTR	Bit Trial Delay	Sample Delay
1*	1 *	1	1*	0*	0*	0 *	0*

Table 10. Bit Function Descriptions

Bit	Mnemonic	Comment
D7–D4	CH3–CH0	These four channel address bits select the analog input channel(s) to be converted. A 1 in any of Bits D7 to D4 selects a channel for conversion. If more than one channel bit is set to 1, the AD7991/AD7995/AD7999 sequence through the selected channels, starting with the lowest channel. All unused channels should be set to 0. Table 11 shows how these four channel address bits are decoded. Prior to initiating a conversion, the channel(s) must be selected in the configuration register.
D3	REF_SEL	This bit allows the user to select the supply voltage as the reference or use an external reference. If this bit is a 0 the supply is used as the reference and the device acts as a four channel input part, if it is set to a 1 an external reference must be used and applied to the Vin3/VREF pin, in this case the device acts as a three channel input part.
D2	FLTR	The value written to this bit of the control register determines whether the filtering on SDA and SCL is enabled or is to be bypassed. If this bit is a 0, then the filtering is enabled; if it is a 1, the filtering is bypassed.
D1	Bit Trial Delay	See paragraph below entitled: SAMPLE DELAY AND BIT TRIAL DELAY
D0	Sample Delay	See paragraph below entitled: SAMPLE DELAY AND BIT TRIAL DELAY

Table 11. Channel Selection

D7	D6	D5	D4	Analog Input Channel	Comments
0	0	0	0	No channel selected.	
0	0	0	1	Convert on $V_{IN}0$.	
0	0	1	0	Convert on $V_{IN}1$.	
0	0	1	1	Sequence between $V_{IN}0$ and $V_{IN}1$.	
0	1	0	0	Convert on $V_{IN}2$.	
0	1	0	1	Sequence between $V_{IN}0$ and $V_{IN}2$.	
0	1	1	0	Sequence between $V_{IN}1$ and $V_{IN}2$.	The AD7991/AD7995/AD7999 converts on the selected channel in the sequence in ascending order, starting with the lowest channel in the sequence.
0	1	1	1	Sequence between $V_{IN}0$, $V_{IN}1$, and $V_{IN}2$.	
1	0	0	0	Convert on $V_{IN}3$.	
1	0	0	1	Sequence between $V_{IN}0$ and $V_{IN}3$.	
1	0	1	0	Sequence between $V_{IN}1$ and $V_{IN}3$.	
1	0	1	1	Sequence between $V_{IN}0$, $V_{IN}1$, and $V_{IN}3$.	
1	1	0	0	Sequence between $V_{IN}2$ and $V_{IN}3$.	
1	1	0	1	Sequence between $V_{IN}0$, $V_{IN}2$, and $V_{IN}3$.	
1	1	1	0	Sequence between $V_{IN}1$, $V_{IN}2$, and $V_{IN}3$.	
1	1	1	1	Sequence between $V_{IN}0$, $V_{IN}1$, $V_{IN}2$, and $V_{IN}3$.	

SAMPLE DELAY AND BIT TRIAL DELAY

It is recommended that no I^2C bus activity occur when a conversion is taking place. However, if this is not always possible, then in order to maintain the performance of the ADC, Bits D0 and D1 in the configuration register are used to delay critical sample intervals and bit trials from occurring while there is activity on the I^2C bus. This results in a quiet period for each bit decision. In certain cases where there

is excessive activity on the interface lines, this may have the effect of increasing the overall conversion time. However, if bit trial delays extend longer than 1 μs, the conversion terminates.

When Bits D0 and D1 are both 0, the bit trial and sample interval delaying mechanism is implemented. The default setting of D0 and D1 is 0. To turn off both delay mechanisms, set D0 and D1 to 1.

CONVERSION RESULT REGISTER

The conversion result register is a 16-bit read-only register that stores the conversion result from the ADC in straight binary format. A 2-byte read is necessary to read data from this register. Table 12 shows the contents of the first byte to be read, from AD7991/AD7995/AD7999 and Table 13 shows the contents of the second byte to be read.

Table 12. Conversion Value Register (First Read)

D15	D14	D13	D12	D11	D10	D9	D8
Leading Zero	Leading Zero	CH_{ID1}	CH_{ID0}	MSB	B10	B9	B8

Table 13. Conversion Value Register (Second Read)

D7	D6	D5	D4	D3	D2	D1	D0
B7	B6	B5	B4	B3 /0	B2 /0	B1/0	B0/0

The AD7991/AD7995/AD7999 conversion result consists of 2 leading zeros, two channel identifier bits, and the 12-/10-/8- bit data result. For the AD7995, the 2 LSB (D1 and D0) of the second read contain two trailing 0s. For the AD7999, the 4 LSB (D3, D2, D1 and D0) of the second read contain 4 trailing zeros

SERIAL INTERFACE

Control of the AD7991/AD7995/AD7999 is carried out via the I²C-compatible serial bus. The AD7991/AD7995/AD7999 is connected to this bus as a slave device under the control of a master device, such as the processor.

SERIAL BUS ADDRESS

Like all I²C-compatible devices, the AD7991/AD7995/AD7999 has a 7-bit serial address. The devices comes in two versions, the AD7991/AD7995/AD7999-0 and the AD7991/AD7995/AD7999-1. Each version has a different address. See Table 8. By giving different addresses for the two versions, up to 2 AD7991/AD7995/AD7999 devices can be connected to a single serial bus.

The serial bus protocol operates as follows:

The master initiates data transfer by establishing a START condition, defined as a high-to-low transition on the serial data line SDA, while the serial clock line, SCL, remains high. This indicates that an address/data stream follows. All slave peripherals connected to the serial bus respond to the START condition and shift in the next eight bits, consisting of a 7-bit address (MSB first) plus an R/$\overline{W}$ bit that determines the direction of the data transfer—that is, whether data is written to or read from the slave device.

The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the acknowledge bit. All other devices on the bus remain idle while the selected device waits for data to be read from or written to it. If the R/$\overline{W}$ bit is a 0, the master writes to the slave device. If the R/$\overline{W}$ bit is a 1, the master reads from the slave device.

Data is sent over the serial bus in sequences of nine clock pulses, eight bits of data followed by an acknowledge bit from the receiver of data. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, because a low-to-high transition when the clock is high may be interpreted as a STOP signal.

When all data bytes have been read or written, stop conditions are established. In write mode, the master pulls the data line high during the 10th clock pulse to assert a STOP condition. In read mode, the master device pulls the data line high during the low period before the ninth clock pulse. This is known as no acknowledge. The master then takes the data line low during the low period before the 10th clock pulse, then high during the 10th clock pulse to assert a STOP condition.

Any number of bytes of data may be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

WRITING TO THE AD7991/AD7995/AD7999

This part can be used in read-only mode if the user wishes to use all 4 channels sequentially as the default on the configure register allows. However, the user must write to the configuration register of the part AD7991/AD7995/AD7999 if they want to change from the default settings on the configuration register.

WRITING A SINGLE BYTE OF DATA TO THE CONFIGURATION REGISTER

The configuration register is an 8-bit register, so only one byte of data can be written. Writing a single byte of data to this register consists of the serial bus write address, followed by the data byte written to the configuration register. See Figure 16 below.

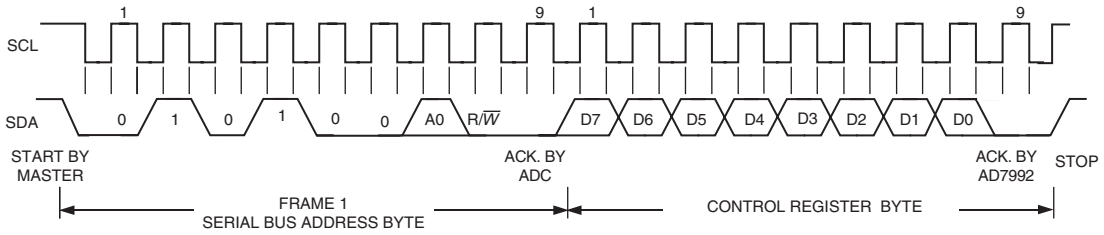


Figure 16.Writing to the AD7991/AD7995/AD7999 Configuration Register

READING FROM THE AD7991/AD7995/AD7999

Reading data from the conversion result register is a 2-byte operation, as shown in Figure 17. Since this register is the only one that a user can read, a read operation is always at least two bytes.

Once the AD7991/AD7995/AD7999 has received a read address any number of reads can be performed from the conversion result register.

Following a start condition, the master writes the 7 bit address of the AD7991/AD7995/AD7999, followed by the R/$\overline{W}$ set to 1. The AD7991/AD7995/AD7999 acknowledges by pulling low the SDA line (A). It then outputs on the I2C bus the conversion result, proceeded by 4 status bits. The status bits are 2 leading zeros, then the channel identifier bits. For the AD7995 there are two trailing zeros and for the AD7999 there are four trailing zeros.

After the master has addressed the AD7991/AD7995/AD7999, the part begins to power up on the 9th SCLK falling edge. After about 0.5us, the input is sampled and a conversion begins. This is done in parallel to the read operation and should not affect the read operation. The master reads back 2 bytes of data. On the 9th SCLK falling edge of the second byte, if the master sends an ACK, this means that the master desires to keep reading back more conversion results, the AD7991/AD7995/AD7999 powers up and performs a second conversion. If the master sends a NO ACK the AD7991/AD7995/AD7999 doesn't power up on the 9th falling edge of SCLK of the second byte. If a further conversion is required the part will convert on the next channel, that is the next channel as selected in the configuration register. See table 10 for Channel selection.

If the master send a NO ACK on the 9th SCLK falling edge of the 2nd byte then the conversion is finished and no further conversion is preformed.

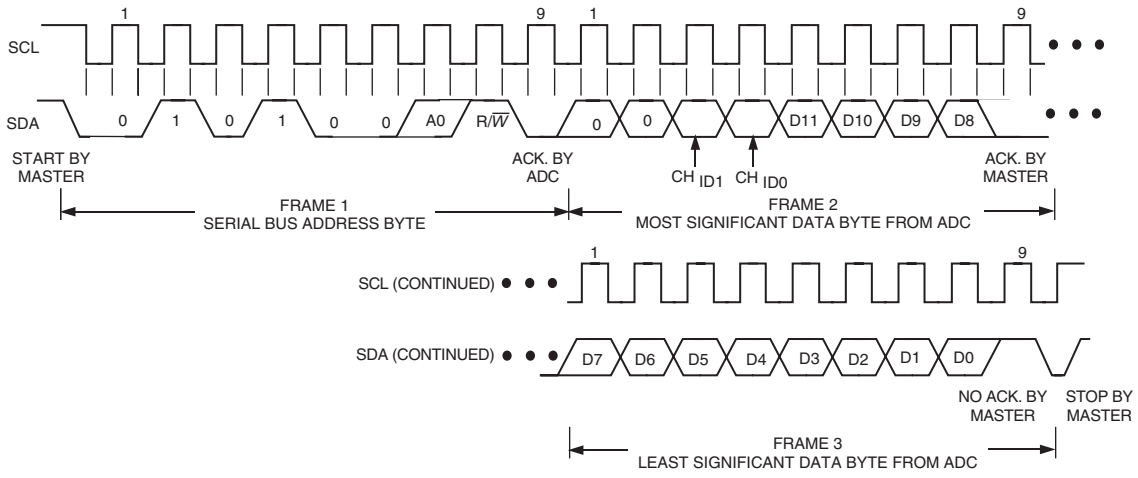


Figure 17. Reading Two Bytes of Data from the Conversion Result Register

PLACING THE AD7991/AD7995/AD7999 INTO HIGH SPEED MODE.

High speed mode communication commences after the master addresses all devices connected to the bus with the master code, 00001XXX, to indicate that a high speed mode transfer is to begin. No device connected to the bus is allowed to acknowledge the high speed master code; therefore, the code is followed by a not-acknowledge (see Figure 18). The master must then issue a repeated start followed by the device address with a R/$\overline{W}$ bit. The selected device then acknowledges its address.

All devices continue to operate in high speed mode until the master issues a STOP condition. When the STOP condition is issued, the devices all return to fast mode.

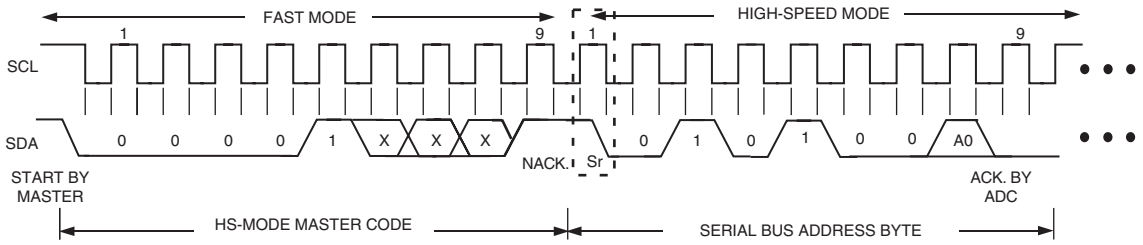


Figure 18. Placing the Part into High Speed Mode

MODE OF OPERATION

The AD7991/AD7995/AD7999 powers up in shut down mode. Once the master addresses the AD7991/AD7995/AD7999 with the correct I²C address the ADC will acknowledge. During this acknowledge the AD7991/AD7995/AD7999 will power up and start a conversion.

During this wake up time the AD7991/AD7995/AD7999 exits shut down mode and begins to acquire the analog input. The channels being converted will depend on the status of the channel bits in the Control register.

After the read address acknowledge the ADC will output two bytes of data. The first byte will contain 4 status bits and the 4 MSBs of the conversion result. The status bits will contain 2 leading zeros and 2 channel identifier bits. After this first byte the AD7991/AD7995/AD7999 will then output the second byte of the conversion result. For the AD7991 this second byte will contain the lower 8 bits of conversion data. For the AD7995 this second byte will contain 6 bits of conversion data plus 2 trailing zeros. For the AD7999 this second byte will contain 4 bits of conversion data and 4 trailing zeros.

The master will then send a NAK to the AD7991/AD7995/AD7999 if no further reads are required. If the master does not issue a NAK and sends an ACK to the AD7991/AD7995/AD7999 the ADC will once again power up and complete a conversion. If more than one channel bit has been set in the control register then this conversion will be preformed on the second channel in the selected sequence. If only one channel was selected the ADC will convert again on the selected channel.

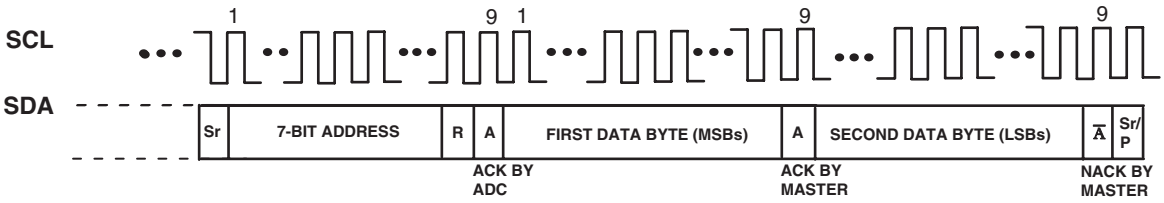
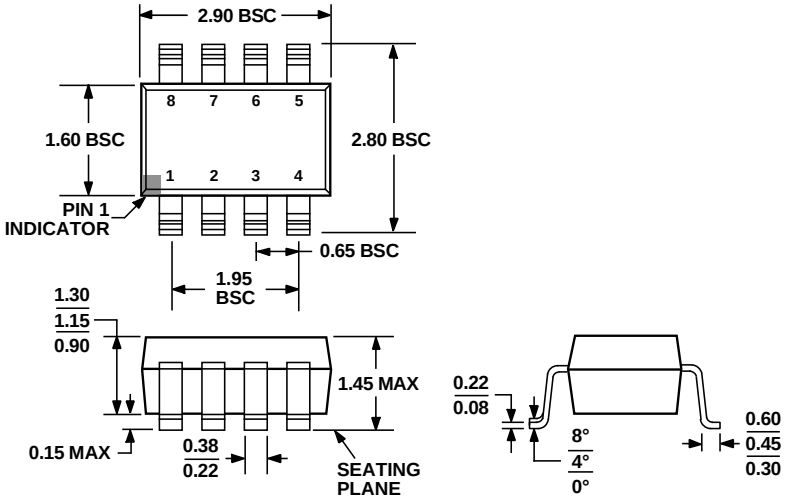


Figure 19. Mode Of Operation

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-178-BA

Figure 20.8-Lead Small Outline Transistor Package (SOT-23)
(RJ-8)
Dimensions shown in millimeter

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7991BRJZ-1[1]	-40°C to 85° C	8-LEAD SOT-23	
AD7991BRJZ-0[1]	-40°C to 85° C	8-LEAD SOT-23	
AD7991YRJZ-1[1]	-40°C to 125° C	8-LEAD SOT-23	
AD7991YRJZ-0[1]	-40°C to 125° C	8-LEAD SOT-23	
AD7995YRJZ-1[1]	-40°C to 125° C	8-LEAD SOT-23	
AD7995YRJZ-0[1]	-40°C to 125° C	8-LEAD SOT-23	
AD7999YRJZ-1[1]	-40°C to 125° C	8-LEAD SOT-23	
AD7999YRJZ-0[1]	-40°C to 125° C	8-LEAD SOT-23	

[1] Z = Pb-free part.

PR06461-0-10/06(PrB)