10-Bit, 170/200 MSPS 3.3 V A/D Converter

AD9411

FEATURES

SNR = 60 dB @ f_{IN} up to 70 MHz @ 200 MSPS
ENOB of 9.8 @ f_{IN} up to 70 MHz @ 200 MSPS (–0.5 dBFS)
SFDR = 80 dBc @ f_{IN} up to 70 MHz @ 200 MSPS (–0.5 dBFS)
Excellent linearity:
- **DNL = ±0.15 LSB (typical)**
- **INL = ±0.25 LSB (typical)**

LVDS output levels
700 MHz full-power analog bandwidth
On-chip reference and track-and-hold
Power dissipation = 1.25 W typical @ 200 MSPS
1.5 V input voltage range
3.3 V supply operation
Output data format option
Clock duty cycle stabilizer
Pin compatible to LVDS mode AD9430

APPLICATIONS

Wireless and wired broadband communications
Cable reverse path
Communications test equipment
Radar and satellite subsystems
Power amplifier linearization

FUNCTIONAL BLOCK DIAGRAM

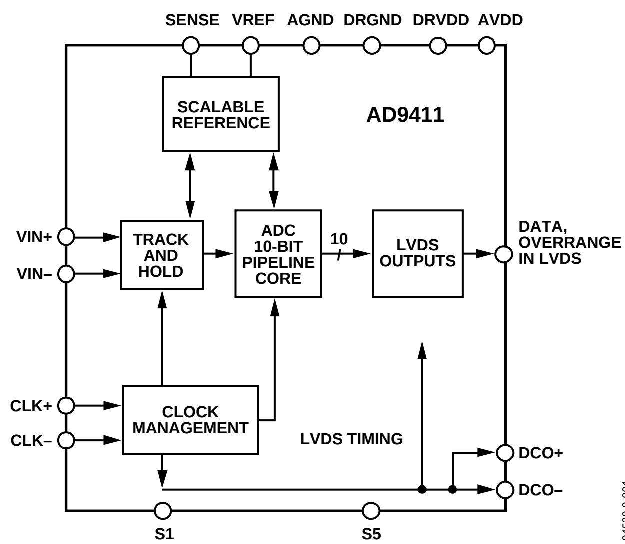

Figure 1.

GENERAL DESCRIPTION

The AD9411 is a 10-bit monolithic sampling analog-to-digital converter optimized for high performance, low power, and ease of use. The product operates up to a 200 MSPS conversion rate and is optimized for outstanding dynamic performance in wideband carrier and broadband systems. All necessary functions, including track-and-hold (T/H) and reference, are included on the chip to provide a complete conversion solution.

The ADC requires a 3.3 V power supply and a differential sample clock for full performance operation. The digital outputs are LVDS compatible and support both twos complement and offset binary format. A data clock output is available to ease data capture.

Fabricated on an advanced BiCMOS process, the AD9411 is available in a 100-lead surface-mount plastic package (e-PAD TQFP-100) specified over the industrial temperature range (–40°C to +85°C).

PRODUCT HIGHLIGHTS

1. High performance.
   Maintains 60 dB SNR @ 200 MSPS with a 70 MHz input.
2. Low power.
   Consumes only 1.25 W @ 200 MSPS.
3. Ease of use.
   LVDS output data and output clock signal allow interface to current FPGA technology. The on-chip reference and sample-and-hold function provide flexibility in system design. Use of a single 3.3 V supply simplifies system power supply design.
4. Out-of-range (OR).
   The OR output bit indicates when the input signal is beyond the selected input range.

Rev. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.326.8703

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REVISION HISTORY

7/04—Data Sheet Changed from Rev. 0 to Rev. A

Added 200 MSPS Grade ... Universal
Updated Outline Dimensions ... 27
Changes to Ordering Guide ... 27

Rev 0 : Initial Version

DC SPECIFICATIONS

AVDD = 3.3 V, DRVDD = 3.3 V, T_{MIN} = −40°C, T_{MAX} = +85°C, f_{IN} = −0.5 dBFS, internal reference, full scale = 1.536 V, unless otherwise noted.

Table 1.

Parameter	Temp	Test Level	AD9411-170 Min	AD9411-170 Typ	AD9411-170 Max	AD9411-200 Min	AD9411-200 Typ	AD9411-200 Max	Unit
RESOLUTION				12			12		Bits
ACCURACY									
No Missing Codes	Full	VI	Guaranteed			Guaranteed			
Offset Error	25°C	I	−3		+3	−3		+3	mV
Gain Error	25°C	I	−5		+5	−5		+5	% FS
Differential Nonlinearity (DNL)	25°C	I	−0.5	± 0.15	+0.5	−0.5	± 0.15	+0.5	LSB
	Full	VI	−0.6	± 0.25	+0.6	−0.6	± 0.25	+0.6	LSB
Integral Nonlinearity (INL)	25°C	I	−0.8	± 0.5	+0.8	−0.8	± 0.5	+0.8	LSB
	Full	VI	−1	± 0.5	+1	−1	± 0.5	+1	LSB
TEMPERATURE DRIFT									
Offset Error	Full	V		58			58		μV/°C
Gain Error	Full	V		0.02			0.02		%/°C
Reference Out (VREF)	Full	V		+0.12/ −0.24			+0.12/ −0.24		mV/°C
REFERENCE									
Reference Out (VREF)	25°C	I	1.15	1.235	1.3	1.15	1.235	1.3	V
Output Current[1]	25°C	IV			3.0			3.0	mA
I_{VREF} Input Current[2]	25°C	I			20			20	mA
I_{SENSE} Input Current	25°C	I		1.6	5.0		1.6	5.0	mA
ANALOG INPUTS (VIN+, VIN−)[3]									
Differential Input Voltage Range (S5 = GND)	Full	V		1.536			1.536		V
Differential Input Voltage Range (S5 = AVDD)	Full	V		0.766			0.766		V
Input Common-Mode Voltage	Full	VI	2.65	2.8	2.9	2.65	2.8	2.9	V
Input Resistance	Full	VI	2.2	3	3.8	2.2	3	3.8	kΩ
Input Capacitance	25°C	V		5			5		pF
POWER SUPPLY (LVDS Mode)									
AVDD	Full	IV	3.1	3.3	3.6	3.2	3.3	3.6	V
DRVDD	Full	IV	3.0	3.3	3.6	3.0	3.3	3.6	V
Supply Currents									
I_{ANALOG} (AVDD = 3.3 V)[4]	Full	VI		335	372		385	425	mA
$I_{DIGITAL}$ (DRVDD = 3.3 V)	Full	VI		49	57		49	57	mA
Power Dissipation	Full	VI		1.27	1.42		1.43	1.59	W
Power Supply Rejection	25°C	V		−7.5			−7.5		mV/V

[1] Internal reference mode; SENSE = floats.
[2] External reference mode; SENSE = DRVDD; VREF driven by external 1.23 V reference.
[3] S5 (Pin 1) = GND. See the Analog Input section. S5 = GND in all dc, ac tests, unless otherwise specified
[4] I_{AVDD} and I_{DRVDD} are measured with an analog input of 10.3 MHz, −0.5 dBFS, sine wave, rated clock rate, and in LVDS output mode. See the Typical Performance Characteristics and Application Notes sections for I_{DRVDD}. Power consumption is measured with a dc input at rated clock rate in LVDS output mode.

AC SPECIFICATIONS[1]

AVDD = 3.3 V, DRVDD = 3.3 V, T_{MIN} = −40°C, T_{MAX} = +85°C, f_{IN} = −0.5 dBFS, internal reference, full scale = 1.536 V, unless otherwise noted.

Table 2.

			AD9411-170			AD9411-200			
Parameter	**Temp**	**Test Level**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SNR									
Analog Input @ –0.5 dBFS									
10 MHz	25°C	I	59	60.2		59	60.2		dB
70 MHz	25°C	I	59	60.1		59	60.1		dB
100 MHz	25°C	V		60			60		dB
240 MHz	25°C	V		59.1			59.1		dB
SINAD									
Analog Input @ –0.5 dBFS									
10 MHz	25°C	I	58.5	60		58.5	60		dB
70 MHz	25°C	I	58.5	60		58.5	60		dB
100 MHz	25°C	V		59.5			59.5		dB
240 MHz	25°C	V		57.5			57.5		dB
EFFECTIVE NUMBER OF BITS (ENOB)									
10 MHz	25°C	I	9.5	9.8		9.5	9.8		Bits
70 MHz	25°C	I	9.5	9.8		9.5	9.8		Bits
100 MHz	25°C	V		9.7			9.7		Bits
240 MHz	25°C	V		9.3			9.3		Bits
WORST HARMONIC (Second or Third)									
Analog Input @ –0.5 dBFS 10 MHz									
10 MHz	25°C	I		–80	–73		–80	–70	dBc
70 MHz	25°C	I		–80	–73		–80	–70	dBc
100 MHz	25°C	V		–74			–74		dBc
240 MHz	25°C	V		–69			–69		dBc
WORST HARMONIC (Fourth or Higher)									
Analog Input @ –0.5 dBFS 10 MHz									
10 MHz	25°C	I		–82	–75		–82	–75	dBc
70 MHz	25°C	I		–82	–75		–82	–75	dBc
100 MHz	25°C	V		–76			–76		dBc
240 MHz	25°C	V		–70			–70		dBc
TWO-TONE IMD[2]									
F1, F2 @ –7 dBFS	25°C	V		70			70		dBc
ANALOG INPUT BANDWIDTH	25°C	V		700			700		MHz

[1] All ac specifications tested by driving CLK+ and CLK– differentially.
[2] F1 = 30.5 MHz, F2 = 31 MHz.

DIGITAL SPECIFICATIONS

AVDD = 3.3 V, DRVDD = 3.3 V, T_{MIN} = −40°C, T_{MAX} = +85°C, unless otherwise noted.

Table 3.

			AD9411-170			AD9411-200			
Parameter	**Temp**	**Test Level**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
CLOCK INPUTS (CLK+, CLK–)[1]									
Differential Input Voltage[2]	Full	IV	0.2			0.2			V
Common-Mode Voltage[3]	Full	VI	1.375	1.5	1.575	1.375	1.5	1.575	V
Input Resistance	Full	VI	3.2	5.5	6.5	3.2	5.5	6.5	kΩ
Input Capacitance	25°C	V		4			4		pF
LOGIC INPUTS (S1, S2, S4, S5)									
Logic 1 Voltage	Full	IV	2.0			2.0			V
Logic 0 Voltage	Full	IV			0.8			0.8	V
Logic 1 Input Current	Full	VI			190			190	µA
Logic 0 Input Current	Full	VI			10			10	µA
Input Resistance	25°C	V		30			30		kΩ
Input Capacitance	25°C	V		4			4		pF
LVDS LOGIC OUTPUTS[4]									
V_{OD} Differential Output Voltage	Full	VI	247		454	247		454	mV
V_{OS} Output Offset Voltage	Full	VI	1.125		1.375	1.125		1.375	V
Output Coding			Twos Complement or Binary			Twos Complement or Binary			

[1] See the Equivalent Circuits section.
[2] All ac specifications tested by driving CLK+ and CLK– differentially, |(CLK+) – (CLK–)| > 200 mV.
[3] Clock inputs' common mode can be externally set, such that 0.9 V < CLK± < 2.6 V.
[4] LVDS R_{TERM} = 100 Ω, LVDS output current set resistor (R_{SET}) = 3.74 kΩ (1% tolerance).

SWITCHING SPECIFICATIONS

AVDD = 3.3 V, DRVDD = 3.3 V, T_{MIN} = −40°C, T_{MAX} = +85°C, unless otherwise noted.

Table 4.

			AD9411-170			AD9411-200			
Parameter (Conditions)	**Temp**	**Test Level**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Maximum Conversion Rate[1]	Full	VI	170			200			MSPS
Minimum Conversion Rate	Full	V			40			40	MSPS
CLK+ Pulse Width High (t_{EH})	Full	IV	2		12.5	2		12.5	ns
CLK+ Pulse Width Low (t_{EL})	Full	IV	2		12.5	2		12.5	ns
OUTPUT (LVDS Mode)									
Valid Time (t_V)	Full	VI	2.0			2.0			ns
Propagation Delay (t_{PD})	Full	VI		3.2	4.3		3.2	4.3	ns
Rise Time (t_R) (20% to 80%)	25°C	V		0.5			0.5		ns
Fall Time (t_F) (20% to 80%)	25°C	V		0.5			0.5		ns
DCO Propagation Delay (t_{CPD})	Full	VI	1.8	2.7	3.8	1.8	2.7	3.8	ns
Data to DCO Skew ($t_{PD}–t_{CPD}$)	Full	IV	0.2	0.5	0.8	0.2	0.5	0.8	ns
Latency	Full	IV		14			14		Cycles
Aperture Delay (t_A)	25°C	V		1.2			1.2		ns
Aperture Uncertainty (Jitter, t_J)	25°C	V		0.25			0.25		ps rms
Out-of-Range Recovery Time	25°C	V			1			1	Cycles

[1] All ac specifications tested by driving CLK+ and CLK– differentially.

EXPLANATION OF TEST LEVELS

I. 100% production tested.

II. 100% production tested at 25°C and sample tested at specified temperatures.

III. Sample tested only.

IV. Parameter is guaranteed by design and characterization testing.

V. Parameter is a typical value only.

VI. 100% production tested at 25°C; guaranteed by design and characterization testing for industrial temperature range; 100% production tested at temperature extremes for military devices.

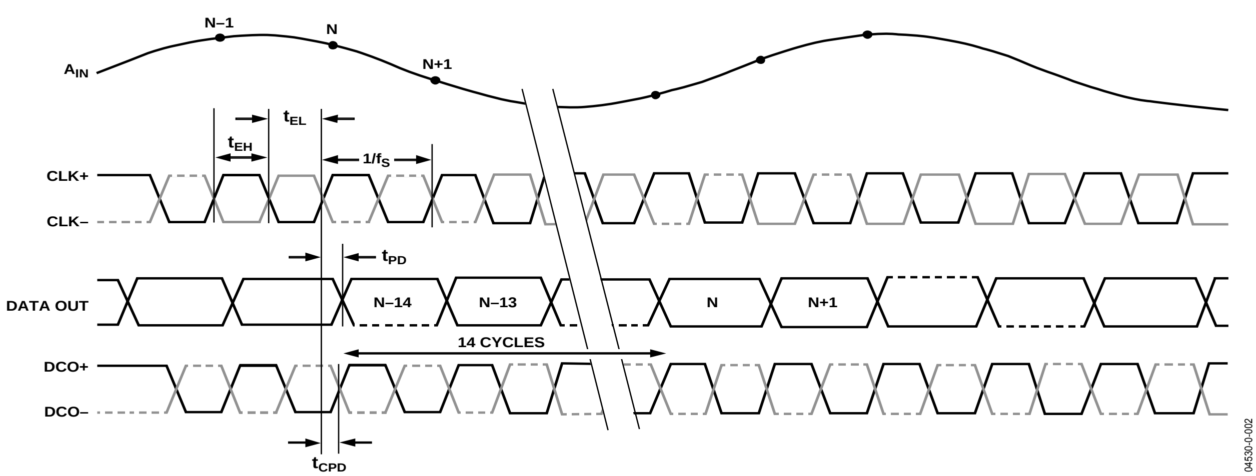


Figure 2. LVDS Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
AVDD, DRVDD	4 V
Analog Inputs	–0.5 V to AVDD +0.5 V
Digital Inputs	–0.5 V to DRVDD +0.5 V
REFIN Inputs	–0.5 V to AVDD +0.5 V
Digital Output Current	20 mA
Operating Temperature	–55ºC to +125°C
Storage Temperature	–65ºC to +150°C
Maximum Junction Temperature	150°C
Maximum Case Temperature	150°C
θ_{JA}[1]	25°C/W, 32°C/W

[1] Typical θ_{JA} = 32°C/W (heat slug not soldered); typical θ_{JA} = 25°C/W (heat slug soldered) for multilayer board in still air with solid ground plane.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside of those indicated in the operation section of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

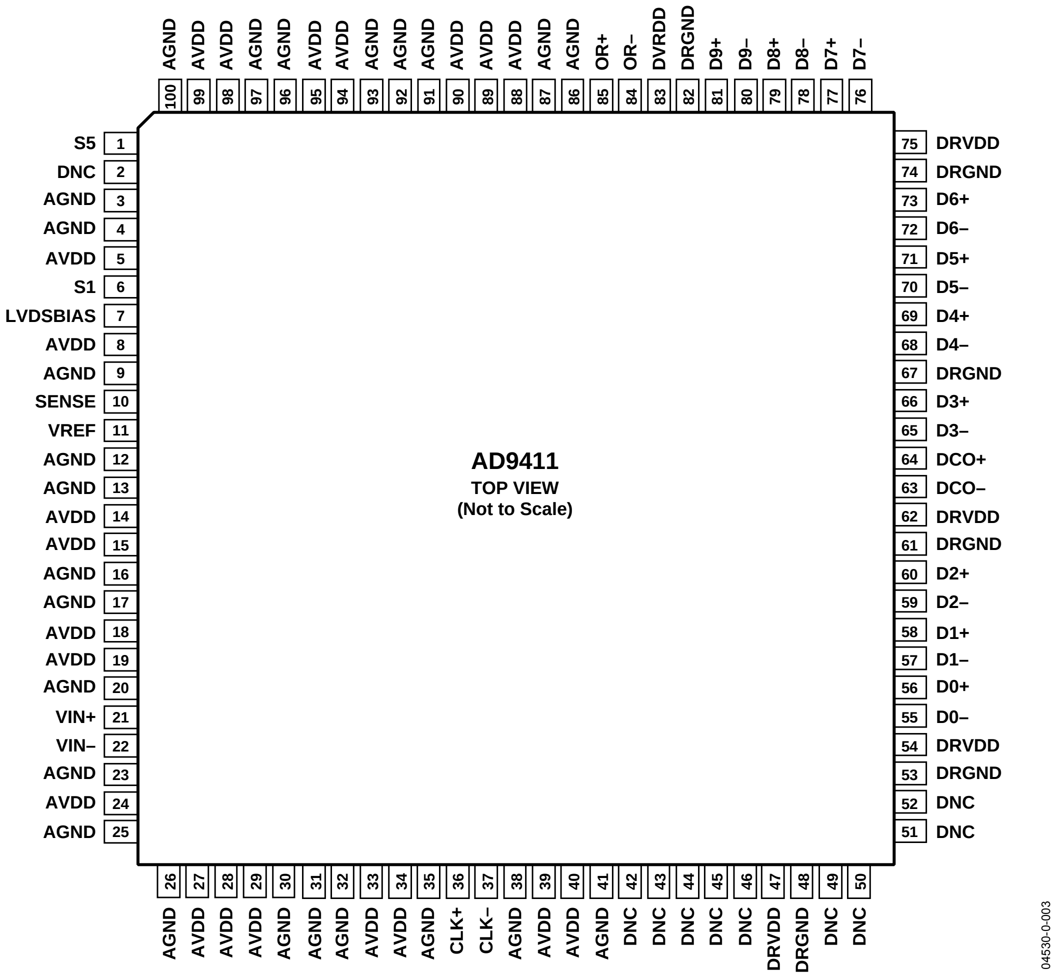


Figure 3. TQFP/EP Pinout

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	S5	Full-Scale Adjust Pin. AVDD sets FS = 0.768 V p-p differential; GND sets FS = 1.536 V p-p differential.
2, 42–46,49–52	DNC	Do Not Connect.
3, 4, 9, 12, 13, 16, 17, 20, 23, 25, 26, 30, 31, 32, 35, 38, 41, 86, 87, 91, 92, 93, 96, 97, 100	AGND	Analog Ground. AGND and DRGND should be tied together to a common ground plane.
5, 8, 14, 15, 18, 19, 24, 27, 28, 29, 33, 34, 39, 40, 88, 89, 90, 94, 95, 98, 99	AVDD	3.3 V Analog Supply.
6	S1	Data Format Select. GND = binary; AVDD = twos complement.
7	LVDSBIAS	Set Pin for LVDS Output Current. Place a 3.74 kΩ resistor terminated to ground.
10	SENSE	Reference Mode Select Pin. Float for internal reference operation.
11	VREF	1.235 V Reference Input/Output. Function depends on SENSE.
21	VIN+	Analog Input. True.
22	VIN–	Analog Input. Complement.
36	CLK+	Clock Input. True (LVPECL levels).
37	CLK–	Clock Input. Complement (LVPECL levels).
47, 54, 62, 75, 83	DRVDD	3.3 V Digital Output Supply (3.0 V to 3.6 V).
48, 53, 61, 67, 74, 82	DRGND	Digital Output Ground. AGND and DRGND should be tied together to a common ground plane.
56	D0+	D0 True Output Bit.
57	D1–	D1 Complement Output Bit.
58	D1+	D1 True Output Bit.
59	D2–	D2 Complement Output Bit.
60	D2+	D2 True Output Bit.
63	DCO–	Data Clock Output. Complement.
64	DCO+	Data Clock Output. True.
65	D3–	D3 Complement Output Bit.
66	D3+	D3 True Output Bit.
68	D4–	D4 Complement Output Bit.
69	D4+	D4 True Output Bit.
70	D5–	D5 Complement Output Bit.
71	D5+	D5 True Output Bit.
72	D6–	D6 Complement Output Bit.
73	D6+	D6 True Output Bit.
76	D7–	D7 Complement Output Bit.
77	D7+	D7 True Output Bit.
78	D8–	D8 Complement Output Bit.
79	D8+	D8 True Output Bit.
80	D9–	D9 Complement Output Bit.
81	D9+	D9 True Output Bit.
84	OR–	Overrange Complement Output Bit.
85	OR+	Overrange True Output Bit.

TERMINOLOGY

Analog Bandwidth

The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay

The delay between the 50% point of the rising edge of the clock command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay.

Crosstalk

Coupling onto one channel being driven by a low level (–40 dBFS) signal when the adjacent interfering channel is driven by a full-scale signal.

Differential Analog Input Resistance, Differential Analog Input Capacitance, and Differential Analog Input Impedance

The real and complex impedances measured at each analog input port. The resistance is measured statically and the capacitance and differential input impedances are measured with a network analyzer.

Differential Analog Input Voltage Range

The peak-to-peak differential voltage that must be applied to the converter to generate a full-scale response. Peak differential voltage is computed by observing the voltage on a single pin and subtracting the voltage from the other pin, which is 180° out of phase. Peak-to-peak differential is computed by rotating the input's phase 180° and again taking the peak measurement. The difference is then computed between both peak measurements.

Differential Nonlinearity

The deviation of any code width from an ideal 1 LSB step.

Effective Number of Bits (ENOB)

Calculated from the measured SNR based on the equation

$$ENOB = \frac{SNR_{MEASURED} - 1.76\ \text{dB}}{6.02}$$

Clock Pulse Width/Duty Cycle

Pulse width high is the minimum amount of time the clock pulse should be left in the Logic 1 state to achieve rated performance; pulse width low is the minimum time the clock pulse should be left in the low state. Refer to the timing implications of changing t_{ENCH} in the Application Notes, Clock Input section. At a given clock rate, these specifications define an acceptable CLOCK duty cycle.

Full-Scale Input Power

Expressed in dBm. Computed using the following equation:

$$Power_{FULLSCALE} = 10\log\left(\frac{\frac{V^2_{FULLSCALE\ RMS}}{Z_{INPUT}}}{0.001}\right)$$

Gain Error

The difference between the measured and ideal full-scale input voltage range of the ADC.

Harmonic Distortion, Second

The ratio of the rms signal amplitude to the rms value of the second harmonic component, reported in dBc.

Harmonic Distortion, Third

The ratio of the rms signal amplitude to the rms value of the third harmonic component, reported in dBc.

Integral Nonlinearity

The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least square curve fit.

Minimum Conversion Rate

The CLOCK rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate

The CLOCK rate at which parametric testing is performed.

Output Propagation Delay

The delay between a differential crossing of CLK+ and CLK– and the time when all output data bits are within valid logic levels.

Noise (for Any Range within the ADC)

Calculated as follows:

$$V_{NOISE} = \sqrt{Z \times 0.001 \times 10^{\left(\frac{FS_{dBM} - SNR_{dBc} - Signal_{dBFS}}{10}\right)}}$$

where *Z* is the input impedance, *FS* is the full scale of the device for the frequency in question, *SNR* is the value of the particular input level, and *Signal* is the signal level within the ADC reported in dB below full scale. This value includes both thermal and quantization noise.

Power Supply Rejection Ratio (PSRR)

The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise-and-Distortion (SINAD)

The ratio of the rms signal amplitude (set 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics but excluding dc.

Signal-to-Noise Ratio (without Harmonics)

The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

Spurious-Free Dynamic Range (SFDR)

The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. May be reported in dBc (i.e., degrades as signal level is lowered) or dBFS (always related back to converter full scale).

Two-Tone Intermodulation Distortion Rejection

The ratio of the rms value of either input tone to the rms value of the worst third-order intermodulation product, reported in dBc.

Two-Tone SFDR

The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. May be reported in dBc (i.e., degrades as signal level is lowered) or in dBFS (always related back to converter full scale).

Worst Other Spur

The ratio of the rms signal amplitude to the rms value of the worst spurious component (excluding the second and third harmonics) reported in dBc.

Transient Response Time

The time it takes for the ADC to reacquire the analog input after a transient from 10% above negative full scale to 10% below positive full scale.

Out-of-Range Recovery Time

The time it takes for the ADC to reacquire the analog input after a transient from 10% above positive full scale to 10% above negative full scale, or from 10% below negative full scale to 10% below positive full scale.

EQUIVALENT CIRCUITS

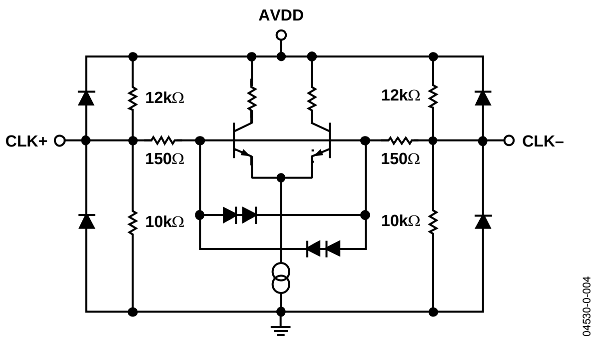


Figure 4. Clock Inputs

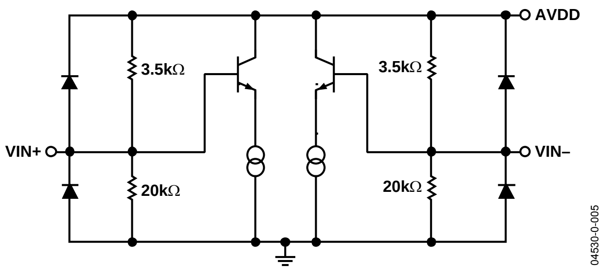


Figure 5. Analog Inputs

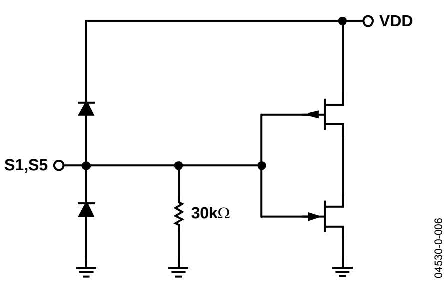


Figure 6. S1 to S5 Inputs

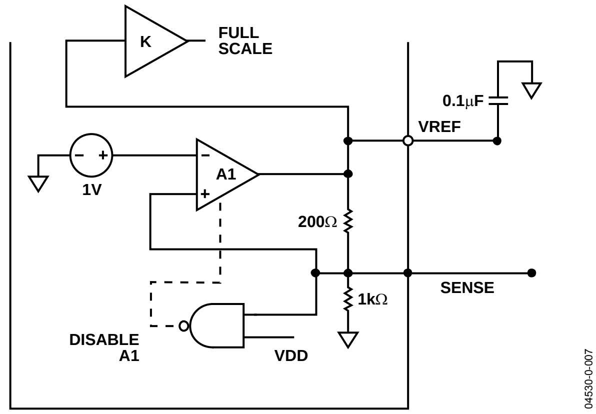


Figure 7. VREF, SENSE I/O

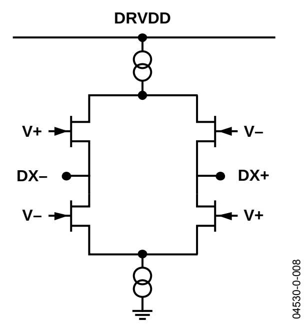


Figure 8. Data Outputs

TYPICAL PERFORMANCE CHARACTERISTICS

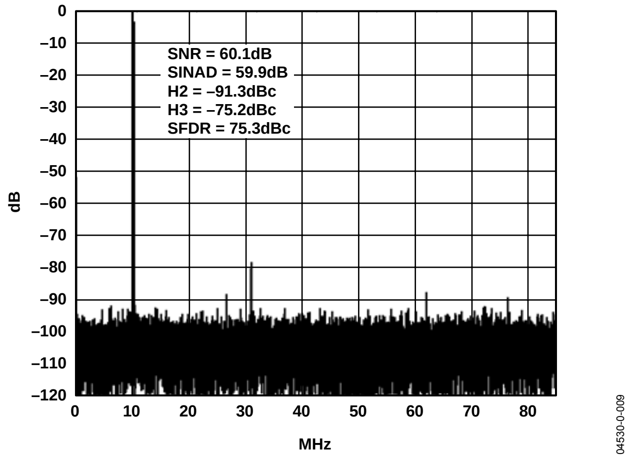


Figure 9. FFT: fS = 170 MSPS, AIN = 10.3 MHz @ –0.5 dBFS

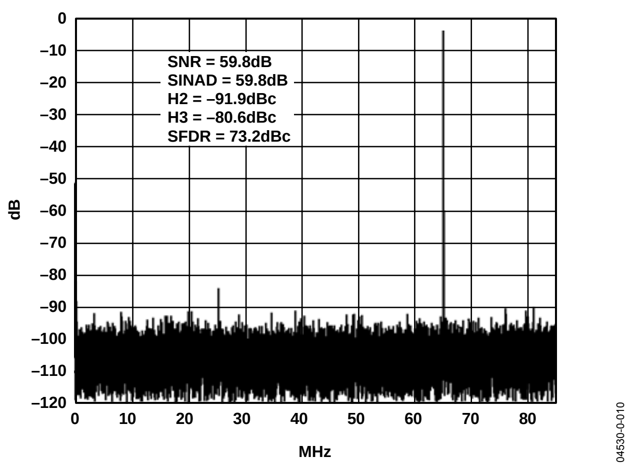


Figure 10. FFT: fS = 170 MSPS, AIN = 65 MHz @ –0.5 dBFS

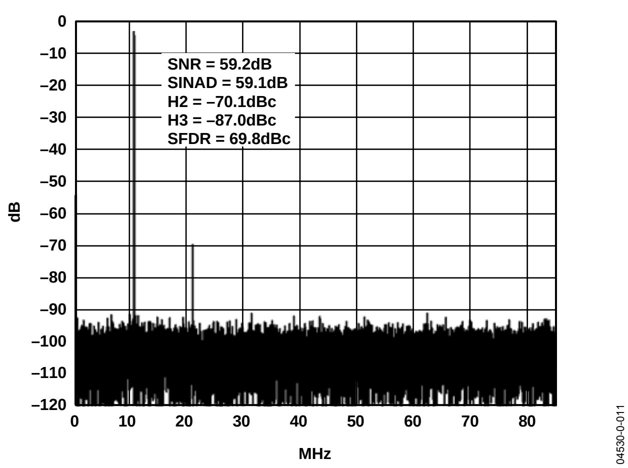


Figure 11. FFT: fS = 170 MSPS, AIN = 10.3, MHz @ –0.5 dBFS, Single-Ended Input, 0.76 V Input Range

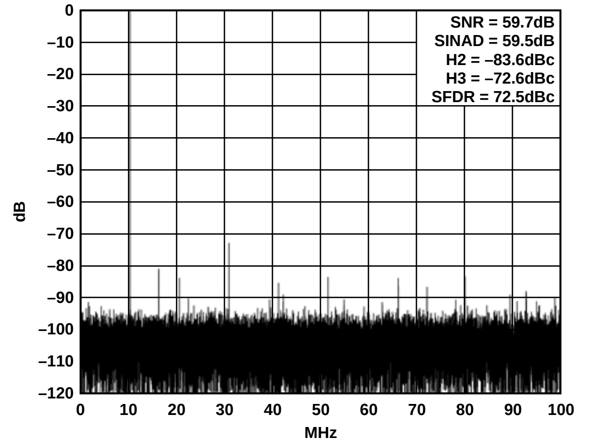


Figure 12. FFT: fS = 200 MSPS, AIN = 10.3 MHz @ –0.5 dBFS

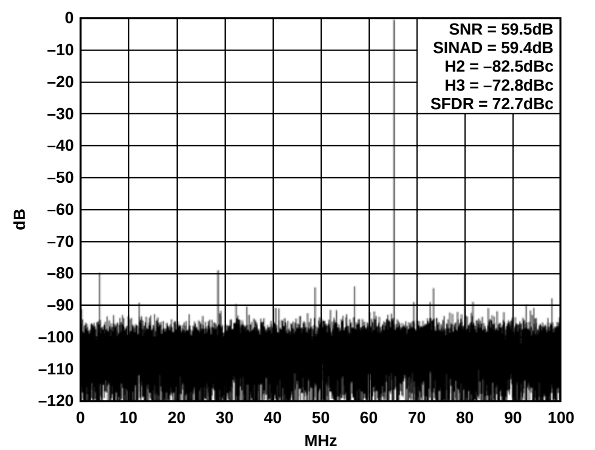


Figure 13. FFT: fS = 200 MSPS, AIN = 65 MHz @ –0.5 dBFS

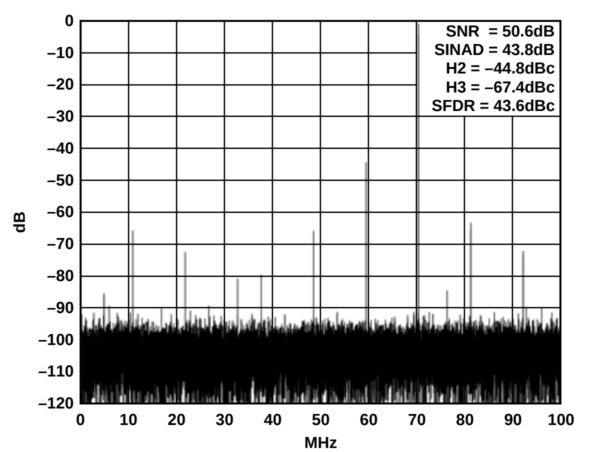


Figure 14. FFT: fS = 200 MSPS, AIN = 70 MHz @ –0.5 dBFS, Single-Ended Drive, 1.5 V Input Range

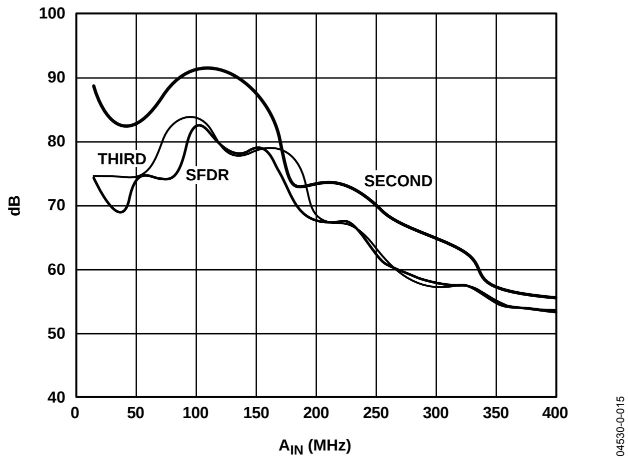


Figure 15. Harmonic Distortion (Second and Third) and SFDR vs. AIN Frequency @ 170 MSPS

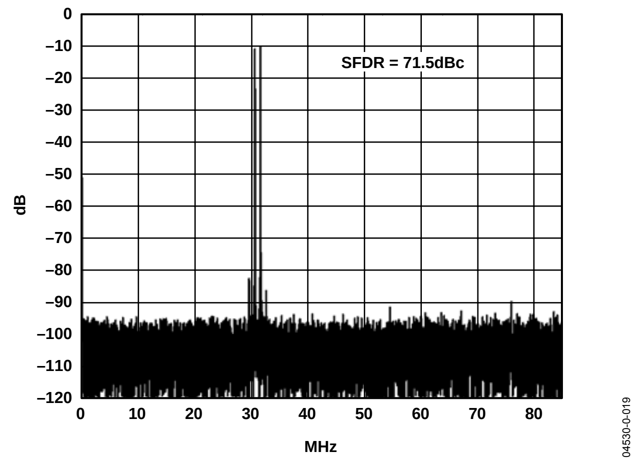


Figure 18. Two-Tone Intermodulation Distortion (30.5 MHz and 31.0 MHz; fS = 170 MSPS)

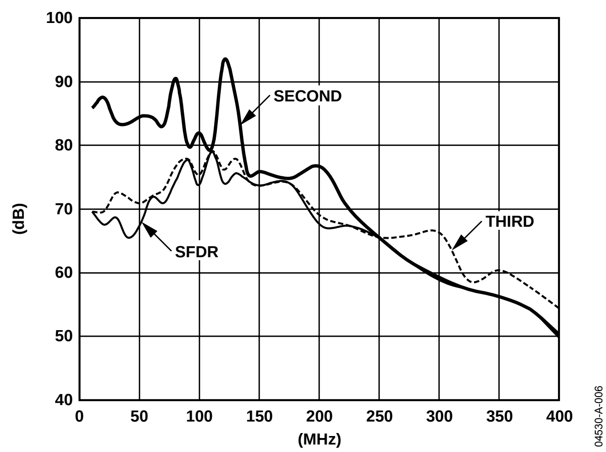


Figure 16. Harmonic Distortion (Second and Third) and SFDR vs. AIN Frequency @ 200 MSPS

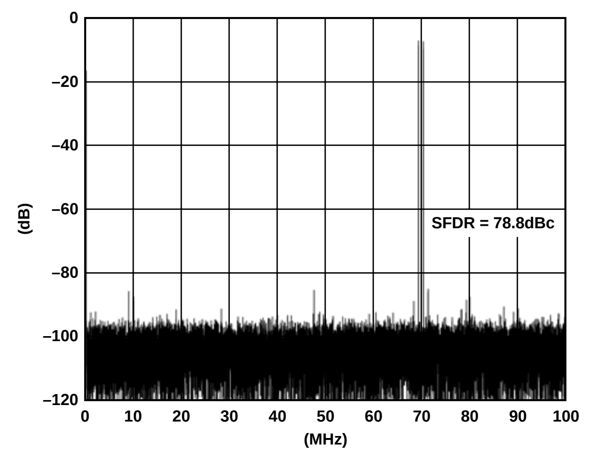


Figure 19. Two-Tone Intermodulation Distortion (69.3 MHz and 70.3 MHz; fS = 200 MSPS)

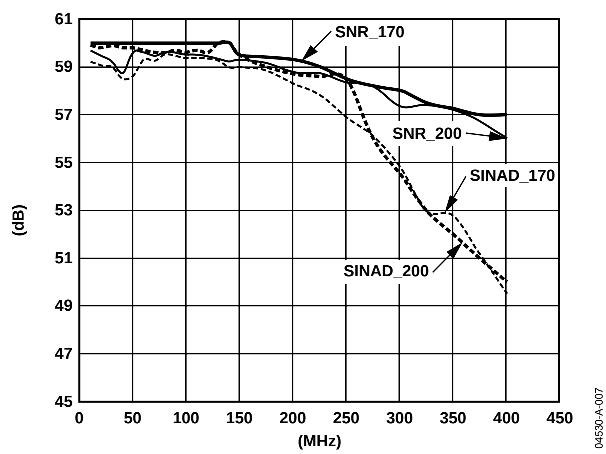


Figure 17. SNR and SINAD vs. AIN Frequency; fS = 170/200 MSPS, AIN @ –0.5 dBFS Full Scale = 1.536 V

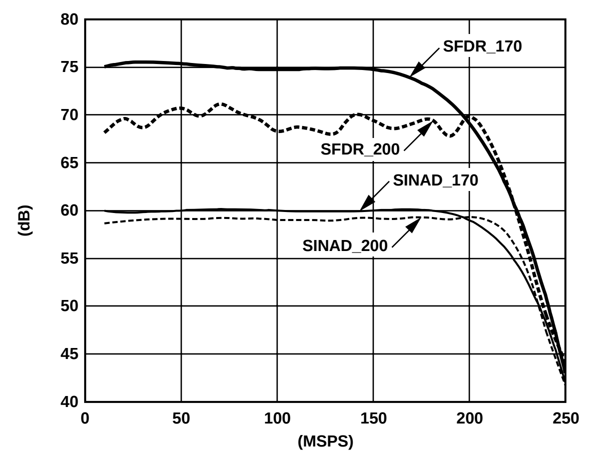


Figure 20. SINAD and SFDR vs. Clock Rate (AIN = 10.3 MHz @ –0.5 dBFS) 170/200 grade

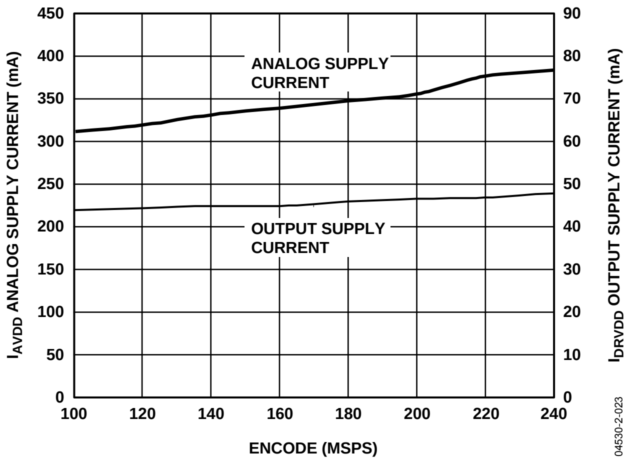


Figure 21. IAVDD and IDRVDD vs. Clock Rate, 170 MSPS Grade, CLOAD = 5 pF (AIN = 10.3 MHz @ −0.5 dBFS)

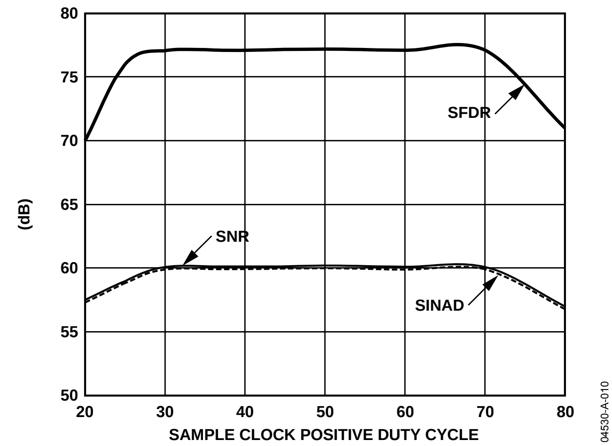


Figure 24. SINAD and SFDR vs. Clock Pulse Width High (AIN = 10.3 MHz @ −0.5 dBFS, 200 MSPS)

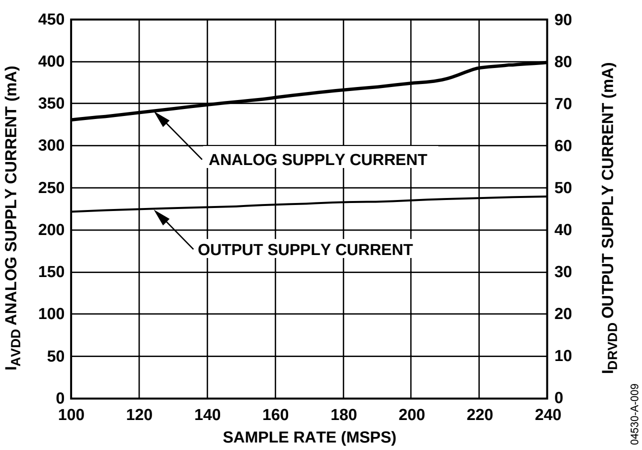


Figure 22. IAVDD and IDRVDD vs. Clock Rate, 200 MSPS Grade, CLOAD = 5 pF (AIN = 10.3 MHz @ −0.5 dBFS)

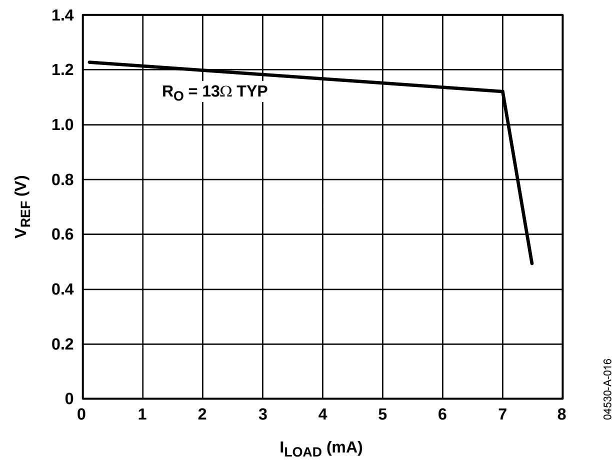


Figure 25. VREFOUT vs. ILOAD (Both Speed Grades)

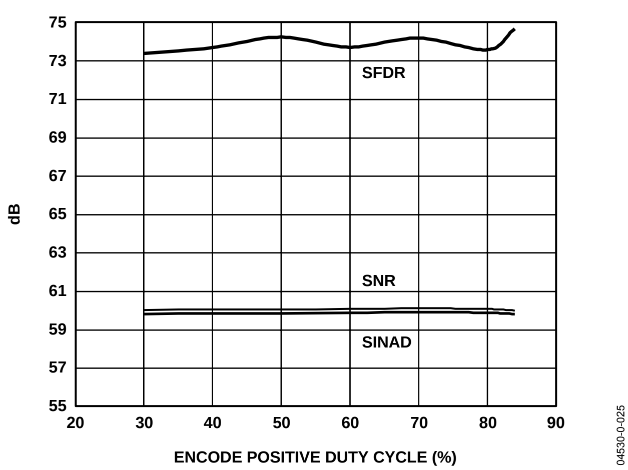


Figure 23. SINAD and SFDR vs. Clock Pulse Width High (AIN = 10.3 MHz @ −0.5 dBFS, 170 MSPS)

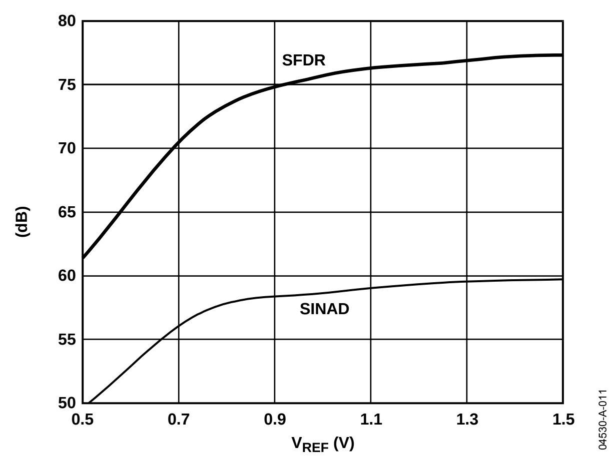


Figure 26. Sinad, SFDR vs. VREF in External Reference Mode (AIN = 70 MHz @ −0.5 dBFS, 200 MSPS)

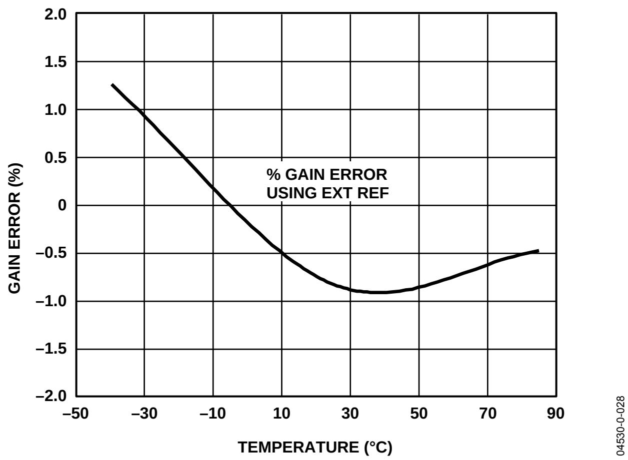


Figure 27. Full-Scale Gain Error vs. Temperature (AIN = 10.3 MHz @ −0.5 dBFS, 170/200 MSPS)

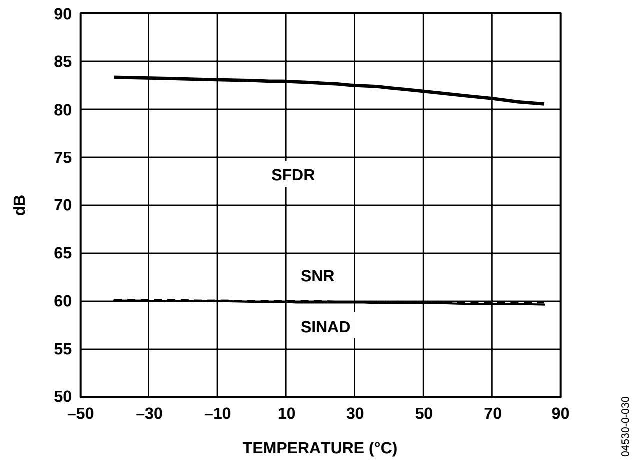


Figure 30. SNR, SINAD, and SFDR vs. Temperature (AIN = 10.3 MHz @ −0.5 dBFS, 170 MSPS)

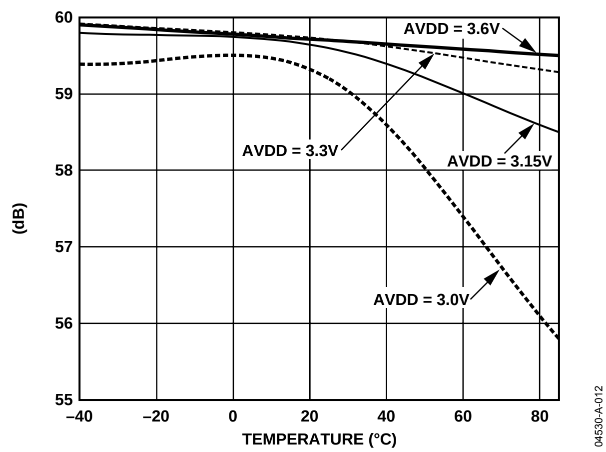


Figure 28. SINAD vs. Temperature and AVDD (AIN = 10.3 MHz @ −0.5 dBFS, 200 MSPS)

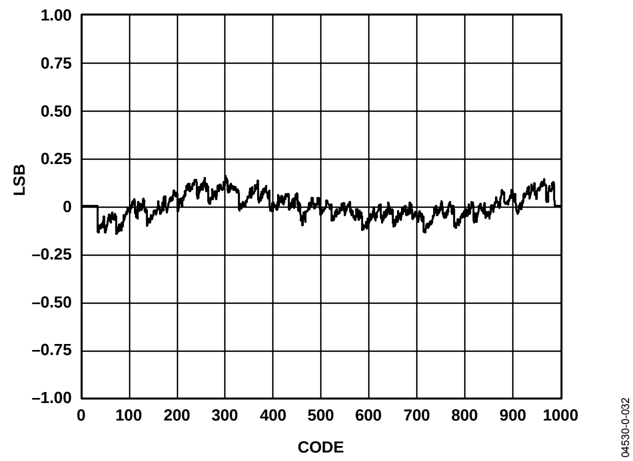


Figure 31. Typical INL Plot (AIN = 10.3 MHz @ −0.5 dBFS, 170/200 MSPS)

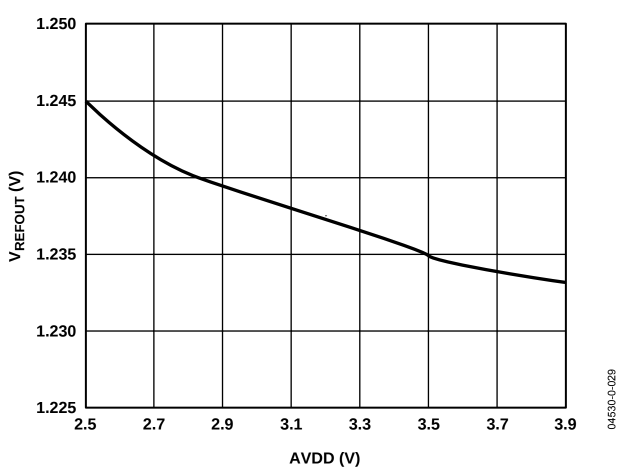


Figure 29. VREF Output Voltage vs. AVDD (Both Speed Grades)

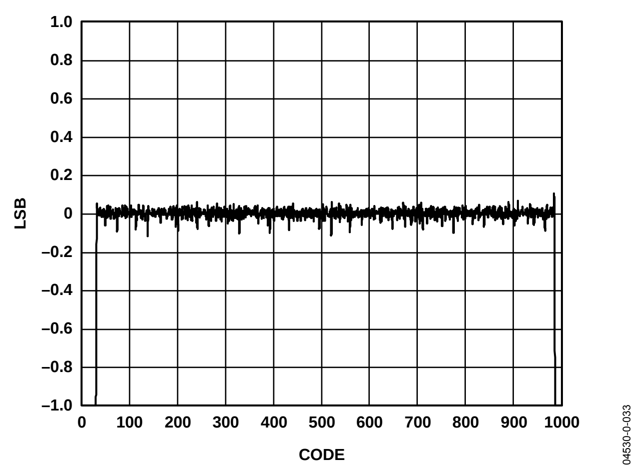


Figure 32. Typical DNL Plot (AIN = 10.3 MHz @ −0.5 dBFS) 170/200 MSPS

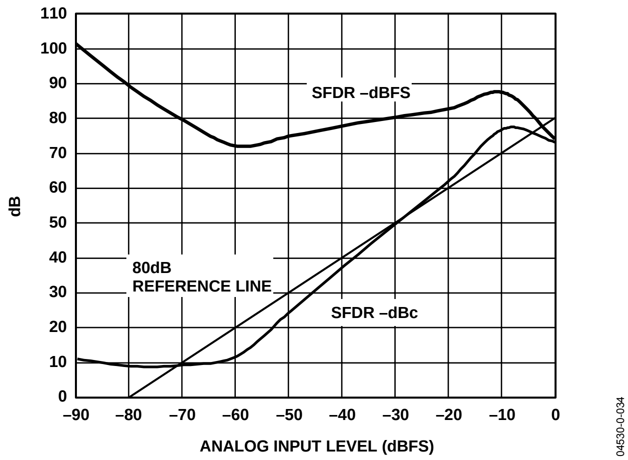


Figure 33. SFDR vs. AIN Input Level 10.3 MHz, AIN @ 170 MSPS

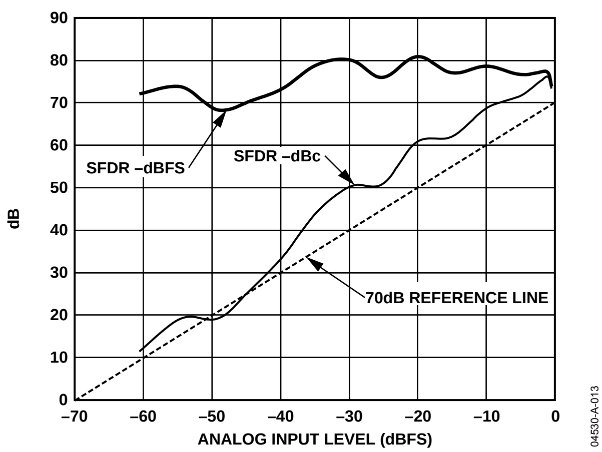


Figure 34. SFDR vs. AIN Input Level 70 MHz, AIN @ 200 MSPS

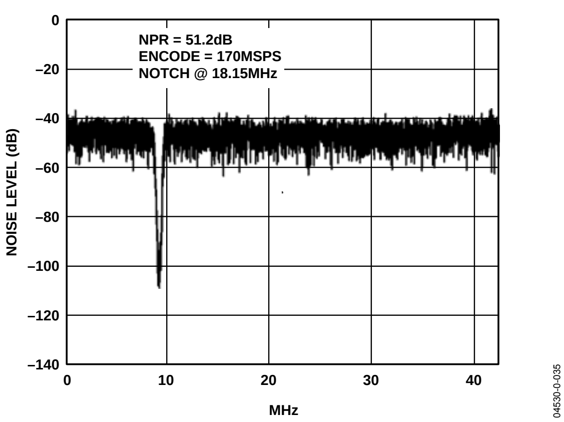


Figure 35. Noise Power Ratio Plot (170 MSPS Grade)

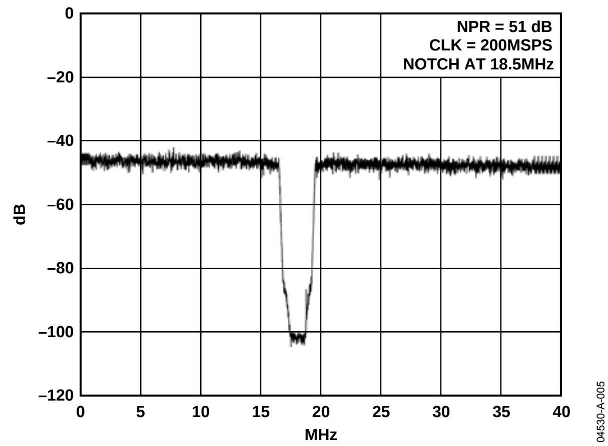


Figure 36. Noise Power Ratio Plot (200 MSPS Grade)

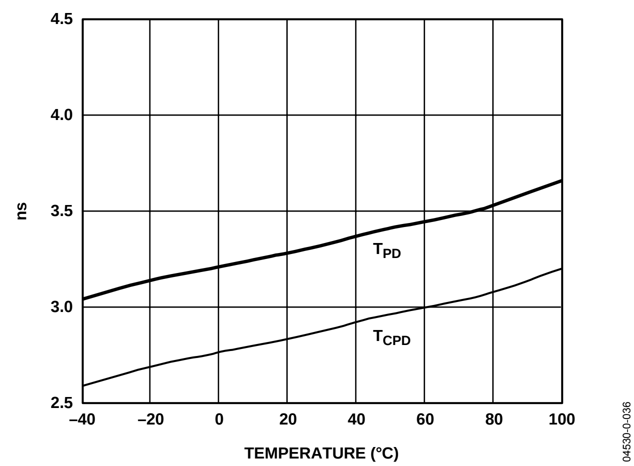


Figure 37. Propagation Delay vs. Temperature (Both Speed Grades)

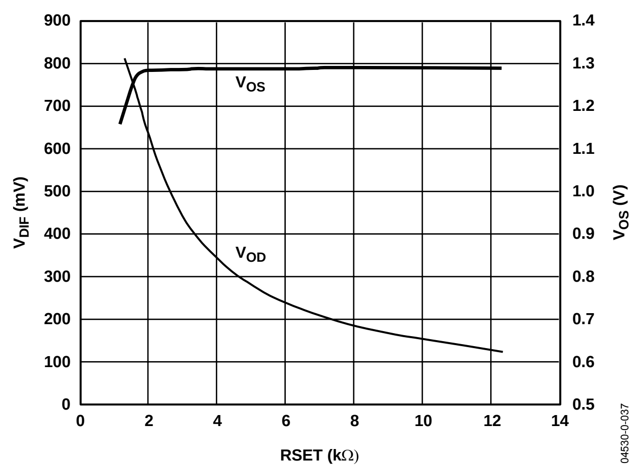


Figure 38. LVDS Output Swing, Common-Mode Voltage vs. RSET, Placed at LVDSBIAS (Both Speed Grades)

APPLICATION NOTES

The AD9411 architecture is optimized for high speed and ease of use. The analog inputs drive an integrated high bandwidth track-and-hold circuit that samples the signal prior to quantization by the 10-bit core. For ease of use, the part includes an on-board reference and input logic that accepts TTL, CMOS, or LVPECL levels. The digital output's logic levels are LVDS (ANSI-644) compatible.

CLOCK INPUT

Any high speed A/D converter is extremely sensitive to the quality of the sampling clock provided by the user. A track-and-hold circuit is essentially a mixer, and any noise, distortion, or timing jitter on the clock is combined with the desired signal at the A/D output. For this reason, considerable care has been taken in the design of the clock inputs of the AD9411, and the user is advised to give careful thought to the clock source.

The AD9411 has an internal clock duty cycle stabilization circuit that locks to the rising edge of CLK+ and optimizes timing internally. This allows a wide range of input duty cycles at the input without degrading performance. Jitter in the rising edge of the input is still of paramount concern and is not reduced by the internal stabilization circuit. The duty cycle control loop does not function for clock rates less than 30 MHz nominally. The time constant associated with the loop should be considered in applications where the clock rate changes dynamically, requiring a wait time of 1.5 μs to 5 μs after a dynamic clock frequency increase before valid data is available. This circuit is always on and cannot be disabled by the user.

The clock inputs are internally biased to 1.5 V (nominal) and support either differential or single-ended signals. For best dynamic performance, a differential signal is recommended. An MC100LVEL16 performs well in the circuit to drive the clock inputs, as illustrated in Figure 39. Note that for this low voltage PECL device, the ac coupling is optional.

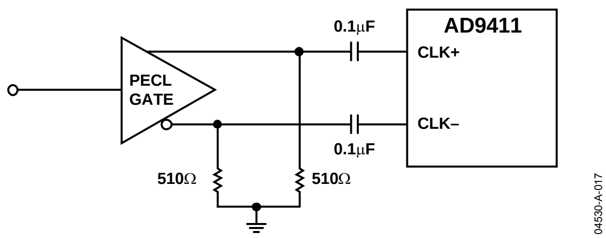


Figure 39. Driving Clock Inputs with LVEL16

Table 7. Output Select Coding[1]

S1 (Data Format Select)	S5 (Full-Scale Select)[2]	Mode
1	X	Twos Complement
0	X	Offset Binary
X	1	Full Scale = 0.768 V
X	0	Full Scale = 1.536 V

[1] X = Don't Care.

[2] S5 full-scale adjust (refer to the Analog Input section).

ANALOG INPUT

The analog input to the AD9411 is a differential buffer. For best dynamic performance, impedances at VIN+ and VIN– should match. The analog input is optimized to provide superior wide-band performance and requires that the analog inputs be driven differentially. SNR and SINAD performance degrades significantly if the analog input is driven with a single-ended signal.

A wideband transformer, such as Mini-Circuits' ADT1-1WT, can provide the differential analog inputs for applications that require a single-ended-to-differential conversion. Both analog inputs are self-biased by an on-chip resistor divider to a nominal 2.8 V (refer to the Equivalent Circuits section). Note that the input common-mode can be overdriven by approximately +/–150 mV around the self-bias point, as shown in Figure 42.

Special care was taken in the design of the analog input section of the AD9411 to prevent damage and corruption of data when the input is overdriven. The nominal differential input range is approximately 1.5 V p-p ~ (768 mV × 2). Note that the best performance is achieved with S5 = 0 (full-scale = 1.5). See Figure 40 and Figure 41.

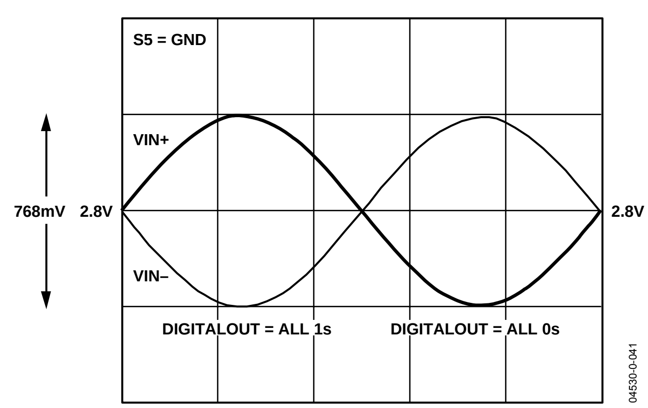


Figure 40. Differential Analog Input Range

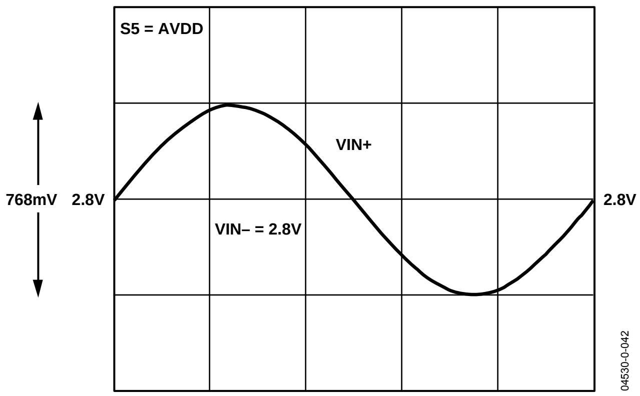


Figure 41. Single-Ended Analog Input Range

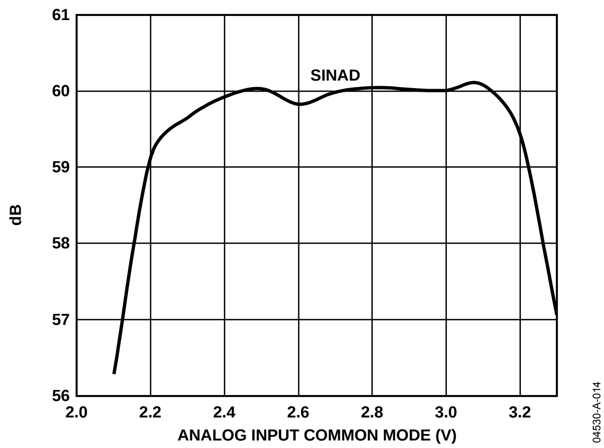


Figure 42. SINAD Sensitivity to Analog Input Common-Mode Voltage, (Ain = –.5 dBfs Differential Drive, S5 = 0)

LVDS OUTPUTS

The off-chip drivers provide LVDS compatible output levels. A 3.74 kΩ RSET resistor placed at Pin 7 (LVDSBIAS) to ground sets the LVDS output current. The RSET resistor current is ratioed on-chip, setting the output current at each output equal to a nominal 3.5 mA (11 × IRSET). A 100 Ω differential termination resistor placed at the LVDS receiver inputs results in a nominal 350 mV swing at the receiver. LVDS mode facilitates interfacing with LVDS receivers in custom ASICs and FPGAs that have LVDS capability for superior switching performance in noisy environments. Single point-to-point network topologies are recommended with a 100 Ω termination resistor as close to the receiver as possible. It is recommended to keep the trace lengths < 4 inches and to keep differential output trace lengths as equal as possible.

CLOCK OUTPUTS (DCO+, DCO–)

The input clock is buffered on-chip and available off-chip at DCO+ and DCO–. These clocks can facilitate latching off-chip, providing a low skew clocking solution (see Figure 2). The on-chip clock buffers should not drive more than 5 pF of capacitance to limit switching transient effects on performance. The output clocks are LVDS signals requiring 100 Ω differential termination at receiver.

VOLTAGE REFERENCE

A stable and accurate 1.23 V voltage reference is built into the AD9411 (VREF). The analog input full-scale range is linearly proportional to the voltage at VREF. Note that an external reference can be used by connecting the SENSE pin to VDD (disabling internal reference) and driving VREF with the external reference source. No appreciable degradation in performance occurs when VREF is adjusted ±5%. A 0.1 μF capacitor to ground is recommended at the VREF pin in internal and external reference applications. Float the SENSE pin for internal reference operation.

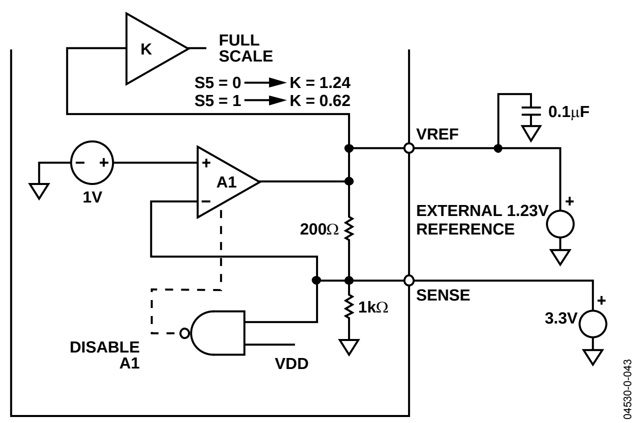


Figure 43. Using an External Reference

NOISE POWER RATIO TESTING (NPR)

NPR is a test that is commonly used to characterize the return path of cable systems where the signals are typically QAM signals with a "noise-like" frequency spectrum. NPR performance of the AD9411 was characterized in the lab yielding an effective NPR = 51.2 dB at an analog input of 18 MHz. This agrees with a theoretical maximum NPR of 51.6 dB for a 10-bit ADC at 13 dB backoff. The rms noise power of the signal inside the notch is compared with the rms noise level outside the notch using an FFT. This test requires sufficiently long record lengths to guarantee a large number of samples inside the notch. A high-order band-stop filter that provides the required notch depth for testing is also needed.

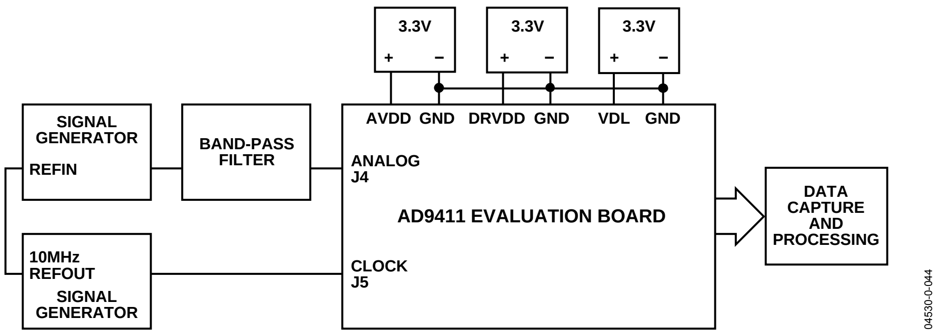


Figure 44. Evaluation Board Connections

EVALUATION BOARD

The AD9411 evaluation board offers an easy way to test the AD9411 in LVDS mode. It requires a clock source, an analog input signal, and a 3.3 V power supply. The clock source is buffered on the board to provide the clocks for the ADC, latches, and a data-ready signal. The digital outputs and output clocks are available at a 40-pin connector, P23. The board has several different modes of operation and is shipped in the following configurations:

- Offset binary
- Internal voltage reference
- Full-scale adjust = low

POWER CONNECTOR

Power is supplied to the board via a detachable 12-lead power strip (three 4-pin blocks).

Table 8. Power Connector, LVDS Mode

AVDD[1] 3.3 V	Analog Supply for ADC (350 mA)
DRVDD[1] 3.3 V	Output Supply for ADC (50 mA)
VDL[1] 3.3 V	Supply for Support Logic
VCLK/V_XTAL	Supply for Clock Buffer/Optional XTAL
EXT_VREF[2]	Optional External Reference Input

[1] AVDD, DRVDD, and VDL are the minimum required power connections.
[2] LVEL16 clock buffer can be powered from AVDD or VCLK at E47 jumper.

ANALOG INPUTS

The evaluation board accepts a 1.3 V p-p analog input signal centered at ground at SMB connector J4. This signal is terminated to ground through 50 Ω by R16. The input can be alternatively terminated at the T1 transformer secondary by R13 and R14. T1 is a wideband RF transformer that provides a single-ended-to-differential conversion, allowing the ADC to be driven differentially, which minimizes even-order harmonics. An optional second transformer, T2, can be placed following T1 if desired. This provides some performance advantage (~1 dB to 2 dB) for high analog input frequencies (>100 MHz). If T2 is placed, cut the two shorting traces at the pads. The analog signal can be low-pass filtered by R41, C12 and R42, C13 at the ADC input. The footprint for transformer T2 can be modified to accept a wideband differential amplifier (AD8351) for low frequency applications where gain is required. See the PCB schematic for more information.

GAIN

Full scale is set at E17–E19, E17–E18 sets S5 low, full scale = 1.5 V differential; E17–E19 sets S5 high, full scale = 0.75 V differential. Best performance is obtained at 1.5 V full scale.

CLOCK

The clock input is terminated to ground through 50 Ω resistor at SMB connector J5. The input is ac-coupled to a high speed differential receiver (LVEL16) that provides the required low jitter, fast edge rates needed for optimum performance. J5 input should be > 0.5 V p-p. Power to the LVEL16 is set at Jumper E47. E47–E45 powers the buffer from AVDD; E47–E46 powers the buffer from VCLK/V_XTAL.

VOLTAGE REFERENCE

The AD9411 has an internal 1.23 V voltage reference. The ADC uses the internal reference as the default when Jumpers E24–E27 and E25–E26 are left open. The full scale can be increased by placing an optional resistor (R3). The required value varies with the process and needs to be tuned for the specific application. Full scale can similarly be reduced by placing R4; tuning is required here as well. An external reference can be used by shorting the SENSE pin to 3.3 V (place Jumper E26–E25). Jumper E27–E24 connects the ADC VREF pin to the EXT_VREF pin at the power connector.

DATA FORMAT SELECT

Data format select (DFS) sets the output data format of the ADC. Setting DFS (E1–E2) low sets the output format to be offset binary; setting DFS high (E1–E3) sets the output to twos complement.

DATA OUTPUTS

The ADC LVDS digital outputs are routed directly to the connector at the card edge. Resistor pads placed at the output connector allow for termination if the connector receiving logic lack the differential termination for the data bits and DCO. Each output trace pair should be terminated differentially at the far end of the line with a single 100 ohm resistor.

CLOCK XTAL

An optional XTAL oscillator can be placed on the board to serve as a clock source for the PCB. Power to the XTAL is through the VCLK/VXTAL pin at the power connector. If an oscillator is used, ensure proper termination for best results. The board was tested with a Valpey Fisher VF561 and a Vectron JN00158-163.84.

Table 9. Evaluation Board Bill of Material—AD9411 PCB

No.	Quantity	Reference Designator	Device	Package	Value
1	33	C1, C3*, C4–C11, C15–C17, C18*, C19–C32, C35, C36, C39*, C40*, C58-C62	Capacitor	0603	0.1 µF
2	4	C33*, C34*, C37*, C38*	Capacitor	0402	0.1 µF
3	4	C63–C66	Capacitor	TAJD CAPL	10 µF
4	1	C2*	Capacitor	0603	10 pF
5	2	C12*, C13*	Capacitor	0603	20 pF
6	2	J4, J5	Jacks	SMB	
7	2	P21, P22	Power Connectors—Top	25.602.5453.0 Wieland	
8	2	P21, P22	Power Connectors—Posts	Z5.531.3425.0 Wieland	
9	1	P23	40-Pin Right Angle Connector	Digi-Key S2131-20-ND	
10	16	R1, R6–R12*, R15*, R31–R37*	Resistor	0402	100
11	1	R2	Resistor	0603	3.7 kΩ
12	3	R5, R16, R27	Resistor	0603	50
13	2	R17, R18	Resistor	0603	510
14	2	R19, R20	Resistor	0603	150
15	2	R29, R30	Resistor	0603	1 kΩ
16	2	R41, R42	Resistor	0603	25
17	2	R3, R4	Resistor	0603	3.8 kΩ
18	2	R13, R14	Resistor	0603	25
19	6	R22*, R23*, R24*, R25*, R26*, R28*	Resistor	0603	100
20	5	R38*, R39*, R40*, R45*, R47*	Resistor	0402	25
21	2	R43*, R44*	Resistor	0402	10 kΩ
22	1	R46*	Resistor	0402	1.2 kΩ
23	2	R48*, R49*	Resistor	0402	0
24	2	R50*, R51*	Resistor	0402	1 kΩ
25				Mini Circuits	
	1	T1, T2*	RF Transformer	ADT1-1WT	
26	1	U2	RF Amp	AD8351	
27	1	U9	Optional XTAL	JN00158 or VF561	
28	1	U1	AD9411	TQFP-100	
29	1	U3	MC100LVEL16	SO8NB	

* C2, C3, C12, C13, C18, C33, C34, C37, C38, C39, C40, R1, R6–R12, R15, R22–R26, R28, R31–R40, R43–R51 and T2 not placed.

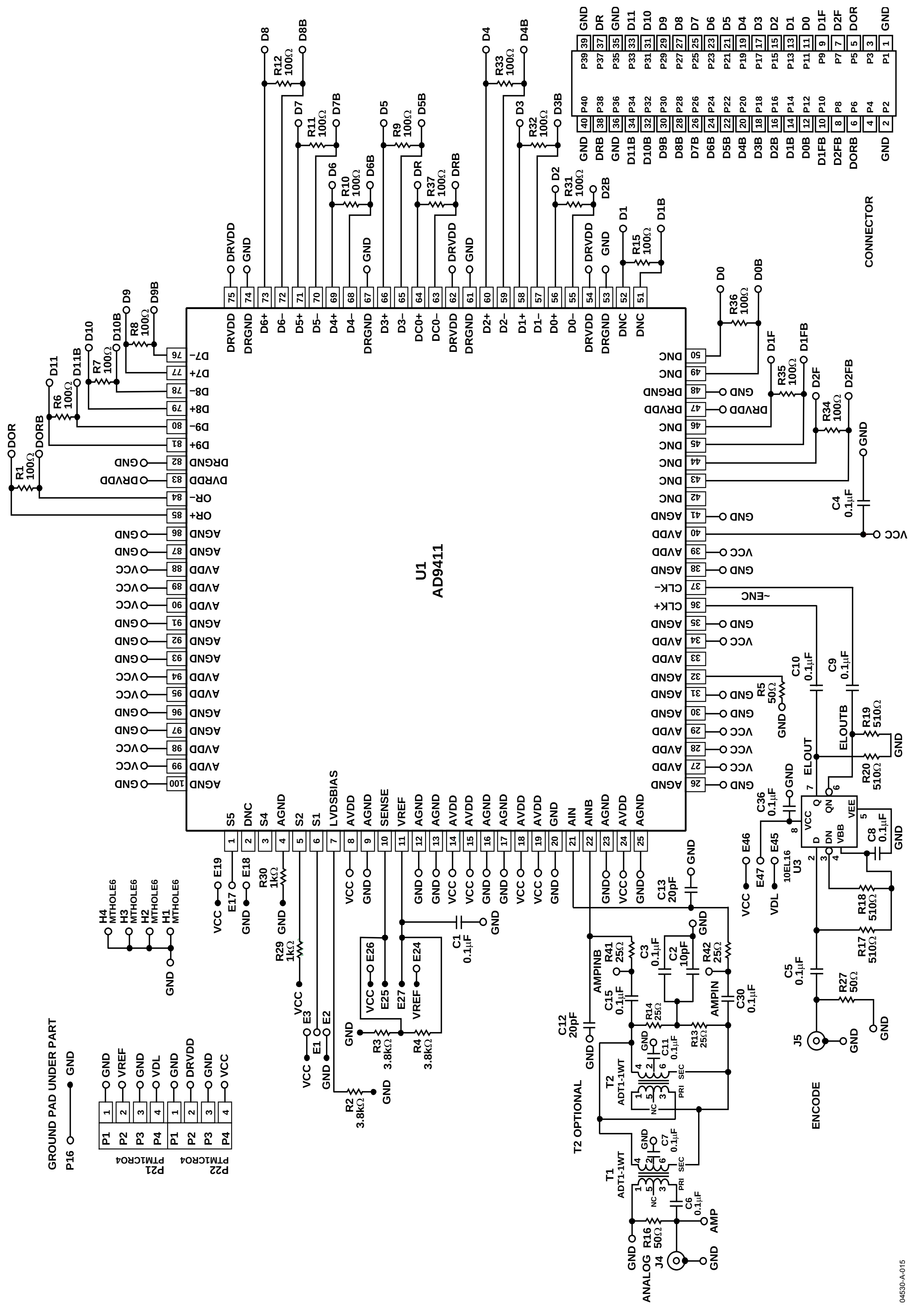


Figure 45. Evaluation Board Schematic

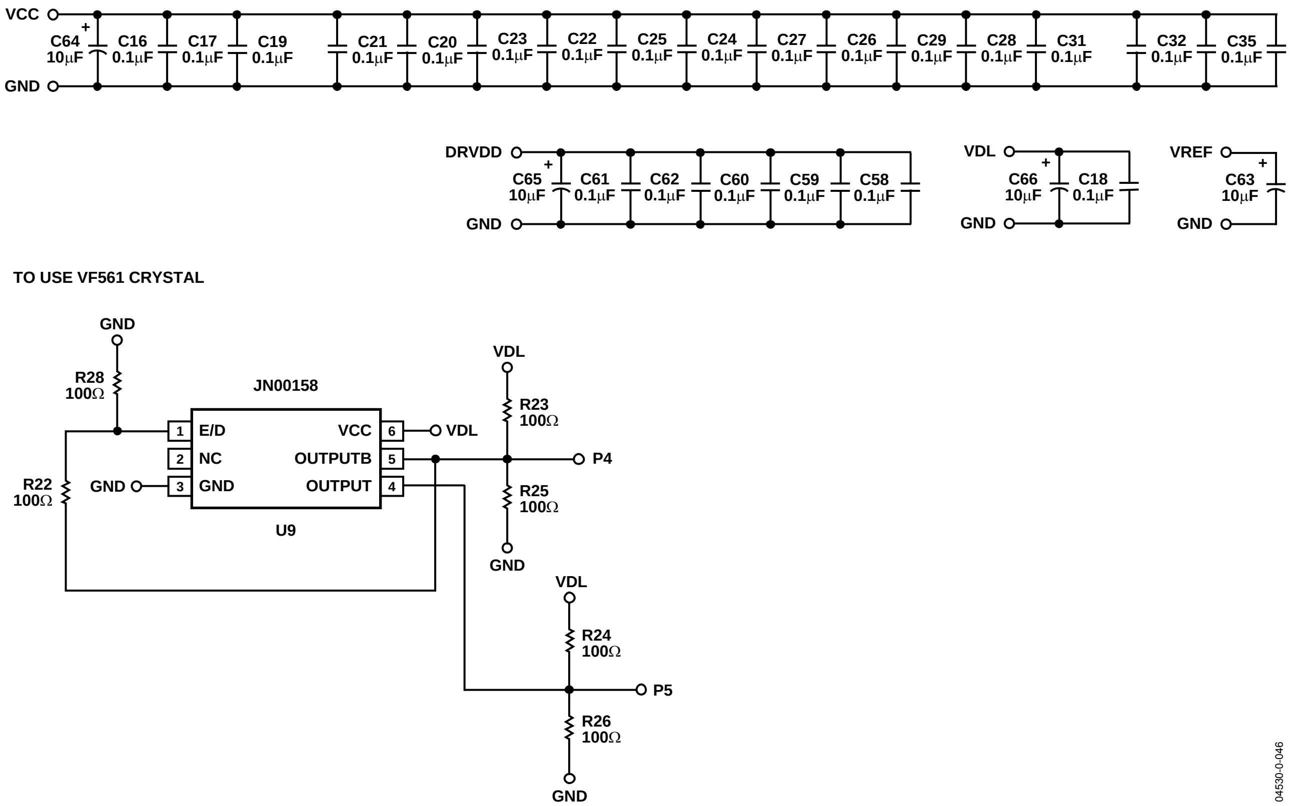


Figure 46. Evaluation Board Schematic (continued)

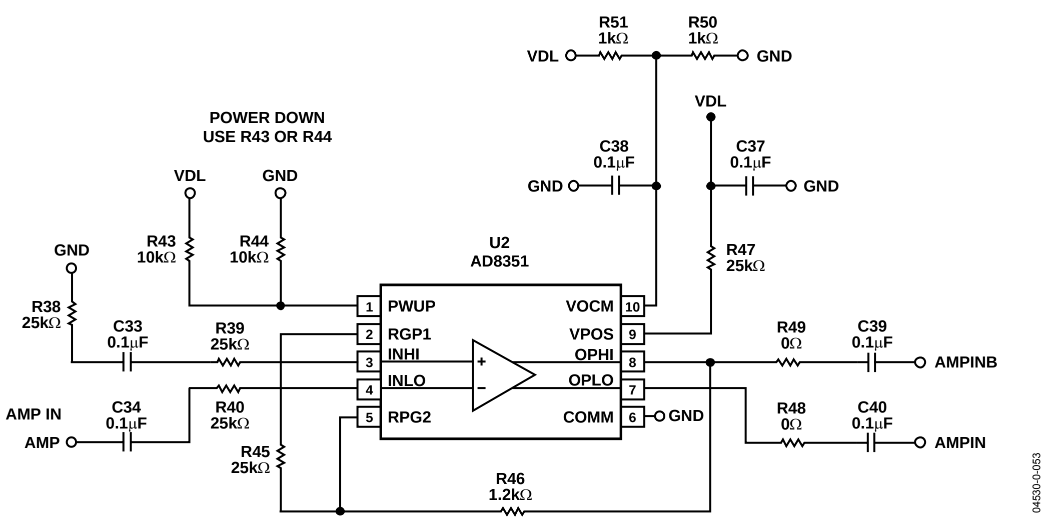


Figure 47. Evaluation Board Schematic (continued)

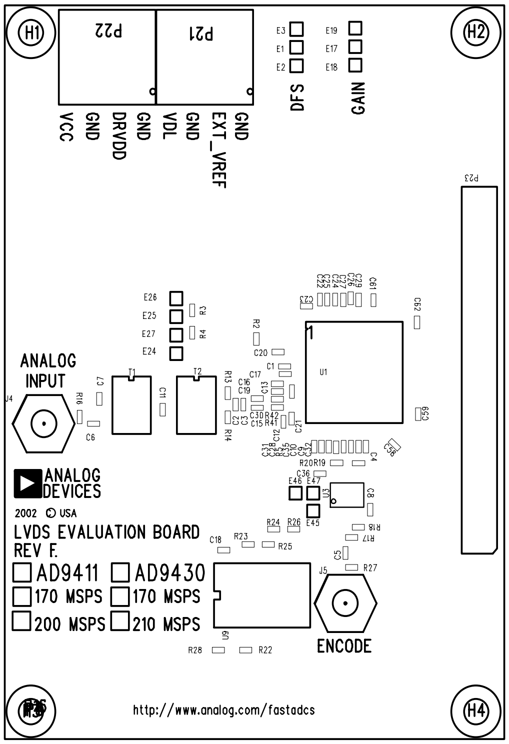


Figure 48. PCB Top Side Silkscreen

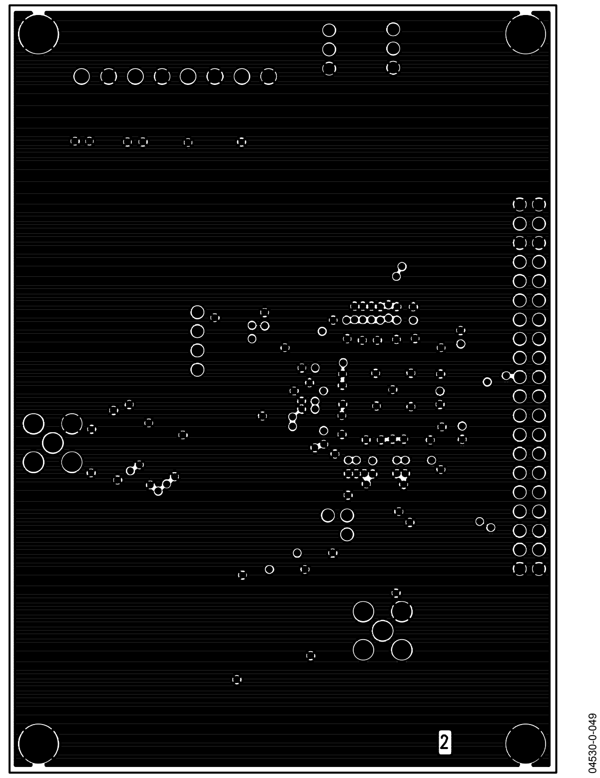


Figure 50. PCB Ground Layer

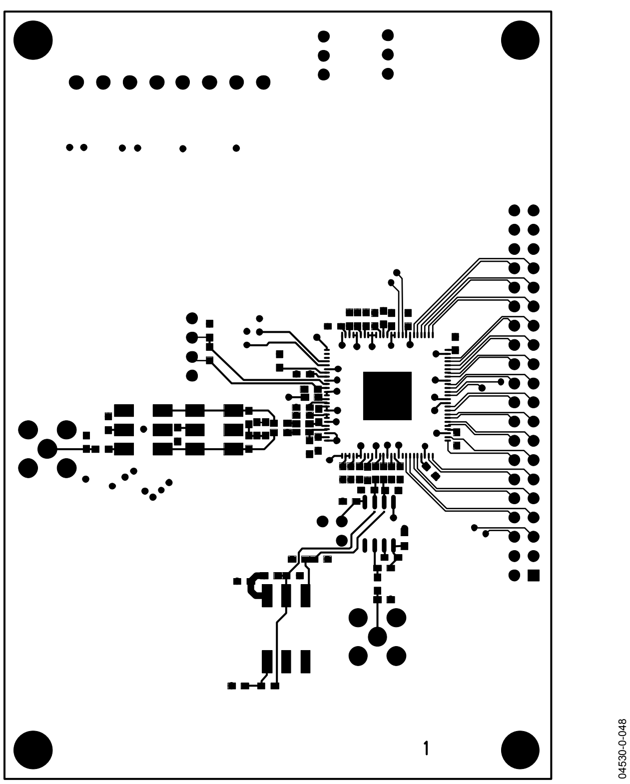


Figure 49. PCB Top Side Copper Routing

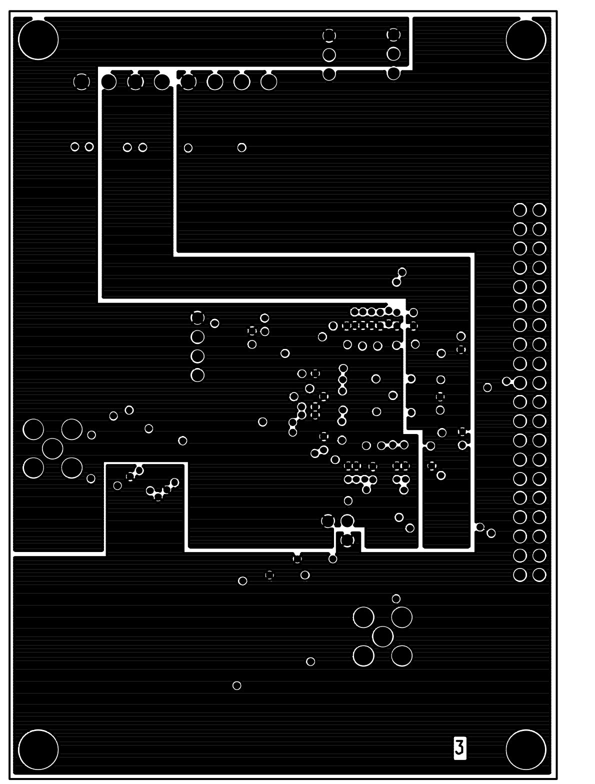


Figure 51. PCB Split Power Plane

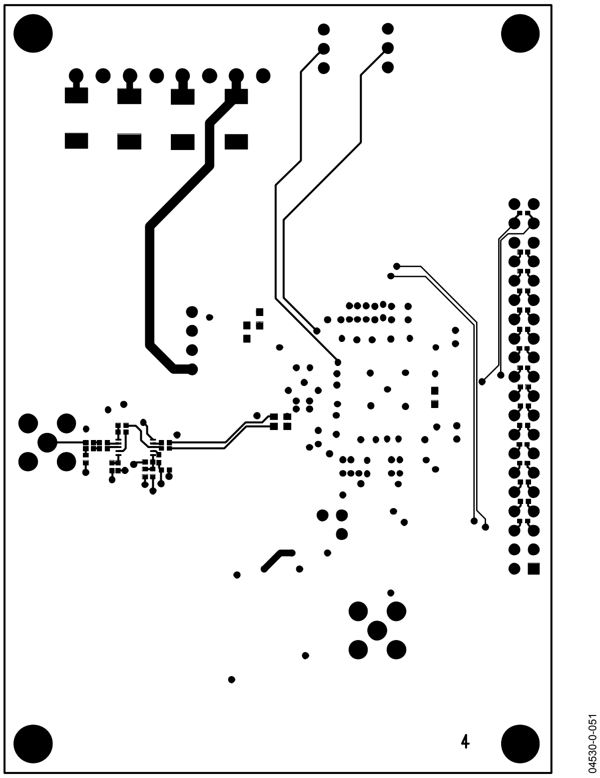


Figure 52. PCB Bottom Side Copper Routing

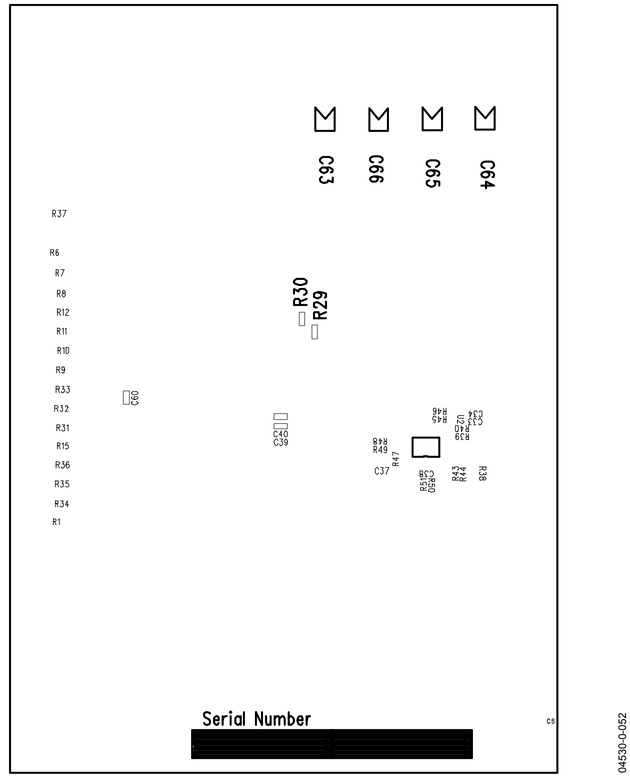
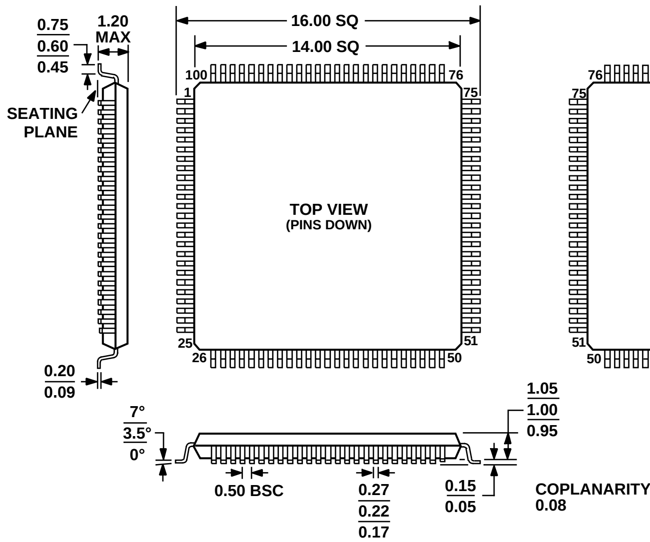


Figure 53. PCB Bottom Side Silkscreen

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026AED-HD

NOTES

1. CENTER FIGURES ARE TYPICAL UNLESS OTHERWISE NOTED.
2. THE AD9411 HAS A CONDUCTIVE HEAT SLUG TO HELP DISSIPATE HEAT AND ENSURE RELIABLE OPERATION OF THE DEVICE OVER THE FULL INDUSTRIAL TEMPERATURE RANGE. THE SLUG IS EXPOSED ON THE BOTTOM OF THE PACKAGE AND ELECTRICALLY CONNECTED TO CHIP GROUND. IT IS RECOMMENDED THAT NO PCB SIGNAL TRACES OR VIAS BE LOCATED UNDER THE PACKAGE THAT COULD COME IN CONTACT WITH THE CONDUCTIVE SLUG. ATTACHING THE SLUG TO A GROUND PLANE WILL REDUCE THE JUNCTION TEMPERATURE OF THE DEVICE WHICH MAY BE BENEFICIAL IN HIGH TEMPERATURE ENVIRONMENTS.

Figure 54. 100-Lead Thin Plastic Quad Flat Package, Exposed Pad [TQFP/EP]
(SV-100)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9411BSV-170	–40°C to +85°C	TQFP/EP	SV-100
AD9411BSV-200	–40°C to +85°C	TQFP/EP	SV-100
AD9411/PCB		EVALUATION BOARD	

NOTES