# Step-Down DC-to-DC Controller

# ADP1821

## FEATURES

**Wide power-input voltage range: 1 V to 24 V**
**Chip supply voltage range: 3 V to 5.5 V**
**Wide output voltage range: 0.6 V to 85% of input voltage**
**1% accuracy, 0.6 V reference voltage**
**All N-channel MOSFET design for low cost**
**Fixed-frequency operation 300 kHz, 600 kHz, or synchronized operation up to 1.2 MHz**
**No current sense resistor required**
**Power-good output**
**Programmable soft start with reverse current protection**
**Soft start, thermal overload, current-limit protection**
**Undervoltage lockout**
**10 µA shutdown supply current**
**Small, 16-lead QSOP**

## APPLICATIONS

**Telecom and networking systems**
**Set-top boxes**
**Printers**
**Servers**
**Medical imaging systems**
**Microprocessor and DSP core power supplies**
**Mobile communication base stations**

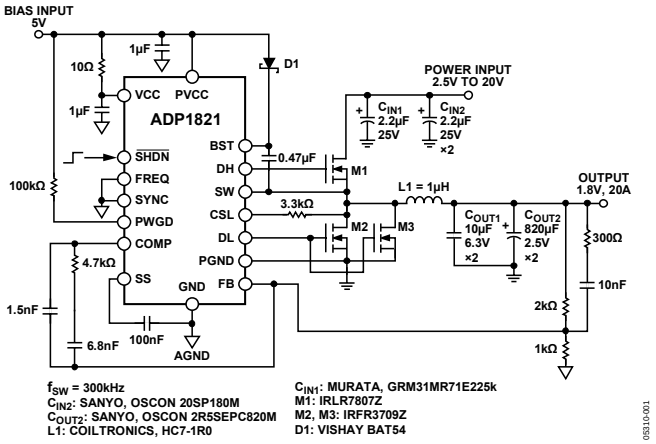


*Figure 1. Typical Operating Circuit*

## GENERAL DESCRIPTION

The ADP1821 is a versatile and inexpensive, synchronous, pulse width-modulated (PWM), voltage-mode, step-down controller. It drives an all N-channel power stage to regulate an output voltage as low as 0.6 V. The ADP1821 can be configured to provide output voltages from 0.6 V to 85% of the input voltage and is sized to handle large MOSFETs for point-of-load regulators.

The ADP1821 is well suited for a wide range of high power applications, such as DSP and processor core power in telecom, medical imaging, high performance servers, and industrial applications. It operates from a 3.0 V to 5.5 V supply with a power input voltage ranging from 1.0 V to 24 V.

The ADP1821 operates at a pin-selectable, fixed switching frequency of either 300 kHz or 600 kHz, minimizing external component size and cost. For noise-sensitive applications, it can be synchronized to an external clock to achieve switching frequencies between 300 kHz and 1.2 MHz. The ADP1821 includes soft start protection to limit the inrush current from the input supply during startup, reverse current protection during soft start for precharged outputs, as well as a unique adjustable lossless current-limit scheme utilizing external MOSFET sensing.

The ADP1821 operates over the −40°C to +85°C temperature range and is available in a 16-lead QSOP.

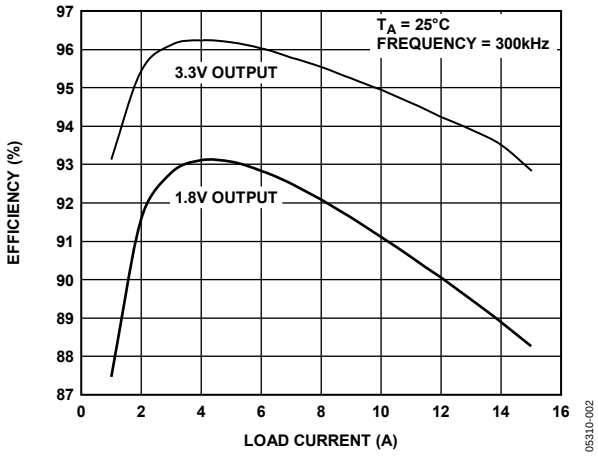


*Figure 2. Efficiency vs. Load Current, 5 V Input*

**Rev. B**



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# TABLE OF CONTENTS

Features ... 1
Applications ... 1
General Description ... 1
Revision History ... 2
Specifications ... 3
Absolute Maximum Ratings ... 5
ESD Caution ... 5
Simplified Block Diagram ... 5
Pin Configuration and Function Descriptions ... 6
Typical Performance Characteristics ... 7
Theory of Operation ... 9
Soft Start ... 9
Error Amplifier ... 9
Current-Limit Scheme ... 9
MOSFET Drivers ... 10
Input Voltage Range ... 10
Setting the Output Voltage ... 10
Switching Frequency Control and Synchronization ... 10
Compensation ... 11
Power-Good Indicator ... 11
Thermal Shutdown ... 11
Shutdown Control ... 11
Application Information ... 12
Selecting the Input Capacitor ... 12
Output LC Filter ... 12
Selecting the MOSFETs ... 13
Setting the Current Limit ... 14
Feedback Voltage Divider ... 14
Compensating the Voltage Mode Buck Regulator ... 14
Setting the Soft Start Period ... 18
PCB Layout Guideline ... 19
Recommended Component Manufacturers ... 20
Application Circuits ... 21
Summary of Equations ... 23
Compensation Equations ... 23
Type II Compensation Equations ... 23
Type III Compensation Equations ... 23
Outline Dimensions ... 24
Ordering Guide ... 24

## REVISION HISTORY

**12/06—Rev. A to Rev. B**

Updated Format ... Universal
Changes to Features Section ... 1
Changes to Applications Section ... 1
Changes to General Description Section ... 1
Changes to Error Amplifier ... 3
Changes to PWM Controller ... 3
Changes to Oscillator Frequency ... 3
Changes to Theory of Operation Section ... 9
Changes to Application Information Section ... 12
Added PCB Layout Section ... 19
Changes to Application Circuits Section ... 21
Added Summary of Equations Section ... 23

**1/06—Rev. 0 to Rev. A**

Changes to Specifications Table ... 3
Changes to Theory of Operation Section ... 10
Changes to Input Voltage Range Section ... 11
Added Equation 1 ... 12
Changes to Equation 7 and Equation 8 ... 13
Added Equation 9 ... 13
Changes to Equation 16 ... 14
Changes to Figure 15 ... 14
Changes to Equation 21 ... 15
Changes to Figure 16 ... 15
Changes to Equation 28 ... 15
Updated Outline Dimensions ... 18

**7/05—Revision 0: Initial Version**

# SPECIFICATIONS

$V_{VCC} = V_{PVCC} = V_{\overline{SHDN}} = V_{FREQ} = 5$ V, SYNC = GND. All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC). $T_A = -40°C$ to $+85°C$, unless otherwise specified.

**Table 1.**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| POWER SUPPLY | | | | | |
| Input Voltage | | 3.0 | | 5.5 | V |
| Undervoltage Lockout Threshold | $V_{VCC}$ rising | 2.5 | 2.7 | 2.9 | V |
| Undervoltage Lockout Hysteresis | $V_{VCC}$ | | 0.1 | | V |
| Quiescent Current | $I_{VCC} + I_{VCC}$, not switching | | 1 | 2 | mA |
| Shutdown Current | $\overline{SHDN}$ = GND | | | 10 | μA |
| Power Stage Supply Voltage | | 1.0 | | 24 | V |
| ERROR AMPLIFIER | | | | | |
| FB Regulation Voltage | | 594 | 600 | 606 | mV |
| FB Input Bias Current | | −100 | +1 | +100 | nA |
| Error Amplifier Open-Loop Voltage Gain | | | 70 | | dB |
| COMP Output Sink Current | | | 600 | | μA |
| COMP Output Source Current | | | 110 | | μA |
| COMP Clamp High Voltage | | | 2.4 | | V |
| COMP Clamp Low Voltage | | | 0.75 | | V |
| PWM CONTROLLER | | | | | |
| PWM Peak Ramp Voltage | | | 1.25 | | V |
| DL Minimum On-Time | FREQ = VCC (300 kHz) | 140 | 170 | 200 | ns |
| DH Maximum Duty Cycle | FREQ = GND (300 kHz) | 85 | 90 | | % |
| DH Minimum Duty Cycle | FREQ = GND (300 kHz) | | 1 | 3 | % |
| SOFT START | | | | | |
| SS Pull-Up Resistance | SS = GND | | 95 | | kΩ |
| SS Pull-Down Resistance | $V_{SS} = 0.6$ V | 1.65 | 2.5 | 4.2 | kΩ |
| OSCILLATOR | | | | | |
| Oscillator Frequency | FREQ = GND | 250 | 310 | 375 | kHz |
| | FREQ = VCC | 470 | 570 | 720 | kHz |
| Synchronization Range | FREQ = GND | 300 | | 600 | kHz |
| | FREQ = VCC | 600 | | 1200 | kHz |
| SYNC Minimum Pulse Width | | | | 80 | ns |
| CURRENT SENSE | | | | | |
| CSL Threshold Voltage | Relative to PGND | −30 | 0 | +30 | mV |
| CSL Output Current | $V_{CSL} = 0$ V | 42 | 50 | 54 | μA |
| Current Sense Blanking Period | | | 160 | | ns |
| GATE DRIVERS | | | | | |
| DH Rise Time | $C_{GATE} = 3$ nF, $V_{DH} = V_{IN}$, $V_{BST} - V_{SW} = 5$ V | | 16 | | ns |
| DH Fall Time | $C_{GATE} = 3$ nF, $V_{DH} = V_{IN}$, $V_{BST} - V_{SW} = 5$ V | | 12 | | ns |
| DL Rise Time | $C_{GATE} = 3$ nF, $V_{DL} = V_{IN}$ | | 19 | | ns |
| DL Fall Time | $C_{GATE} = 3$ nF, $V_{DL} = 0$ V | | 13 | | ns |
| DL Low to DH High Dead Time | | | 33 | | ns |
| DH Low to DL High Dead Time | | | 42 | | ns |
| LOGIC THRESHOLDS ($\overline{SHDN}$, SYNC, FREQ) | | | | | |
| $\overline{SHDN}$, SYNC, FREQ Input High Voltage | $V_{VCC} = 3.0$ V to 5.5 V | 2.0 | | | V |
| $\overline{SHDN}$, SYNC, FREQ Input Low Voltage | $V_{VCC} = 3.0$ V to 5.5 V | | | 0.8 | V |
| SYNC, FREQ Input Leakage Current | SYNC = FREQ = GND | | 0.1 | 1 | μA |
| $\overline{SHDN}$ Pull-Down Resistance | | | 100 | | kΩ |

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| THERMAL SHUTDOWN | | | | | |
| Thermal Shutdown Threshold | | | 145 | | °C |
| Thermal Shutdown Hysteresis | | | 10 | | °C |
| PWGD OUTPUT | | | | | |
| FB Overvoltage Threshold | $V_{FB}$ rising | | 750 | | mV |
| FB Overvoltage Hysteresis | | | 35 | | mV |
| FB Undervoltage Threshold | $V_{FB}$ rising | | 550 | | mV |
| FB Undervoltage Hysteresis | | | 35 | | mV |
| PWGD Off Current | $V_{PWGD}$ = 5 V | | | 1 | µA |
| PWGD Low Voltage | $I_{PWGD}$ = 10 mA | | 150 | 500 | mV |

# ABSOLUTE MAXIMUM RATINGS

**Table 2.**

| Parameter | Rating |
|---|---|
| VCC, $\overline{\text{SHDN}}$, SYNC, FREQ, COMP, SS, FB to GND, PVCC to PGND, BST to SW | −0.3 V to +6 V |
| BST to GND | −0.3 V to +30 V |
| CSL to GND | −1 V to +30 V |
| DH to GND | ($V_{SW}$ − 0.3 V) to ($V_{BST}$ + 0.3 V) |
| DL to PGND | −0.3 V to ($V_{PVCC}$ + 0.3 V) |
| SW to GND | −2 V to +30 V |
| PGND to GND | ±2 V |
| $\theta_{JA}$, 2-Layer (SEMI Standard Board) | 150°C/W |
| $\theta_{JA}$, 4-Layer (JEDEC Standard Board) | 105°C/W |
| Operating Ambient Temperature Range | −40°C to +85°C |
| Operating Junction Temperature Range | −55°C to +125°C |
| Storage Temperature Range | −65°C to +150°C |
| Maximum Soldering Lead Temperature | 260°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other condition s above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified, all other voltages are referenced to GND.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## SIMPLIFIED BLOCK DIAGRAM

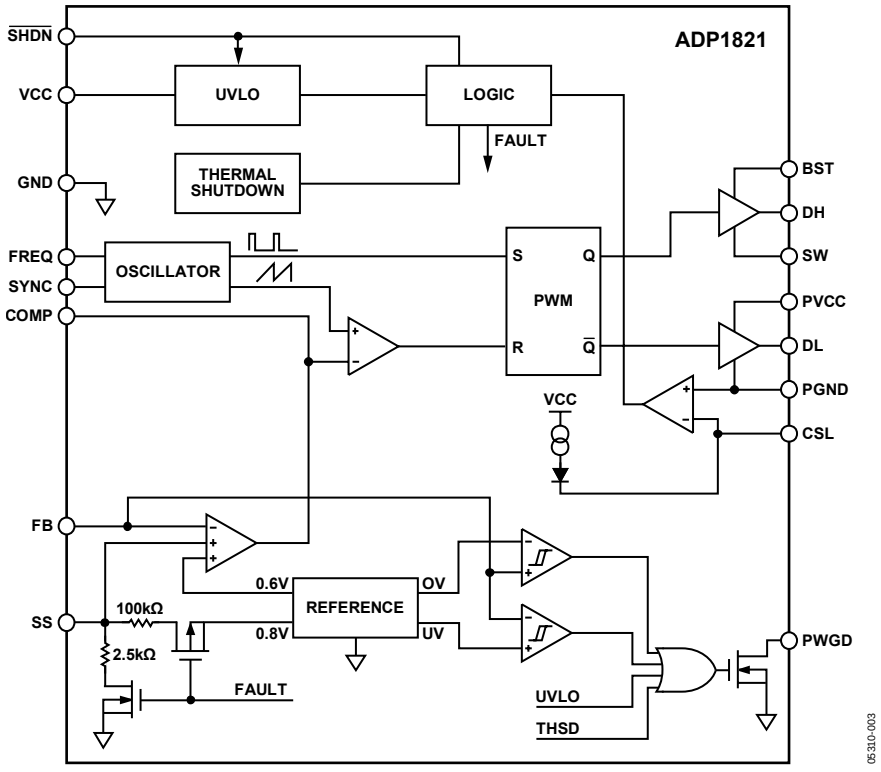



*Figure 3. Simplified Block Diagram*

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

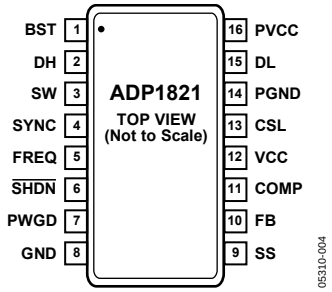



*Figure 4. Pin Configuration*

**Table 3. Pin Function Description**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | BST | High-Side Gate Driver Boost Capacitor Input. A capacitor between SW and BST powers the high-side gate driver, DH. The capacitor is charged through a diode from PVCC when the low-side MOSFET is on. Connect a 0.1 µF or greater ceramic capacitor from BST to SW and a Schottky diode from PVCC to BST to power the high-side gate driver. |
| 2 | DH | High-Side Gate Driver Output. Connect DH to the gate of the external high-side, N-channel MOSFET switch. DH is powered from the capacitor between SW and BST, and its voltage swings between $V_{SW}$ and $V_{BST}$. |
| 3 | SW | Power Switch Node. Connect the source of the high-side, N-channel MOSFET switch and the drain of the low-side, N-channel MOSFET synchronous rectifier to SW. SW powers the output through the output LC filter. |
| 4 | SYNC | Frequency Synchronization Input. Drive SYNC with an external 300 kHz to 1.2 MHz signal to synchronize the converter switching frequency to the applied signal. The maximum SYNC frequency is limited to 2 times the nominal internal frequency selected by FREQ. Do not leave SYNC unconnected; when not used, connect SYNC to GND. |
| 5 | FREQ | Frequency Select Input. FREQ selects the converter switching frequency. Drive FREQ low to select 300 kHz, or high to select 600 kHz. Do not leave FREQ unconnected. |
| 6 | $\overline{\text{SHDN}}$ | Active-Low DC-to-DC Shutdown Input. Drive $\overline{\text{SHDN}}$ high to turn on the converter and low to turn it off. Connect $\overline{\text{SHDN}}$ to VCC for automatic startup. |
| 7 | PWGD | Open-Drain Power-Good Output. PWGD sinks current to GND when the output voltage is above or below the regulation voltage. Connect a pull-up resistor from PWGD to VDD for a logical power-good indicator. |
| 8 | GND | Analog Ground. Connect GND to PGND at a single point as close as possible to the internal circuitry (IC). |
| 9 | SS | Soft Start Control Input. A capacitor from SS to GND controls the soft start period. When the output is overloaded, SS is discharged to prevent excessive input current while the output recovers. Connect a 1 nF capacitor to 1 µF capacitor from SS to GND to set the soft start period. See the Soft Start section. |
| 10 | FB | Voltage Feedback Input. Connect to a resistive voltage divider from the output to FB to set the output voltage. See the Setting the Output Voltage section. |
| 11 | COMP | Compensation Node. Connect a resistor-capacitor network from COMP to FB to compensate the regulation control system. See the Compensation section. |
| 12 | VCC | Internal Power Supply Input. VCC powers the internal circuitry. Bypass VCC to GND with a 0.1 µF or greater capacitor connected as close as possible to the IC. |
| 13 | CSL | Low-Side Current Sense Input. Connect CSL to SW through a resistor to set the current limit. See the Setting the Current Limit section. |
| 14 | PGND | Power Ground. Connect GND to PGND at a single point as close as possible to the IC. |
| 15 | DL | Low-Side Gate Driver Output. Connect DL to the gate of the low-side N-channel MOSFET synchronous rectifier. The DL voltage swings between PGND and PVCC. |
| 16 | PVCC | Internal Gate Driver Power Supply Input. PVCC powers the low-side gate driver, DL. Bypass PVCC to PGND with a 1 µF or greater capacitor connected as close as possible to the IC. |

# TYPICAL PERFORMANCE CHARACTERISTICS

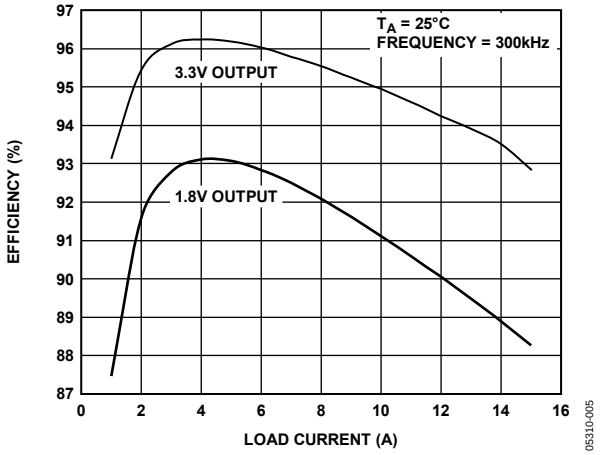



*Figure 5. Efficiency vs. Load Current, $V_{IN}$ = 5 V, $V_{OUT}$ = 3.3 V, 1.8 V*

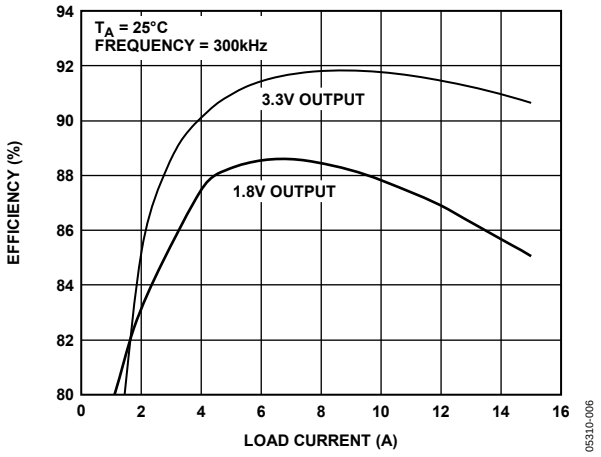



*Figure 6. Efficiency vs. Load Current, $V_{IN}$ = 12 V, $V_{OUT}$ = 3.3 V, 1.8 V*

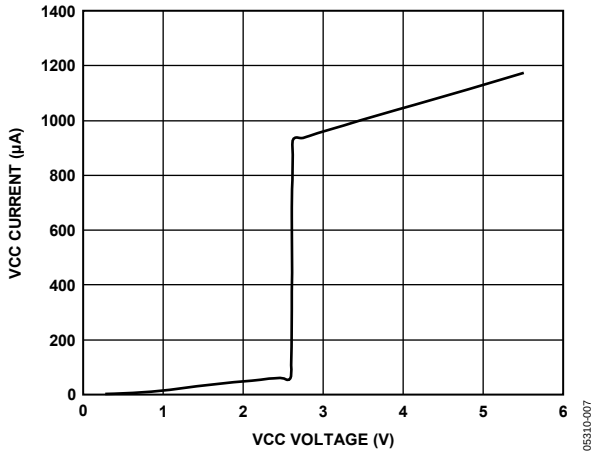



*Figure 7. VCC Supply Current vs. VCC Voltage*

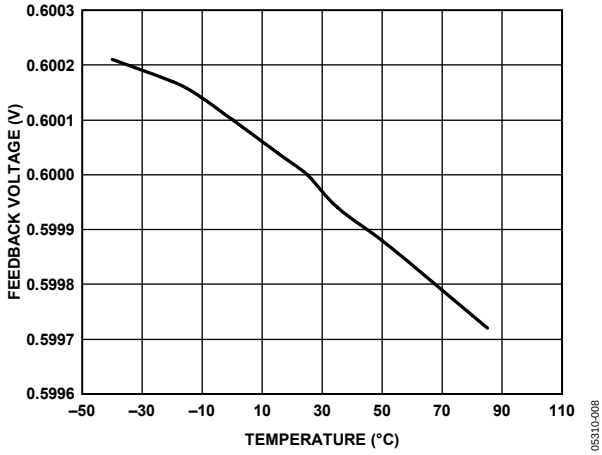



*Figure 8. FB Regulation Voltage vs. Temperature*

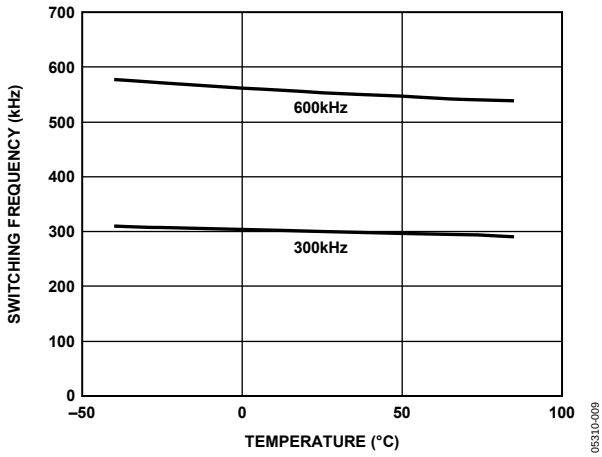



*Figure 9. Switching Frequency vs. Temperature*

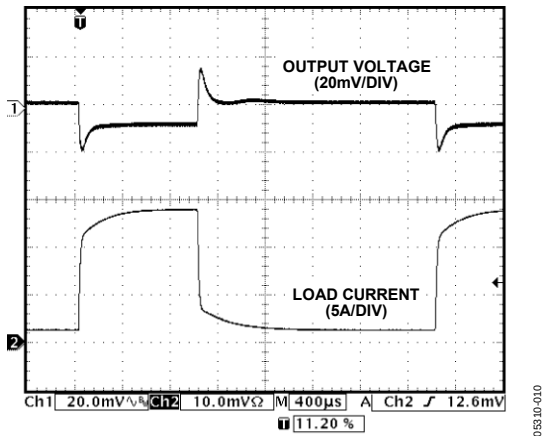



*Figure 10. Load Transient Response, 1.5 A to 15 A*

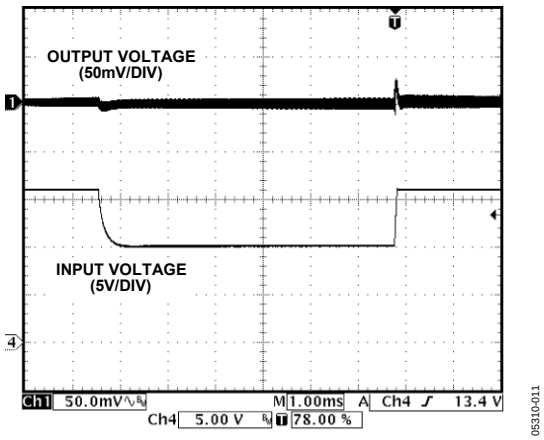



Figure 11. Line Transient Response, 10 V to 16 V

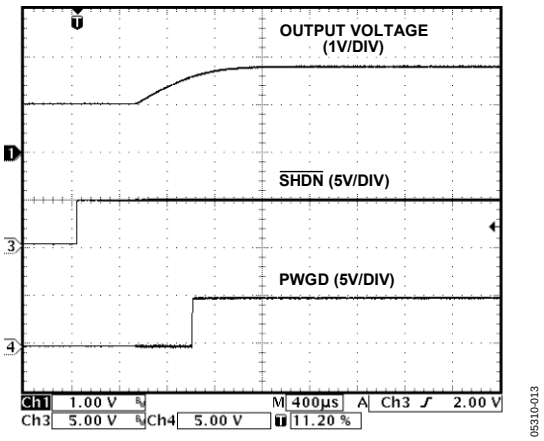



Figure 13. Power-On Response, Prebiased Output

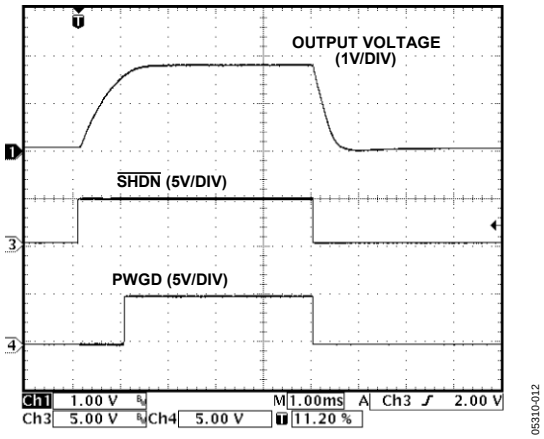



Figure 12. Power-On Response

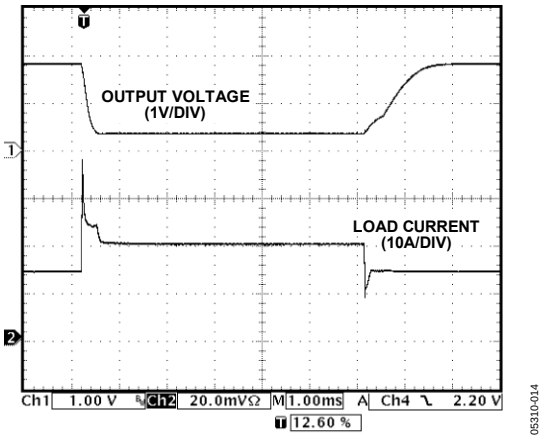



Figure 14. Output Short-Circuit Response and Recovery

# THEORY OF OPERATION

The ADP1821 is a versatile, economical, synchronous-rectified, fixed-frequency, PWM, voltage mode step-down controller capable of generating an output voltage as low as 0.6 V. It is ideal for a wide range of high power applications, such as DSP power and processor core power in telecom, medical imaging, and industrial applications. The ADP1821 controller operates from a 3.0 V to 5.5 V supply with a power input voltage ranging from 1.0 V to 24 V.

The ADP1821 operates at a fixed, internally set 300 kHz or 600 kHz switching frequency that is controlled by the state of the FREQ input. The high frequency reduces external component size and cost while maintaining high efficiency. For noise sensitive applications where the switching frequency needs to be more tightly controlled, synchronize the ADP1821 to an external signal whose frequency is between 300 kHz and 1.2 MHz.

The ADP1821 includes adjustable soft start with output reverse-current protection, and a unique adjustable, lossless current limit. It operates over the −40°C to +85°C temperature range and is available in a space-saving, 16-lead QSOP.

## SOFT START

When powering up or resuming operation after shutdown, overload, or short-circuit conditions, the ADP1821 employs an adjustable soft start feature that reduces input current transients and prevents output voltage overshoot at start-up and overload conditions. The soft start period is set by the value of the soft start capacitor, $C_{SS}$, between SS and GND.

When starting the ADP1821, $C_{SS}$ is initially discharged. It is enabled when $\overline{SHDN}$ is high and VCC is above the undervoltage lockout threshold. $C_{SS}$ begins charging to 0.8 V through an internal 100 kΩ resistor. As $C_{SS}$ charges, the regulation voltage at FB is limited to the lesser of either the voltage at SS or the internal 0.6 V reference voltage. As the voltage at SS rises, the output voltage rises proportionally until the voltage at SS exceeds 0.6 V. At this time, the output voltage is regulated to the desired voltage.

If the output voltage is precharged prior to turn-on, the ADP1821 limits reverse inductor current, which would discharge the output voltage. Once the voltage at SS exceeds the 0.6 V regulation voltage, the reverse current is re-enabled to allow the output voltage regulation to be independent of load current.

## ERROR AMPLIFIER

The ADP1821 error amplifier is an operational amplifier. The ADP1821 senses the output voltages through an external resistor divider at the FB pin. The FB pin is the inverting input to the error amplifier. The error amplifier compares this feedback voltage to the internal 0.6 V reference, and the output of the error amplifier appears at the COMP pin. The COMP pin voltage then directly controls the duty cycle of the switching converter.

A series/parallel RC network is tied between the FB pin and the COMP pin to provide the compensation for the buck converter control loop. A detailed design procedure for compensating the system is provided in the Compensating the Voltage Mode Buck Regulator section.

The error amplifier output is clamped between a lower limit of about 0.7 V and a higher limit of about 2.4 V. When the COMP pin is low, the switching duty cycle goes to 0%, and when the COMP pin is high, the switching duty cycle goes to the maximum.

The SS pin is an auxiliary positive input to the error amplifier. Whichever voltage is lowest, SS or the internal 0.6 V reference, controls the FB pin voltage and thus the output. As a consequence, if two of these inputs are close to each other, a small offset is imposed on the error amplifier.

## CURRENT-LIMIT SCHEME

The ADP1821 employs a unique, programmable, cycle-by-cycle, lossless current limit circuit that uses an ordinary, inexpensive resistor to set the threshold. Every switching cycle, the synchronous rectifier turns on for a minimum time and the voltage drop across the MOSFET $R_{DSON}$ is measured to determine if the current is too high.

This measurement is done by an internal current limit comparator and an external current limit set resistor. The resistor is connected between the switch node (that is the drain of the rectifier MOSFET) and the CSL pin. The CSL pin, which is the inverting input of the comparator, forces 50 μA through the resistor to create an offset voltage drop across it.

When the inductor current is flowing in the MOSFET rectifier, its drain is forced below PGND by the voltage drop across its $R_{DSON}$. If the $R_{DSON}$ voltage drop exceeds the preset drop on the current-limit-set resistor, the inverting comparator input is similarly forced below PGND and an overcurrent fault is flagged.

The normal transient ringing on the switch node is ignored for 100 ns after the synchronous rectifier turns on, so the over current condition must also persist for 100 ns in order for a fault to be flagged.

When the ADP1821 senses an overcurrent condition, the next switching cycle is suppressed, the soft start capacitor is discharged through an internal 2.5 kΩ resistor, and the error amplifier output voltage is pulled down. The ADP1821 remains in this mode for as long as the overcurrent condition persists. When the overcurrent condition is removed, operation resumes in soft start mode.

See the Setting the Current Limit section for more information.

## MOSFET DRIVERS

The DH pin drives the high-side switch MOSFET. This is a boosted 5 V gate driver that is powered by a bootstrap capacitor circuit. This configuration allows the high-side, N-channel MOSFET gate to be driven above the input voltage, allowing full enhancement and a low voltage drop across the MOSFET. The bootstrap capacitor is connected from the SW pin to the BST pin. A bootstrap Schottky diode connected from the PVCC pin to the BST pin recharges the bootstrap capacitor every time the SW node goes low. Use a bootstrap capacitor value greater than 100× the high-side MOSFET input capacitance.

In practice, the switch node can run up to 24 V of input voltage, and the boost nodes can operate more than 5 V above this to allow full gate drive. The power input voltage can be run from 1 V to 24 V.

The switching cycle is initiated by the internal clock signal. The high-side MOSFET is turned on by the DH driver, and the SW node goes high, pulling up on the inductor. When the internally generated ramp signal crosses the COMP pin voltage, the switch MOSFET is turned off and the low-side synchronous rectifier MOSFET is turned on by the DL driver. Active break-before-make circuitry as well as a supplemental fixed dead time are used to prevent cross-conduction in the switches.

The DL pin provides the gate drive for the low-side MOSFET synchronous rectifier. Internal circuitry monitors the external MOSFETs to ensure break-before-make switching to prevent cross-conduction. An active dead-time reduction circuit reduces the break-before-make time of the switching to limit the losses due to current flowing through the synchronous rectifier body diode.

The PVCC pin provides power to the low-side drivers. It is limited to 5.5 V maximum input and should have a local decoupling capacitor to PGND.

The synchronous rectifier is turned on for a minimum time of about 200 ns on every switching cycle in order to sense the current. This and the nonoverlap dead time put a limit on the maximum high-side switch duty cycle based on the selected switching frequency. Typically, this is about 90% at 300 kHz switching, and at 1 MHz switching, it reduces to about 70% maximum duty cycle.

## INPUT VOLTAGE RANGE

The ADP1821 takes its internal power from the VCC and PVCC inputs. PVCC powers the low-side MOSFET gate drive (DL), and VCC powers the internal control circuitry. Both of these inputs are limited to between 3.0 V and 5.5 V. Bypass PVCC to PGND with a 1 μF or greater capacitor. Bypass VCC to GND with a 0.1 μF or greater capacitor.

The power input to the dc-to-dc converter can range between 1.2× the output voltage and 24 V. Bypass the power input to PGND with a suitably large capacitor. See the Selecting the Input Capacitor section.

## SETTING THE OUTPUT VOLTAGE

The output voltage is set using a resistive voltage divider from the output to FB. The voltage divider drops the output voltage to the 0.6 V FB regulation voltage to set the regulation output voltage. The output voltage is set to voltages as low as 0.6 V and as high as 85% of the minimum power input voltage (see the Feedback Voltage Divider section).

## SWITCHING FREQUENCY CONTROL AND SYNCHRONIZATION

The ADP1821 has a logic-controlled frequency select input (FREQ) which sets the switching frequency to 300 kHz or 600 kHz. Drive FREQ low for 300 kHz and high for 600 kHz.

The SYNC input is used to synchronize the converter switching frequency to an external signal. The converter switching can be synchronized to an external signal. This allows multiple ADP1821 converters to be operated at the same frequency to prevent frequency beating or other interactions.

To synchronize the ADP1821 switching to an external signal, drive the SYNC input with a synchronizing signal. The ADP1821 can only synchronize up to 2× the nominal oscillator frequency. If the frequency is set to 300 kHz (FREQ connected to GND), then the synchronization frequency needs to be in between 300 kHz and 600 kHz. Since the 300 kHz setting has a minimum specification (see Table 1) of 250 kHz and a maximum of 375 kHz over the specified temperature range, the recommended synchronization frequency range is between 375 kHz and 500 kHz to cover the whole range of part-to-part variation and over the operating temperature range. If the frequency is set to 600 kHz (FREQ connected to VCC), then the synchronization frequency needs to be in between 600 kHz and 1.2 MHz. Since the 600 kHz setting has a minimum specification (see Table 1) of 470 kHz and a maximum of 720 kHz over the specified temperature range, the recommended synchronization frequency range is between 720 kHz and 940 kHz to cover the whole range of part-to-part variation and over the operating temperature range. Driving SYNC faster than recommended for the FREQ setting results in a small ramp signal, which could affect the signal-to-noise ratio and the modulator gain and stability.

When an external clock is detected at the first SYNC edge, the internal oscillator is reset and clock control shifts to SYNC. The SYNC edges then trigger subsequent clocking of the PWM outputs. The DH rising edges appear about 320 ns after the corresponding SYNC edge, and the frequency is locked to the external signal. If the external SYNC signal disappears during operation, the ADP1821 reverts to its internal oscillator and experiences a delay of no more than a single cycle of the internal oscillator.

## COMPENSATION

The control loop is compensated by an external series RC network from COMP to FB and sometimes requires a series RC in parallel with the top voltage divider resistor. COMP is the output of the internal error amplifier.

The internal error amplifier compares the voltage at FB to the internal 0.6 V reference voltage. The difference between the two (the feedback voltage error) is amplified by the error amplifier. To optimize the ADP1821 for stability and transient response for a given set of external components and input/output voltage conditions, choose the compensation components carefully. For more information on choosing the compensation components, see the Compensating the Voltage Mode Buck Regulator section.

## POWER-GOOD INDICATOR

The ADP1821 features an open-drain, power-good output (PWGD) that sinks current when the output voltage drops 8.3% below or 25% above the nominal regulation voltage. Two comparators measure the voltage at FB to set these thresholds. The PWGD comparator directly monitors FB, and the threshold is fixed at 0.55 V for undervoltage and 0.75 V for overvoltage. The PWGD output also sinks current if an over temperature or input undervoltage condition is detected and is operational with VCC voltage as low as 1.0 V.

Use this output as a logical power-good signal by connecting a pull-up resistor from PWGD to an appropriate supply voltage.

## THERMAL SHUTDOWN

The ADP1821 controller does not generate much heat under normal conditions, even when driving a relatively large MOSFET. However, the surrounding power components or other circuits on the same PCB could heat up the PCB to an unsafe operating temperature. The ADP1821 controller goes into shutdown and shuts off the gate drivers when its junction temperature reaches about 145°C. When the junction temperature drops below about 135°C, the ADP1821 resumes normal operation in a soft start mode.

## SHUTDOWN CONTROL

The ADP1821 dc-to-dc converter features a low-power shutdown mode that reduces quiescent supply current to 1 μA. To shut down the ADP1821, drive $\overline{\text{SHDN}}$ low. To turn it on, drive $\overline{\text{SHDN}}$ high. For automatic startup, connect $\overline{\text{SHDN}}$ to VCC.

# APPLICATION INFORMATION

## SELECTING THE INPUT CAPACITOR

The input current to a buck converter is a pulsed waveform. It is zero when the high-side switch is off and approximately equal to the load current when it is on. The input capacitor carries the input ripple current, allowing the input power source to supply only the dc current. The input capacitor needs sufficient ripple current rating to handle the input ripple and the equivalent series resistance (ESR) that is low enough to mitigate input voltage ripple. For the usual current ranges for these converters, good practice is to use two parallel capacitors placed close to the drains of the high-side switch MOSFETs, one bulk capacitor of sufficiently high current rating as calculated in Equation 1, along with 10 µF of ceramic capacitor.

Select an input bulk capacitor based on its ripple current rating. First, determine the duty cycle of the output with the larger load current:

$$D = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

Second, determine the input capacitor ripple current, which is approximately

$$I_{RIPPLE} \approx I_L \sqrt{D(1-D)} \quad (2)$$

where:
$I_L$ is the maximum inductor or load current for the channel.
$D$ is the duty cycle.

Use this method to determine the input capacitor ripple current rating for duty cycles between 20% and 80%.

For duty cycles less than 20% or greater than 80%, use an input capacitor with a ripple current rating:

$$I_{RIPPLE} > 0.4\ I_L \quad (3)$$

## OUTPUT LC FILTER

The output LC filter smoothes the switched voltage at SW, making the output voltage an almost dc voltage. Choose the output LC filter to achieve the desired output ripple voltage. Because the output LC filter is part of the regulator negative-feedback control loop, the choice of the output LC filter components affects the regulation control loop stability.

Choose an inductor value such that the inductor ripple current is approximately 1/3 of the maximum dc output load current. Using a larger value inductor results in a physical size larger than required and using a smaller value results in increased losses in the inductor and/or MOSFET switches.

Use the following equation to choose the inductor value:

$$L = \frac{1}{f_{SW} \times \Delta I_L} V_{OUT}\left[1 - \frac{V_{OUT}}{V_{IN}}\right] \quad (4)$$

where:
$L$ is the inductor value.
$f_{SW}$ is the switching frequency.
$V_{OUT}$ is the output voltage.
$V_{IN}$ is the input voltage.
$\Delta I_L$ is the inductor ripple current, typically 1/3 of the maximum dc load current.

Choose the output bulk capacitor to set the desired output voltage ripple. The impedance of the output capacitor at the switching frequency multiplied by the ripple current gives the output voltage ripple. The impedance is made up of the capacitive impedance plus the nonideal parasitic characteristics, the ESR and the equivalent series inductance (ESL). The output voltage ripple can be approximated with

$$\Delta V_{OUT} = \Delta I_L \sqrt{ESR^2 + \left(\frac{1}{8 f_{SW} C_{OUT}}\right)^2 + (4 f_{SW} ESL)^2} \quad (5)$$

where:
$\Delta V_{OUT}$ is the output ripple voltage.
$\Delta I_L$ is the inductor ripple current.
*ESR* is the equivalent series resistance of the output capacitor (or the parallel combination of ESR of all output capacitors).
*ESL* is the equivalent series inductance of the output capacitor (or the parallel combination of ESL of all capacitors).

Note that the factors of 8 and 4 in Equation 5 would normally be 2π for sinusoidal waveforms, but the ripple current waveform in this application is triangular. Parallel combinations of different types of capacitors, for example, a large aluminum electrolytic in parallel with MLCCs, may give different results.

Usually the impedance is dominated by ESR at the switching frequency so this equation reduces to

$$\Delta V_{OUT} \cong \Delta I_L ESR \quad (6)$$

Electrolytic capacitors have significant ESL also, on the order of 5 nH to 20 nH, depending on type, size, and geometry; and PCB traces contribute some ESR and ESL as well. However, using the maximum ESR rating from a capacitor data sheet usually provides some margin such that measuring the ESL is not usually required.

In the case of output capacitors where the impedance of the ESR and ESL are small at the switching frequency, for instance, where the output capacitor is a bank of parallel MLCC capacitors, the capacitive impedance dominates and the ripple equation reduces to

$$\Delta V_{OUT} \cong \frac{\Delta I_L}{8\, C_{OUT} f_{SW}} \quad (7)$$

Make sure that the ripple current rating of the output capacitors is greater than the maximum inductor ripple current.

During a load step transient on the output, the output capacitor supplies the load until the control loop has a chance to ramp the inductor current. This initial output voltage deviation due to a change in load is dependent on the output capacitor characteristics. Again, usually the capacitor ESR dominates this response, and the $\Delta V_{OUT}$ in Equation 6 can be used with the load step current value for $\Delta I_L$.

## SELECTING THE MOSFETS

The choice of MOSFET directly affects the dc-to-dc converter performance. The MOSFET must have low on resistance to reduce $I^2R$ losses and low gate charge to reduce transition losses. In addition, the MOSFET must have low thermal resistance to ensure that the power dissipated in the MOSFET does not result in excessive MOSFET die temperature.

The high-side MOSFET carries the load current during on-time and carries all the transition losses of the converter. Typically, the lower the MOSFET on resistance, the higher the gate charge and vice versa. Therefore, it is important to choose a high-side MOSFET that balances the two losses. The conduction loss of the high-side MOSFET is determined by the equation

$$P_C \cong (I_{LOAD})^2 R_{DSON} \left( \frac{V_{OUT}}{V_{IN}} \right) \quad (8)$$

where:
$P_C$ = conduction power loss.
$R_{DSON}$ = MOSFET on resistance.

The gate charging loss is approximated by the equation

$$P_G \cong V_{PVCC} Q_G f_{SW} \quad (9)$$

where:
$P_G$ = gate charging loss power.
$V_{PVCC}$ = gate driver supply voltage.
$Q_G$ = MOSFET total gate charge.
$f_{SW}$ = converter switching frequency.

The high-side MOSFET transition loss is approximated by the equation

$$P_T = \frac{V_{IN} I_{LOAD} (t_R + t_F) f_{SW}}{2} \quad (10)$$

where:
$P_T$ = high-side MOSFET switching loss power.
$t_R$ = MOSFET rise time.
$t_F$ = MOSFET fall time.

The total power dissipation of the high-side MOSFET is the sum of all the previous losses, or

$$P_D \cong P_C + P_G + P_T \quad (11)$$

where $P_D$ is the total high-side MOSFET power loss.

The conduction losses may need an adjustment to account for the MOSFET $R_{DSON}$ variation with temperature. Note that MOSFET $R_{DSON}$ increases with increasing temperature. A MOSFET data sheet should list the thermal resistance of the package, $\theta_{JA}$, along with a normalized curve of the temperature coefficient of the $R_{DSON}$. For the power dissipation estimated above, calculate the MOSFET junction temperature rise over the ambient temperature of interest.

$$T_J = T_A + \theta_{JA} P_D \quad (12)$$

Then calculate the new $R_{DSON}$ from the temperature coefficient curve and the $R_{DSON}$ spec at 25°C. A typical value of the temperature coefficient (TC) of the $R_{DSON}$ is 0.004/°C, so an alternate method to calculate the MOSFET $R_{DSON}$ at a second temperature, $T_J$, is

$$R_{DSON} @ T_J = R_{DSON} @ 25°C(1 + TC(T_J - 25°C)) \quad (13)$$

Then the conduction losses can be recalculated and the procedure iterated once or twice until the junction temperature calculations are relatively consistent.

The synchronous rectifier, or low-side MOSFET, carries the inductor current when the high-side MOSFET is off. The low-side MOSFET transition loss is small and can be neglected in the calculation. For high input voltage and low output voltage, the low-side MOSFET carries the current most of the time. Therefore, to achieve high efficiency, it is critical to optimize the low-side MOSFET for low on resistance. In cases where the power loss exceeds the MOSFET rating or lower resistance is required than is available in a single MOSFET, connect multiple low-side MOSFETs in parallel. The equation for low-side MOSFET power loss is

$$P_{LS} \cong (I_{LOAD})^2 R_{DSON} \left[ 1 - \frac{V_{OUT}}{V_{IN}} \right] \quad (14)$$

where:
$P_{LS}$ is the low-side MOSFET on resistance.
$R_{DSON}$ is the total on resistance of the low-side MOSFET(s).

Check the gate charge losses of the synchronous rectifier using the $P_G$ equation (Equation 9) to be sure it is reasonable. If multiple low-side MOSFETs are used in parallel, then use the parallel combination of the on resistances for determining $R_{DSON}$ to solve this equation.

## SETTING THE CURRENT LIMIT

The current limit comparator measures the voltage across the low-side MOSFET to determine the load current.

The current limit is set through the current limit resistor, $R_{CL}$. CSL, the current sense pin, sources 50 µA through $R_{CL}$. This creates an offset voltage of $R_{CL}$ multiplied by the 50 µA CSL current. When the drop across the low-side MOSFET $R_{DSON}$ is equal to or greater than this offset voltage, the ADP1821 flags a current-limit event.

Because the CSL current and the MOSFET $R_{DSON}$ vary over process and temperature, the minimum current limit should be set to ensure that the system can handle the maximum desired load current. To do this, use the peak current in the inductor, which is the desired current-limit level plus the ripple current, the maximum $R_{DSON}$ of the MOSFET at its highest expected temperature, and the minimum CSL current.

$$R_{CL} = \frac{I_{LPK}\ R_{DSON(MAX)}}{42\,\mu A} \quad (15)$$

where $I_{LPK}$ is the peak inductor current.

When an over-current event occurs, the over-current comparator does prevent switching cycles until the rectifier current has decayed below the threshold. The over-current comparator is blanked for the first 100 ns of the synchronous rectifier cycle to prevent switch node ringing from falsely tripping the current limit. The ADP1821 senses the current limit during the off cycle. When the current limit condition occurs, the ADP1821 resets the internal clock until the over-current condition disappears. This suppresses the start clock cycles until the overload condition is removed. At the same time, the SS cap is discharged through a 2.5 kΩ resistor. The SS input is an auxiliary positive input of the error amplifier, so it behaves like another voltage reference. The lowest reference voltage wins. Discharging the SS voltage causes the converter to use a lower voltage reference when switching is allowed again. Therefore, as switching cycles continue around the current limit, the output looks roughly like a constant current source due to the rectifier limit, and the output voltage droops as the load resistance decreases. When the overload condition is removed, the output recovers with the normal soft start slope and does not overshoot.

Because the buck converter is usually running at a fairly high current, PCB layout and component placement may affect the current-limit setting. An iteration of the $R_{CL}$ values may be required for a particular board layout and MOSFET selection. If alternate MOSFETs are substituted at some point in production, the values of the $R_{CL}$ resistor may also need an iteration.

## FEEDBACK VOLTAGE DIVIDER

The output regulation voltage is set through the feedback voltage divider. The output voltage is reduced through the voltage divider and drives the FB feedback input. The regula tion threshold at FB is 0.6 V. The maximum input bias current into FB is 100 nA. For a 0.15% degradation in regulation voltage and with 100 nA bias current, the low-side resistor, $R_{BOT}$, needs to be less than 9 kΩ, which results in 67 µA of divider current. For $R_{BOT}$, use 1 kΩ to 10 kΩ. A larger value resistor can be used, but results in a reduction in output voltage accuracy due to the input bias current at the FB pin, while lower values cause increased quiescent current consumption. Choose $R_{TOP}$ to set the output voltage by using the following equation:

$$R_{TOP} = R_{BOT}\left(\frac{V_{OUT} - V_{FB}}{V_{FB}}\right) \quad (16)$$

where:
$R_{TOP}$ is the high-side voltage divider resistance.
$R_{BOT}$ is the low-side voltage divider resistance.
$V_{OUT}$ is the regulated output voltage.
$V_{FB}$ is the feedback regulation threshold, 0.6 V.

## COMPENSATING THE VOLTAGE MODE BUCK REGULATOR

Assuming the LC filter design is complete, the feedback control system can then be compensated. Good compensation is critical to proper operation of the regulator. Calculate the quantities in Equation 17 through Equation 58 to derive the compensation values. For convenience, a summary of the design equations is located in the Summary of Equations section. The information can then be added to an Excel spreadsheet, for automated calculation.

The goal is to guarantee that the voltage gain of the buck converter crosses unity at a slope that provides adequate phase margin for stable operation. Additionally, at frequencies above the crossover frequency, $f_{CO}$, guaranteeing sufficient gain margin and attenuation of switching noise are important secondary goals. For initial practical designs, a good choice for the crossover frequency is one tenth of the switching frequency; so first calculate

$$f_{CO} = \frac{f_{SW}}{10} \quad (17)$$

This gives sufficient frequency range to design a compensation that attenuates switching artifacts, while also giving sufficient control loop bandwidth to provide good transient response.

The output LC filter is a resonant network that inflicts two poles upon the response at a frequency $f_{LC}$, so next calculate

$$f_{LC} = \frac{1}{2\pi\sqrt{LC}} \quad (18)$$

Generally speaking, the LC corner frequency is about two orders of magnitude below the switching frequency, and therefore about one order of magnitude below crossover. To achieve sufficient phase margin at crossover to guarantee stability, the design must compensate for the two poles at the LC corner frequency with two zeros to boost the system phase prior to crossover. The two zeros require an additional pole or two above the crossover frequency to guarantee adequate gain margin and attenuation of switching noise at high frequencies.

Depending on component selection, one zero might already be generated by the ESR of the output capacitor. Calculate this zero corner frequency, $f_{ESR}$, as

$$f_{ESR} = \frac{1}{2\pi R_{ESR} C_{OUT}} \quad (19)$$

This zero is often near or below crossover and is useful in bringing back some of the phase lost at the LC corner.

Figure 15 shows a typical bode plot of the LC filter by itself.

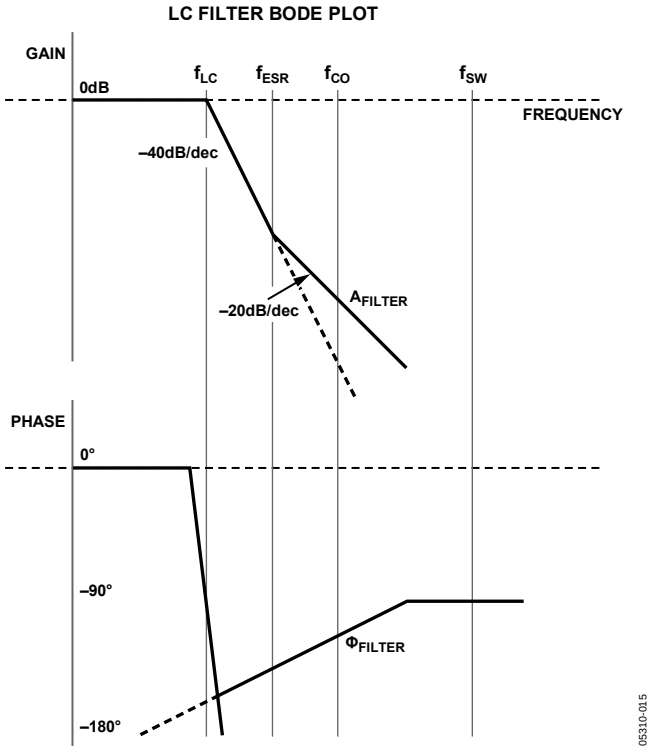



*Figure 15. LC Filter Bode Plot*

The gain of the LC filter at crossover can be linearly approximated from Figure 15 as

$$A_{FILTER} = A_{LC} + A_{ESR}$$

$$A_{FILTER} = -40\ \text{dB} \times \log\left(\frac{f_{ESR}}{f_{LC}}\right) - 20\ \text{dB} \times \log\left(\frac{f_{CO}}{f_{ESR}}\right) \quad (20)$$

If $f_{ESR} \approx f_{CO}$, then add another 3 dB to account for the local difference between the exact solution and the preceding linear approximation.

To compensate the control loop, the gain of the system must be brought back up so that it is 0 dB at the desired crossover frequency. Some gain is provided by the PWM modulation itself, so next calculate

$$A_{MOD} = 20\log\left(\frac{V_{IN}}{V_{RAMP}}\right) \quad (21)$$

For systems using the internal oscillator, this becomes

$$A_{MOD} = 20\log\left(\frac{V_{IN}}{1.25\ \text{V}}\right) \quad (22)$$

Note that if the converter is being synchronized, the ramp voltage, $V_{RAMP}$, is lower than 1.25 V by the percentage of frequency increase over the nominal setting of the FREQ pin:

$$V_{RAMP} = 1.25\ \text{V}\left(\frac{f_{FREQ}}{f_{SYNC}}\right) \quad (23)$$

The rest of the system gain needed to reach 0 dB at crossover is provided by the error amplifier and is covered in the compensation design information that follows. The total gain of the system therefore, is given by

$$A_T = A_{MOD} + A_{FILTER} + A_{COMP} \quad (24)$$

where:
$A_{MOD}$ is the gain of the PWM modulator
$A_{FILTER}$ is the gain of the LC filter including the effects of the ESR zero
$A_{COMP}$ is the gain of the compensated error amplifier.

Additionally, the phase of the system must be brought back up to guarantee stability. Note from the bode plot of the filter that the LC contributes −180 degrees of phase shift. Additionally, because the error amplifier is an integrator at low frequency, it contributes an initial −90 degrees. Therefore, before adding compensation or accounting for the ESR zero, the system is already down −270 degrees. To avoid loop inversion at crossover, or −180 degrees phase shift, a good initial practical design is to require a phase margin of 60 degrees, which is therefore an overall phase loss of −120 degrees from the initial low frequency dc phase. The goal of the compensation is to boost the phase back up from −270 degrees to −120 degrees at crossover.

Two common compensation schemes are used, which are sometimes referred to as Type II or Type III compensation, depending on whether the compensation design includes two or three poles. (Dominant pole compensations, or single pole compensation, is referred to as Type I compensation, but unfortunately it is not very useful for dealing successfully with switching regulators.)

If the zero produced by the ESR of the output capacitor provides sufficient phase boost at crossover, Type II compensation is adequate. If the phase boost produced by the ESR of the output capacitor is not sufficient, another zero is added to the compensation network, and thus Type III is used. A general rule to determine the scheme whether the phase contribution of the ESR zero is greater than 70 degrees at crossover.

In Figure 16, the location of the ESR zero corner frequency gives significantly different net phase at the crossover frequency.

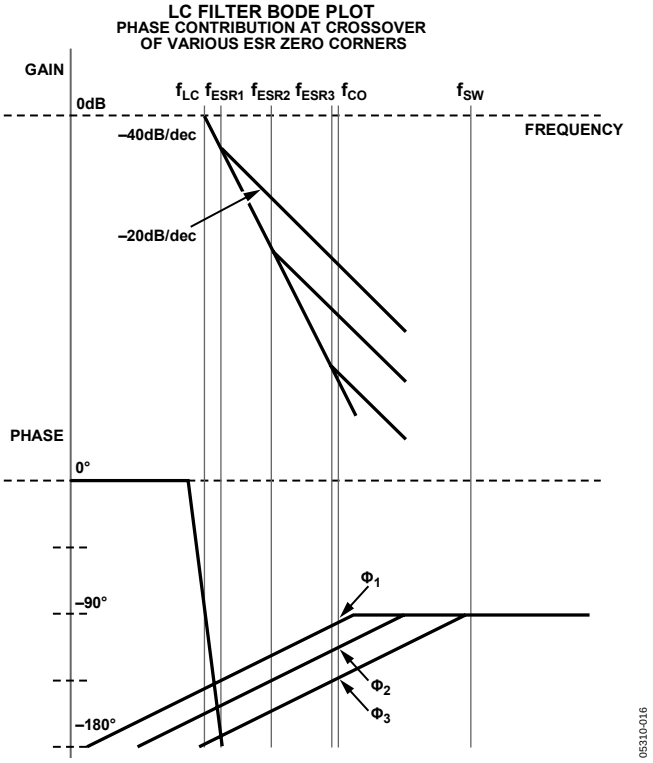



*Figure 16. LC Filter Bode Plot*

Using a linear approximation from Figure 16, the phase contribution of the ESR zero at crossover can be estimated by

$$\varphi_{ESR} = 45 \times \log \frac{10 \times f_{CO}}{f_{ESR}} \quad (25)$$

If $\varphi_{ESR} \geq 70$, then Type II compensation is adequate.

If $\varphi_{ESR} < 70$, use Type III, as an additional zero is needed.

The total phase of the system at crossover is the sum of the contributing elements, namely

$$\varphi_T = \varphi_{LC} + \varphi_{ESR} + \varphi_{COMP} \quad (26)$$

where:

$\varphi_{LC} = -180$.

$\varphi_{ESR}$ is as calculated in Equation 25.

$$\varphi_{COMP} = -90 + \varphi_P + \varphi_Z \quad (27)$$

Note in the compensator phase expression shown in Equation 27, the −90 degree term is the phase contributed by the initial integrator pole. The $\varphi_P$ is the additional phase contributed by the high frequency compensation poles placed above crossover, and $\varphi_Z$ is the phase contributed by the compensation zeros placed below crossover. For the system to be stable at crossover, phase boost is required from the compensator.

For stability, the total phase at crossover is designed to be equal to −120 degrees

$$\varphi_T = \varphi_{LC} + \varphi_{ESR} + \varphi_{COMP} \quad (28)$$

$$-120 = -180 + \varphi_{ESR} + -90 + \varphi_P + \varphi_Z \quad (29)$$

Define phase boost, $\varphi_B$, to be that portion of the phase at crossover contributed by the compensator's higher order poles and zeros:

$$\varphi_B = \varphi_P + \varphi_Z \quad (30)$$

$$\varphi_B = 150 - \varphi_{ESR} \quad (31)$$

D. Venable, in his article "The K Factor: A New Mathematical Tool for Stability Analysis and Synthesis," 1983, showed that an optimum compensation solution was to place the zeros and poles symmetrically around the crossover frequency. He derived a factor known as K with which the frequencies of the compensation zeros and poles may be calculated. K is calculated for the type of compensation selected Figure 17.

### *Type II Compensator*

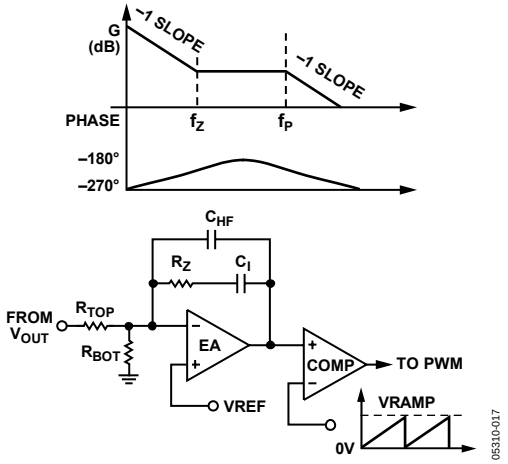



*Figure 17. Type II Compensation*

To calculate K for Type II compensation use

$$K = \tan\left(\frac{\varphi_B}{2} + 45\right) \quad (32)$$

Values of K between 4 and 15 are practical for implementation, so if the selected type of compensation does not yield a reasonable value of K, try the other type.

From K, the frequency of the added zeros, $f_Z$, is below crossover for Type II by

$$f_Z = \frac{f_{CO}}{K} \quad (33)$$

Similarly, the frequency of the added poles, $f_P$, should be previous crossover by for Type II

$$f_P = f_{CO}K \quad (34)$$

Select $R_{TOP}$ between 1 k and 10 k. A good starting value is 2 k.

Next, calculate $R_{BOT}$ as

$$R_{BOT} = \frac{V_{FB}R_{TOP}}{V_{OUT} - V_{FB}} \quad (35)$$

$$R_{BOT} = \frac{0.6\text{ V} \times R_{TOP}}{V_{OUT} - 0.6\text{ V}} \quad (36)$$

Calculate the compensator gain needed at crossover to achieve 0 dB total system gain:

$$A_T = A_{MOD} + A_{FILTER} + A_{COMP} \quad (37)$$

$$0\text{ dB} = A_{MOD} + A_{FILTER} + A_{COMP} \quad (38)$$

$$A_{COMP} = 0\text{ dB} - A_{MOD} - A_{FILTER} \quad (39)$$

Calculate the value of $R_Z$ to achieve that gain

$$A_{COMP} = 20 \times \log\left(\frac{R_Z}{R_{TOP}}\right) \quad (40)$$

$$R_Z = R_{TOP} \times 10^{\left(\frac{A_{COMP}}{20}\right)} \quad (41)$$

Calculate the integrator cap value to place the compensation zero at the desired frequency using the following equation:

$$C_I = \frac{1}{2\pi R_Z f_Z} \quad (42)$$

Calculate the capacitor value for the high frequency pole by

$$C_{HF} = \frac{1}{2\pi R_Z f_P} \quad (43)$$

### Type III Compensator

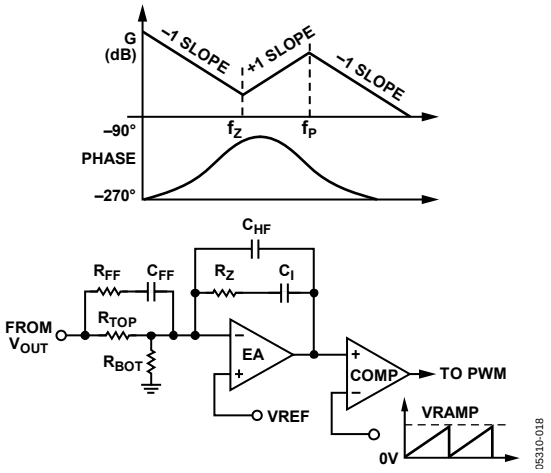



*Figure 18. Type III Compensation*

$$K = \left(\tan\left(\frac{\varphi_B}{2} + 45\right)\right)^2 \quad (44)$$

$$f_Z = \frac{f_{CO}}{\sqrt{K}} \quad (45)$$

$$f_P = f_{CO}\sqrt{K} \quad (46)$$

Select $R_{TOP}$ between 1 k and 10 k. A good starting value is 2 k.

Next, calculate $R_{BOT}$ as

$$R_{BOT} = \frac{V_{FB}R_{TOP}}{V_{OUT} - V_{FB}} \quad (47)$$

$$R_{BOT} = \frac{0.6\text{ V} \times R_{TOP}}{V_{OUT} - 0.6\text{ V}} \quad (48)$$

Calculate the feedforward capacitor to produce the first compensator zero

$$C_{FF} = \frac{1}{2\pi R_{TOP} f_Z} \quad (49)$$

Calculate the resistor of the feedforward network to provide the first high frequency compensator pole

$$R_{FF} = \frac{1}{2\pi C_{FF} f_P} \quad (50)$$

Calculate the impedance of the feedforward network at the crossover frequency, as this is required to set the gain of the compensator.

$$Z_{FF} = \frac{1}{2\pi C_{FF} f_{CO}} + R_{FF} \quad (51)$$

Calculate the compensator gain needed at crossover to achieve 0 dB total system gain:

$$A_T = A_{MOD} + A_{FILTER} + A_{COMP} \quad (52)$$

$$0\ \text{dB} = A_{MOD} + A_{FILTER} + A_{COMP} \quad (53)$$

$$A_{COMP} = 0\ \text{dB} - A_{MOD} - A_{FILTER} \quad (54)$$

Calculate the value of $R_Z$ to achieve the previous gain by

$$A_{COMP} = 20 \times \log\left(\frac{R_Z}{R_{TOP} \,||\, Z_{FF}}\right) \quad (55)$$

$$R_Z = \left(R_{TOP} \,||\, Z_{FF}\right) \times 10^{\left(\frac{A_{COMP}}{20}\right)} \quad (56)$$

Calculate the integrator capacitor value to place the compensation zero at the desired frequency:

$$C_I = \frac{1}{2\pi R_Z f_Z} \quad (57)$$

Calculate the capacitor value for the high frequency pole by

$$C_{HF} = \frac{1}{2\pi R_Z f_P} \quad (58)$$

Check that the calculated component values are reasonable. For instance, capacitors smaller than about 10 pF should be avoided. In addition, the ADP1821 error amplifier has finite output current drive, so $R_Z$ values less than a few kilohm and $C_I$ values greater than 10 nF should be avoided. If necessary, recalculate the compensation network with a different starting value of $R_{TOP}$. If $C_{HF}$ is too small, start with a smaller value $R_{TOP}$. If $R_Z$ is too small and $C_I$ is too big, start with a larger value of $R_{TOP}$.

## SETTING THE SOFT START PERIOD

The ADP1821 uses an adjustable soft start to limit the output voltage ramp-up period, limiting the input inrush current. The soft start is set by selecting the capacitor, $C_{SS}$, from SS to GND. The ADP1821 charges $C_{SS}$ to 0.8 V through an internal 100 kΩ resistor. The voltage on $C_{SS}$ while it is charging is

$$V_{CSS} = 0.8\ \text{V}\left(1 - e^{\frac{t}{RC_{SS}}}\right) \quad (59)$$

where $R$ is the internal 100 kΩ resistor.

The soft start period, $t_{SS}$, is achieved when $V_{CSS}$ = 0.6 V or

$$0.6\ \text{V} = 0.8\ \text{V}\left(1 - e^{\frac{t_{SS}}{100\ \text{k}\Omega(C_{SS})}}\right) \quad (60)$$

or

$$\frac{t_{SS}}{100\ \text{k}\Omega(C_{SS})} = -1\text{n}\left(1 - \frac{0.6\ \text{V}}{0.8\ \text{V}}\right) = 1.386 \quad (61)$$

Solve for $C_{SS}$ by

$$C_{SS} = t_{SS} \times 7.21\ \mu\text{F/sec} \quad (62)$$

# PCB LAYOUT GUIDELINE

In any switching converter, there are some circuit paths that carry high dI/dt, which can create spikes and noise. Other circuit paths are sensitive to noise and still others carry high dc current and can produce significant IR voltage drops. The key to proper PCB layout of a switching converter is to identify these critical paths and arrange the components and copper area accordingly. When designing PCB layouts, be sure to keep high current loops small. In addition, keep compensation and feedback components away from the switch nodes and their associated components.

The following is a list of recommended layout practices for ADP1821, arranged in approximately decreasing order of importance. A PCB layout example of the circuit shown in Figure 22 is shown in Figure 19 and Figure 20.

- The current waveform in the top and bottom FETs is a pulse with very high dI/dt, so the path to, through, and from each individual FET should be as short as possible and the two paths should be as similar as possible. In designs that use a pair of D-Paks or SO-8 FETs on one side of the PCB, it is best to counter-rotate the two so that the switch node is on one side of the pair and the high side drain can be bypassed to the low side source with a suitable ceramic bypass capacitor, placed as close as possible to the FETs in order to minimize inductance around this loop through the FETs and capacitor. The recommended bypass ceramic capacitor values range from 1 µF to 22 µF depending upon the output current. This bypass capacitor is usually connected to a larger value bulk filter capacitor and should be grounded to the PGND plane.
- GND, VCC bypass, PVCC bypass, soft start capacitor, and the bottom end of the output feedback divider resistors should be tied to an almost isolated, small AGND plane. All of these connections to the AGND plane should be kept as short as possible. No high current or high dI/dt signals should be connected to this AGND plane. The AGND area should be connected through one wide trace to the negative terminal of the output filter capacitors.
- The PGND pin handles high dI/dt gate drive current returning from the source of the low side MOSFET. The voltage at this pin also establishes the 0 V reference for the over-current limit protection (OCP) function and the CSL pin. A small PGND plane should connect the PGND pin and the PVCC bypass capacitor through a wide and direct path to the source of the low side MOSFET. The placement of $C_{IN}$ is critical for controlling ground bounce. The negative terminal of $C_{IN}$ needs to be placed very close to the source of the low-side MOSFET.
- Avoid long traces or large copper areas at the FB and CSL pins, which are low, signal-level inputs that are sensitive to capacitive and inductive noise pickup. It is best to position any series resistors and capacitors as closely as possible to these pins. Avoid running these traces close and parallel to high dI/dt traces.
- The switch node is the noisiest place in the switcher circuit with large ac and dc voltage and current. This node should be wide to keep resistive voltage drop down. But to minimize the generation of capacitively coupled noise, the total area should be small. Place the FETs and inductor close together on a small copper plane in order to minimize series resistance and keep the copper area small.
- Gate drive traces (DH and DL) handle high dI/dt and tend to produce noise and ringing. They should be as short and direct as possible. If possible, avoid using feed-through vias in the gate drive traces. If vias are needed, it is best to use two relatively large ones in parallel to reduce the peak current density and the current in each via. If the overall PCB layout is less than optimal, slowing down the gate drive slightly can be very helpful to reduce noise and ringing. It is occasionally helpful to place small value resistors (such as 5 Ω or 10 Ω) in series with the gate leads, mainly DH traces to the high side FET gates. These can be populated with 0 Ω resistors if resistance is not needed. Note that the added gate resistance increases the switching rise and fall times, and that also increases the switching power loss in the MOSFET.
- The negative terminal of output filter capacitors should be tied closely to the source of the low side FET. Doing this helps to minimize voltage difference between GND and PGND at the ADP1821.
- Generally be sure that all traces should be sized according to the current being handled as well as their sensitivity in the circuit. Standard PCB layout guidelines mainly address heating effects of current in a copper conductor. While these are completely valid, they do not fully cover other concerns such as stray inductance or dc voltage drop. Any dc voltage differential in connections between ADP1821 GND and the converter power output ground can cause a significant output voltage error, as it affects converter output voltage according to the ratio with the 600 mV feedback reference. For example, a 6 mV offset between ground on the ADP1821 and the converter power output causes a 1% error in the converter output voltage.

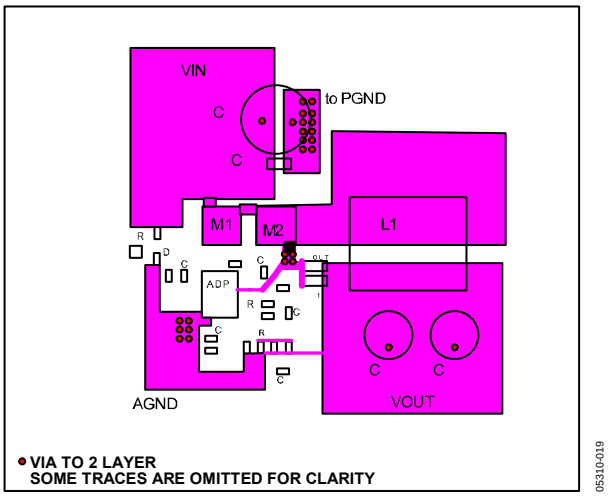



*Figure 19. Top Layer Layout Example of Circuit (see Figure 22)*

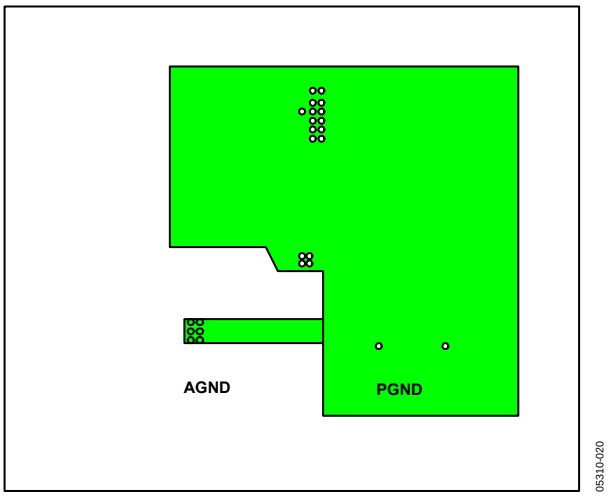



*Figure 20. Bottom Layer Layout Example of Circuit (See Figure 22)*

## RECOMMENDED COMPONENT MANUFACTURERS

**Table 4.**

| Vendor | Components |
|---|---|
| AVX Corporation | Capacitors |
| Central Semiconductor Corp. | Diodes |
| Coilcraft®, Inc. | Inductors |
| Diodes, Inc. | Diodes |
| International Rectifier | Diodes, MOSFETs |
| Murata Manufacturing Co., Ltd. | Capacitors, inductors |
| ON Semiconductor® | Diodes, MOSFETs |
| Rubycon Corporation | Capacitors |
| Sanyo | Capacitors |
| Sumida Corporation | Inductors |
| Taiyo Yuden, Inc. | Capacitors, inductors |
| Toko America, Inc. | Inductors |
| United Chemi-Con, Inc. | Capacitors |
| Vishay Siliconix | Diodes, MOSFETs, resistors, capacitors |

# APPLICATION CIRCUITS

The ADP1821 controller can be configured to regulate an output with a load of more than 20 A if the power components, such as the inductor, MOSFETs, and the bulk capacitors, are chosen carefully to meet the power requirement. The maximum load and power dissipation are limited by the power-train components. Figure 1 shows a typical application circuit that can drive an output load of 20 A. Note that two low-side MOSFETs are needed to deliver the 20 A load. In this example, two power rails are needed: a 5 V bias supply, which needs to supply about 30 mA to power the ADP1821 at full load, and a power input rail, which ranges from 2.5 V to 20 V. The bulk input and output capacitors used in this example are Sanyo's OSCON™ capacitors, which have low ESR and high-current ripple rating. An alternative to the OSCON capacitors are the polymer aluminum capacitors that are available from other manufacturers such as United Chemi-Con. Aluminum electrolytic capacitors, such as Rubycon's ZLG low-ESR series, can also be paralleled up at the input or output to meet the current ripple requirement. Since the aluminum electrolytic capacitors have higher ESR and much larger variation in capacitance over the operating temperature range, a larger bulk input and output capacitance is needed to reduce the effective ESR and suppress the current ripple.

The ADP1821 can be configured to drive an output load of less than 1 A. Figure 21 shows a typical application circuit that drives a 3 A load in an all multilayer ceramic capacitor (MLCC) solution. Notice that the two MOSFETs used in this example are dual-channel MOSFETs in a PowerPAK® SO-8 package, which reduces cost and saves layout space. For input voltages less than 3.7 V, it is recommended to use MOSFETs that are fully turned on at $V_{GS}$ less than 3 V. Because there's a forward voltage ($V_F$) drop across the Schottky diode D1, for input voltages less than 3.3 V, the effective voltage to the internal gate drivers may not be enough to drive a large load at the output. A Schottky diode with $V_F$ less than 0.5 V at $I_F$ of 100 mA is recommended for input voltages less than 3.3 V.

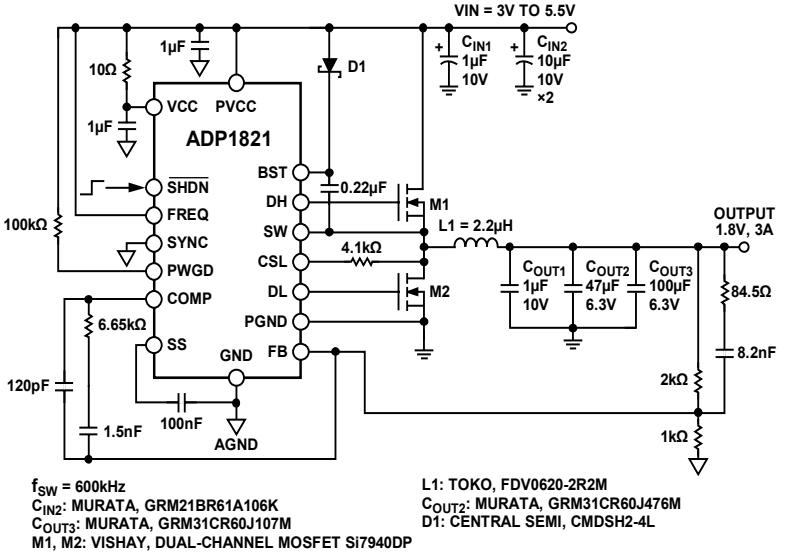



*Figure 21. Typical Application Circuit with all Multilayer Ceramic Capacitors (MLCC), 3.3 V to 5 V Input*

The ADP1821 can also be configured to run with an input voltage higher than 5.5 V. Figure 22 shows a typical application circuit that operates from a 12 V input. An external LDO is built, with a NPN, a 5.6 V Zener diode and a resistor, to step down the input voltage from 12 V to 5 V to power the ADP1821. These external signal components are cheap and small in size. Alternatively, LDOs such as the ADP3300 or the ADP3330 in a small SOT-23 package can be used for input voltages up to 12 V.

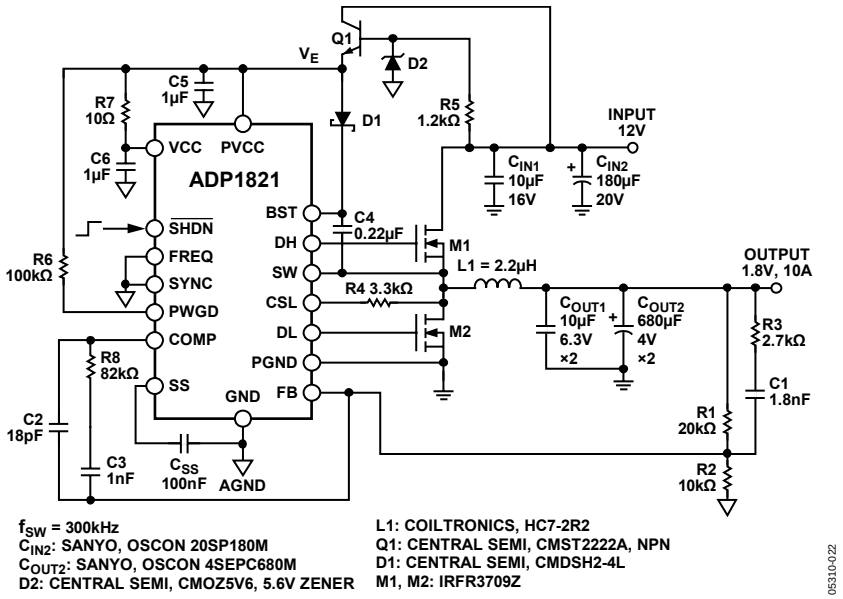



*Figure 22. Typical Application Circuit, 12 V Input*

# SUMMARY OF EQUATIONS

The following equations are for the reference and convenience of the user. Equations are replicated from the Compensating the Voltage Mode Buck Regulator section.

## COMPENSATION EQUATIONS

See the Compensating the Voltage Mode Buck Regulator section.

$$f_{CO} = \frac{f_{SW}}{10}$$

$$f_{LC} = \frac{1}{2\pi\sqrt{LC}}$$

$$f_{ESR} = \frac{1}{2\pi R_{ESR} C_{OUT}}$$

$$A_{FILTER} = -40\ \text{dB} \times \log\left(\frac{f_{ESR}}{f_{LC}}\right) - 20\ \text{dB} \times \log\left(\frac{f_{CO}}{f_{ESR}}\right)$$

$$A_{MOD} = 20 \log\left(\frac{V_{IN}}{V_{RAMP}}\right)$$

$$\varphi_{ESR} = 45 \times \log\frac{10 \times f_{CO}}{f_{ESR}}$$

$$\varphi_B = 150 - \varphi_{ESR}$$

If $\varphi_{ESR} \geq 70$, use Type II compensation.

If $\varphi_{ESR} < 70$, use Type III compensation.

## TYPE II COMPENSATION EQUATIONS

See the Type II Compensator section.

$$K = \tan\left(\frac{\phi_B}{2} + 45\right)$$

$$f_Z = \frac{f_{CO}}{K}$$

$$f_P = f_{CO} K$$

Select $R_{TOP}$ between 1 k and 10 k; a good starting value is 2 k.

$$R_{BOT} = \frac{V_{FB} R_{TOP}}{V_{OUT} - V_{FB}}$$

$$A_{COMP} = 0\ \text{dB} - A_{MOD} - A_{FILTER}$$

$$R_Z = R_{TOP} \times 10^{\left(\frac{A_{COMP}}{20}\right)}$$

$$C_I = \frac{1}{2\pi R_Z f_Z}$$

$$C_{HF} = \frac{1}{2\pi R_Z f_P}$$

## TYPE III COMPENSATION EQUATIONS

See the Type III Compensator section.

$$K = \left(\tan\left(\frac{\varphi_B}{2} + 45\right)\right)^2$$

$$f_Z = \frac{f_{CO}}{\sqrt{K}}$$

$$f_P = f_{CO} \sqrt{K}$$

Select $R_{TOP}$ between 1 k and 10 k. A good starting value is 2 k.

$$R_{BOT} = \frac{0.6\ V \times R_{TOP}}{V_{OUT} - 0.6\ V}$$

$$C_{FF} = \frac{1}{2\pi R_{TOP} f_Z}$$

$$R_{FF} = \frac{1}{2\pi C_{FF} f_P}$$

$$Z_{FF} = \frac{1}{2\pi C_{FF} f_{CO}} + R_{FF}$$

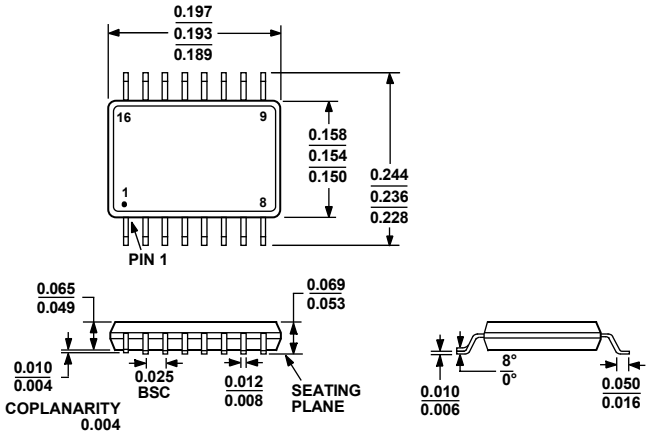
$$A_{COMP} = 0\ \text{dB} - A_{MOD} - A_{FILTER}$$

$$R_Z = \left(R_{TOP} \,||\, Z_{FF}\right) \times 10^{\left(\frac{A_{COMP}}{20}\right)}$$

$$C_I = \frac{1}{2\pi R_Z f_Z}$$

$$C_{HF} = \frac{1}{2\pi R_Z f_P}$$

# OUTLINE DIMENSIONS




COMPLIANT TO JEDEC STANDARDS MO-137-AB

*Figure 23. 16-Lead Shrink Small Outline Package [QSOP]*
*(RQ-16)*
*Dimensions shown in inches*

## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option | Quantity |
|---|---|---|---|---|
| ADP1821ARQZ-R7[1] | –40°C to +85°C | 16-Lead Shrink Small Outline Package [QSOP] | RQ-16 | 1000 |
| ADP1821-EVAL | | Evaluation Board | | |

[1] Z = Pb-free part.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