AC'97 SoundMAX® Codec

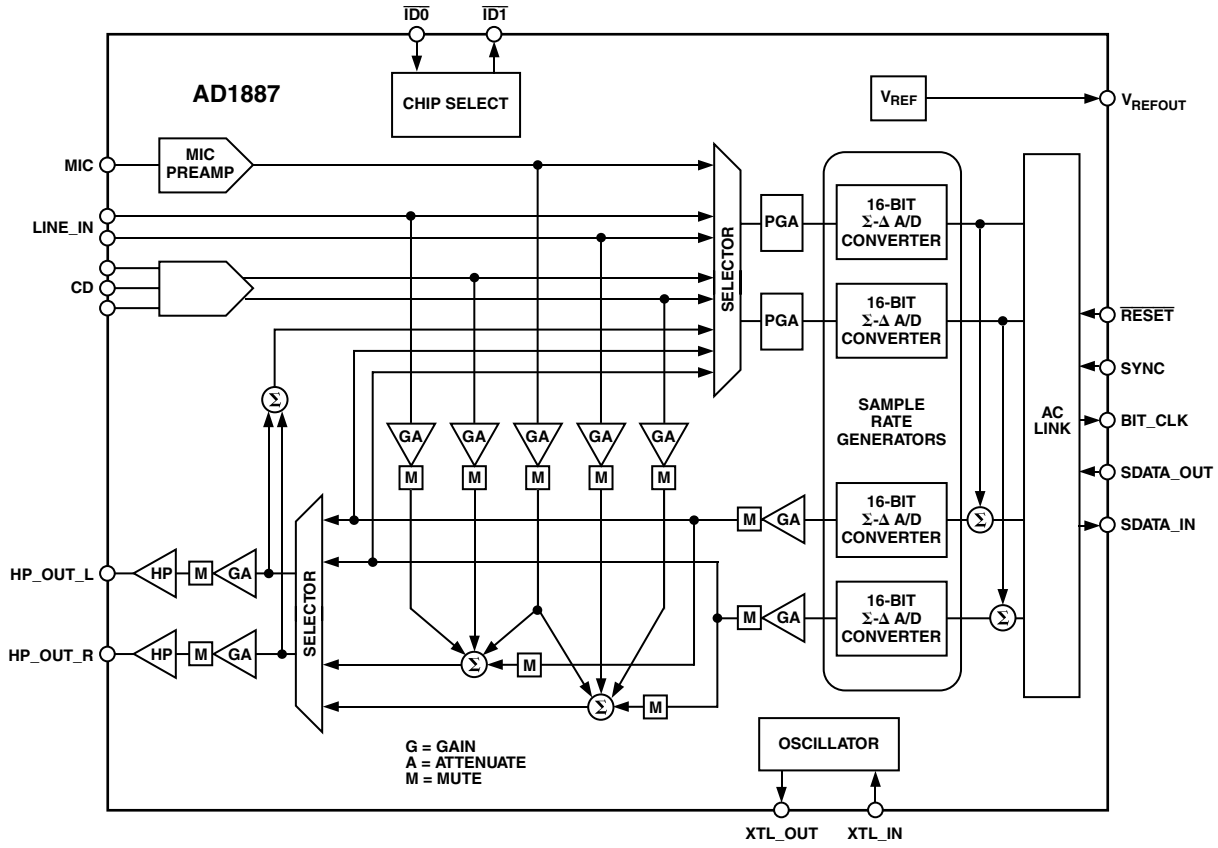
AD1887

AC'97 2.1 FEATURES
Variable Sample Rate Audio

AC'97 FEATURES
AC'97 2.2 Compliant
Greater than 90 dB Dynamic Range
Integrated Stereo Headphone Amplifier
Multibit Σ-Δ Converter Architecture for Improved S/N Ratio Greater than 90 dB
16-Bit Stereo Full-Duplex Codec
Two Analog Line-Level Stereo Inputs for: LINE-IN and CD
Mono MIC Input with Built-In Programmable Preamp
High-Quality CD Input with Ground Sense
Power Management Support
48-Terminal TQFP Package

ENHANCED FEATURES
Full Duplex Variable Sample Rates from 7040 Hz to 48 kHz with 1 Hz Resolution
Software-Enabled V_{REFOUT} Output for Microphones and External Power Amp
Split Power Supplies (3.3 V Digital/5 V Analog)
Mobile Low-Power Mixer Mode
Extended 6-Bit Headphone Volume Control
Digital Audio Mixer Mode

FUNCTIONAL BLOCK DIAGRAM



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REV. 0

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AD1887–SPECIFICATIONS

STANDARD TEST CONDITIONS UNLESS OTHERWISE NOTED

Temperature	25°C	*DAC Test Conditions*
Digital Supply (V_{DD})	3.3 V	Calibrated
Analog Supply (V_{CC})	5.0 V	–3 dB Attenuation Relative to Full Scale
Sample Rate (f_S)	48 kHz	Input 0 dB
Input Signal	1008 Hz	32 Ω Output Load (HP_OUT)
Analog Output Pass Band	20 Hz to 20 kHz	
V_{IH}	2.0 V	*ADC Test Conditions*
V_{IL}	0.8 V	Calibrated
V_{IH} (CS0, CS1)	4.0 V	0 dB Gain
V_{IL}	1.0 V	Input –3.0 dB Relative to Full Scale

ANALOG INPUT

Parameter	Min	Typ	Max	Unit
Input Voltage (RMS Values Assume Sine Wave Input)				
LINE_IN, CD		1		V rms
		2.83		V p-p
MIC with 20 dB Gain		0.1		V rms
		0.283		V p-p
MIC with 0 dB Gain		1		V rms
		2.83		V p-p
Input Impedance*		20		kΩ
Input Capacitance*		5	7.5	pF

HEADPHONE OUT VOLUME

Parameter	Min	Typ	Max	Unit
Step Size (+6 dB to –88.5 dB); HP_OUT_R, HP_OUT_L		1.5		dB
Output Attenuation Range Span*		–94.5		dB
Mute Attenuation of 0 dB Fundamental*			80	dB

PROGRAMMABLE GAIN AMPLIFIER—ADC

Parameter	Min	Typ	Max	Unit
Step Size (0 dB to 22.5 dB)		1.5		dB
PGA Gain Range Span		22.5		dB

ANALOG MIXER—INPUT GAIN/AMPLIFIERS/ATTENUATORS

Parameter	Min	Typ	Max	Unit
Signal-to-Noise Ratio (SNR)				
CD to HP_OUT		90		dB
Other to HP_OUT		90		dB
Step Size (+12 dB to –34.5 dB): (All Steps Tested)				
MIC, LINE_IN, CD, DAC		1.5		dB
Input Gain/Attenuation Range:				
MIC, LINE_IN, CD, DAC		–46.5		dB

DIGITAL DECIMATION AND INTERPOLATION FILTERS*

Parameter	Min	Typ	Max	Unit
Pass Band	0		$0.4 \times f_S$	Hz
Pass-Band Ripple			±0.09	dB
Transition Band	$0.4 \times f_S$		$0.6 \times f_S$	Hz
Stop Band	$0.6 \times f_S$		∞	Hz
Stop-Band Rejection	–74			dB
Group Delay			$12/f_S$	sec
Group Delay Variation over Pass Band			0.0	µs

*Guaranteed but not tested.

ANALOG-TO-DIGITAL CONVERTERS

Parameter	Min	Typ	Max	Unit
Resolution		16		Bits
Total Harmonic Distortion (THD)		–84		dB
Dynamic Range (–60 dB Input THD + N Referenced to Full Scale, A-Weighted)	84	87		dB
Signal-to-Intermodulation Distortion* (CCIF Method)		85		dB
ADC Crosstalk*				
Line Inputs (Input L, Ground R, Read R; Input R, Ground L, Read L)		–100	–90	dB
LINE_IN to Other		–90	–85	dB
Gain Error (Full-Scale Span Relative to Nominal Input Voltage)			±10	%
Interchannel Gain Mismatch (Difference of Gain Errors)			±0.5	dB
ADC Offset Error			±5	mV

DIGITAL-TO-ANALOG CONVERTERS

Parameter	Min	Typ	Max	Unit
Resolution		16		Bits
Total Harmonic Distortion (THD) HP_OUT		–75		dB
Dynamic Range (–60 dB Input THD + N Referenced to Full Scale, A-Weighted)	85	90		dB
Signal-to-Intermodulation Distortion* (CCIF Method)		–100		dB
Gain Error (Full-Scale Span Relative to Nominal Input Voltage)		±10		%
Interchannel Gain Mismatch (Difference of Gain Errors)			±0.7	dB
DAC Crosstalk* (Input L, Zero R, Measure R_OUT; Input R, Zero L, Measure L_OUT)			–80	dB
Total Audible Out-of-Band Energy (Measured from $0.6 \times f_S$ to 20 kHz)*		–40		dB

ANALOG OUTPUT

Parameter	Min	Typ	Max	Unit
Full-Scale Output Voltage; HP_OUT		1		V rms
		2.83		V p-p
Output Impedance*			800	Ω
External Load Impedance*	32			Ω
Output Capacitance*			15	pF
External Load Capacitance			100	pF
V_{REF}	2.05	2.25	2.45	V
V_{REF_OUT}		2.25		V
V_{REF_OUT} Current Drive			5	mA
Mute Click (Muted Output Minus Unmuted Midscale DAC Output)		±5		mV

STATIC DIGITAL SPECIFICATIONS

Parameter	Min	Typ	Max	Unit
High-Level Input Voltage (V_{IH}): Digital Inputs	$0.65 \times DV_{DD}$			V
Low-Level Input Voltage (V_{IL})			$0.35 \times DV_{DD}$	V
High-Level Output Voltage (V_{OH}), I_{OH} = 2 mA	$0.9 \times DV_{DD}$			V
Low-Level Output Voltage (V_{OL}), I_{OL} = 2 mA			$0.1 \times DV_{DD}$	V
Input Leakage Current	–10		+10	µA
Output Leakage Current	–10		+10	µA

POWER SUPPLY

Parameter	Min	Typ	Max	Unit
Power Supply Range—Analog (AV_{DD})	4.75		5.25	V
Power Supply Range—Digital (DV_{DD})	3.15		3.45	V
Power Dissipation—5 V/3.3 V		253		mW
Analog Supply Current—5 V (AV_{DD})		36		mA
Digital Supply Current—3.3 V (DV_{DD})		22		mA
Power Supply Rejection (100 mV p-p Signal @ 1 kHz)* (At Both Analog and Digital Supply Pins, Both ADCs and DACs)		40		dB

*Guaranteed but not tested.

AD1887–SPECIFICATIONS

CLOCK SPECIFICATIONS*

Parameter	Min	Typ	Max	Unit
Input Clock Frequency		24.576		MHz
Recommended Clock Duty Cycle	40	50	60	%

POWER-DOWN STATES

Parameter	Set Bits	DV_{DD} Typ	AV_{DD} Typ	Unit
ADC	PR0	15.82	30.0	mA
DAC	PR1	15.08	26.3	mA
ADC + DAC	PR1, PR0	3.79	19.9	mA
ADC + DAC + Mixer (Analog CD On)	LPMIX, PR1, PR0	3.85	18.1	mA
Mixer	PR2	17.65	17.4	mA
ADC + Mixer	PR2, PR0	15.70	11.1	mA
DAC + Mixer	PR2, PR1	15.07	8.3	mA
ADC + DAC + Mixer	PR2, PR1, PR0	3.80	2.1	mA
Analog CD Only (AC-Link On)	LPMIX, PR5, PR1, PR0	3.85	18.1	mA
Analog CD Only (AC-Link Off)	LPMIX, PR1, PR0, PR4, PR5	0.06	18.1	mA
Standby	PR5, PR4, PR3, PR2, PR1, PR0	0.06	0	mA
Headphone Standby	PR6	17.66	26.1	mA

*Guaranteed but not tested.

Specifications subject to change without notice.

TIMING PARAMETERS (GUARANTEED OVER OPERATING TEMPERATURE RANGE)

Parameter	Symbol	Min	Typ	Max	Unit
RESET Active Low Pulsewidth	t_{RST_LOW}		1.0		µs
RESET Inactive to BIT_CLK Startup Delay	$t_{RST2CLK}$	162.8			ns
SYNC Active High Pulsewidth	t_{SYNC_HIGH}		1.3		µs
SYNC Low Pulsewidth	t_{SYNC_LOW}		19.5		µs
SYNC Inactive to BIT_CLK Startup Delay	$t_{SYNC2CLK}$	162.8			ns
BIT_CLK Frequency			12.288		MHz
BIT_CLK Period	t_{CLK_PERIOD}		81.4		ns
BIT_CLK Output Jitter*				750	ps
BIT_CLK High Pulsewidth	t_{CLK_HIGH}	32.56	42	48.84	ns
BIT_CLK Low Pulsewidth	t_{CLK_LOW}	32.56	38	48.84	ns
SYNC Frequency			48.0		kHz
SYNC Period	t_{SYNC_PERIOD}		20.8		µs
Setup to Falling Edge of BIT_CLK	t_{SETUP}	5	2.5		ns
Hold from Falling Edge of BIT_CLK	t_{HOLD}	5			ns
BIT_CLK Rise Time	$t_{RISECLK}$	2	4	6	ns
BIT_CLK Fall Time	$t_{FALLCLK}$	2	4	6	ns
SYNC Rise Time	$t_{RISESYNC}$	2	4	6	ns
SYNC Fall Time	$t_{FALLSYNC}$	2	4	6	ns
SDATA_IN Rise Time	$t_{RISEDIN}$	2	4	6	ns
SDATA_IN Fall Time	$t_{FALLDIN}$	2	4	6	ns
SDATA_OUT Rise Time	$t_{RISEDOUT}$	2	4	6	ns
SDATA_OUT Fall Time	$t_{FALLDOUT}$	2	4	6	ns
End of Slot 2 to BIT_CLK, SDATA_IN Low	t_{S2_PDOWN}	0		1.0	µs
Setup to Trailing Edge of RESET (Applies to SYNC, SDATA_OUT)	$t_{SETUP2RST}$	15			ns
Rising Edge of RESET to HI-Z Delay	t_{OFF}			25	ns
Propagation Delay				15	ns
RESET Rise Time				50	ns
Output Valid Delay from Rising Edge of BIT_CLK to SDI Valid				15	ns

*Output jitter is directly dependent on crystal input jitter.

Specifications subject to change without notice.

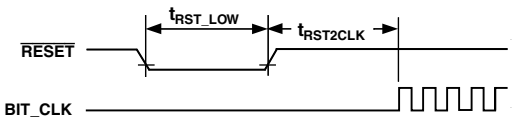


Figure 1. Cold Reset

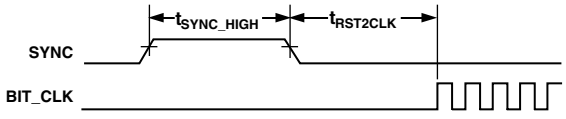


Figure 2. Warm Reset

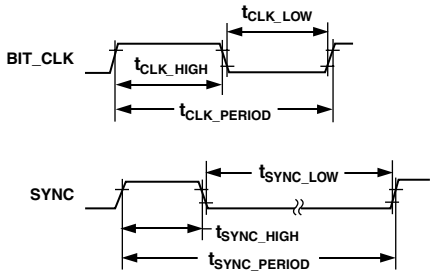


Figure 3. Clock Timing

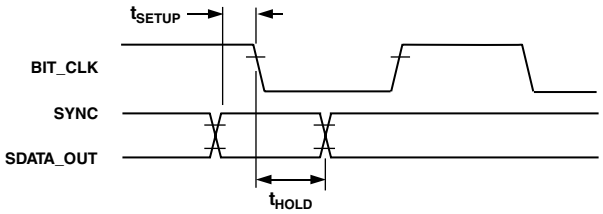


Figure 4. Data Setup and Hold

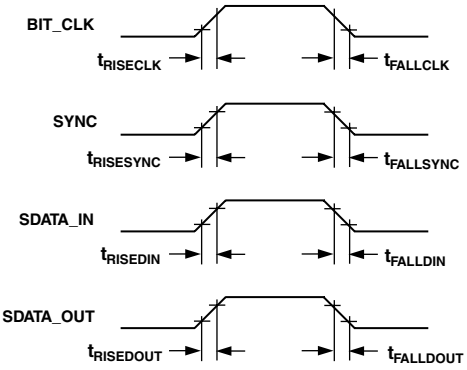


Figure 5. Signal Rise and Fall Time

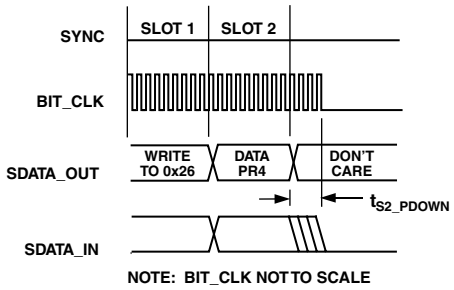


Figure 6. AC Link Low Power Mode Timing

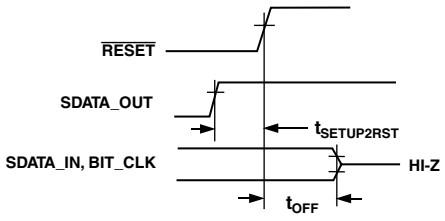


Figure 7. ATE Test Mode

ABSOLUTE MAXIMUM RATINGS*

Parameter	Min	Max	Unit
Power Supplies			
Digital (DV_{DD})	–0.3	+3.6	V
Analog (AV_{CC})	–0.3	+6.0	V
Input Current (Except Supply Pins)		±10.0	mA
Analog Input Voltage (Signal Pins)	–0.3	AV_{DD} + 0.3	V
Digital Input Voltage (Signal Pins)	–0.3	DV_{DD} + 0.3	V
Ambient Temperature (Operating)	0	70	°C
Storage Temperature	–65	+150	°C

*Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD1887JST	0°C to 70°C	Thin-Quad Flatpack	ST-48

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating

$T_{AMB} = T_{CASE} - (P_D \times \theta_{CA})$

T_{CASE} = Case Temperature in °C

P_D = Power Dissipation in W

θ_{CA} = Thermal Resistance (Case-to-Ambient)

θ_{JA} = Thermal Resistance (Junction-to-Ambient)

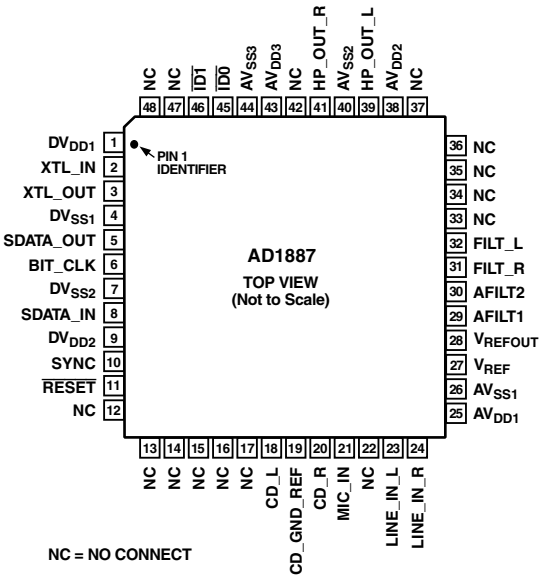
θ_{JC} = Thermal Resistance (Junction-to-Case)

Package	θ_{JA}	θ_{JC}	θ_{CA}
TQFP	76.2°C/W	17°C/W	59.2°C/W

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1887 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Digital I/O

Pin Name	TQFP	I/O	Description
XTL_IN	2	I	Crystal (or Clock) Input, 24.576 MHz
XTL_OUT	3	O	Crystal Output
SDATA_OUT	5	I	AC-Link Serial Data Output, AD1887 Input Stream
BIT_CLK	6	O/I	AC-Link Bit Clock 12288 MHz Serial Data Clock Daisy Chain Output Clock
SDATA_IN	8	O	AC-Link Serial Data Input AD1887 Output Stream
SYNC	10	I	AC-Link Frame Sync
$\overline{\text{RESET}}$	11	I	AC-Link Reset AD1887 Master H/W Reset

Chip Selects

Pin Name	TQFP	Type	Description
$\overline{\text{ID0}}$	45	I	Chip Select Input 0 (Active Low)
$\overline{\text{ID1}}$	46	I	Chip Select Input 1 (Active Low)

Analog I/O

These signals connect the AD1887 component to analog sources and sinks, including microphones and speakers

Pin Name	TQFP	I/O	Description
CD_L	18	I	CD Audio Left Channel
CD_GND_REF	19	I	CD Audio Analog Ground Reference for Differential CD Input
CD_ R	20	I	CD Audio Right Channel
MIC	21	I	Microphone Input
LINE_IN_L	23	I	Line in Left Channel
LINE_IN_R	24	I	Line in Right Channel
HP_OUT_L	39	O	Headphones Out Left Channel
HP_OUT_R	41	O	Headphones Out Right Channel

Filter/Reference

These signals are connected to resistors, capacitors, or specific voltages

Pin Name	TQFP	I/O	Description
V_{REF}	27	O	Voltage Reference Filter
V_{REFOUT}	28	O	Voltage Reference Output 5 mA Drive (Intended for Mic Bias)
AFILT1	29	O	Antialiasing Filter Capacitor—ADC Right Channel
AFLIT2	30	O	Antialiasing Filter Capacitor—ADC Left Channel
FILT_R	31	O	AC-Coupling Filter Capacitor—ADC Right Channel
FILT_L	32	O	AC-Coupling Filter Capacitor—ADC Left Channel

Power and Ground Signals

Pin Name	TQFP	Type	Description
$DV_{DD}1$	1	I	Digital V_{DD} 33 V
$DV_{SS}1$	4	I	Digital GND
$DV_{SS}2$	7	I	Digital GND
$DV_{DD}2$	9	I	Digital V_{DD} 33 V
$AV_{DD}1$	25	I	Analog V_{DD} 50 V
$AV_{SS}1$	26	I	Analog GND
$AV_{DD}2$	38	I	Analog V_{DD} 50 V
$AV_{SS}2$	40	I	Analog GND
$AV_{DD}3$	43	I	Analog V_{DD} 50 V
$AV_{SS}3$	44	I	Analog GND

No Connects

Pin Name	TQFP	Type	Description
NC	12		No Connect
NC	13		No Connect
NC	14		No Connect
NC	15		No Connect
NC	16		No Connect
NC	17		No Connect
NC	22		No Connect
NC	33		No Connect
NC	34		No Connect
NC	35		No Connect
NC	36		No Connect
NC	37		No Connect
NC	42		No Connect
NC	47		No Connect
NC	48		No Connect

Indexed Control Registers

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	X	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	0010h
04h	Headphones Volume	HPM	X	LHV5	LHV4	LHV3	LHV2	LHV1	LHV0	X	X	RHV5	RHV4	RHV3	RHV2	RHV1	RHV0	8000h
08h	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
00Eh	Mic Volume	MCM	X	X	X	X	X	X	X	X	M30	X	MCV4	MCV3	MCV2	MCV1	MCV0	8008h
10h	Line-In Volume	LM	X	X	LLV4	LLV3	LLV2	LLV1	LLV0	X	X	X	RLV4	RLV3	RLV2	RLV1	RLV0	8808h
12h	CD Volume	CVM	X	X	LCV4	LCV3	LCV2	LCV1	LCV0	X	X	X	RCV4	RCV3	RCV2	RCV1	RCV0	8808h
18h	PCM Out Vol	OM	X	X	LOV4	LOV3	LOV2	LOV1	LOV0	X	X	X	ROV4	ROV3	ROV2	ROV1	ROV0	8808h
1Ah	Record Select	X	X	X	X	X	LS2	LS1	LS0	X	X	X	X	X	RS2	RS1	RS0	0000h
1Ch	Record Gain	IM	X	X	X	LIM3	LIM2	LIM1	LIM0	X	X	X	X	RIM3	RIM2	RIM1	RIM0	8000h
20h	General-Purpose	X	X	X	X	X	X	X	X	LPBK	X	X	X	X	X	X	X	0000h
26h	Power-Down Ctrl/Stat	X	X	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	000Xh
28h	Ext'd Audio ID	ID1	ID0	X	X	X	X	X	X	X	X	X	X	X	X	X	VRA	0005h
2Ah	Ext'd Audio Stat/Ctrl	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	VRA	0000h
2Ch/ (7Ah)*	PCM DAC Rate (SR1)	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
32h/ (78h)*	PCM ADC Rate (SR0)	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
74h	Serial Configuration	SLOT16	REGM2	REGM1	REGM0	X	X	X	X	X	X	X	X	X	X	X	X	7000h
76h	Misc Control Bits	DACZ	LPMIX	X	DAM	DMS	DLSR	X	ALSR	MOD EN	SRX10 D7	SRX8 D7	X	X	DRSR	X	ARSR	0404h
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	4144h
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	5362h

NOTES
All registers not shown and bits containing an X are assumed to be reserved.
Odd register addresses are aliased to the next lower even address.
Reserved registers should not be written.
Zeros should be written to reserved bits.
*Indicates Aliased register for AD1819, AD1819A backward compatibility.

Reset (Index 00h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	X	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	0010h

Note: Writing any value to this register performs a register reset, which causes all registers to revert to their default values (except 74h, which forces the serial configuration). Reading this register returns the ID code of the part and a code for the type of 3D Stereo Enhancement.

ID[9:0] Identify Capability. The ID decodes the capabilities of AD1887 based on the following:

Bit = 1	Function	AD1887*
ID0	Dedicated Mic PCM in Channel	0
ID1	Modem Line Codec Support	0
ID2	Bass and Treble Control	0
ID3	Simulated Stereo (Mono to Stereo)	0
ID4	Headphone Out Support	1
ID5	Loudness (Bass Boost) Support	0
ID6	18-Bit DAC Resolution	0
ID7	20-Bit DAC Resolution	0
ID8	18-Bit ADC Resolution	0
ID9	20-Bit ADC Resolution	0

*The AD1887 contains none of the optional features identified by these bits.

SE[4:0] Stereo Enhancement. The 3D stereo enhancement identifies the Analog Devices 3D stereo enhancement.

Headphones Volume Registers (Index 04h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
04h	Headphones Volume	HPM	X	LHV5	LHV4	LHV3	LHV2	LHV1	LHV0	X	X	RHV5	RHV4	RHV3	RHV2	RHV1	RHV0	8000h

RHV[5:0] Right Headphone Volume Control. The least significant bit represents 1.5 dB. This register controls the output from +6 dB to a maximum attenuation of –88.5 dB.

LHV[5:0] Left Headphone Volume Control. The least significant bit represents 1.5 dB. This register controls the output from +6 dB to a maximum attenuation of –88.5 dB.

HPM Headphones Volume Mute. When this bit is set to "1," the channel is muted.

HPM	xHV5 . . . xHV0	Function
0	00 0000	6 dB Gain
0	01 1111	–40.5 dB Attenuation
0	11 1111	–88.5 dB Attenuation
1	xx xxxx	–∞ dB Attenuation

Mic Volume (Index 0Eh)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0Eh	MIC Volume	MCM	X	X	X	X	X	X	X	X	M30	X	MCV4	MCV3	MCV2	MCV1	MCV0	8008h

MCV[4:0] Mic Volume Gain. Allows setting the Mic Volume attenuator in 32 steps. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.

M30 Mic Boost Gain: Amplifies the Mic input. 0 = 0 dB, 1 = 30 dB

MCM Mic Mute. When this bit is set to "1," the channel is muted.

Line In Volume (Index 10h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
10h	Line In Volume	LM	X	X	LLV4	LLV3	LLV2	LLV1	LLV0	X	X	X	RLV4	RLV3	RLV2	RLV1	RLV0	8808h

RLV[4:0] Right Line In Volume. Allows setting the Line In right channel attenuator in 32 steps. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.

LLV[4:0] Line In Volume Left. Allows setting the Line In left channel attenuator in 32 steps. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.

LM Line In Mute. When this bit is set to "1," the channel is muted.

CD Volume (Index 12h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
12h	CD Volume	CVM	X	X	LCV4	LCV3	LCV2	LCV1	LCV0	X	X	X	RCV4	RCV3	RCV2	RCV1	RCV0	8808h

RCV[4:0] Right CD Volume. Allows setting the CD right channel attenuator in 32 steps. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.

LCV[4:0] Left CD Volume. Allows setting the CD left channel attenuator in 32 steps. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.

CVM CD Volume Mute. When this bit is set to "1," the channel is muted.

PCM Out Volume (Index 18h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
18h	PCM Out Volume	OM	X	X	LOV4	LOV3	LOV2	LOV1	LOV0	X	X	X	ROV4	ROV3	ROV2	ROV1	ROV0	8808h

ROV[4:0] Right PCM Out Volume. Allows setting the PCM right channel attenuator in 32 steps. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.

LOV[4:0] Left PCM Out Volume. Allows setting the PCM left channel attenuator in 32 steps. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.

OM PCM Out Volume Mute. When this bit is set to "1," the channel is muted.

Volume Table (Index 0Ch to 18h)

Mute	x4 . . . x0	Function
0	00000	+12 dB Gain
0	01000	0 dB Gain
0	11111	–34.5 dB Gain
1	xxxxx	–∞ dB Gain

Record Select Control Register (Index 1Ah)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
1Ah	Record Select	X	X	X	X	X	LS2	LS1	LS0	X	X	X	X	X	RS2	RS1	RS0	0000h

RS[2:0] Right Record Select

LS[2:0] Left Record Select

Used to select the record source independently for right and left. See table for legend.

The default value is 0000h, which corresponds to Mic in.

LS2 . . . LS0	Left Record Source
0	MIC
1	CD_L
4	LINE_IN_L
5	Stereo Mix (L)
6	Mono Mix

RS2 . . . RS0	Right Record Source
0	MIC
1	CD_L
4	LINE_IN_R
5	Stereo Mix (R)
6	Mono Mix

Record Gain (Index 1Ch)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
1Ch	Record Gain	IM	X	X	X	LIM3	LIM2	LIM1	LIM0	X	X	X	X	RIM3	RIM2	RIM1	RIM0	8000h

RIM[3:0] Right Input Mixer Gain Control. Each LSB represents 1.5 dB, 0000 = 0 dB and the range is 0 dB to 22.5 dB.

LIM[3:0] Left Input Mixer Gain Control. Each LSB represents 1.5 dB, 0000 = 0 dB and the range is 0 dB to 22.5 dB.

IM Input Mute
0 = Unmuted
1 = Muted or –∞ dB Gain

IM	xIM3 . . . xIM0	Function
0	1111	22.5 dB Gain
0	0000	0 dB Gain
1	xxxxx	–∞ dB Gain

General Purpose Register (Index 20h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
20h	General Purpose	X	X	X	X	X	X	X	X	LPBK	X	X	X	X	X	X	X	0000h

Note: This register should be read before writing to generate a mask for only the bit(s) that need to be changed. The function default value is 0000h, which is all off.

LPBK Loopback Control. ADC/DAC digital loopback mode.

Subsection Ready Register (Index 26h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
26h	Power-Down Cntrl/Stat	X	PR6	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	NA

Note: The ready bits are read only, writing to REF, ANL, DAC, ADC will have no effect. These bits indicate the status for the AD1887 subsections. If the bit is a one, that subsection is "ready." Ready is defined as the subsection able to perform in its nominal state.

ADC ADC section ready to transmit data.

DAC DAC section ready to accept data.

ANL Analog gainuators, attenuators, and mixers ready.

REF Voltage References, V_{REF} and V_{REFOUT} up to nominal level.

PR[5:0] AD1887 Power-Down Modes. The first three bits are to be used individually rather than in combination with each other. The last bit, PR3, can be used in combination with PR2 or by itself. The mixer and reference cannot be powered down via PR3 unless the ADCs and DACs are also powered down. Nothing else can be powered up until the reference is up.

PR0 – Powered-Down ADC
PR1 – Powered-Down DAC
PR2 – Powered-Down Analog Mixer
PR3 – Powered-Down V_{REF} and V_{REFOUT}
PR4 – Powered-Down AC-Link
PR5 – Powered-Down Internal Clock
PR6 – Powered-Down Headphone
PR5 has no effect unless all ADCs, DACs, and the AC-Link are powered down. The reference and the mixer can be either up or down, but all power-up sequences must be allowed to run to completion before PR5 and PR4 are both set.

In multiple-codec systems, the master codec's PR5 and PR4 bits control the slave codec. PR5 is also effective in the slave codec if the master's PR5 bit is clear, but the PR4 bit has no effect or disable PR5.

Power-Down State	PR6	PR5	PR4	PR3	PR2	PR1	PR0
ADC Power-Down	0	0	0	0	0	0	1
DACs Power-Down	0	0	0	0	0	1	0
ADC and DAC Power-Down	0	0	0	0	0	1	1
Mixer Power-Down	0	0	0	0	1	0	0
ADC + Mixer Power-Down	0	0	0	0	1	0	1
DAC + Mixer Power-Down	0	0	0	0	1	1	0
ADC + DAC + Mixer Power-Down	0	0	0	0	1	1	1
Standby	1	1	1	1	1	1	1

Extended Audio ID Register (Index 28h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
28h	Extended Audio ID	ID1	ID0	X	X	X	X	X	X	X	X	X	X	X	X	X	VRA	0001h

Note: The Extended Audio ID is a read only register.

VRA Variable Rate Audio. VRA = 1 indicates support for Variable Rate Audio.

ID[1:0] ID1, ID0 is a 2-bit field which indicates the codec configuration: Primary is 00; Secondary is 01, 10, or 11.

Extended Audio Status and Control Register (Index 2Ah)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
2Ah	Ext'd Audio Stat/Ctrl	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	VRA	0000h

Note: The Extended Audio Status and Control Register is a read/write register that provides status and control of the extended audio features.

VRA Variable Rate Audio. VRA = 1 indicates support for Variable Rate Audio mode (sample rate control registers and SLOTREQ signaling).

PCM DAC Rate Register (Index 2Ch)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
2Ch/(7Ah)	PCM DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h

Note: 2Ch is an alias for 7Ah. The VRA bit in register 2Ah must be set for the alias to work; if a zero is written to VRA then both sample rates are reset to 48 kHz.

SR[15:0] Writing to this register allows programming of the sampling frequency from 7 kHz (1B58h) to 48 kHz (BB80h) in 1 Hz increments. Programming a value outside of the range 7040 Hz (1b80h) to 48000 Hz (bb80h) causes the codec to saturate. For all rates, if the value written to the register is supported that value will be echoed back when read, otherwise the closest rate supported is returned.

PCM ADC Rate Register (Index 32h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
32h/(78h)	PCM ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h

Note: 32h is an alias for 78h. The VRA bit in register 2Ah must be set for the alias to work; if a zero is written to VRA then both sample rates are reset to 48 kHz.

SR[15:0] Writing to this register allows programming of the sampling frequency from 7 kHz (1B58h) to 48 kHz (BB80h) in 1 Hz increments. Programming a value outside of the range 7040 Hz (1b80h) to 48000 Hz (bb80h) causes the codec to saturate. For all rates, if the value written to the register is supported that value will be echoed back when read, otherwise the closest rate supported is returned.

Serial Configuration (Index 74h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
74h	Serial Configuration	SLOT 16	REGM2	REGM1	REGM0	X	X	X	X	X	X	X	X	X	X	X	X	7000h

Note: This register is not reset when the reset register (Register 00h) is written.

DHWR Disable Hardware Reset.

REGM0 Master Codec Register Mask.

REGM1 Slave 1 Codec Register Mask.

REGM2 Slave 2 Codec Register Mask.

SLOT16 Enable 16-bit slots.

If your system uses only a single AD1887, you can ignore the register mask bits.

SLOT16 makes all AC Link slots 16 bits in length, formatted into 16 slots.

Miscellaneous Control Bits (Index 76h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
76h	Misc Control Bits	DACZ	LPMIX	X	DAM	DMS	DLSR	X	ALSR	MOD EN	SRX10 D7	SRX8 D7	X	X	DRSR	X	ARSR	0404h

ARSR ADC Right Sample Generator Select
0 = SR0 Selected (32h)
1 = SR1 Selected (2Ch)

DRSR DAC Right Sample Generator Select
0 = SR0 Selected (32h)
1 = SR1 Selected (2Ch)

SRX8D7 Multiply SR1 rate by 8/7.

SRX10D7 Multiply SR1 rate by 10/7. SRX10D7 and SRX8D7 are mutually exclusive; SRX10D7 has priority if both are set.

MODEN Modem filter enable (left channel only). Change only when DACs are powered down.

ALSR ADC Left Sample Generator Select
0 = SR0 Selected (32h)
1 = SR1 Selected (2Ch)

DLSR DAC Left Sample Generator Select
0 = SR0 Selected (32h)
1 = SR1 Selected (2Ch)

DMS Digital Mono Select
0 = Mixer
1 = Left DAC + Right DAC

DAM Digital Audio Mode. DAC Outputs bypass analog mixer and sent directly to the codec output.

LPMIX Low-Power Mixer

DACZ Zero-fill (vs. repeat) if DAC is starved for data.

Sample Rate 0 (Index 78h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
(32h)/78h	Sample Rate 0	SR015	SR014	SR013	SR012	SR011	SR010	SR09	SR08	SR07	SR06	SR05	SR04	SR03	SR02	SR01	SR00	BB80h

Note: 32h is an alias for 78h. The VRA bit in Register 2Ah must be set for the alias to work; if a zero is written to VRA then both sample rates are reset to 48 kHz.

SR0[15:0] Writing to this register allows the user to program the sampling frequency from 7 kHz (1B58h) to 48 kHz (BB80h) in 1 Hertz increments. Programming a value greater than 48 kHz or less than 7 kHz may cause unpredictable results.

Sample Rate 1 (Index 7Ah)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
(2Ch)/7Ah	Sample Rate 1	SR115	SR114	SR113	SR112	SR111	SR110	SR19	SR18	SR17	SR16	SR15	SR14	SR13	SR12	SR11	SR10	BB80h

Note: 2Ch is an alias for 7Ah. The VRA bit in Register 2Ah must be set for the alias to work; if a zero is written to VRA then both sample rates are reset to 48 kHz.

SR1[15:0] Writing to this register allows the user to program the sampling frequency from 7 kHz (1B58h) to 48 kHz (BB80h) in 1 Hertz increments. Programming a value greater than 48 kHz or less than 7 kHz may cause unpredictable results.

Vendor ID Registers (Index 7Ch–7Eh)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	4144h

S[7:0] This register is ASCII encoded to ‘A.’

F[7:0] This register is ASCII encoded to ‘D.’

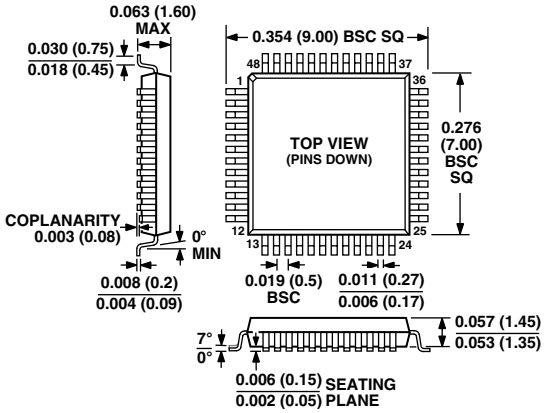
Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	5362h

T[7:0] This register is ASCII encoded to ‘S.’

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

48-Lead Thin Plastic Quad Flatpack (LQFP)
(ST-48)



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