# Microprocessor Supervisory Circuits

# ADM696/ADM697

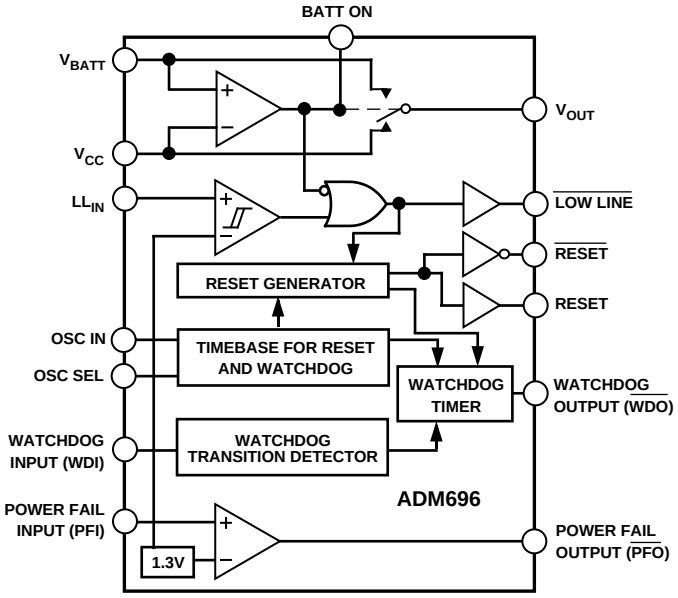
## FEATURES

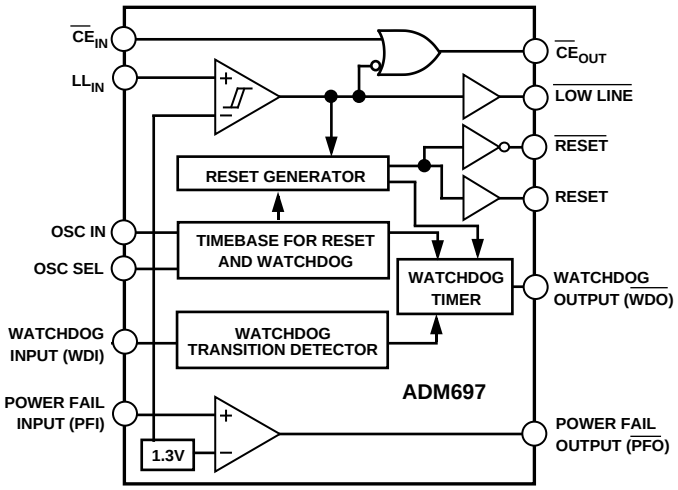
**Superior Upgrade for MAX696/MAX697**
**Specified Over Temperature**
**Adjustable Low Line Voltage Monitor**
**Power OK/Reset Time Delay**
**Reset Assertion Down to 1 V $V_{CC}$**
**Watchdog Timer—100 ms, 1.6 s, or Adjustable**
**Low Switch On Resistance**
**1.5 Ω Normal, 20 Ω in Backup**
**600 nA Standby Current**
**Automatic Battery Backup Switching (ADM696)**
**Fast On-Board Gating of Chip Enable Signals (ADM697)**
**Voltage Monitor for Power Fail or Low Battery Warning**

## APPLICATIONS

**Microprocessor Systems**
**Computers**
**Controllers**
**Intelligent Instruments**
**Automotive Systems**
**Critical μP Power Monitoring**

## FUNCTIONAL BLOCK DIAGRAMS




## GENERAL DESCRIPTION

The ADM696/ADM697 supervisory circuits offer complete single chip solutions for power supply monitoring and battery control functions in microprocessor systems. These functions include μP reset, backup-battery switchover, watchdog timer, CMOS RAM write protection, and power failure warning.

The ADM696/ADM697 are available in 16-pin DIP and small outline packages and provide the following functions:

1. Power-On Reset output during power-up, power-down and brownout conditions. The RESET voltage threshold is adjustable using an external voltage divider. The $\overline{\text{RESET}}$ output remains operational with $V_{CC}$ as low as 1 V.
2. A Reset pulse if the optional watchdog timer has not been toggled within specified time.
3. Separate watchdog time-out and low line status outputs.
4. Adjustable reset and watchdog timeout periods.
5. A 1.3 V threshold detector for power fail warning, low battery detection, or to monitor a power supply other than $V_{CC}$.
6. Battery backup switching for CMOS RAM, CMOS microprocessor or other low power logic (ADM696).
7. Write protection of CMOS RAM or EEPROM (ADM697).

The ADM696/ADM697 is fabricated using an advanced epitaxial CMOS process combining low power consumption (5 mW), extremely fast Chip Enable gating (5 ns) and high reliability. $\overline{\text{RESET}}$ assertion is guaranteed with $V_{CC}$ as low as 1 V. In addition, the power switching circuitry is designed for minimal voltage drop thereby permitting increased output current drive of up to 100 mA without the need for an external pass transistor.

REV. 0

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# ADM696/ADM697–SPECIFICATIONS

($V_{CC}$ = Full Operating Range, $V_{BATT}$ = +2.8 V, $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted.)

| Parameter | Min | Typ | Max | Units | Test Conditions/Comments |
|---|---|---|---|---|---|
| $V_{CC}$ Operating Voltage Range | 3.0 | | 5.5 | V | |
| $V_{BATT}$ Operating Voltage Range | 2.0 | | $V_{CC}$ – 0 3 | V | |
| BATTERY BACKUP SWITCHING (ADM696) | | | | | |
| $V_{OUT}$ Output Voltage | $V_{CC}$ – 0.05 | $V_{CC}$ – 0.025 | | V | $I_{OUT}$ = 1 mA |
| | $V_{CC}$ – 0.5 | $V_{CC}$ – 0.25 | | V | $I_{OUT}$ ≤ 100 mA |
| $V_{OUT}$ in Battery Backup Mode | $V_{BATT}$ – 0.05 | $V_{BATT}$ – 0.02 | | V | $I_{OUT}$ = 250 µA, $V_{CC}$ < $V_{BATT}$ – 0.2 V |
| Supply Current (Excludes $I_{OUT}$) | | 1 | 1.95 | mA | $I_{OUT}$ = 100 mA |
| Supply Current in Battery Backup Mode | | 0.6 | 1 | µA | $V_{CC}$ = 0 V, $V_{BATT}$ = 2.8 V |
| Battery Standby Current | | | | | 5.5 V > $V_{CC}$ > $V_{BATT}$ + 0.2 V |
| (+ = Discharge, – = Charge) | –0.1 | | +0.02 | µA | $T_A$ = +25°C |
| | –1 | | +0.02 | µA | |
| Battery Switchover Threshold | | 70 | | mV | Power-Up |
| $V_{CC}$ – $V_{BATT}$ | | 50 | | mV | Power-Down |
| Battery Switchover Hysteresis | | 20 | | mV | |
| BATT ON Output Voltage | | | 0.4 | V | $I_{SINK}$ = 1.6 mA |
| BATT ON Output Short Circuit Current | | 7 | | mA | BATT ON = $V_{OUT}$ = 2.4 V Sink Current |
| | 0.5 | 1 | 25 | µA | BATT ON = $V_{OUT}$, $V_{CC}$ = 0 V, Source Current |
| RESET AND WATCHDOG TIMER | | | | | |
| Low Line Threshold ($LL_{IN}$) | 1.25 | 1.3 | 1.35 | V | $V_{CC}$ = +5 V, +3 V |
| Reset Timeout Delay | 35 | 50 | 70 | ms | OSC SEL = HIGH, $V_{CC}$= 5 V, $T_A$ = +25°C |
| Watchdog Timeout Period, Internal Oscillator | 1.0 | 1.6 | 2.25 | s | Long Period, $V_{CC}$ = 5 V, $T_A$ = +25°C |
| | 70 | 100 | 140 | ms | Short Period, $V_{CC}$ = 5 V, $T_A$ = +25°C |
| Watchdog Timeout Period, External Clock | 4032 | | 4097 | Cycles | Long Period |
| | 960 | | 1025 | Cycles | Short Period |
| Minimum WDI Input Pulse Width | 50 | | | ns | $V_{IL}$ = 0.4, $V_{IH}$ = 3.5 V, $V_{CC}$ = 5 V |
| $\overline{RESET}$ Output Voltage @ $V_{CC}$ = +1 V | | 4 | 200 | mV | $I_{SINK}$ = 10 µA, $V_{CC}$ = 1 V |
| RESET, $\overline{RESET}$ Output Voltage | | | 0.4 | V | $I_{SINK}$ = 400 µA, $V_{CC}$ = 2 V, $V_{BATT}$ = 0 V |
| | | | 0.4 | V | $I_{SINK}$ = 1.6 mA, 3 V < $V_{CC}$ < 5.5 V |
| | 3.5 | | | V | $I_{SOURCE}$ = 1 µA, $V_{CC}$ = 5 V |
| $\overline{LOW\ LINE}$, $\overline{WDO}$ Output Voltage | | | 0.4 | V | $I_{SINK}$ = 1.6 mA, |
| | 3.5 | | | V | $I_{SOURCE}$ = 1 µA, $V_{CC}$ = 5 V |
| Output Short Circuit Source Current | 1 | 3 | 25 | µA | |
| WDI Input Threshold | | | | | $V_{CC}$ = 5 V[1] |
| Logic Low | | | 0.8 | V | |
| Logic High | 3.5 | | | V | |
| WDI Input Current | | 20 | 50 | µA | WD1 = $V_{OUT}$, ($V_{CC}$) $T_A$ = +25°C |
| | –50 | –15 | | µA | WD1 = 0 V, $T_A$ = +25°C |
| POWER FAIL DETECTOR | | | | | |
| PFI Input Threshold | 1.2 | 1.3 | 1.4 | V | $V_{CC}$ = +3 V, +5 V |
| PFI–$LL_{IN}$ Threshold Difference | –50 | ±15 | +50 | mV | $V_{CC}$ = +3 V, +5 V |
| PFI Input Current | –25 | ±0.01 | +25 | nA | |
| $LL_{IN}$ Input Current | –50 | ±0.01 | +50 | nA | |
| $\overline{PFO}$ Output Voltage | | | 0.4 | V | $I_{SINK}$ = 1.6 mA |
| | 3.5 | | | V | $I_{SOURCE}$ = 1 µA, $V_{CC}$ = 5 V |
| $\overline{PFO}$ Short Circuit Source Current | 1 | 3 | 25 | µA | PFI = Low, $\overline{PFO}$ = 0 V |
| CHIP ENABLE GATING (ADM697) | | | | | |
| $\overline{CE}_{IN}$ Threshold | | | 0.8 | V | $V_{IL}$ |
| | 3.0 | | | V | $V_{IH}$, $V_{CC}$ = 5 V |
| $\overline{CE}_{IN}$ Pullup Current | | 3 | | µA | |
| $\overline{CE}_{OUT}$ Output Voltage | | | 0.4 | V | $I_{SINK}$ = 1.6 mA |
| | $V_{CC}$ – 0.5 | | | V | $I_{SOURCE}$ = 800 µA |
| $\overline{CE}$ Propagation Delay | | 5 | 25 | ns | |
| OSCILLATOR | | | | | |
| OSC IN Input Current | | ±2 | | µA | |
| OSC SEL Input Pullup Current | | 5 | | µA | |
| OSC IN Frequency Range | 0 | | 250 | kHz | OSC SEL = 0 V |
| OSC IN Frequency with Ext. Capacitor | | 4 | | kHz | OSC SEL = 0 V, $C_{OSC}$ = 47 pF |

NOTE

[1]WDI is a three-level input which is internally biased to 38% of $V_{CC}$ and has an input impedance of approximately 125 kΩ.

Specifications subject to change without notice.

## ABSOLUTE MAXIMUM RATINGS*

($T_A$ = +25°C unless otherwise noted)

$V_{CC}$ . . . . . –0.3 V to +6 V
$V_{BATT}$ . . . . . –0.3 V to +6 V
All Other Inputs . . . . . –0.3 V to $V_{OUT}$ + 0.5 V
Input Current
  $V_{CC}$ . . . . . 200 mA
  $V_{BATT}$ . . . . . 50 mA
  GND . . . . . 20 mA
Digital Output Current . . . . . 20 mA
Power Dissipation, N-16 DIP . . . . . 600 mW
  $\theta_{JA}$ Thermal Impedance . . . . . 135°C/W
Power Dissipation, Q-16 DIP . . . . . 600 mW
  $\theta_{JA}$ Thermal Impedance . . . . . 100°C/W
Power Dissipation, R-16 SOIC . . . . . 600 mW
  $\theta_{JA}$ Thermal Impedance . . . . . 110°C/W
Operating Temperature Range
  Industrial (A Version) . . . . . –40°C to +85°C
  Extended (S Version) . . . . . –55°C to +125°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
  Vapor Phase (60 sec) . . . . . +215°C
  Infrared (15 sec) . . . . . +220°C
Storage Temperature Range . . . . . –65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

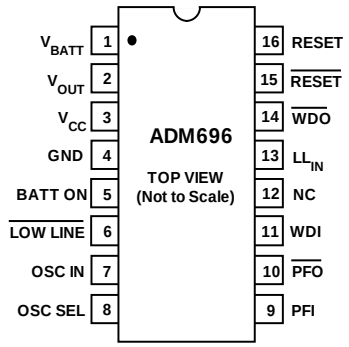
**CAUTION**

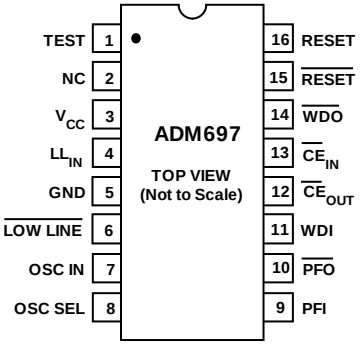
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADM696/ADM697 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

### ORDERING GUIDE

| Model | Temperature Range | Package Option |
|---|---|---|
| ADM696AN | –40°C to +85°C | N-16 |
| ADM696AR | –40°C to +85°C | R-16 |
| ADM696AQ | –40°C to +85°C | Q-16 |
| ADM696SQ | –55°C to +125°C | Q-16 |
| ADM697AN | –40°C to +85°C | N-16 |
| ADM697AR | –40°C to +85°C | R-16 |
| ADM697AQ | –40°C to +85°C | Q-16 |
| ADM697SQ | –55°C to +125°C | Q-16 |

### PIN CONFIGURATIONS



**PIN FUNCTION DESCRIPTION**

| Mnemonic | Pin No. ADM696 | Pin No. ADM697 | Function |
|---|---|---|---|
| $V_{CC}$ | 3 | 3 | Power Supply Input +3 V to +5 V. |
| $V_{BATT}$ | 1 | — | Backup Battery Input. Connect to Ground if a backup battery is not used. |
| $V_{OUT}$ | 2 | — | Output Voltage, $V_{CC}$ or $V_{BATT}$ is internally switched to $V_{OUT}$ depending on which is at the highest potential. $V_{OUT}$ can supply up to 100 mA to power CMOS RAM. Connect $V_{OUT}$ to $V_{CC}$ if $V_{OUT}$ and $V_{BATT}$ are not used. |
| GND | 4 | 5 | 0 V. Ground reference for all signals. |
| $\overline{RESET}$ | 15 | 15 | Logic Output. $\overline{RESET}$ goes low whenever $LL_{IN}$ falls below 1.3 V or when $V_{CC}$ falls below the $V_{BATT}$ input voltage. $\overline{RESET}$ remains low for 50 ms after $LL_{IN}$ goes above 1.3 V, $\overline{RESET}$ also goes low for 50 ms if the watchdog timer is enabled but not serviced within its timeout period. The $\overline{RESET}$ pulse width can be adjusted as shown in Table I. |
| WDI | 11 | 11 | Watchdog Input, WDI is a three level input. If WDI remains either high or low for longer than the watchdog timeout period, $\overline{RESET}$ pulses low and $\overline{WDO}$ goes low. The timer resets with each transition at the WDI input. The watchdog timer is disabled when WDI is left floating or is driven to midsupply. |
| PFI | 9 | 9 | Power Fail Input. PFI is the noninverting input to the Power Fail Comparator when PFI is less than 1.3 V, $\overline{PFO}$ goes low. Connect PFI to GND or $V_{OUT}$ when not used. See Figure 1. |
| $\overline{PFO}$ | 10 | 10 | Power Fail Output. $\overline{PFO}$ is the output of the Power Fail Comparator. It goes low when PFI is less than 1.3 V. The comparator is turned off and $\overline{PFO}$ goes low when $V_{CC}$ is below $V_{BATT}$. |
| $\overline{CE}_{IN}$ | — | 13 | Logic Input. The input to the CE gating circuit. Connect to GND or $V_{OUT}$ if not used. |
| $CE_{OUT}$ | — | 12 | Logic Output. $\overline{CE}_{OUT}$ is a gated version of the $\overline{CE}_{IN}$ signal. $\overline{CE}_{OUT}$ tracks $\overline{CE}_{IN}$ when $LL_{IN}$ is above 1.3 V. If $LL_{IN}$ is below 1.3 V, $\overline{CE}_{OUT}$ is forced high. |
| BATT ON | 5 | — | Logic Output. BATT ON goes high when $V_{OUT}$ is internally switched to the $V_{BATT}$ input. It goes low when $V_{OUT}$ is internally switched to $V_{CC}$. The output typically sinks 7 mA and can directly drive the base of an external PNP transistor to increase the output current above the 100 mA rating of $V_{OUT}$. |
| $\overline{LOW\ LINE}$ | 6 | 6 | Logic Output. $\overline{LOW\ LINE}$ goes low when $LL_{IN}$ falls below 1.3 V. It returns high as soon as $LL_{IN}$ rises above 1.3 V. |
| RESET | 16 | 16 | Logic Output. RESET is an active high output. It is the inverse of $\overline{RESET}$. |
| OSC SEL | 8 | 8 | Logic Oscillator Select Input. When OSC SEL is unconnected or driven high, the internal oscillator sets the reset time delay and watchdog time-out period. When OSC SEL is low, the external oscillator input, OSC IN, is enabled. OSC SEL has a 3 µA internal pullup. See Table I and Figure 4. |
| OSC IN | 7 | 7 | Logic Oscillator Input. When OSC SEL is low, OSC IN can be driven by an external clock to adjust both the reset delay and the watchdog time-out period. The timing can also be adjusted by connecting an external capacitor to this pin. See Table I and Figure 4. When OSC SEL is high or floating, OSC IN selects between fast and slow watchdog time-out periods. |
| $\overline{WDO}$ | 14 | 14 | Logic Output. The Watchdog Output, $\overline{WDO}$, goes low if WDI remains either high or low for longer than the watchdog time-out period. $\overline{WDO}$ is set high by the next transition at WDI. If WDI is unconnected or at midsupply, $\overline{WDO}$ remains high. $\overline{WDO}$ also goes high when $\overline{LOW\ LINE}$ goes low. |
| NC | 12 | 2 | No Connect. It should be left open. |
| $LL_{IN}$ | 13 | 4 | Voltage Sensing Input. The voltage on the low line input, $LL_{IN}$, is compared with a 1.3 V reference voltage. This input is normally used to monitor the power supply voltage. The output of the comparator generates a $\overline{LOW\ LINE}$ output signal. It also generates a RESET/$\overline{RESET}$ output. |
| TEST | — | 1 | This is a special test pin using during device manufacture. It should be connected to GND. |

## CIRCUIT INFORMATION

### Battery-Switchover Section (ADM696)

The battery switchover circuit compares $V_{CC}$ to the $V_{BATT}$ input, and connects $V_{OUT}$ to whichever is higher. Switchover occurs when $V_{CC}$ is 50 mV higher than $V_{BATT}$ as $V_{CC}$ falls, and when $V_{CC}$ is 70 mV greater than $V_{BATT}$ as $V_{CC}$ rises. This 20 mV of hysteresis prevents repeated rapid switching if $V_{CC}$ falls very slowly or remains nearly equal to the battery voltage.

During normal operation with $V_{CC}$ higher than $V_{BATT}$, $V_{CC}$ is internally switched to $V_{OUT}$ via an internal PMOS transistor switch. This switch has a typical on resistance of 1.5 Ω and can supply up to 100 mA at the $V_{OUT}$ terminal. $V_{OUT}$ is normally used to drive a RAM memory bank which may require instantaneous currents of greater than 100 mA. If this is the case, then a bypass capacitor should be connected to $V_{OUT}$. The capacitor will provide the peak current transients to the RAM. A capacitance value of 0.1 µF or greater may be used.

If the continuous output current requirement at $V_{OUT}$ exceeds 100 mA or if a lower $V_{CC}$–$V_{OUT}$ voltage differential is desired, an external PNP pass transistor may be connected in parallel with the internal transistor. The BATT ON output can directly drive the base of the external transistor.

A 20 Ω MOSFET switch connects the $V_{BATT}$ input to $V_{OUT}$ during battery backup. This MOSFET has very low input-to-output differential (dropout voltage) at the low current levels required for battery backup of CMOS RAM or other low power CMOS circuitry. The supply current in battery backup is typically 0.6 µA.

The ADM696 operates with battery voltages from 2.0 V to $V_{CC}$ –0.3 V). High value capacitors, either standard electrolytic or the farad-size double layer capacitors, can also be used for short-term memory backup. A small charging current of typically 10 nA (0.1 µA max) flows out of the $V_{BATT}$ terminal. This current is useful for maintaining rechargeable batteries in a fully charged condition. This extends the life of the backup battery by compensating for its self discharge current. Also note that this current poses no problem when lithium batteries are used for backup since the maximum charging current (0.1 µA) is safe for even the smallest lithium cells.

If the battery-switchover section is not used, $V_{BATT}$ should be connected to GND and $V_{OUT}$ should be connected to $V_{CC}$.

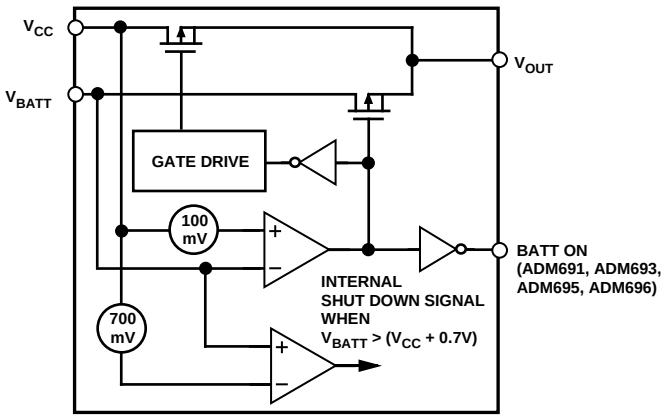



*Figure 1. Battery Switchover Schematic*

### Low Line $\overline{\text{RESET}}$ OUTPUT

$\overline{\text{RESET}}$ is an active low output which provides a $\overline{\text{RESET}}$ signal to the microprocessor whenever the Low Line Input ($LL_{IN}$) is below 1.3 V. The $LL_{IN}$ input is normally used to monitor the power supply voltage. An internal timer holds $\overline{\text{RESET}}$ low for 50 ms after the voltage on $LL_{IN}$ rises above 1.3 V. This is intended as a power-on $\overline{\text{RESET}}$ signal for the processor. It allows time for the power supply and microprocessor to stabilize. On power-down, the $\overline{\text{RESET}}$ output remains low with $V_{CC}$ as low as 1 V. This ensures that the microprocessor is held in a stable shutdown condition.

The $LL_{IN}$ comparator has approximately 12 mV of hysteresis for enhanced noise immunity.

In addition to $\overline{\text{RESET}}$, an active high RESET output is also available. This is the complement of $\overline{\text{RESET}}$ and is useful for processors requiring an active high RESET.

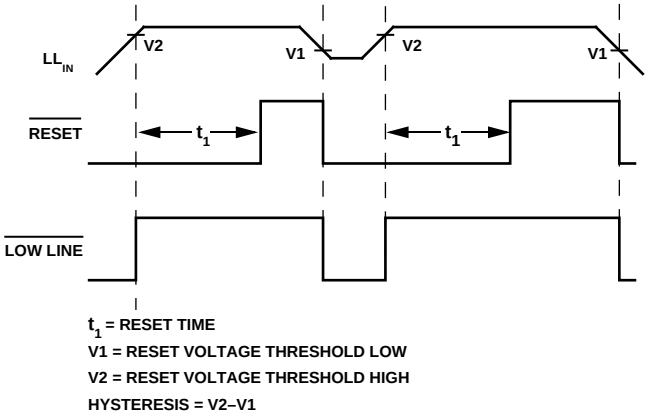



*Figure 2. Power-Fail Reset Timing*

### Watchdog Timer $\overline{\text{RESET}}$

The watchdog timer circuit monitors the activity of the microprocessor in order to check that it is not stalled in an indefinite loop. An output line on the processor is used to toggle the Watchdog Input (WDI) line. If this line is not toggled within the selected timeout period, a $\overline{\text{RESET}}$ pulse is generated. The ADM696/ADM697 may be configured for either a fixed "short" 100 ms or a "long" 1.6 second timeout period or for an adjustable timeout period. If the "short" period is selected some systems may be unable to service the watchdog timer immediately after a reset, so a "long" timeout is automatically initiated directly after a reset is issued. The watchdog timer is restarted at the end of Reset, whether the Reset was caused by lack of activity on WDI or by $LL_{IN}$ falling below the reset threshold.

The normal (short) timeout period becomes effective following the first transition of WDI after $\overline{\text{RESET}}$ has gone inactive. The watchdog timeout period restarts with each transition on the WDI pin. To ensure that the watchdog timer does not time out, either a high-to-low or low-to high transition on the WDI pin must occur at or less than the minimum timeout period. If WDI remains permanently either high or low, reset pulses will be issued after each timeout period (1.6 s). The watchdog monitor can be deactivated by floating the Watchdog Input (WDI) or by connecting it to midsupply.

**Table I. ADM696, ADM697 Reset Pulse Width and Watchdog Timeout Selections**

| OSC SEL | OSC IN | Watchdog Timeout Period | | Reset Active Period |
|---|---|---|---|---|
| | | Normal | Immediately After Reset | |
| Low | External Clock Input | 1024 CLKS | 4096 CLKS | 512 CLKS |
| Low | External Capacitor | 400 ms × C/47 pF | 1.6 s × C/47 pF | 200 ms × C/47 pF |
| Floating or High | Low | 100 ms | 1.6 s | 50 ms |
| Floating or High | Floating or High | 1.6 s | 1.6 s | 50 ms |

NOTE
With the OSC SEL pin low, OSC IN can be driven by an external clock signal, or an external capacitor can be connected between OSC IN and GND. The nominal internal oscillator frequency is 10.24 kHz. The nominal oscillator frequency with external capacitor is: $F_{OSC}$ (Hz) = 184,000/C (pF).

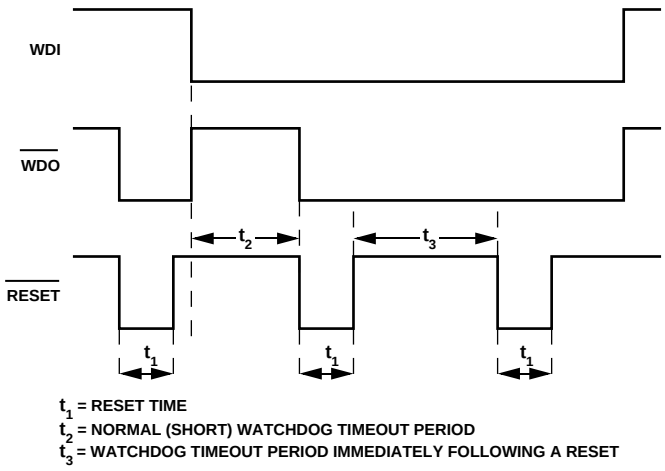



*Figure 3. Watchdog Timeout Period and Reset Active Time*

The watchdog timeout period defaults to 1.6 s and the reset pulse width defaults to 50 ms but these times to be adjusted as shown in Table I. Figure 4 shows the various oscillator configurations which can be used to adjust the reset pulse width and watchdog timeout period.

The internal oscillator is enabled when OSC SEL is high or floating. In this mode, OSC IN selects between the 1.6 second and 100 ms watchdog timeout periods. In either case, immediately after a reset the timeout period is 1.6 s. This gives the microprocessor time to reinitialize the system. If OSC IN is low, then the 100 ms watchdog period becomes effective after the first transition of WDI. The software should be written such that the I/O port driving WDI is left in its power-up reset state until the initialization routines are completed and the microprocessor is able to toggle WDI at the minimum watchdog timeout period of 70 ms.

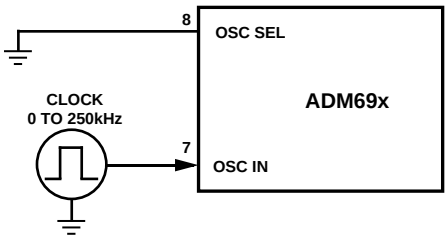



*Figure 4a. External Clock Source*

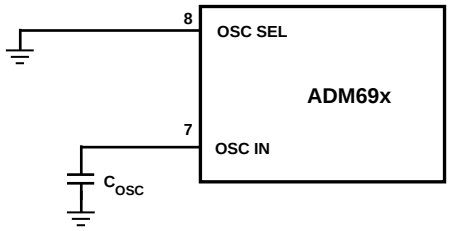



*Figure 4b. External Capacitor*

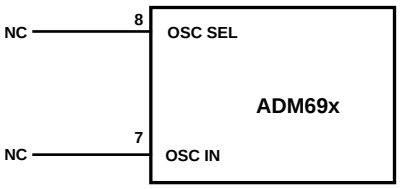



*Figure 4c. Internal Oscillator (1.6 s Watchdog)*

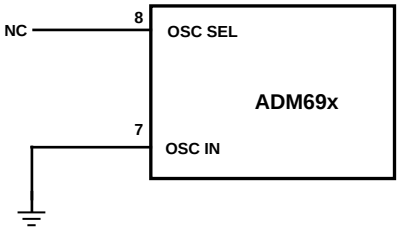



*Figure 4d. Internal Oscillator (100 ms Watchdog)*

**Watchdog Output ($\overline{\text{WDO}}$)**

The Watchdog Output $\overline{\text{WDO}}$ provides a status output which goes low if the watchdog timer "times out" and remains low until set high by the next transition on the watchdog input. $\overline{\text{WDO}}$ is also set high when $LL_{IN}$ goes below the reset threshold.

**CE Gating and RAM Write Protection (ADM697)**

The ADM697 contains memory protection circuitry which ensures the integrity of data in memory by preventing write operations when $LL_{IN}$ is below the threshold voltage. When $LL_{IN}$ is greater than 1.3 V, $\overline{CE}_{OUT}$ is a buffered replica of $\overline{CE}_{IN}$, with a 5 ns propagation delay. When $LL_{IN}$ falls below the 1.3 V threshold, an internal gate forces $\overline{CE}_{OUT}$ high, independent of $\overline{CE}_{IN}$.

$\overline{CE}_{OUT}$ typically drives the CE, CS, or Write input of battery backed up CMOS RAM. This ensures the integrity of the data in memory by preventing write operations when $V_{CC}$ is at an invalid level.

If the 5 ns typical propagation delay of $\overline{CE}_{OUT}$ is excessive, connect $\overline{CE}_{IN}$ to GND and use the resulting $\overline{CE}_{OUT}$ to control a high speed external logic gate.

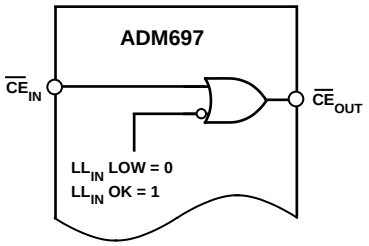



*Figure 5. Chip Enable Gating*

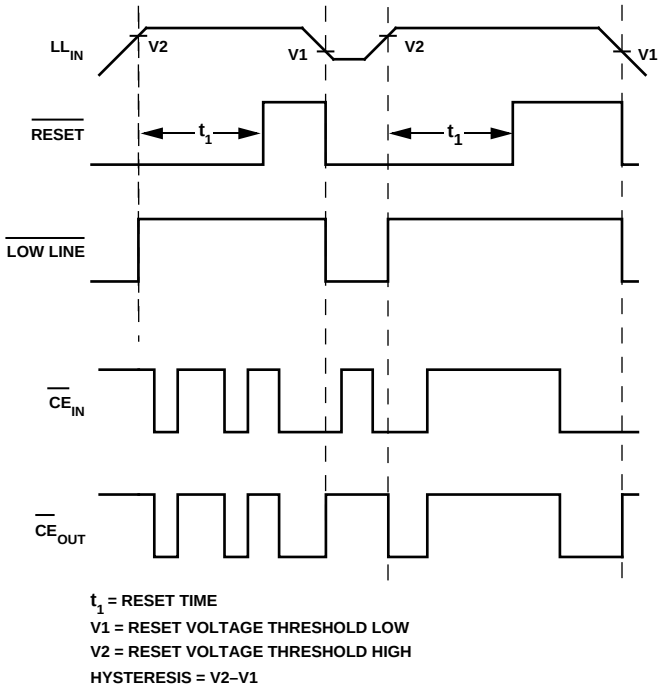



*Figure 6. Chip Enable Timing*

**Power Fail Warning Comparator**

An additional comparator is provided for early warning of failure in the microprocessor's power supply. The Power Fail Input (PFI) is compared to an internal +1.3 V reference. The Power Fail Output ($\overline{PFO}$) goes low when the voltage at PFI is less than 1.3 V. Typically PFI is driven by an external voltage divider which senses either the unregulated dc input to the system's 5 V regulator or the regulated 5 V output. The voltage divider ratio can be chosen such that the voltage at PFI falls below 1.3 V several milliseconds before the +5 V power supply falls below the reset threshold. $\overline{PFO}$ is normally used to interrupt the microprocessor so that data can be stored in RAM and the shutdown procedure executed before power is lost.

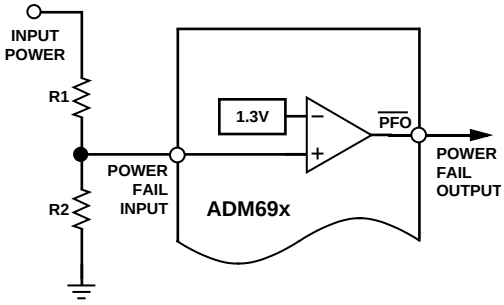



*Figure 7. Power Fail Comparator*

**Table II. Input and Output Status In Battery Backup Mode**

| Signal | Status |
|---|---|
| $V_{OUT}$ | (ADM696) $V_{OUT}$ is connected to $V_{BATT}$ via an internal PMOS switch. |
| $\overline{RESET}$ | Logic low. |
| RESET | Logic high. The open circuit output voltage is equal to $V_{OUT}$. |
| $\overline{LOW\ LINE}$ | Logic low. |
| BATT ON | (ADM696) Logic high. The open circuit voltage is equal to $V_{OUT}$. |
| WDI | WDI is ignored. It is internally disconnected from the internal pullup resistor and does not source or sink current as long as its input voltage is between GND and $V_{OUT}$. The input voltage does not affect supply current. |
| $\overline{WDO}$ | Logic high. The open circuit voltage is equal to $V_{OUT}$. |
| PFI | The Power Fail Comparator is turned off and has no effect on the Power Fail Output. |
| $\overline{PFO}$ | Logic low. |
| $\overline{CE}_{IN}$ | $\overline{CE}_{IN}$ is ignored. It is internally disconnected from its internal pullup and does not source or sink current as long as its input voltage is between GND and $V_{OUT}$. The input voltage does not affect supply current. |
| $\overline{CE}_{OUT}$ | Logic high. The open circuit voltage is equal to $V_{OUT}$. |
| OSC IN | OSC IN is ignored. |
| OSC SEL | OSC SEL is ignored. |

# ADM696/ADM697–Typical Performance Curves

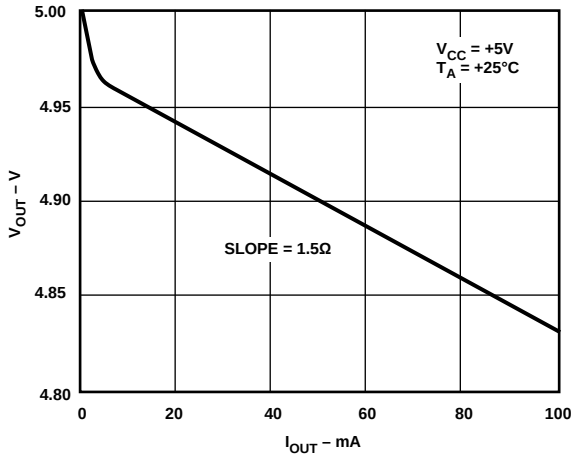



*Figure 8. $V_{OUT}$ vs. $I_{OUT}$ Normal Operation*

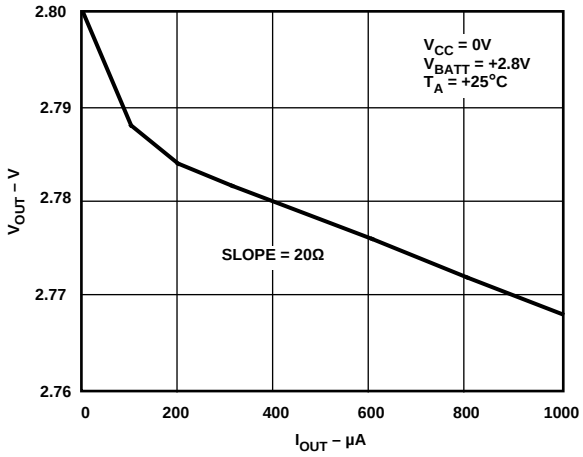



*Figure 9. $V_{OUT}$ vs. Battery Backup*

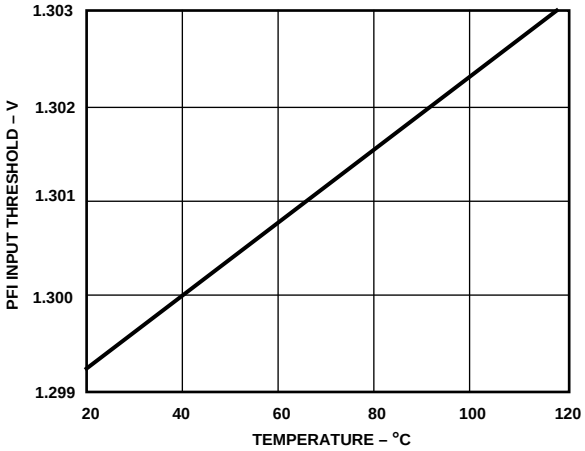



*Figure 10. PFI Input Threshold vs. Temperature*

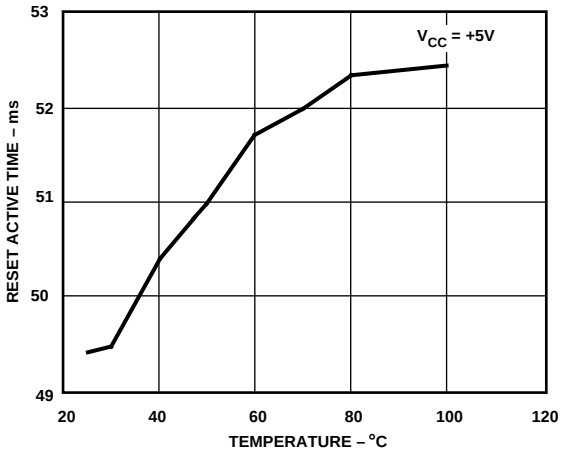



*Figure 11. RESET Active Time vs. Temperature*

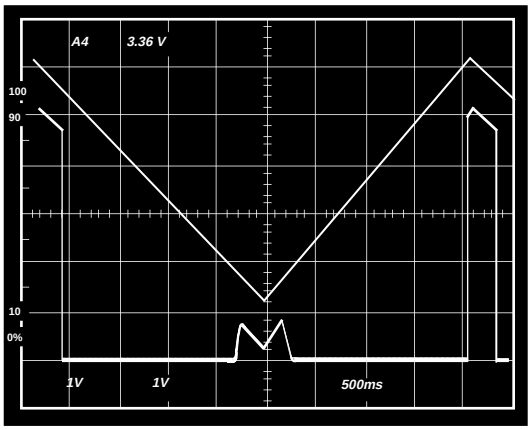



*Figure 12. $\overline{RESET}$ Output Voltage vs. Supply Voltage*

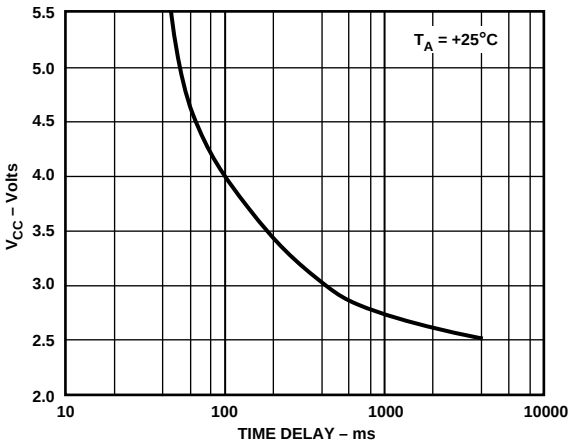



*Figure 13. $\overline{RESET}$ Timeout Delay vs. $V_{CC}$*

## APPLICATIONS INFORMATION

### Increasing the Drive Current (ADM696)

If the continuous output current requirements at $V_{OUT}$ exceeds 100 mA or if a lower $V_{CC}$–$V_{OUT}$ voltage differential is desired, an external PNP pass transistor may be connected in parallel with the internal transistor. The BATT ON output (ADM696) can directly drive the base of the external transistor.

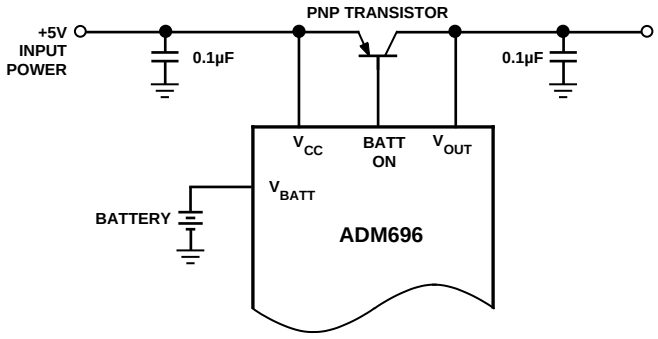



*Figure 14. Increasing the Drive Current*

### Using a Rechargeable Battery for Backup (ADM696)

If a capacitor or a rechargeable battery is used for backup, then the charging resistor should be connected to $V_{OUT}$ since this eliminates the discharge path that would exist during power-down if the resistor is connected to $V_{CC}$.

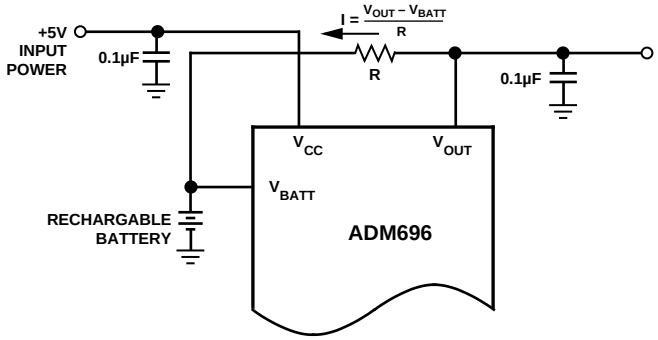



*Figure 15. Rechargeable Battery*

### Adding Hysteresis to the Power Fail Comparator

For increased noise immunity, hysteresis may be added to the power fail comparator. Since the comparator circuit is noninverting, hysteresis can be added simply by connecting a resistor between the PFO output and the PFI input as shown in Figure 16. When PFO is low, resistor R3 sinks current from the summing junction at the PFI pin. When PFO is high, the series combination of R3 and R4 source current into the PFI summing junction. This results in differing trip levels for the comparator.

### Alternate Watchdog Input Drive Circuits

The watchdog feature can be enabled and disabled under program control by driving WDI with a 3-state buffer (Figure 17a). When three-stated, the WDI input will float thereby disabling the watchdog timer.

This circuit is not entirely foolproof, and it is possible that a software fault could erroneously 3-state the buffer. This would then prevent the ADM69x from detecting that the microprocessor is no longer operating correctly. In most cases a better

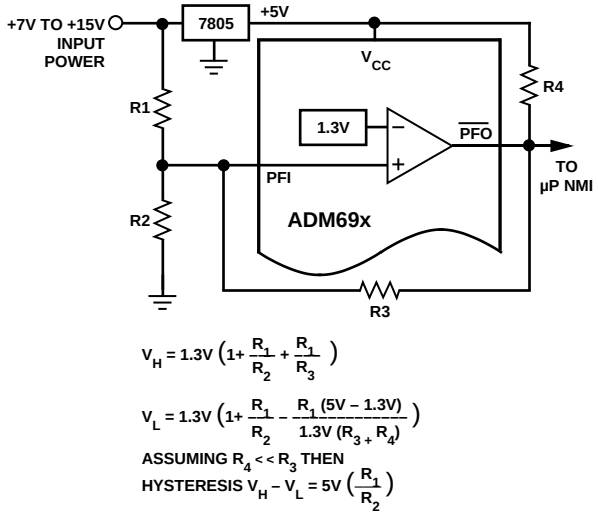



*Figure 16. Adding Hysteresis to the Power Fail Comparator*

method is to extend the watchdog period rather than disabling the watchdog. This may be done under program control using the circuit shown in Figure 17b. When the control input is high, the OSC SEL pin is low and the watchdog timeout is set by the external capacitor. A 0.01 µF capacitor sets a watchdog timeout delay of 100 s. When the control input is low, the OSC SEL pin is driven high, selecting the internal oscillator. The 100 ms or the 1.6 s period is chosen, depending on which diode in Figure 17b is used. With D1 inserted, the internal timeout is set at 100 ms while with D2 inserted the timeout is set at 1.6 s.

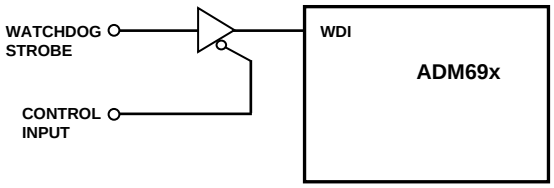



*Figure 17a. Programming the Watchdog Input*

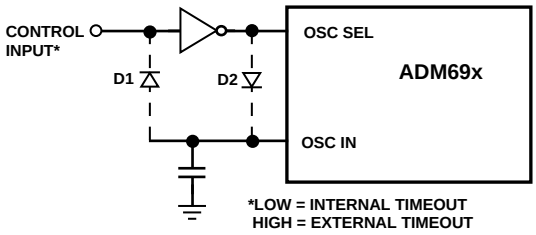



*Figure 17b. Programming the Watchdog Input*

**Replacing the Back-Up Battery**

When changing the back-up battery with system power on, spurious resets can occur when the battery is removed. This occurs because the leakage current flowing out of the $V_{BATT}$ pin will charge up the stray capacitance. If the voltage on $V_{BATT}$ reaches within 50 mV of $V_{CC}$, a reset pulse is generated.

If spurious resets during battery replacement are acceptable, then no action is required. If not, then one of the following solutions should be considered:

1. A capacitor from $V_{BATT}$ to GND. This gives time while the capacitor is charging up to change the battery. The leakage current will charge up the external capacitor towards the $V_{CC}$ level. The time taken is related to the charging current, the size of external capacitor and the voltage differential between the capacitor and the charging voltage supply.

   $$t = C_{EXT} \times V_{DIFF}/I$$

   The maximum leakage (charging) current is 1 µA over temperature and $V_{DIFF} = V_{CC}\ V_{BATT}$. Therefore, the capacitor size should be chosen such that sufficient time is available to make the battery replacement.

   $$C_{EXT} = T_{REQD}\ (1\ \mu A/(V_{CC} - V_{BATT}))$$

   If a replacement time of 5 s is allowed and assuming a $V_{CC}$ of 4.5 V and a $V_{BATT}$ of 3 V,

   $$C_{EXT} = 3.33\ \mu F$$

2. A resistor from $V_{BATT}$ to GND. This will prevent the voltage on $V_{BATT}$ from rising to within 50 mV of $V_{CC}$ during battery replacement.

   $$R = (V_{CC} - 50\ mV)/1\ \mu A$$

   Note that the resistor will discharge the battery slightly. With a $V_{CC}$ supply of 4.5 V, a suitable resistor is 4.3 MΩ. With a 3 V battery, this will draw around 700 nA. This will be negligible in most cases.

## TYPICAL APPLICATIONS

### ADM696

Figure 18 shows the ADM696 in a typical power monitoring, battery backup application. $V_{OUT}$ powers the CMOS RAM. Under normal operating conditions with $V_{CC}$ present, $V_{OUT}$ is internally connected to $V_{CC}$. If a power failure occurs, $V_{CC}$ will decay and $V_{OUT}$ will be switched to $V_{BATT}$, thereby maintaining power for the CMOS RAM.

**Power Fail $\overline{\text{RESET}}$**

The $V_{CC}$ power supply is also monitored by the Low Line Input, $LL_{IN}$. A $\overline{\text{RESET}}$ pulse is generated when $LL_{IN}$ falls below 1.3 V. $\overline{\text{RESET}}$ will remain low for 50 ms after $LL_{IN}$ returns above 1.3 V. This allows for a power-on reset and prevents repeated toggling of $\overline{\text{RESET}}$ if the $V_{CC}$ power supply is unstable. Resistors R3 and R4 should be chosen to give the desired $V_{CC}$ reset threshold.

**Watchdog Timer**

The Watchdog Timer Input (WDI) monitors an I/O line from the µP system. This line must be toggled once every 1.6 s to verify correct software execution. Failure to toggle the line indicates that the µP system is not correctly executing its program and may be tied up in an endless loop. If this happens, a reset pulse is generated to initialize the processor.

If the watchdog timer is not needed the WDI input should be left floating.

**Power Fail Detector**

The Power Fail Input, PFI, monitors the input power supply via a resistive divider network R1 and R2. This input is intended as an early warning power fail input. The voltage on the PFI input is compared with a precision 1.3 V internal reference. If the input voltage drops below 1.3 V, a power fail output (PFO) signal is generated. This warns of an impending power failure and may be used to interrupt the processor so that the system may be shut down in an orderly fashion. The resistors in the sensing network are ratioed to give the desired power fail threshold voltage $V_T$. The threshold should be set at a higher voltage than the RESET threshold so that there is sufficient time available to complete the shutdown procedure before the processor is RESET and power is lost.

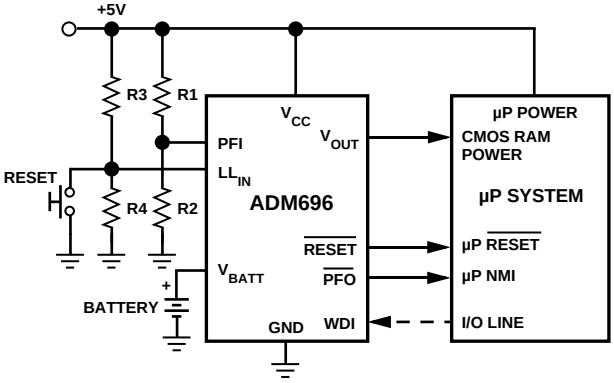



*Figure 18a. ADM696 Typical Application Circuit A*

Figure 18b shows a similar application for the ADM696 but in this case the PFI input monitors the unregulated input to the 7805 voltage regulator. This gives an earlier warning of an impending power failure. It is useful with processors operating at low speeds or where there are a significant number of housekeeping tasks to be completed before the power is lost.

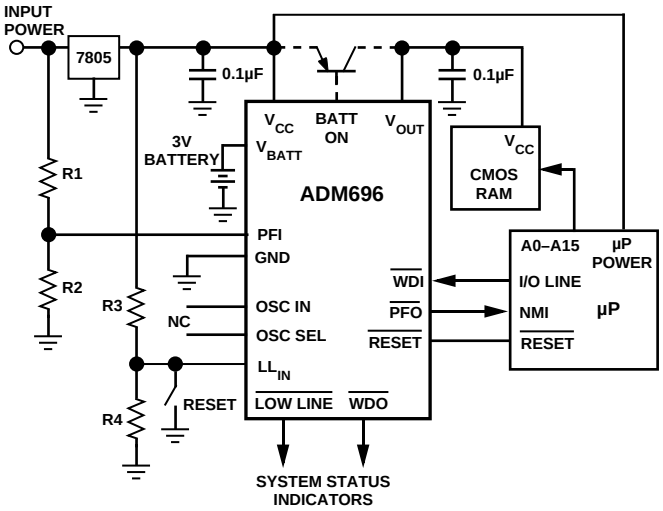



*Figure 18b. ADM696 Typical Application Circuit B*

This application also shows an optional, external transistor which may be used to provide in excess of 100 mA current on $V_{OUT}$. When $V_{CC}$ is higher than $V_{BATT}$, the BATT ON output goes low, providing 25 mA of base drive for the external PNP transistor. The maximum current available is dependent on the power rating of the external transistor.

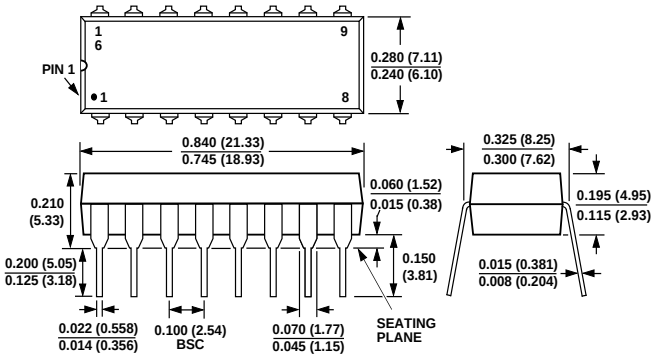
**RAM Write Protection**

The ADM697 $\overline{CE}_{OUT}$ line drives the Chip Select inputs of the CMOS RAM. $\overline{CE}_{OUT}$ follows $\overline{CE}_{IN}$ as long as $LL_{IN}$ is above the reset threshold. If $LL_{IN}$ falls below the reset threshold, $\overline{CE}_{OUT}$ goes high, independent of the logic level at $\overline{CE}_{IN}$. This prevents the microprocessor from writing erroneous data into RAM during power-up, power-down, brownouts and momentary power interruptions.

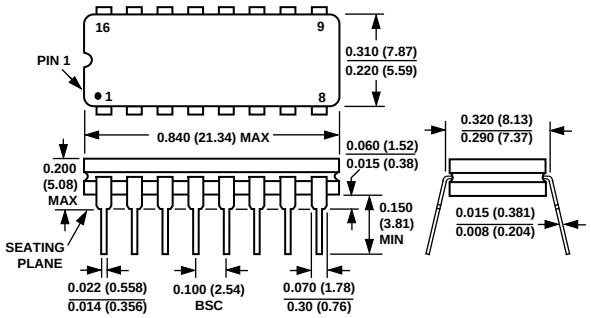
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

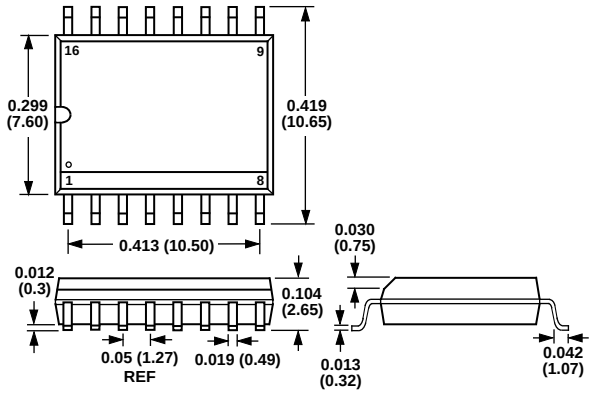
### 16-Pin Plastic DIP (N-16)




### 16-Pin Cerdip (Q-16)




### 16-Lead SOIC (R-16)



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