4-/6-Channel Digital Potentiometers

AD5204/AD5206

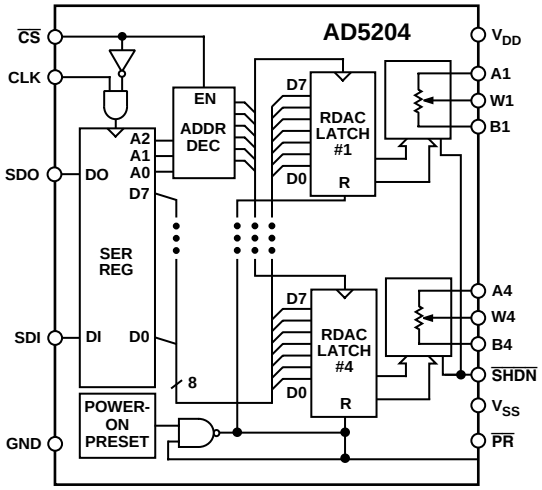
FEATURES

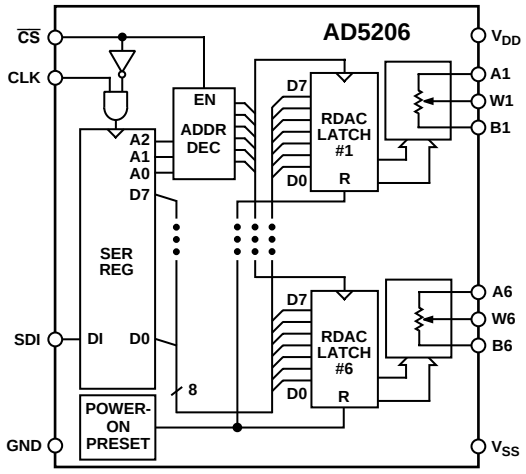
256 Position
Multiple Independently Programmable Channels
AD5204—4-Channel
AD5206—6-Channel
Potentiometer Replacement
10 kΩ, 50 kΩ, 100 kΩ
3-Wire SPI-Compatible Serial Data Input
+2.7 V to +5.5 V Single Supply; ±2.7 V Dual Supply Operation
Power ON Midscale Preset

APPLICATIONS

Mechanical Potentiometer Replacement
Instrumentation: Gain, Offset Adjustment
Programmable Voltage-to-Current Conversion
Programmable Filters, Delays, Time Constants
Line Impedance Matching

FUNCTIONAL BLOCK DIAGRAMS





GENERAL DESCRIPTION

The AD5204/AD5206 provides four-/six-channel, 256 position digitally-controlled Variable Resistor (VR) devices. These devices perform the same electronic adjustment function as a potentiometer or variable resistor. Each channel of the AD5204/AD5206 contains a fixed resistor with a wiper contact that taps the fixed resistor value at a point determined by a digital code loaded into the SPI-compatible serial-input register. The resistance between the wiper and either endpoint of the fixed resistor varies linearly with respect to the digital code transferred into the VR latch. The variable resistor offers a completely programmable value of resistance between the A terminal and the wiper or the B Terminal and the wiper. The fixed A-to-B terminal resistance of 10 kΩ, 50 kΩ, or 100 kΩ has a nominal temperature coefficient of 700 ppm/°C.

Each VR has its own VR latch which holds its programmed resistance value. These VR latches are updated from an internal serial-to-parallel shift register that is loaded from a standard 3-wire serial-input digital interface. Eleven data bits make up the data word clocked into the serial input register. The first three bits are decoded to determine which VR latch will be loaded with the last eight bits of the data word when the $\overline{CS}$ strobe is returned to logic high. A serial data output pin at the opposite end of the serial register (AD5204 only) allows simple daisy-chaining in multiple VR applications without additional external decoding logic.

An optional reset ($\overline{PR}$) pin forces all the AD5204 wipers to the midscale position by loading 80_H into the VR latch.

The AD5204/AD5206 is available in both surface mount (SOL-24), TSSOP-24 and the 24-lead plastic DIP package. All parts are guaranteed to operate over the extended industrial temperature range of –40°C to +85°C. For additional single, dual, and quad channel devices, see the AD8400/AD8402/AD8403 products.

REV. 0

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AD5204/AD5206–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_{DD} = +5 V ± 10% or +3 V ± 10%, V_{SS} = 0 V, V_A = $+V_{DD}$, V_B = 0 V, –40°C < T_A < +85°C unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Units
DC CHARACTERISTICS RHEOSTAT MODE Specifications Apply to All VRs						
Resistor Differential NL[2]	R-DNL	R_{WB}, V_A = No Connect	–1	±1/4	+1	LSB
Resistor Nonlinearity Error[2]	R-INL	R_{WB}, V_A = No Connect	–2	±1/2	+2	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}	T_A = +25°C	–30		+30	%
Resistance Temperature Coefficient	$\Delta R_{AB}/\Delta T$	V_{AB} = V_{DD}, Wiper = No Connect		700		ppm/°C
Nominal Resistance Match	$\Delta R/R_{AB}$	CH1 to 2, 3, 4, or 5, 6; V_{AB} = V_{DD}		0.25	1.5	%
Wiper Resistance	R_W	I_W = 1 V/R, V_{DD} = +5 V		50	100	Ω
DC CHARACTERISTICS POTENTIOMETER DIVIDER MODE Specifications Apply to All VRs						
Resolution	N		8			Bits
Differential Nonlinearity[4]	DNL		–1	±1/4	+1	LSB
Integral Nonlinearity[4]	INL		–2	±1/2	+2	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 40_H		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = $7F_H$	–2	–1	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 00_H	0	+1	+2	LSB
RESISTOR TERMINALS						
Voltage Range[5]	V_A, V_B, V_W		V_{SS}		V_{DD}	V
Capacitance[6] Ax, Bx	C_A, C_B	f = 1 MHz, Measured to GND, Code = 40_H		45		pF
Capacitance[6] Wx	C_W	f = 1 MHz, Measured to GND, Code = 40_H		60		pF
Shutdown Current[7]	I_{A_SD}			0.01	5	µA
Common-Mode Leakage	I_{CM}	V_A = V_B = V_W = 0, V_{DD} = +2.7 V, V_{SS} = –2.5 V		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	V_{DD} = +5 V/+3 V	2.4/2.1			V
Input Logic Low	V_{IL}	V_{DD} = +5 V/+3 V			0.8/0.6	V
Output Logic High	V_{OH}	$R_{PULL-UP}$ = 1 kΩ to +5 V	4.9			V
Output Logic Low	V_{OL}	I_{OL} = 1.6 mA, V_{LOGIC} = +5 V			0.4	V
Input Current	I_{IL}	V_{IN} = 0 V or +5 V			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Power Single Supply Range	V_{DD} Range	V_{SS} = 0 V	2.7		5.5	V
Power Dual Supply Range	$V_{DD/SS}$ Range		±2.3		±2.7	V
Positive Supply Current	I_{DD}	V_{IH} = +5 V or V_{IL} = 0 V		12	60	µA
Negative Supply Current	I_{SS}	V_{SS} = –2.5 V, V_{DD} = +2.7 V		12	60	µA
Power Dissipation[8]	P_{DISS}	V_{IH} = +5 V or V_{IL} = 0 V			0.3	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = +5 V ± 10%		0.0002	0.005	%/%
DYNAMIC CHARACTERISTICS[6, 9]						
Bandwidth –3 dB	BW_10K	R_{AB} = 10 kΩ		721		kHz
	BW_50K	R_{AB} = 50 kΩ		137		kHz
	BW_100K	R_{AB} = 100 kΩ		69		kHz
Total Harmonic Distortion	THD_W	V_A = 1.414 V rms, V_B = 0 V dc, f = 1 kHz		0.004		%
V_W Settling Time (10K/50K/100K)	t_S	V_A = 5 V, V_B = 0 V, ±1 LSB Error Band		2/9/18		µs
Resistor Noise Voltage	e_{N_WB}	R_{WB} = 5 kΩ, f = 1 kHz, $\overline{PR}$ = 0		9		nV/√Hz
INTERFACE TIMING CHARACTERISTICS Applies to All Parts[6, 10]						
Input Clock Pulsewidth	t_{CH}, t_{CL}	Clock Level High or Low	20			ns
Data Setup Time	t_{DS}		5			ns
Data Hold Time	t_{DH}		5			ns
CLK to SDO Propagation Delay[11]	t_{PD}	R_L = 2 kΩ, C_L < 20 pF	1		150	ns
$\overline{CS}$ Setup Time	t_{CSS}		15			ns
$\overline{CS}$ High Pulsewidth	t_{CSW}		40			ns
Reset Pulsewidth	t_{RS}		90			ns
CLK Fall to $\overline{CS}$ Fall Setup	t_{CSH0}		0			ns
CLK Fall to $\overline{CS}$ Rise Hold Time	t_{CSH1}		0			ns
$\overline{CS}$ Rise to Clock Rise Setup	t_{CS1}		10			ns

NOTES

[1]Typicals represent average readings at +25°C and V_{DD} = +5 V.

[2]Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic. See Figure 23 test circuit. I_W = V_{DD}/R for both V_{DD} = +3 V or V_{DD} = +5 V.

[3]V_{AB} = V_{DD}, Wiper (V_W) = No connect.

[4]INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. V_A = V_{DD} and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions. See Figure 22 test circuit.

[5]Resistor Terminals A, B, W, have no limitations on polarity with respect to each other.
[6]Guaranteed by design and not subject to production test.
[7]Measured at the Ax terminals. All Ax terminals are open-circuited in shutdown mode.
[8]P_{DISS} is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.
[9]All dynamic characteristics use V_{DD} = +5 V.
[10]See timing diagrams for location of measured values. All input control voltages are specified with $t_R = t_F$ = 2.5 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V. Switching characteristics are measured using both V_{DD} = +3 V or +5 V.
[11]Propagation delay depends on value of V_{DD}, R_L and C_L. See Operation section.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C, unless otherwise noted)

V_{DD} to GND	–0.3 V, +7 V
V_{SS} to GND	0 V, –7 V
V_{DD} to V_{SS}	+7 V
V_A, V_B, V_W to GND	V_{SS}, V_{DD}
Ax–Bx, Ax–Wx, Bx–Wx	±20 mA
Digital Input and Output Voltage to GND	0 V, +7 V
Operating Temperature Range	–40°C to +85°C
Maximum Junction Temperature (T_J MAX)	+150°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C
Package Power Dissipation	(T_J max–T_A)/θ_{JA}
Thermal Resistance θ_{JA}	
P-DIP (N-24)	63°C/W
SOIC (SOL-24)	70°C/W
TSSOP-24	143°C/W

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5204/AD5206 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

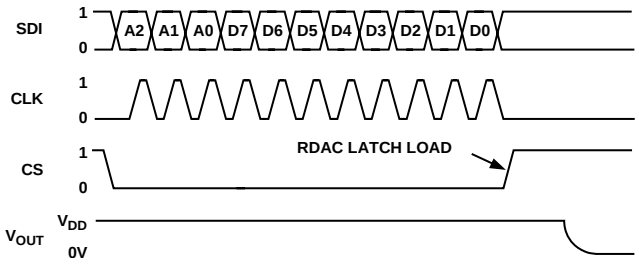


Figure 1. Timing Diagram

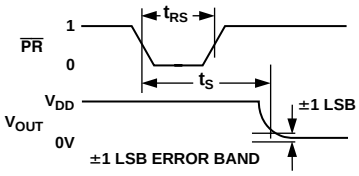


Figure 3. AD5204 Preset Timing Diagram

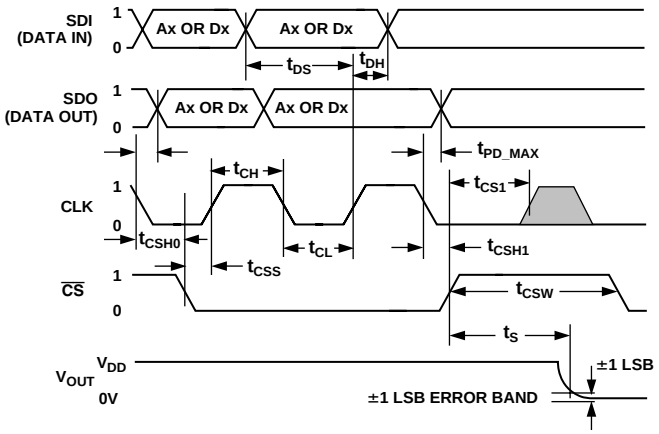


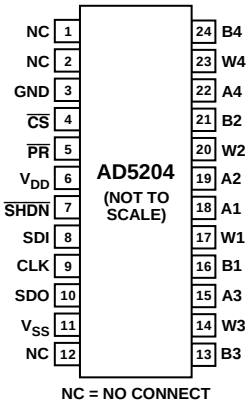
Figure 2. Detail Timing Diagram

ORDERING GUIDE

Model	kΩ	Temperature Range	Package Descriptions	Package Options
AD5204BN10	10	–40°C to +85°C	24-Lead Narrow Body (PDIP)	N-24
AD5204BR10	10	–40°C to +85°C	24-Lead Wide Body (SOIC)	R-24/SOL-24
AD5204BRU10	10	–40°C to +85°C	24-Lead Thin Shrink SO Package (TSSOP)	RU-24
AD5204BN50	50	–40°C to +85°C	24-Lead Narrow Body (PDIP)	N-24
AD5204BR50	50	–40°C to +85°C	24-Lead Wide Body (SOIC)	R-24/SOL-24
AD5204BRU50	50	–40°C to +85°C	24-Lead Thin Shrink SO Package (TSSOP)	RU-24
AD5204BN100	100	–40°C to +85°C	24-Lead Narrow Body (PDIP)	N-24
AD5204BR100	100	–40°C to +85°C	24-Lead Wide Body (SOIC)	R-24/SOL-24
AD5204BRU100	100	–40°C to +85°C	24-Lead Thin Shrink SO Package (TSSOP)	RU-24
AD5206BN10	10	–40°C to +85°C	24-Lead Narrow Body (PDIP)	N-24
AD5206BR10	10	–40°C to +85°C	24-Lead Wide Body (SOIC)	R-24/SOL-24
AD5206BRU10	10	–40°C to +85°C	24-Lead Thin Shrink SO Package (TSSOP)	RU-24
AD5206BN50	50	–40°C to +85°C	24-Lead Narrow Body (PDIP)	N-24
AD5206BR50	50	–40°C to +85°C	24-Lead Wide Body (SOIC)	R-24/SOL-24
AD5206BRU50	50	–40°C to +85°C	24-Lead Thin Shrink SO Package (TSSOP)	RU-24
AD5206BN100	100	–40°C to +85°C	24-Lead Narrow Body (PDIP)	N-24
AD5206BR100	100	–40°C to +85°C	24-Lead Wide Body (SOIC)	R-24/SOL-24
AD5206BRU100	100	–40°C to +85°C	24-Lead Thin Shrink SO Package (TSSOP)	RU-24

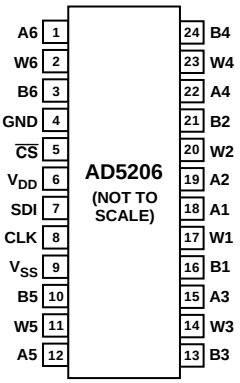
The AD5204/AD5206 contains 5,925 transistors. Die size; 92 mil × 114 mil, 10,488 sq. mil.

AD5204 PIN CONFIGURATION



NC = NO CONNECT

AD5206 PIN CONFIGURATION



AD5204 PIN FUNCTION DESCRIPTIONS

Pin No.	Name	Description
1, 2, 12	NC	Not Connected.
3	GND	Ground.
4	$\overline{CS}$	Chip Select Input, Active Low. When $\overline{CS}$ returns high, data in the serial input register is decoded based on the address bits and loaded into the target RDAC latch.
5	$\overline{PR}$	Active low preset to midscale; sets RDAC registers to 80H.
6	V_{DD}	Positive power supply, specified for operation at both +3 V or +5 V. (Sum of $\|V_{DD}\| + \|V_{SS}\| < 5.5$ V.)
7	$\overline{SHDN}$	Active low input. Terminal A open-circuit. Shutdown controls Variable Resistors #1 through #4.
8	SDI	Serial Data Input. MSB First.
9	CLK	Serial Clock Input, positive edge triggered.
10	SDO	Serial Data Output, Open Drain transistor requires pull-up resistor.
11	V_{SS}	Negative Power Supply, specified for operation at both 0 V or –2.7 V. (Sum of $\|V_{DD}\| + \|V_{SS}\| < 5.5$ V.)
13	B3	B Terminal RDAC #3.
14	W3	Wiper RDAC #3, addr = 010_2.
15	A3	A Terminal RDAC #3.
16	B1	B Terminal RDAC #1.
17	W1	Wiper RDAC #1, addr = 000_2.
18	A1	A Terminal RDAC #1.
19	A2	A Terminal RDAC #2.
20	W2	Wiper RDAC #2, addr = 001_2.
21	B2	B Terminal RDAC #2.
22	A4	A Terminal RDAC #4.
23	W4	Wiper RDAC #4, addr = 011_2.
24	B4	B Terminal RDAC #4.

AD5206 PIN FUNCTION DESCRIPTIONS

Pin No.	Name	Description
1	A6	A Terminal RDAC #6.
2	W6	Wiper RDAC #6, addr = 101_2.
3	B6	B Terminal RDAC #6.
4	GND	Ground.
5	$\overline{CS}$	Chip Select Input, Active Low. When $\overline{CS}$ returns high, data in the serial input register is decoded based on the address bits and loaded into the target RDAC latch.
6	V_{DD}	Positive power supply, specified for operation at both +3 V or +5 V. (Sum of $\|V_{DD}\| + \|V_{SS}\| < 5.5$ V.)
7	SDI	Serial Data Input. MSB First.
8	CLK	Serial Clock Input, positive edge triggered.
9	V_{SS}	Negative Power Supply, specified for operation at both 0 V or –2.7 V. (Sum of $\|V_{DD}\| + \|V_{SS}\| < 5.5$ V.)
10	B5	B Terminal RDAC #5.
11	W5	Wiper RDAC #5, addr = 100_2.
12	A5	A Terminal RDAC #5.
13	B3	B Terminal RDAC #3.
14	W3	Wiper RDAC #3, addr = 010_2.
15	A3	A Terminal RDAC #3.
16	B1	B Terminal RDAC #1.
17	W1	Wiper RDAC #1, addr = 000_2.
18	A1	A Terminal RDAC #1.
19	A2	A Terminal RDAC #2.
20	W2	Wiper RDAC #2, addr = 001_2.
21	B2	B Terminal RDAC #2.
22	A4	A Terminal RDAC #4.
23	W4	Wiper RDAC #4, addr = 011_2.
24	B4	B Terminal RDAC #4.

AD5204/AD5206–Typical Performance Characteristics

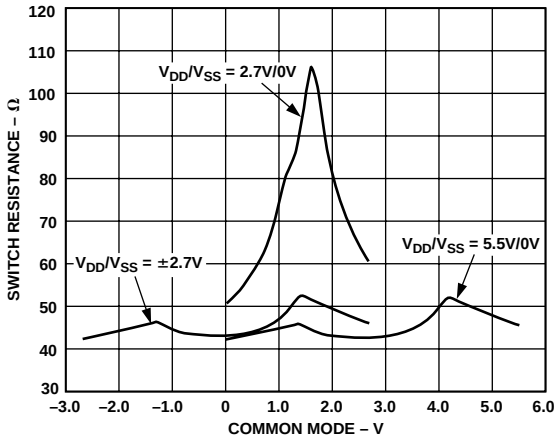


Figure 4. Incremental Wiper ON Resistance vs. Voltage

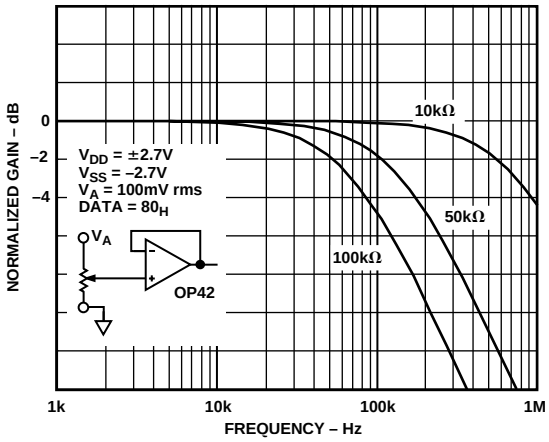


Figure 7. –3 dB Bandwidth vs. Terminal Resistance, ±2.7 V Dual Supply Operation

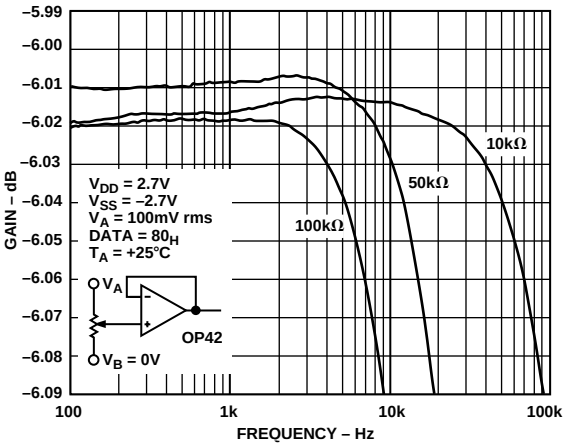


Figure 5. Gain Flatness vs. Frequency

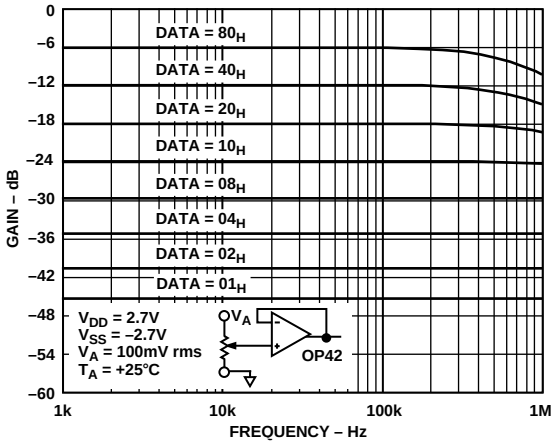


Figure 8. Bandwidth vs. Code, 10K Version

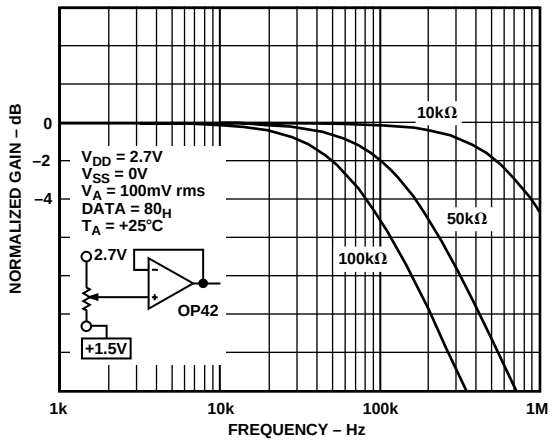


Figure 6. –3 dB Bandwidth vs. Terminal Resistance, 2.7 V Single Supply Operation

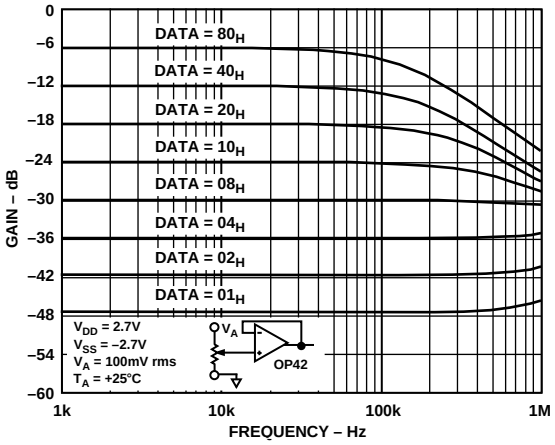


Figure 9. Bandwidth vs. Code, 50K Version

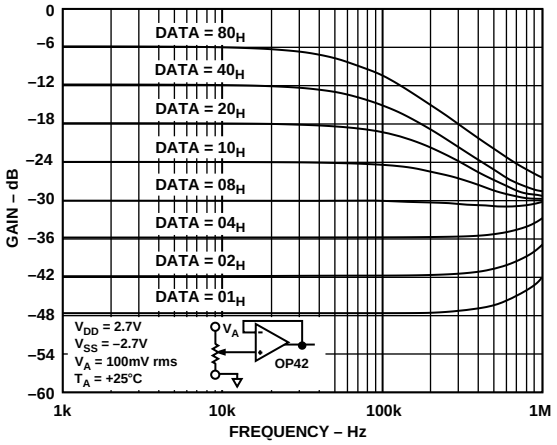


Figure 10. Bandwidth vs. Code, 100K Version

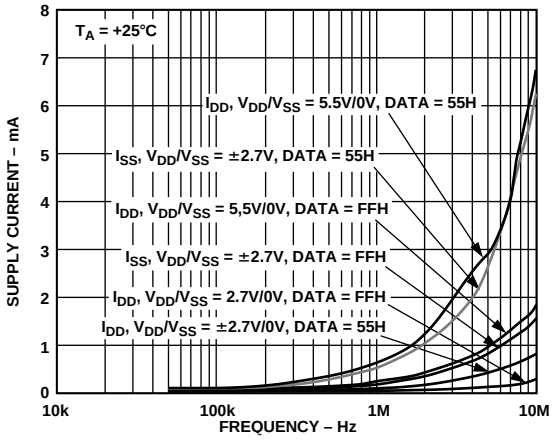


Figure 13. Supply Current vs. Clock Frequency

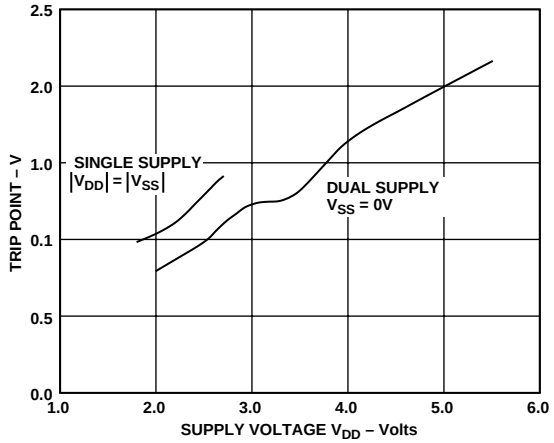


Figure 11. Digital Input Trip Point vs. Supply Voltage

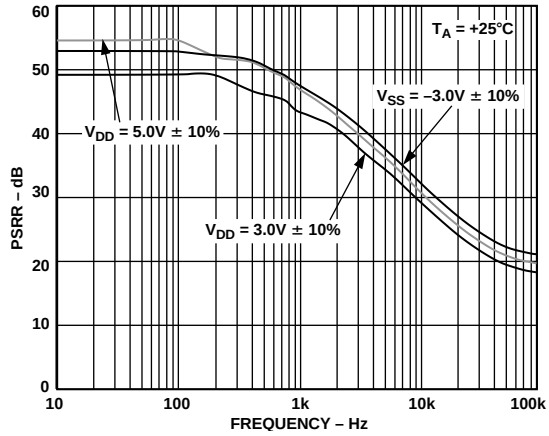


Figure 14. Power Supply Rejection vs. Frequency

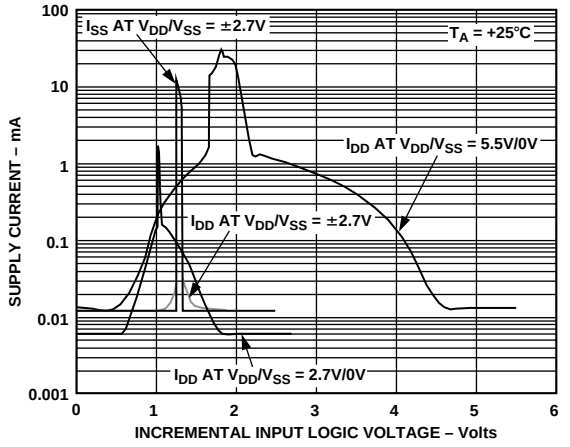


Figure 12. Supply Current vs. Input Logic Voltage

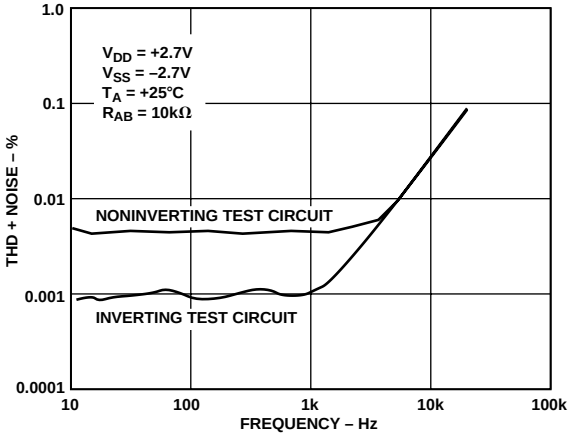


Figure 15. Total Harmonic Distortion Plus Noise vs. Frequency

OPERATION

The AD5204/AD5206 provides a four-/six-channel, 256-position digitally-controlled variable resistor (VR) device. Changing the programmed VR settings is accomplished by clocking in a 11-bit serial data word into the SDI (Serial Data Input) pin. The format of this data word is three address bits, MSB first, followed by eight data bits, MSB first. Table I provides the serial register data word format.

Table I. Serial-Data Word Format

ADDR			DATA							
B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
MSB		LSB	MSB							LSB
2^{10}		2^8	2^7							2^0

See Table IV for the AD5204/AD5206 address assignments to decode the location of VR latch receiving the serial register data in Bits B7 through B0. VR outputs can be changed one at a time in random sequence. The AD5204 presets to a midscale by asserting the PR pin, simplifying fault condition recovery at power up. Both parts have an internal power ON preset that places the wiper in a preset midscale condition at power ON. In addition, the AD5204 contains a power shutdown SHDN pin which places the RDAC in a zero power consumption state where Terminals Ax are open circuited and the wiper Wx is connected to Bx resulting in only leakage currents being consumed in the VR structure. In shutdown mode the VR latch settings are maintained, so that, returning to operational mode from power shutdown, the VR settings return to their previous resistance values.

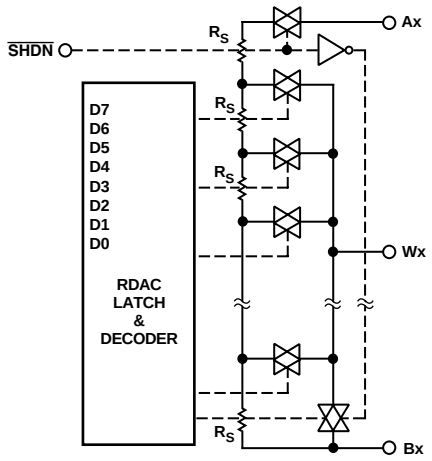


Figure 16. AD5204/AD5206 Equivalent RDAC Circuit

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation

The nominal resistance of the RDAC between Terminals A and B are available with values of 10 kΩ, 50 kΩ and 100 kΩ. The last digits of the part number determine the nominal resistance value, e.g., 10 kΩ = 10; 100 kΩ = 100. The nominal resistance (R_{AB}) of the VR has 256 contact points accessed by the wiper terminal, plus the B terminal contact. The eight-bit data word in the RDAC latch is decoded to select one of the 256 possible settings. The wiper's first connection starts at the B terminal for data 00_H. This B terminal connection has a wiper contact resistance of 45 Ω. The second connection (10 kΩ part) is the first tap point located at 84 Ω [= R_{BA} (nominal resistance)/256 + R_W = 84 Ω + 45 Ω] for data 01_H. The third connection is the next tap point representing 78 + 45 = 123 Ω for data 02_H. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 10006 Ω. The wiper does not directly connect to the A terminal. See Figure 16 for a simplified diagram of the equivalent RDAC circuit.

The general transfer equation determining the digitally programmed output resistance between Wx and Bx is:

$$R_{WB}(Dx) = (Dx)/256 \times R_{BA} + R_W \quad (1)$$

where *Dx* is the data contained in the 8-bit RDACx latch, and R_{BA} is the nominal end-to-end resistance.

For example, when V_B = 0 V and A terminal is open-circuit, the following output resistance values will be set for the following RDAC latch codes (applies to the 10K potentiometer):

Table II.

D (DEC)	R_{WB}-Ω	Output State
255	10006	Full Scale
128	5045	Midscale ($\overline{PR}$ = 0 Condition)
1	84	1 LSB
0	45	Zero Scale (Wiper Contact Resistance)

Note that in the zero-scale condition a finite wiper resistance of 45 Ω is present. Care should be taken to limit the current flow between W and B in this state to a maximum value of 20 mA to avoid degradation or possible destruction of the internal switch contact.

Like the mechanical potentiometer the RDAC replaces, it is totally symmetrical. The resistance between the Wiper W and Terminal A produces a digitally controlled resistance R_{WA}. When these terminals are used the B terminal should be tied to the wiper. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch is increased in value. The general transfer equation for this operation is:

$$R_{WA}(Dx) = (256-Dx)/256 \times R_{BA} + R_W \quad (2)$$

where *Dx* is the data contained in the 8-bit RDACx latch, and R_{BA} is the nominal end-to-end resistance. For example, when V_A = 0 V and B terminal is tied to the Wiper W the following output resistance values will be set for the following RDAC latch codes:

Table III.

D (DEC)	R_{WA}-Ω	Output State
255	84	Full Scale
128	5045	Midscale ($\overline{PR}$ = 0 Condition)
1	10006	1 LSB
0	10045	Zero Scale

The typical distribution of R_{BA} from channel-to-channel matches within ±1%. However, device-to-device matching is process lot dependent, having a ±30% variation. The change in R_{BA} with temperature has a 700 ppm/°C temperature coefficient.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates an output voltage proportional to the input voltage applied to a given terminal. For example, connecting A terminal to +5 V and B terminal to ground produces an output voltage at the wiper which can be any value starting at zero volts up to 1 LSB less than +5 V. Each LSB of voltage is equal to the voltage applied across Terminal AB divided by the 256-position resolution of the potentiometer divider. The general equation defining the output voltage with respect to ground for any given input voltage applied to terminals AB is:

$$V_W(Dx) = Dx/256 \times V_{AB} + V_B \quad (3)$$

Operation of the digital potentiometer in the divider mode results in more accurate operation over temperature. Here the output voltage is dependent on the ratio of the internal resistors not the absolute value, therefore, the drift improves to 15 ppm/°C.

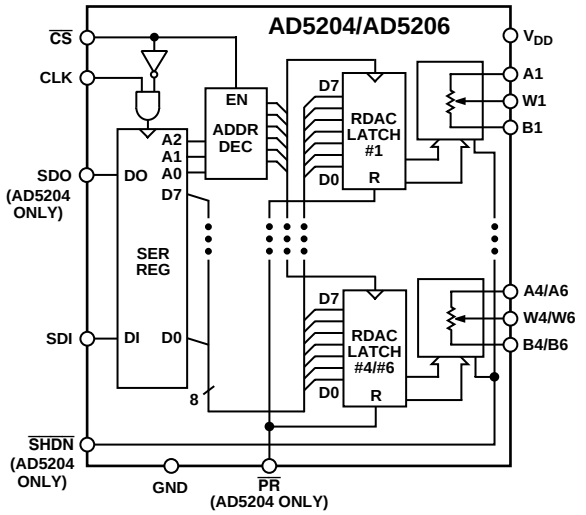


Figure 17. Block Diagram

DIGITAL INTERFACING

The AD5204/AD5206 contain a standard three-wire serial input control interface. The three inputs are clock (CLK), $\overline{CS}$ and serial data input (SDI). The positive-edge sensitive CLK input requires clean transitions to avoid clocking incorrect data into the serial input register. Standard logic families work well. If mechanical switches are used for product evaluation they should be debounced by a flip-flop or other suitable means. Figure 17 shows more detail of the internal digital circuitry. When $\overline{CS}$ is taken active low the clock loads data into the serial register on each positive clock edge, see Table IV. When using a positive (V_{DD}) and negative (V_{SS}) supply voltage, the logic levels are still referenced to digital ground (GND).

The serial-data-output (SDO) pin contains an open drain n-channel FET. This output requires a pull-up resistor in order to transfer data to the next package's SDI pin. The pull-up resistor termination voltage may be larger than the V_{DD} supply of the AD5204 SDO output device, e.g., the AD5204 could operate at V_{DD} = 3.3 V and the pull-up for interface to the next device could be set at +5 V. This allows for daisy chaining several RDACs from a single processor serial-data line. Clock period needs to be increased when using a pull-up resistor to the SDI pin of the following device in the series. Capacitive loading at the daisy chain node SDO-SDI between devices must be accounted for to successfully transfer data. When daisy chaining is used, the $\overline{CS}$ should be kept low until all the bits of every package are clocked into their respective serial registers insuring that the address bits and data bits are in the proper decoding location. This would require 22 bits of address and data complying to the word format provided in Table I if two AD5204 four-channel RDACs are daisy chained. During shutdown ($\overline{SHDN}$) the SDO output pin is forced to the off (logic high state) to disable power dissipation in the pull-up resistor. See Figure 19 for equivalent SDO output circuit schematic.

Table IV. Input Logic Control Truth Table

CLK	$\overline{CS}$	$\overline{PR}$	$\overline{SHDN}$	Register Activity
L	L	H	H	No SR effect, enables SDO pin.
P	L	H	H	Shift one bit in from the SDI pin. The eleventh previously entered bit is shifted out of the SDO pin.
X	P	H	H	Load SR data into RDAC latch based on A2, A1, A0 decode (Table V).
X	H	H	H	No Operation.
X	X	L	H	Sets all RDAC latches to midscale, wiper centered and SDO latch cleared.
X	H	P	H	Latches all RDAC latches to 80_H.
X	H	H	L	Open circuits all Resistor A terminals, connects W to B, turns off SDO output transistor.

NOTE: P = positive edge, X = don't care, SR = shift register.

Table V. Address Decode Table

A2	A1	A0	Latch Decoded
0	0	0	RDAC#1
0	0	1	RDAC#2
0	1	0	RDAC#3
0	1	1	RDAC#4
1	0	0	RDAC#5 AD5206 Only
1	0	1	RDAC#6 AD5206 Only

The data setup and data hold times in the specification table determine the data valid time requirements. The last 11 bits of the data word entered into the serial register are held when $\overline{CS}$ returns high. At the same time $\overline{CS}$ goes high it gates the address decoder enabling one of four or six positive edge triggered RDAC latches, see Figure 18 detail.

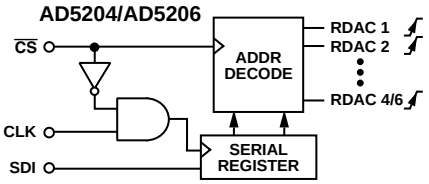


Figure 18. Equivalent Input Control Logic

The target RDAC latch is loaded with the last eight bits of the serial data word completing one DAC update. Four separate 8-bit data words must be clocked in to change all four VR settings.

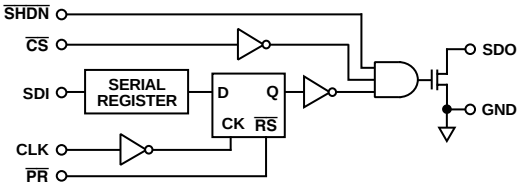


Figure 19. Detail SDO Output Schematic of the AD5204

All digital pins are protected with a series input resistor and parallel Zener ESD structure shown in Figure 20. Applies to digital pins $\overline{CS}$, SDI, SDO, $\overline{PR}$, $\overline{SHDN}$, CLK

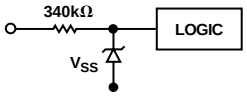


Figure 20. ESD Protection of Digital Pins

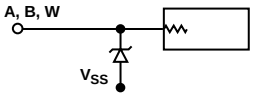


Figure 21. ESD Protection of Resistor Terminals

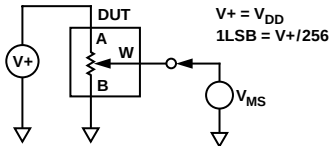


Figure 22. Potentiometer Divider Nonlinearity Error Test Circuit (INL, DNL)

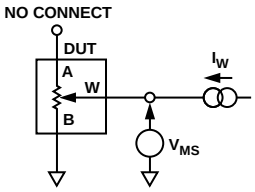


Figure 23. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

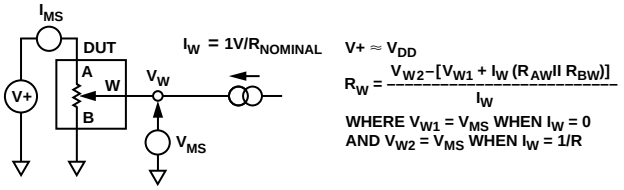


Figure 24. Wiper Resistance Test Circuit

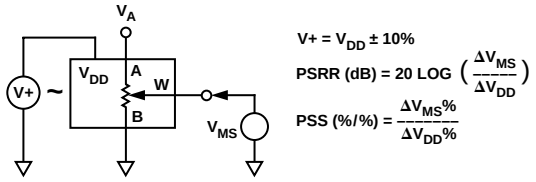


Figure 25. Power Supply Sensitivity Test Circuit (PSS, PSRR)

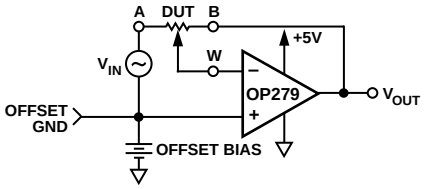


Figure 26. Inverting Programmable Gain Test Circuit

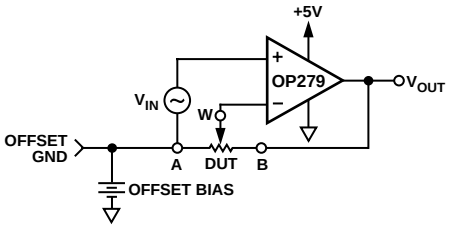


Figure 27. Noninverting Programmable Gain Test Circuit

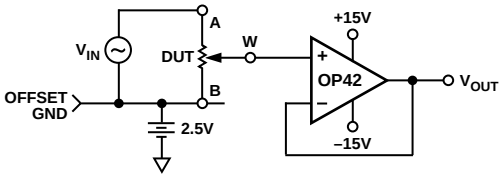


Figure 28. Gain vs. Frequency Test Circuit

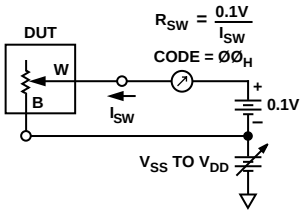
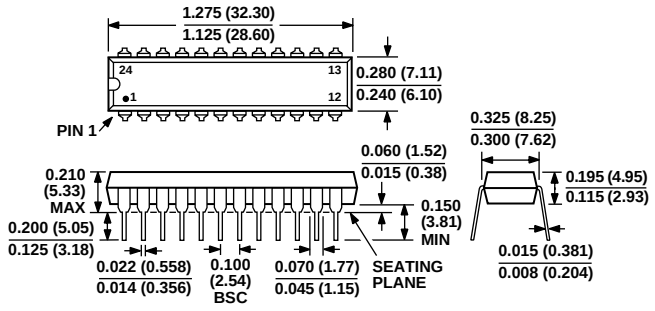


Figure 29. Incremental ON Resistance Test Circuit

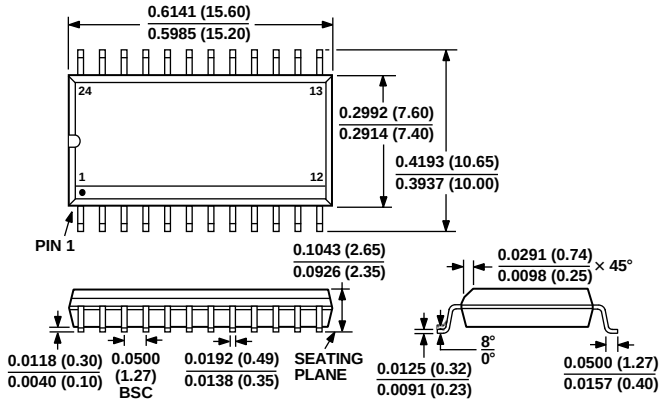
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

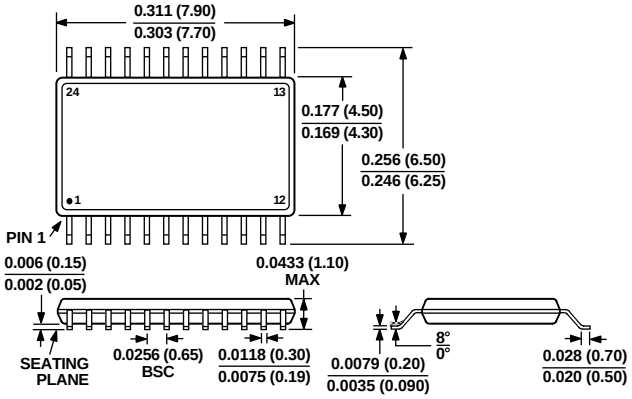
24-Lead Narrow Body PDIP
(N-24)



24-Lead SOIC
(R-24/SOL-24)



24-Lead Thin Shrink SO Package (TSSOP)
(RU-24)



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