AC '97 SoundMAX® Codec

AD1981A

AC '97 2.2-COMPLIANT CODEC

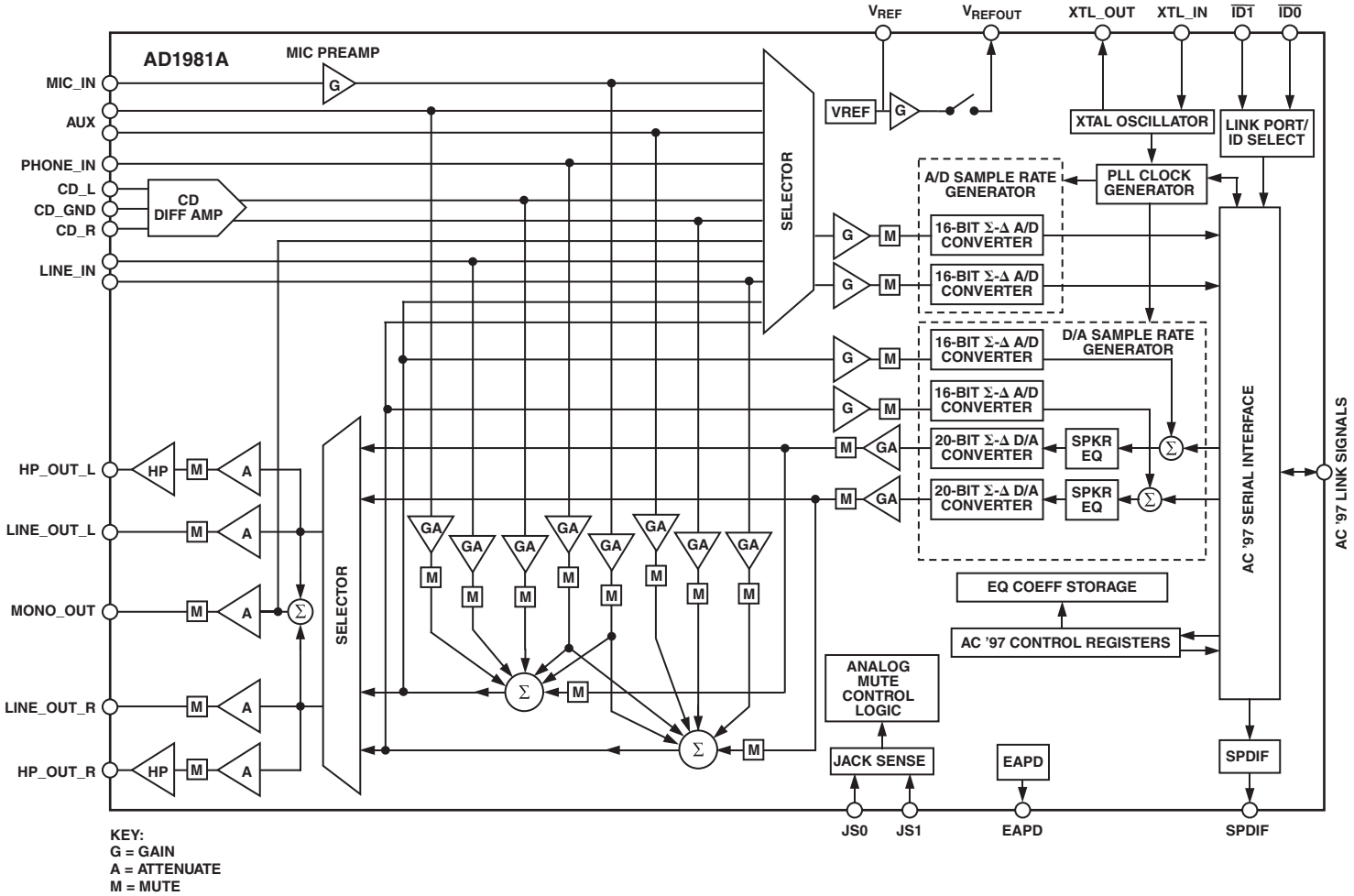
FEATURES

- S/PDIF Output, 20 Bits Data Format, Supporting 48 kHz and 44.1 kHz Sample Rates
- Integrated Stereo Headphone Amplifier
- Variable Sample Rate Audio
- External Audio Power-Down Control
- Greater than 90 dB Dynamic Range
- 16-Bit Stereo Full-Duplex Codec
- 20-Bit DAC Input
- Three Analog Line-Level Stereo Inputs for LINE-IN, AUX, and CD
- Mono Line-Level Phone Input
- Mono MIC Input with Built-In Programmable Preamp
- High Quality CD Input with Ground Sense
- Mono Output for Speakerphone or Internal Speaker
- Power Management Support
- 48-Lead LQFP Package

ENHANCED FEATURES

- Built-in Digital Equalizer Function for Optimized Speaker Sound
- Full Duplex Variable Sample Rates from 7040 Hz to 48 kHz with 1 Hz Resolution
- Jack Sense Pins Provide Automatic Output Switching
- Software-Programmed V_{REFOUT} Output for Microphone Bias and External Power Amp
- Split Power Supplies: 3.3 V Digital and 5 V Analog
- Multiple Codec Configuration Options

FUNCTIONAL BLOCK DIAGRAM



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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703
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AD1981A–SPECIFICATIONS

STANDARD TEST CONDITIONS UNLESS OTHERWISE NOTED

Temperature	25°C	DAC Test Conditions	
Digital Supply (DV_{DD})	3.3 V		Calibrated
Analog Supply (V_{DD})	5.0 V		0 dB Gain/Attenuation Relative to Full Scale
Sample Rate (F_S)	48 kHz		0 dB Input
Input Signal	1008 Hz		10 kΩ Output Load (LINE_OUT)
Analog Output Pass Band	20 Hz to 20 kHz		32 Ω Output Load (HP_OUT)
V_{IH}	2.0 V		
V_{IL}	0.8 V	ADC Test Conditions	
V_{IH} ($\overline{ID0}$, $\overline{ID1}$)	4.0 V		Calibrated
V_{IL} ($\overline{ID0}$, $\overline{ID1}$)	1.0 V		0 dB Gain
			Input –3.0 dB Relative to Full Scale

Parameter	Min	Typ	Max	Unit
ANALOG INPUT				
Input Voltage (RMS values assume sine-wave input)				
LINE_IN, AUX, CD, PHONE_IN		1		Vrms
		2.83		Vp-p
MIC_IN with 20 dB gain		0.1		Vrms
		0.283		Vp-p
MIC_IN with 0 dB gain		1		Vrms
		2.83		Vp-p
Input Impedance[1]		20		kΩ
Input Capacitance[1]		5	7.5	pF
MASTER VOLUME				
Step Size (0 dB to –46.5 dB);				
LINE_OUT_L, LINE_OUT_R		1.5		dB
Output Attenuation Range[1]		46.5		dB
Step Size (0 dB to –46.5 dB); MONO_OUT		1.5		dB
Output Attenuation Range[1]		46.5		dB
Step Size (0 dB to –46.5 dB); HP_OUT_R, HP_OUT_L		1.5		dB
Output Attenuation Range[1]		46.5		dB
Mute Attenuation of 0 dB Fundamental[1]	80			dB
PROGRAMMABLE GAIN AMPLIFIER—ADC				
Step Size (0 dB to 22.5 dB)		1.5		dB
PGA Gain Range		22.5		dB
ANALOG MIXER—INPUT GAIN/AMPLIFIERS/ATTENUATORS				
Signal-to-Noise Ratio (SNR)				
CD to LINE_OUT		90		dB
Other to LINE_OUT		90		dB
Step Size (+12 dB to –34.5 dB): (All steps tested)				
MIC_IN, LINE_IN, CD, AUX, PHONE_IN, DAC		1.5		dB
Input Gain/Attenuation Range:				
MIC_IN, LINE_IN, CD, AUX, PHONE_IN, DAC		46.5		dB
DIGITAL DECIMATION AND INTERPOLATION FILTERS[1]				
Pass Band	0		$0.4 \times F_S$	Hz
Pass Band Ripple			±0.09	dB
Transition Band	$0.4 \times F_S$		$0.6 \times F_S$	Hz
Stop Band	$0.6 \times F_S$		∞	Hz
Stop Band Rejection	–74			dB
Group Delay		$16/F_S$		s
Group Delay Variation over Pass Band		0		µs

SPECIFICATIONS

Parameter	Min	Typ	Max	Unit
ANALOG-TO-DIGITAL CONVERTERS				
Resolution		16		Bits
Total Harmonic Distortion (THD)		–84		dB
Dynamic Range				
(–60 dB Input THD+N Referenced to Full Scale, A-Weighted)	80	85		dB
Signal-to-Intermodulation Distortion (CCIF Method)[1]		85		dB
ADC Crosstalk[1]				
Line Inputs (Input L, Ground R, Read R; Input R, Ground L, Read L)		–80		dB
LINE_IN to Other		–100	–80	dB
Gain Error[2] (Full-Scale Span Relative to Nominal Input Voltage)			±10	%
Interchannel Gain Mismatch (Difference of Gain Errors)			±0.5	dB
ADC Offset Error[1]			±5	mV
DIGITAL-TO-ANALOG CONVERTERS				
Resolution		20		Bits
Total Harmonic Distortion (THD) LINE_OUT		–85		dB
Total Harmonic Distortion (THD) HP_OUT		–75		dB
Dynamic Range				
(–60 dB Input THD+N Referenced to Full Scale, A-Weighted)	85	90		dB
Signal-to-Intermodulation Distortion (CCIF Method)[1]		–100		dB
Gain Error (Actual Output Full-Scale Voltage Relative to Nominal Output Full-Scale)		±10		%
Interchannel Gain Mismatch (Difference of Gain Errors)			±0.7	dB
DAC Crosstalk (Input L, Zero R, Measure R_OUT; Input R, Zero L, Measure L_OUT)[1]			–80	dB
Total Audible Out-of-Band Energy (Measured from $0.6 \times F_S$ to 20 kHz)[1]		–40		dB
ANALOG OUTPUT				
Full-Scale Output Voltage; LINE_OUT and MONO_OUT		1		Vrms
		2.83		Vp-p
Output Impedance[1]			800	Ω
External Load Impedance[1]	10			kΩ
Output Capacitance[1]		15		pF
External Load Capacitance			100	pF
Full-Scale Output Voltage; HP_OUT (0 dB Gain)		1		Vrms
External Load Capacitance[1]			100	pF
External Load Impedance[1]	32			Ω
V_{REF}	2.05	2.25	2.45	V
V_{REFOUT} (selectable to 3.70 V nominal)		2.25		V
V_{REFOUT} Current Drive			5	mA
Mute Click				
(Muted Output Minus Unmuted Midscale DAC Output)		±5		mV
STATIC DIGITAL SPECIFICATIONS				
High Level Input Voltage (V_{IH}): Digital Inputs	0.65 × DVDD			V
Low Level Input Voltage (V_{IL})			0.35 × DVDD	V
High Level Output Voltage (V_{OH}), I_{OH} = 2 mA	0.9 × DVDD			V
Low Level Output Voltage (V_{OL}), I_{OL} = 2 mA			0.1 × DVDD	V
Input Leakage Current	–10		10	µA
Output Leakage Current	–10		10	µA
POWER SUPPLY				
Power Supply Range – Analog (AV_{DD})	4.65		5.25	V
Power Supply Range – Digital (DV_{DD})	3.15		3.45	V
Power Dissipation – 5 V/3.3 V			555	mW
Analog Supply Current – 5 V (AV_{DD})			78	mA
Digital Supply Current – 3.3 V(DV_{DD})			50	mA
Power Supply Rejection (100 mV p-p Signal @ 1 kHz)[1]				
(At Both Analog and Digital Supply Pins, Both ADCs and DACs)		40		dB
CLOCK SPECIFICATIONS[1]				
Input Clock Frequency		24.576		MHz
Recommended Clock Duty Cycle	40	50	60	%

AD1981A–SPECIFICATIONS

Parameter	Set Bits	DV_{DD} Typ	AV_{DD} Typ	Unit
POWER-DOWN STATES[3]				
(Fully Active)	(No Bits Value)	47	53	mA
ADC	PR0	39	47	mA
DAC	PR1	32	40	mA
ADC + DAC	PR1, PR0	13	34	mA
Mixer	PR2	47	21	mA
ADC + Mixer	PR2, PR0	39	16	mA
DAC + Mixer	PR2, PR1	32	8	mA
ADC + DAC + Mixer	PR2, PR1, PR0	13	1	mA
Standby	PR5, PR4, PR3, PR2, PR1, PR0	0	0	mA
Headphone Standby	PR6	47	40	mA

Parameter	Symbol	Min	Typ	Max	Unit
TIMING PARAMETERS					
(Guaranteed over Operating Temperature Range)					
RESET Active Low Pulsewidth	t_{RST_LOW}		1.0		ms
RESET Inactive to BIT_CLK Start-Up Delay	$t_{RST2CLK}$	162.8			ns
SYNC Active High Pulsewidth	t_{SYNC_HIGH}		1.3		ms
SYNC Low Pulsewidth	t_{SYNC_LOW}		19.5		
SYNC Inactive to BIT_CLK Start-Up Delay	$t_{SYNC2CLK}$	162.8			ns
BIT_CLK Frequency			12.288		MHz
BIT_CLK Period	t_{CLK_PERIOD}		81.4		ns
BIT_CLK Output Jitter[1]			750	48.84	ps
BIT_CLK High Pulsewidth	t_{CLK_HIGH}	32.56	42	48.84	ns
BIT_CLK Low Pulsewidth	t_{CLK_LOW}	32.56	38		ns
SYNC Frequency			48.0		kHz
SYNC Period	t_{SYNC_PERIOD}		20.8		ms
Setup to Falling Edge of BIT_CLK	t_{SETUP}	5	2.5		ns
Hold from Falling Edge of BIT_CLK	t_{HOLD}	5			ns
BIT_CLK Rise Time	$t_{RISECLK}$	2	4	6	ns
BIT_CLK Fall Time	$t_{FALLCLK}$	2	4	6	ns
SYNC Rise Time	$t_{RISESYNC}$	2	4	6	ns
SYNC Fall Time	$t_{FALLSYNC}$	2	4	6	ns
SDATA_IN Rise Time	$t_{RISEDIN}$	2	4	6	ns
SDATA_IN Fall Time	$t_{FALLDIN}$	2	4	6	ns
SDATA_OUT Rise Time	$t_{RISEDOUT}$	2	4	6	ns
SDATA_OUT Fall Time	$t_{FALLDOUT}$	2	4	6	ns
End of Slot 2 to BIT_CLK, SDATA_IN Low	t_{S2_PDOWN}	0		1.0	ms
Setup to Trailing Edge of RESET (Applies to SYNC, SDATA_OUT)	$t_{SETUP2RST}$	15			ns
Rising Edge of RESET to HI-Z Delay	t_{OFF}			25	ns
Propagation Delay				15	ns
RESET Rise Time				50	ns
Output Valid Delay from Rising Edge of BIT_CLK to SDI Valid				15	ns

NOTES
[1]Guaranteed but not tested.
[2]Measurement reflects main ADC.
[3]Values presented with V_{REFOUT} not loaded.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C unless otherwise noted.)

Power Supplies
- Digital (DV_{DD}) ..... –0.3 V to +3.6 V
- Analog (AV_{DD}) ..... –0.3 V to +6.0 V

Input Current (except Supply Pins) . . . . . ±10 mA

Signals Pins
- Digital Input Voltage . . . . . –0.3 V to DV_{DD} +0.3 V
- Analog Input Voltage . . . . . –0.3 V to AV_{DD} +0.3 V

Ambient Temperature Range (Operating) . . . . . 0°C to 70°C

Ambient Temperature Rating (TQFP Package)
- TAMB = TCASE – (PD × θ_{CA})
- TCASE = Case Temperature in °C
- PD = Power Dissipation in W
- θ_{JA} Thermal Resistance (Junction-to-Ambient) . . . 76.2°C/W
- θ_{JC} Thermal Resistance (Junction-to-Case) . . . . . 17°C/W
- θ_{JA} Thermal Resistance (Case-to-Ambient) . . . . . 52.2°C/W

Storage Temperature Range . . . . . –65°C to +150°C

*Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

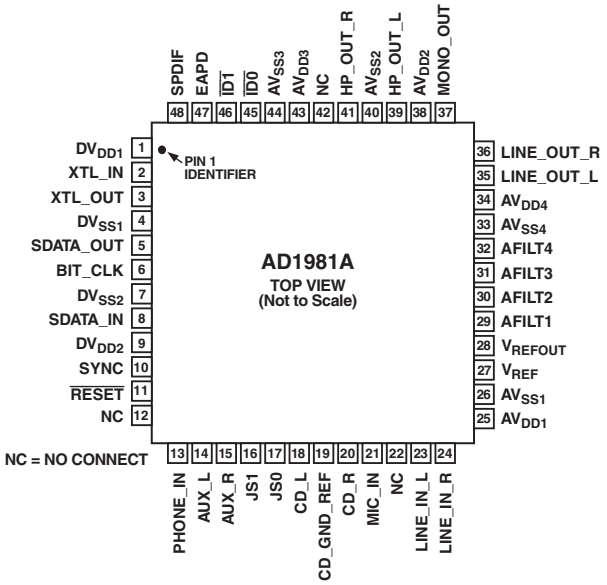
Model	Temperature Range	Package Description	Package Option*
AD1981AJST	0°C to 70°C	48-Lead LQFP	ST-48

*ST = Thin Quad Flatpack

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1981A features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	I/O	Function
DIGITAL I/O			
2	XTL_IN	I	Crystal Input (24.576 MHz) or External Clock Input
3	XTL_OUT	O	Crystal Output
5	SDATA_OUT	I	AC-Link Serial Data Output, AD1981A Data Input Stream
6	BIT_CLK	O/I	AC-Link Bit Clock Output (12.288 MHz) or Bit Clock Input if Secondary Mode Selected
8	SDATA_IN	O	AC-Link Serial Data Input, AD1981A Data Output Stream
10	SYNC	I	AC-Link Frame Sync
11	$\overline{\text{RESET}}$	I	AC-Link Reset, AD1981A Master H/W Reset
48	SPDIF	O	S/PDIF Output
CHIP SELECTS (These pins can also be used to select an external clock. See Table II.)			
45	$\overline{\text{ID0}}$	I	Chip Select Input 0 (Active Low) This pin can also be used as the chain input from a secondary Codec.
46	$\overline{\text{ID1}}$	I	Chip Select Input 1 (Active Low)
JACK SENSE AND EAPD			
17	JS0	I	JACK SENSE 0 Input
16	JS1	I	JACK SENSE 1 Input
47	EAPD	O	External Amp Power-Down Control
ANALOG I/O			
13	PHONE_IN	I	PHONE Input. Mono input from telephony subsystem speaker phone or handset.
14	AUX_L	I	AUXILIARY Input Left Channel
15	AUX_R	I	AUXILIARY Input Right Channel
18	CD_L	I	CD Audio Left Channel
19	CD_GND_REF	I	CD Audio Analog Ground Reference for Differential CD Input
20	CD_ R	I	CD Audio Right Channel
21	MIC_IN	I	Microphone Input (Mono)
23	LINE_IN_L	I	Line In Left Channel
24	LINE_IN_R	I	Line In Right Channel
35	LINE_OUT_L	O	Line Out (Front) Left Channel
36	LINE_OUT_R	O	Line Out (Front) Right Channel
37	MONO_OUT	O	Monaural Output to Telephony Subsystem Speakerphone
39	HP_OUT_L	O	Headphone Left Channel Output
41	HP_OUT_R	O	Headphone Right Channel Output
FILTER/REFERENCE (These signals are connected to resistors, capacitors, or specific voltages.)			
27	V_{REF}	O	Voltage Reference Filter
28	V_{REFOUT}	O	Voltage Reference Output 5 mA Drive (Intended for Mic Bias and Power Amp Bias)
29	AFILT1	O	Antialiasing Filter Capacitor—ADC Right Channel
30	AFILT2	O	Antialiasing Filter Capacitor—ADC Left Channel
31	AFILT3	O	Antialiasing Filter Capacitor—Mixer ADC Right Channel
32	AFILT4	O	Antialiasing Filter Capacitor—Mixer ADC Left Channel
POWER AND GROUND SIGNALS			
1	DV_{DD1}	I	Digital V_{DD} 3.3 V
4	DV_{SS1}	I	Digital GND
7	DV_{SS2}	I	Digital GND
9	DV_{DD2}	I	Digital V_{DD} 3.3 V
25	AV_{DD1}	I	Analog V_{DD} 5.0 V
26	AV_{SS1}	I	Analog GND
33	AV_{SS4}	I	Analog GND
34	AV_{DD4}	I	Analog V_{DD} 5.0 V
38	AV_{DD2}	I	Analog V_{DD} 5.0 V
40	AV_{SS2}	I	Analog GND
43	AV_{DD3}	I	Analog V_{DD} 5.0 V
44	AV_{SS3}	I	Analog GND
NO CONNECTS			
12	NC		No Connect
22	NC		No Connect
42	NC		No Connect

Indexed Control Registers

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	X	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	0090h
02h	Master Volume	MM	X	X	LMV4	LMV3	LMV2	LMV1	LMV0	RM*	X	X	RMV4	RMV3	RMV2	RMV1	RMV0	8000h
04h	Headphones Volume	HPM	X	X	LHV4	LHV3	LHV2	LHV1	LHV0	RM*	X	X	RHV4	RHV3	RHV2	RHV1	RHV0	8000h
06h	Mono Volume	MVM	X	X	X	X	X	X	X	X	X	X	MV4	MV2	MV2	MV1	MV0	8000h
0Ch	Phone Volume	PHM	X	X	X	X	X	X	X	X	X	X	PHV4	PHV3	PHV2	PHV1	PHV0	8008h
0Eh	Mic Volume	MCM	X	X	X	X	X	X	X	X	M20	X	MCV4	MCV3	MCV2	MCV1	MCV0	8008h
10h	Line In Volume	LM	X	X	LLV4	LLV3	LLV2	LLV1	LLV0	RM*	X	X	RLV4	RLV3	RLV2	RLV1	RLV0	8808h
12h	CD Volume	CM	X	X	LCV4	LCV3	LCV2	LCV1	LCV0	RM*	X	X	RCV4	RCV3	RCV2	RCV1	RCV0	8808h
16h	AUX Volume	AM	X	X	LAV4	LAV3	LAV2	LAV1	LAV0	RM*	X	X	RAV4	RAV3	RAV2	RAV1	RAV0	8808h
18h	PCM Out Vol	OM	X	X	LOV4	LOV3	LOV2	LOV1	LOV0	RM*	X	X	ROV4	ROV3	ROV2	ROV1	ROV0	8808h
1Ah	Record Select	X	X	X	X	X	LS2	LS1	LS0	X	X	X	X	X	RS2	RS1	RS0	0000h
1Ch	Record Gain	IM	X	X	X	LIM3	LIM2	LIM1	LIM0	RM*	X	X	X	RIM3	RIM2	RIM1	RIM0	8000h
20h	General Purpose	X	X	X	X	X	X	X	X	LPBK	X	X	X	X	X	X	X	0000h
26h	Power-Down Ctrl/Stat	EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	000Xh
28h	Ext'd Audio ID	ID1	ID0	X	X	REV1	REV0	AMAP	X	X	X	DSA1	DSA0	X	SPDIF	X	VRA	X605h
2Ah	Ext'd Audio Stat/Ctrl	VFORCE	X	X	X	X	SPCV	X	X	X	X	SPSA1	SPSA0	X	SPDIF	X	VRA	0000h
2Ch	PCM Front DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
	(SR1)																	
32h	PCM L/R ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
	(SR0)																	
3Ah	SPDIF Control	V	X	SPSR1	SPSR0	L	CC6	CC5	CC4	CC3	CC2	CC1	CC0	PRE	COPY	/AUD	PRO	2000h
60h	EQ CTRL	EQM	MAD LBEN	X	X	X	X	X	X	SYM	CHS	BCA5	BCA4	BCA3	BCA2	BCA1	BCA0	8080h
62h	EQ DATA	CFD15	CFD14	CFD13	CFD12	CFD11	CFD10	CFD9	CFD8	CFD7	CFD6	CFD5	CFD4	CFD3	CFD2	CFD1	CFD0	0000h
64h	Mixer ADC, Volume	MXM	X	X	X	LMG3	LMG2	LMG1	LMG0	RM*	X	X	X	RMG3	RMG2	RMG1	RMG0	8000h
72h	JACK SENSE	X	X	X	JS MT2	JS MT1	JS MT0	JS1 EQB	JS0 EQB	JS1 TMR	JS0 TMR	JS1 MD	JS0 MD	JS1 ST	JS0 ST	JS1 INT	JS0 INT	0000h
74h	Serial Configuration	SLOT 16	REGM 2	REGM 1	REGM 0	X	X	X	CHEN	X	X	X	INTS	X	SPAL	SPDZ	SPLNK	7001h
76h	Misc Control Bits	DACZ	X	M SPLT	X	DAM	X	FMXE	X	X	MAD PD	X	MAD ST	VREFH	VREFD	MBG1	MBG0	0000h
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	4144h
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	5372h

NOTES
All registers not shown. Bits containing an X are assumed to be reserved.
Odd registers are reserved, not aliased.
Reserved registers should not be written to.
Zeros should be written to bits containing an X.
*For AC '97 compatibility, Bit D7 (RM) is only available by setting the MSPLT Bit Register 76h. The MSPLT bit enables separate mute bits for the left and right channels. If MSPLT is not set, RM bit has no effect.

Reset (Index 00h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	X	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	0090h

Writing any value to this register performs a register reset, which causes all registers to revert to their default values (except 74h, which forces the serial configuration). Reading this register returns the ID code of the part and a code for the type of 3D Stereo Enhancement.

ID[9:0] Identify Capability. The ID decodes the capabilities of AD1981A based on the following:

Bit	Function	AD1981A
ID0	Dedicated Mic PCM In Channel	0
ID1	Modem Line Codec Support	0
ID2	Bass and Treble Control	0
ID3	Simulated Stereo (Mono to Stereo)	0
ID4	Headphone Out Support	1
ID5	Loudness (Bass Boost) Support	0
ID6	18-Bit DAC Resolution	0
ID7	20-Bit DAC Resolution	1
ID8	18-Bit ADC Resolution	0
ID9	20-Bit ADC Resolution	0

SE[4:0] Stereo Enhancement: The AD1981A does not provide hardware 3D stereo enhancement (all bits are zeros).

Master Volume Register (Index 02h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
02h	Master Volume	MM	X	X	LMV4	LMV3	LMV2	LMV1	LMV0	RM*	X	X	RMV4	RMV3	RMV2	RMV1	RMV0	8000h

* For AC '97 compatibility, Bit D7 (RM) is only available by setting the MSPLT bit Register 76h. The MSPLT bit enables separate mute bits for the left and right channels. If MSPLT is not set, RM bit has no effect.

This register controls the line_out volume controls for both stereo channels and mute bit. Each volume subregister contains 5 bits, generating 32 volume levels with 31 steps of 1.5 dB each.

Because AC '97 defines 6-bit volume registers, to maintain compatibility whenever the D5 or D13 bits are set to "1," their respective lower five volume bits are automatically set to "1" by the Codec logic. On readback, all lower 5 bits will read ones whenever these bits are set to "1."

RMV[4:0]	Right Master Volume Control: The least significant bit represents 1.5 dB. This register controls the output from 0 dB to a maximum attenuation of –46.5 dB.
RM	Right Channel Mute: Once enabled by the MSPLT Bit in Register 76h, this bit mutes the right channel separately from the MM bit. Otherwise, this bit will always read "0" and will have no effect when set to "1."
LMV[4:0]	Left Master Volume Control: The least significant bit represents 1.5 dB. This register controls the output from 0 dB to a maximum attenuation of –46.5 dB.
MM	Master Volume Mute: When this bit is set to "1," both L/R channels are muted, unless the MSPLT bit in Register 76h is set to "1," in which case this mute bit will only affect the left channel.

	xMV5…xMV0		
MM	WRITE	READBACK	Function
0	00 0000	00 0000	0 dB Gain
0	00 1111	00 1111	–22.5 dB Gain
0	01 1111	01 1111	–46.5 dB Gain
0	1x xxxx	01 1111	–46.5 dB Gain
1	xx xxxx	xx xxxx	–∞ dB Gain

Headphones Volume Register (Index 04h)[1]

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
04h	Headphones Volume	HPM	X	X	LHV4	LHV3	LHV2	LHV1	LHV0	RM[2]	X	X	RHV4	RHV3	RHV2	RHV1	RHV0	8000h

NOTES
[1]This register controls the headphone volume controls for both stereo channels and mute bit. Each volume subregister contains 5 bits, generating 32 volume levels with 31 steps of 1.5 dB each. Because AC '97 defines 6-bit volume registers, to maintain compatibility whenever the D5 or D13 Bits are set to "1," their respective lower five volume bits are automatically set to "1" by the CODEC logic. On readback, all lower 5 bits will read ones when ever these bits are set to "1."
[2]For AC '97 compatibility, Bit D7 (RM) is only available by setting the MSPLT bit Register 76h. The MSPLT bit enables separate mute bits for the left and right channels. If MSPLT is not set, RM bit has no effect.

RHV [4:0]	Right Headphone Volume Control: The least significant bit represents 1.5 dB. This register controls the output from 0 dB to a maximum attenuation of –46.5 dB.
RM	Right Channel Mute: Once enabled by the MSPLT Bit in Register 76h, this bit mutes the right channel separately from the HPM Bit. Otherwise, this bit will always read "0" and will have no effect when set to "1."
LHV [4:0]	Left Headphone Volume Control: The least significant bit represents 1.5 dB. This register controls the output from 0 dB to a maximum attenuation of –46.5 dB.
HPM	Headphones Volume Mute: When this bit is set to "1," both L/R channels are muted, unless the MSPLT Bit in Register 76h is set to "1," in which case, this mute bit will only affect the left channel.

	xHV5…xHV0 Function		
HPM	WRITE	READBACK	Function
0	00 0000	00 0000	0 dB Gain
0	00 1111	00 1111	–22.5 dB Gain
0	01 1111	01 1111	–46.5 dB Gain
0	1x xxxx	01 1111	–46.5 dB Gain
1	xx xxxx	xx xxxx	–∞ dB Gain

Mono Volume (Index 06h)*

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
06h	Mono Volume	MVM	X	X	X	X	X	X	X	X	X	X	MV4	MV3	MV2	MV1	MV0	8000h

*This register controls the headphone volume controls for both stereo channels and mute bit. Each volume subregister contains 5 bits, generating 32 volume levels with 31 steps of 1.5 dB each. Because AC '97 defines 6-bit volume registers, to maintain compatibility whenever the D5 or D13 Bits are set to "1," their respective lower five volume bits are automatically set to "1" by the CODEC logic. On readback, all lower 5 bits will read ones when ever these bits are set to "1."

MV[4:0]	Mono Volume Control: The least significant bit represents 1.5 dB. This register controls the output from 0 dB to a maximum attenuation of –46.5 dB.
MVM	Mono Volume Mute: When this bit is set to "1," the channel is muted.

	xMV5…xMV0		
MVM	WRITE	READBACK	Function
0	00 0000	00 0000	0 dB Gain
0	00 1111	00 1111	–22.5 dB Gain
0	01 1111	01 1111	–46.5 dB Gain
0	1x xxxx	01 1111	–46.5 dB Gain
1	xx xxxx	xx xxxx	–∞ dB Gain

Phone Volume (Index 0Ch)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0Ch	Phone Volume	PHM	X	X	X	X	X	X	X	X	X	X	PHV4	PHV3	PHV2	PHV1	PHV0	8008h

PHV[4:0]	Phone Volume: Allows setting the phone volume attenuator in 32 volume levels. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB with mute bit enabled.
PHM	Phone Mute: When this bit is set to "1," the phone channel is muted.

Mic Volume (Index 0Eh)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0Eh	Mic Volume	MCM	X	X	X	X	X	X	X	X	M20	X	MCV4	MCV3	MCV2	MCV1	MCV0	8008h

MCV[4:0]	MIC Volume Gain: Allows setting the mic volume attenuator in 32 volume levels. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB with mute enabled.
M20	MIC Gain Boost: This bit allows setting additional MIC gain to increase the microphone sensitivity. The nominal gain boost by default is 20 dB; however, bits D0 and D1 (MBG[1:0]) on the miscellaneous control bits register (76h) allow changing the gain boost to 10 dB or 30 dB if necessary. 0 = Disabled; Gain = 0 dB 1 = Enabled; Default Gain = 20 dB (see Register 76h, bits D0, D1)
MCM	MIC Mute: When this bit is set to "1," the MIC channel is muted.

Line In Volume (Index 10h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
10h	Line In Volume	LM	X	X	LLV4	LLV3	LLV2	LLV1	LLV0	RM*	X	X	RLV4	RLV3	RLV2	RLV1	RLV0	8808h

*For AC '97 compatibility, Bit D7 (RM) is only available by setting the MSPLT bit Register 76h. The MSPLT bit enables separate mute bits for the left and right channels. If MSPLT is not set, RM bit has no effect.

RLV[4:0]	Line In Volume Right: Allows setting the line in right channel attenuator in 32 volume levels. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.
RM	Right Channel Mute: Once enabled by the MSPLT Bit in Register 76h, this bit mutes the right channel separately from the LM bit. Otherwise, this bit will always read "0" and will have no effect when set to "1."
LLV[4:0]	Line In Volume Left: Allows setting the line in left channel attenuator in 32 volume levels. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.
LM	Line In Mute: When this bit is set to "1," both L/R channels are muted unless the MSPLT Bit in Register 76h is set to "1," in which case this mute bit will only affect the left channel.

CD Volume (Index 12h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
12h	CD Volume	CM	X	X	LCV4	LCV3	LCV2	LCV1	LCV0	RM*	X	X	RCV4	RCV3	RCV2	RCV1	RCV0	8808h

*For AC '97 compatibility, Bit D7 (RM) is only available by setting the MSPLT bit Register 76h. The MSPLT bit enables separate mute bits for the left and right channels. If MSPLT is not set, RM bit has no effect.

RCV[4:0]	Right CD Volume: Allows setting the CD right channel attenuator in 32 volume levels. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.
RM	Right Channel Mute: Once enabled by the MSPLT Bit in Register 76h, this bit mutes the right channel separately from the CM bit. Otherwise, this bit will always read "0" and will have no effect when set to "1."
LCV[4:0]	Left CD Volume: Allows setting the CD left channel attenuator in 32 volume levels. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.
CM	CD Volume Mute: When this bit is set to "1," both L/R channels are muted, unless the MSPLT Bit in Register 76h is set to "1," in which case, this mute bit will only affect the left channel.

AUX Volume (Index 16h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
16h	AUX Volume	AM	X	X	LAV4	LAV3	LAV2	LAV1	LAV0	RM*	X	X	RAV4	RAV3	RAV2	RAV1	RAV0	8808h

*For AC '97 compatibility, Bit D7 (RM) is only available by setting the MSPLT bit Register 76h. The MSPLT bit enables separate mute bits for the left and right channels. If MSPLT is not set, RM bit has no effect.

RAV[4:0]	Right AUX Volume: Allows setting the AUX right channel attenuator in 32 volume levels. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.
RM	Right Channel Mute: Once enabled by the MSPLT Bit in Register 76h, this bit mutes the right channel separately from the AM bit. Otherwise, this bit will always read "0" and will have no effect when set to "1."
LAV[4:0]	Left AUX Volume: Allows setting the AUX left channel attenuator in 32 volume levels. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.
AM	AUX Mute: When this bit is set to "1," both L/R channels are muted unless the MSPLT Bit in Register 76h is set to "1," in which case this mute bit will only affect the left channel.

PCM Out Volume (Index 18h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
18h	PCM Out Vol	OM	X	X	LOV4	LOV3	LOV2	LOV1	LOV0	RM*	X	X	ROV4	ROV3	ROV2	ROV1	ROV0	8808h

*For AC '97 compatibility, Bit D7 (RM) is only available by setting the MSPLT bit Register 76h. The MSPLT bit enables separate mute bits for the left and right channels. If MSPLT is not set, RM bit has no effect.

ROV[4:0]	Right PCM Out Volume: Allows setting the PCM right channel attenuator in 32 volume levels. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.
RM	Right Channel Mute: Once enabled by the MSPLT Bit in Register 76h, this bit mutes the right channel separately from the OM bit. Otherwise, this bit will always read "0" and will have no effect when set to "1."
LOV[4:0]	Left PCM Out Volume: Allows setting the PCM left channel attenuator in 32 volume levels. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.
OM	PCM Out Volume Mute: When this bit is set to "1," both L/R channels are muted unless the MSPLT Bit in Register 76h is set to "1," in which case this mute bit will only affect the left channel.

Volume Table (Index 0Ch to 18h)

Mute	x4…x0	Function
0	00000	+12 dB Gain
0	01000	0 dB Gain
0	11111	–34.5 dB Gain
1	xxxxx	–∞ dB Gain

Record Select Control Register (Index 1Ah)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
1Ah	Record Select	X	X	X	X	X	LS2	LS1	LS0	X	X	X	X	X	RS2	RS1	RS0	0000h

RS[2:0]	Right Record Select
LS[2:0]	Left Record Select

NOTES

Used to select the record source independently for right and left. See table for legend.

The default value is 0000h, which corresponds to MIC in.

RS1…RS0	Right Record Source
0	MIC
1	CD_R
2	Muted
3	AUX_R
4	LINE_IN_R
5	Stereo Mix (R)
6	Mono Mix
7	PHONE_IN

LS1…LS0	Left Record Source
0	MIC
1	CD_L
2	Muted
3	AUX_L
4	LINE_IN_L
5	Stereo Mix (L)
6	Mono Mix
7	PHONE_IN

Record Gain (Index 1Ch)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
1Ch	Record Gain	IM	X	X	X	LIM3	LIM2	LIM1	LIM0	RM*	X	X	X	RIM3	RIM2	RIM1	RIM0	8000h

*For AC '97 compatibility, Bit D7 (RM) is only available by setting the MSPLT bit Register 76h. The MSPLT bit enables separate mute bits for the left and right channels. If MSPLT is not set, RM bit has no effect.

RIM[3:0]	Right Input Mixer Gain Control: Each LSB represents 1.5 dB, 0000 = 0 dB, and the range is 0 dB to 22.5 dB.
RM	Right Channel Mute: Once enabled by the MSPLT Bit in Register 76h, this bit mutes the right channel separately from the IM bit. Otherwise, this bit will always read "0" and will have no effect when set to "1."
LIM[3:0]	Left Input Mixer Gain Control: Each LSB represents 1.5 dB, 0000 = 0 dB, and the range is 0 dB to 22.5 dB.
IM	Input Mute: When this bit is set to "1," both L/R channels are muted unless the MSPLT Bit in Register 76h is set to "1," in which case this mute bit will only affect the left channel.

IM	xIM3…xIM0	Function
0	1111	+22.5 dB Gain
0	0000	0 dB Gain
1	xxxxx	–∞ dB Gain

General Purpose Register (Index 20h)*

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
20h	General Purpose	X	X	X	X	X	X	X	X	LPBK	X	X	X	X	X	X	X	0000h

*This register should be read before writing to generate a mask for only the bit(s) that need to be changed.

LPBK	Loop-Back Control: ADC/DAC digital loop-back mode

Power-Down Control/Status Register (Index 26h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
26h	Power-Down Cntrl/Stat	EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	000Xh

NOTES
The ready bits are read only; writing to REF, ANL, DAC, ADC will have no effect. These bits indicate the status for the AD1981A subsections. If the bit is a "1" then that subsection is "ready." Ready is defined as the subsection able to perform in its nominal state.

ADC	ADC sections ready to transmit data
DAC	DAC sections ready to accept data
ANL	Analog amplifiers, attenuators, and mixers ready
REF	Voltage references, V_{REF} and V_{REFOUT} up to nominal level
PR[6:0]	CODEC Power-Down Modes. The first 3 bits are to be used individually rather than in combination with each other. PR3 can be used in combination with PR2 or by itself. The mixer and reference cannot be powered down via PR3 unless the ADCs and DACs are also powered down. Nothing else can be powered up until the reference is up. PR5 has no effect unless all ADCs, DACs, and the AC Link are powered down. The reference and mixer can be either up or down, but all power-up sequences must be allowed to run to completion before PR5 and PR4 are both set. In multiple-codec systems, the master CODEC's PR5 and PR4 bits control the slave CODEC. PR5 is also effective in the slave CODEC if the master's PR5 bit is clear, but the PR4 bit has no effect except to enable or disable PR5.
EAPD	External Audio Power-Down Control: Controls the state of the EAPD Pin EAPD = 0 sets the EAPD Pin low, enabling an external power amplifier (reset default). EAPD = 1 sets the EAPD Pin high, shutting the external power amplifier off.

Power-Down State	Set Bits
ADCs and Input Mux Power-Down	PR0
DACs Power-Down	PR1
Analog Mixer Power-Down (V_{REF} and V_{REFOUT} on)	PR1, PR2
Analog Mixer Power-Down (V_{REF} and V_{REFOUT} off)	PR0, PR1, PR3
AC-Link Interface Power-Down	PR4
Internal Clocks Disabled	PR0, PR1, PR4, PR5
ADC and DAC Power Down	PR0, PR1
V_{REF} Standby Mode	PR0, PR1, PR2, PR4, PR5
Total Power-Down	PR0, PR1, PR2, PR3, PR4, PR5
Headphone Amp Power in Standby	PR6

Extended Audio ID Register (Index 28h)

REG	NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
28h	Ext'd Audio ID	ID1	ID0	X	X	REV1	REV0	AMAP	X	X	X	DSA1	DSA0	X	SPDIF	X	VRA	X605h

The extended audio ID register identifies which extended audio features are supported. A non-zero extended audio ID value indicates one or more of the extended audio features are supported.

VRA	Variable Rate PCM Audio Support: (read-only) This bit returns a "1" when read to indicate that variable rate PCM audio is supported.
SPDIF	SPDIF Support: (read-only) This bit returns a "1" when read to indicate that SPDIF transmitter is supported (IEC958).
DSA[1:0]	DAC Slot Assignments: (read/write) (reset default = 00) 00 DACs 1, 2 = 3 and 4 01 DACs 1, 2 = 7 and 8 10 DACs 1, 2 = 6 and 9 11 DACs 1, 2 = 10 and 11
AMAP	Slot DAC mappings based on Codec ID: (read only) This bit returns a "1" when read to indicate that slot/DAC mappings based on Codec ID is supported.
REV[1:0]	REV[1, 0] = 01 indicates Codec is AC '97 revision 2.2-compliant (read-only).
ID[1:0]	Indicates Codec Configuration: (read-only) 00 = Primary 01, 10, 11 = Secondary

Extended Audio Status and Control Register (Index 2Ah)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
2Ah	Ext'd Audio Stat/Ctrl	VFORCE	X	X	X	X	SPCV	X	X	X	X	SPSA1	SPSA0	X	SPDIF	X	VRA	0000h

*The extended audio status and control register is a read/write register that provides status and control of the extended audio features.

VRA	Variable Rate Audio: (read/write) VRA = 0, sets fixed sample rate audio at 48 KHz (reset default). VRA = 1, enables variable rate audio mode (enables sample rate registers and SLOTREQ signaling).
SPDIF	SPDIF Transmitter Subsystem Enable/Disable Bit: (read/write) SPDIF = 1 enables the SPDIF transmitter. SPDIF = 0 disables the SPDIF transmitter (default). This bit is also used to validate that the SPDIF transmitter output is actually enabled. The SPDIF bit is only allowed to be set high if the SPDIF pin (48) is pulled down at power-up enabling the Codec transmitter logic. If the SPDIF pin is floating or pulled high at power-up, the transmitter logic is disabled and this bit therefore returns a low, indicating that the SPDIF transmitter is not available. This bit must always be read back to verify that the SPDIF transmitter is actually enabled.
SPSA[1:0]	SPDIF Slot Assignment Bits: (read/write) These bits control the SPDIF slot assignment and respective defaults, depending on the Codec ID configuration.
SPCV	SPDIF Configuration Valid: (read-only) Indicates the status of the SPDIF transmitter subsystem, enabling the driver to determine if the currently programmed SPDIF configuration is supported. SPCV is always valid, independent of the SPDIF-enable bit status. SPCV = 0 indicates current SPDIF configuration {SPSA, SPSR, DAC slot rate, DRS} is not valid (not supported). SPCV = 1 indicates current SPDIF configuration {SPSA, SPSR, DAC slot rate, DRS} is valid (supported).
VFORCE	Validity Force Bit: (reset default = 0) When asserted, this bit forces the SPDIF stream "Validity" flag (Bit 28 within each SPDIF L/R subframe) to be controlled by the "V" bit (D15) in Register 3Ah (SPDIF control register). VFORCE = 0 and "V" = 0; The "Validity" bit is managed by the Codec error detection logic. VFORCE = 0 and "V" = 1; The "Validity" bit is forced high, indicating subframe data is invalid. VFORCE = 1 and "V" = 0; The "Validity" bit is forced low, indicating subframe data is valid. VFORCE = 1 and "V" = 1; The "Validity" bit is forced high, indicating subframe data is invalid.

AC '97 2.2 AMAP-Compliant Default SPDIF Slot Assignments

CODEC ID	Function	SPSA = 00	SPSA = 01	SPSA = 10	SPSA = 11
00	2-Ch Primary w/SPDIF	3 and 4	7 and 8 [default]	6 and 9	10 and 11
00	4-Ch Primary w/SPDIF	3 and 4	7 and 8	6 and 9 [default]	10 and 11
00	6-Ch Primary w/SPDIF	3 and 4	7 and 8	6 and 9	10 and 11 [default]
01	+2-Ch Secondary w/SPDIF	3 and 4	7 and 8	6 and 9 [default]	
01	+4-Ch Secondary w/SPDIF	3 and 4	7 and 8	6 and 9	10 and 11 [default]
10	+2-Ch Secondary w/SPDIF	3 and 4	7 and 8	6 and 9 [default]	
10	+4-Ch Secondary w/SPDIF	3 and 4	7 and 8	6 and 9	10 and 11 [default]
11	+2-Ch Secondary w/SPDIF	3 and 4	7 and 8	6 and 9	10 and 11 [default]

PCM Front DAC Rate Register (Index 2Ch)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
2Ch	PCM Front DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h

*This read/write sample rate control register contains 16-bit unsigned value, representing the rate of operation in Hz.

SR[15:0]	Sample Rate: The sampling frequency range is from 7 kHz (1B58h) to 48 kHz (BB80h) in 1 Hz increments. If "0" is written to VRA, then the sample rate is reset to 48k.

PCM ADC Rate Register (Index 32h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
32h	PCM L/R ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h

This read/write sample rate control register contains 16-bit unsigned value, representing the rate of operation in Hz.

SR[15:0]	Sample Rate: The sampling frequency range is from 7 kHz (1B58h) to 48 kHz (BB80h) in 1 Hz increments. If "0" is written to VRA, then the sample rate is reset to 48k.

SPDIF Control Register (Index 3Ah)

Reg. Num.	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
3Ah	SPDIF Control	V	X	SPSR1	SPSR0	L	CC6	CC5	CC4	CC3	CC2	CC1	CC0	PRE	COPY	/AUD	PRO	2000h

*Register 3Ah is a read/write register that controls SPDIF functionality and manages bit fields propagated as channel status (or subframe in the V case). With the exception of V, this register should only be written to when the SPDIF transmitter is disabled (SPDIF bit in Register 2Ah is "0"). This ensures that control and status information start up correctly at the beginning of SPDIF transmission.

PRO	Professional: "1" indicates professional use of channel status, "0" indicates consumer.
/AUD	Non-Audio: "1" indicates data is non-PCM format, "0" data is PCM.
COPY	Copyright: "1" indicates copyright is asserted, "0" copyright is not asserted.
PRE	Pre-Emphasis: "1" indicates filter pre-emphasis is 50/15 msec, "0" pre-emphasis is none.
CC[6:0]	Category Code: Programmed according to IEC standards, or as appropriate.
L	Generation Level: Programmed according to IEC standards, or as appropriate.
SPSR[1:0]	SPDIF Transmit Sample Rate: SPSR[1:0] = "00" Transmit Sample Rate = 44.1 kHz SPSR[1:0] = "01" Reserved SPSR[1:0] = "10" Transmit Sample Rate = 48 kHz (Reset Default) SPSR[1:0] = "11" Not Supported
V	Validity: This bit affects the "Validity" flag (Bit 28 transmitted in each SPDIF L/R subframe) and enables the SPDIF transmitter to maintain connection during error or mute conditions. V = 1 Each SPDIF subframe (L + R) has Bit 28 set to "1." This tags both samples as invalid. V = 0 Each SPDIF subframe (L + R) has Bit 28 set to "0" for valid data and "1" for invalid data (error condition). Note that when V = 0, asserting the VFORCE bit (D15) in Register 2Ah (Ext'd Audio Stat/Ctrl) will force the "Validity" flag low, marking both samples as valid.

EQ Control Register (Index 60h)

Reg. Num.	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
60h	EQCTRL	EQM	MAD LBEN	X	X	X	X	X	X	SYM	CHS	BCA5	BCA4	BCA3	BCA2	BCA1	BCA0	8080h

*Register 60h is a read/write register that controls the equalizer functionality and data setup. The register also contains the biquad and coefficient address pointer, which is used in conjunction with the EQ data register (78h) to set up the equalizer coefficients.

The reset default disables the equalizer function until the coefficients can be properly set up by the software and sets the Symmetry Bit to allow equal coefficients for left and right channels.

BCA[5,0]	Biquad and Coefficient Address Pointer: biquad 0 coef a0 BCA[5,0] = 011011 biquad 0 coef a1 BCA[5,0] = 011010 biquad 0 coef a2 BCA[5,0] = 011001 biquad 0 coef b1 BCA[5,0] = 011101 biquad 0 coef b2 BCA[5,0] = 011100 biquad 1 coef a0 BCA[5,0] = 100000 biquad 1 coef a1 BCA[5,0] = 011111 biquad 1 coef a2 BCA[5,0] = 011110 biquad 1 coef b1 BCA[5,0] = 100010 biquad 1 coef b2 BCA[5,0] = 100001 biquad 2 coef a0 BCA[5,0] = 100101 biquad 2 coef a1 BCA[5,0] = 100100 biquad 2 coef a2 BCA[5,0] = 100011 biquad 2 coef b1 BCA[5,0] = 100111 biquad 2 coef b2 BCA[5,0] = 100110 biquad 3 coef a0 BCA[5,0] = 101010 biquad 3 coef a1 BCA[5,0] = 101001 biquad 3 coef a2 BCA[5,0] = 101000 biquad 3 coef b1 BCA[5,0] = 101100 biquad 3 coef b2 BCA[5,0] = 101011 biquad 4 coef a0 BCA[5,0] = 101111 biquad 4 coef a1 BCA[5,0] = 101110 biquad 4 coef a2 BCA[5,0] = 101101 biquad 4 coef b1 BCA[5,0] = 110001 biquad 4 coef b2 BCA[5,0] = 110000 biquad 5 coef a0 BCA[5,0] = 110100 biquad 5 coef a1 BCA[5,0] = 110011 biquad 5 coef a2 BCA[5,0] = 110010 biquad 5 coef b1 BCA[5,0] = 110110 biquad 5 coef b2 BCA[5,0] = 110101 biquad 6 coef a0 BCA[5,0] = 111001 biquad 6 coef a1 BCA[5,0] = 111000 biquad 6 coef a2 BCA[5,0] = 110111 biquad 6 coef b1 BCA[5,0] = 111011 biquad 6 coef b2 BCA[5,0] = 111010

CHS	Channel Select: CHS = 0 Selects Left Channel Coefficients Data Block CHS = 1 Selects Right Channel Coefficients Data Block
SYM	Symmetry: When set to "1," this bit indicates that the left and right channel coefficients are equal. This shortens the coefficients setup sequence since only the left channel coefficients need to be addressed and set up (the right channel coefficients are fetched from the left channel memory).
MAD LBEN	Mixer ADC Loop-Back Enable: Enables mixer ADC data to be summed into PCM stream. 0 = No Loop-Back allowed (default) 1 = Enable Loop-Back
EQM	Equalizer Mute: When set to "1," this bit disables the equalizer function (allows all data pass-through). The reset default sets this bit to "1," disabling the equalizer function until the biquad coefficients can be properly set.

EQ Data Register (Index 62h)

Reg. Num.	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
62h	EQ DATA	CFD15	CFD14	CFD13	CFD12	CFD11	CFD10	CFD9	CFD8	CFD7	CFD6	CFD5	CFD4	CFD3	CFD2	CFD1	CFD0	0000h

This read/write register is used to transfer EQ biquad coefficients into memory.
The register data is transferred to, or retrieved from, the address pointed by the BCA bits in the EQ CNTRL Register (60h). Data will only be written to memory if the EQM Bit (Register 60h Bit 15) is asserted. DACs should be powered down when new EQ coefficients are being added.

CFD[15:0]	Coefficient Data: The biquad coefficients are fixed point format values with 16 bits of resolution. The CFD15 bit is the MSB, and the CFD0 bit is the LSB.

Mixer ADC, Input Gain Register (Index 64h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
64h	Mixer Volume	MXM	X	X	X	LMG3	LMG2	LMG1	LMG0	RM*	X	X	X	RMG3	RMG2	RMG1	RMG0	8000h

*For AC '97 compatibility, Bit D7 (RM) is only available by setting the MSPLT bit in Register 76h. The MSPLT bit enables separate mute bits for the left and right channels. If MSPLT is not set, RM bit has no effect.

RMG[3:0]	Right Mixer Gain Control: This register controls the gain into the mixer ADC, from 0 dB to a maximum gain of +22.5 dB. The least significant bit represents 1.5 dB.
RM	Right Channel Mute: Once enabled by the MSPLT bit in Register 76h, this bit mutes the right channel separately from the IM bit. Otherwise, this bit will always read "0" and will have no effect when set to "1."
LMG[3:0]	Left Mixer Gain Control: This register controls the gain into the mixer ADC, from 0 dB to a maximum gain of +22.5 dB. The least significant bit represents 1.5 dB.
MXM	Mixer Gain Mute: 0 = Unmuted, 1 = Muted or –∞ dB gain.

MXM	xMG3…xMG0	Function
0	1111	+22.5 dB gain
0	0000	0 dB gain
1	xxxxx	–∞ dB gain

Jack Sense/Audio Interrupt/Status Register (Index 72h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
72h	JACK SENSE	X	X	X	JS MT2	JS MT1	JS MT0	JS1 EQB	JS0 EQB	JS1 TMR	JS0 TMR	JS1 MD	JS0 MD	JS1 ST	JS0 ST	JS1 INT	JS0 INT	0000h

All register bits are read/write except for JS0ST and JS1ST, which are read only.

JS0INT	Indicates Pin JS0 has generated an interrupt. Remains set until the software services JS0 interrupt, i.e., JS0 ISR, should clear this bit by writing a "0" to it. Note that the interrupt to the system is actually an OR combination of this bit and JS1INT. Also note that the actual interrupt implementation is selected by the INTS Bit (Reg 74h). It is also possible to generate a software system interrupt by writing a "1" to this bit.
JS1INT	Indicates Pin JS1 has generated an interrupt. Remains set until the software services JS1 interrupt, i.e., JS1 ISR should clear this bit by writing a "0" to it. See JS0INT description above for additional details.
JS0ST	JS0 STATE: This bit always reports the logic state of JS0 Pin.
JS1ST	JS1 STATE: This bit always reports the logic state of JS1 Pin.
JS0MD	JS0 MODE: This bit selects the operation mode for the JS0 Pin. 0 = Jack Sense Mode (Default) 1 = Interrupt Mode
JS1MD	JS1 MODE: This bit selects the operation mode for the JS1 Pin. 0 = Jack Sense Mode (Default) 1 = Interrupt Mode
JS0TMR	JS0 Timer Enable: If this bit is set to a "1," JS0 must be high for greater than 250 ms to be recognized.
JS1TMR	JS1 Timer Enable: If this bit is set to a "1," JS1 must be high for greater than 250 ms to be recognized.
JS0EQB	JS0 EQ Bypass Enable: This bit enables JS0 to control the EQ bypass. When this bit is set to "1," JS0 = 1 will cause the EQ to be bypassed.
JS1EQB	JS1 EQ Bypass Enable: This bit enables JS1 to control the EQ bypass. When this bit is set to "1," JS1 = 1 will cause the EQ to be bypassed.
JSMT[2,0]	JS Mute Enable Selector: These 3 bits select and enable the Jack Sense muting action (see Table I).

Table I. Jack Sense Mute Table – JSMT [2:0]

REF	JS1 HEADPHONE	JS0 LINE OUT	JSMT2	JSMT1	JSMT0	H.P. OUT	LINE OUT	MONO OUT	NOTES
0	OUT (0)	OUT (0)	0	0	0	ACTIVE	ACTIVE	ACTIVE	JS0 and JS1
1	OUT (0)	IN (1)	0	0	0	ACTIVE	ACTIVE	ACTIVE	Ignored
2	IN (1)	OUT (0)	0	0	0	ACTIVE	ACTIVE	ACTIVE	
3	IN (1)	IN (1)	0	0	0	ACTIVE	ACTIVE	ACTIVE	
4	OUT (0)	OUT (0)	0	0	1	FMUTE	FMUTE	ACTIVE	JS0 no mute action,
5	OUT (0)	IN (1)	0	0	1	FMUTE	ACTIVE	ACTIVE	JS1 mutes Line_out
6	IN (1)	OUT (0)	0	0	1	ACTIVE	FMUTE	ACTIVE	
7	IN (1)	IN (1)	0	0	1	ACTIVE	FMUTE	ACTIVE	
8	OUT (0)	OUT (0)	0	1	0	FMUTE	FMUTE	ACTIVE	JS0 no mute action,
9	OUT (0)	IN (1)	0	1	0	FMUTE	ACTIVE	ACTIVE	JS1 mutes Mono and
10	IN (1)	OUT (0)	0	1	0	ACTIVE	FMUTE	FMUTE	Line_out
11	IN (1)	IN (1)	0	1	0	ACTIVE	FMUTE	FMUTE	
12	OUT (0)	OUT (0)	0	1	1	**	**	**	** RESERVED
13	OUT (0)	IN (1)	0	1	1	**	**	**	
14	IN (1)	OUT (0)	0	1	1	**	**	**	
15	IN (1)	IN (1)	0	1	1	**	**	**	
16	OUT (0)	OUT (0)	1	0	0	FMUTE	FMUTE	ACTIVE	JS0 mutes Mono,
17	OUT (0)	IN (1)	1	0	0	FMUTE	ACTIVE	FMUTE	JS1 no mute action
18	IN (1)	OUT (0)	1	0	0	ACTIVE	FMUTE	ACTIVE	
19	IN (1)	IN (1)	1	0	0	ACTIVE	ACTIVE	FMUTE	
20	OUT (0)	OUT (0)	1	0	1	FMUTE	FMUTE	ACTIVE	JS0 mutes Mono,
21	OUT (0)	IN (1)	1	0	1	FMUTE	ACTIVE	FMUTE	JS1 mutes Line_out
22	IN (1)	OUT (0)	1	0	1	ACTIVE	FMUTE	ACTIVE	
23	IN (1)	IN (1)	1	0	1	ACTIVE	FMUTE	FMUTE	
24	OUT (0)	OUT (0)	1	1	0	FMUTE	FMUTE	ACTIVE	JS0 mutes Mono,
25	OUT (0)	IN (1)	1	1	0	FMUTE	ACTIVE	FMUTE	JS1 mutes Mono and
26	IN (1)	OUT (0)	1	1	0	ACTIVE	FMUTE	FMUTE	Line_out
27	IN (1)	IN (1)	1	1	0	ACTIVE	FMUTE	FMUTE	
28	OUT (0)	OUT (0)	1	1	1	**	**	**	** RESERVED
29	OUT (0)	IN (1)	1	1	1	**	**	**	
30	IN (1)	OUT (0)	1	1	1	**	**	**	
31	IN (1)	IN (1)	1	1	1	**	**	**	

FMUTE = Output is forced to mute independent of the respective volume register setting.
ACTIVE = Output is not muted and its status is dependent on the respective volume register setting.
OUT = Nothing plugged into the jack and, therefore, the JS status is low (via the load resistor pull-down).
IN = Jack has plug inserted and therefore the JS status is high (via the CODEC JS internal pull-up).

Serial Configuration (Index 74h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
74h	Serial Configuration	SLOT16	REGM2	REGM1	REGM0	X	X	X	CHEN	X	X	X	INTS	X	SPAL	SPDZ	SPLNK	7001h

This register is not reset when the reset register (Register 00h) is written.

SPLNK	SPDIF LINK: This bit enables the SPDIF to link with the DAC for data requesting. 0 = SPDIF and DAC are not linked. 1 = SPDIF and DAC are linked and receive same data requests (reset default).
SPDZ	SPDIF DACZ: 0 = Repeat last sample out the SPDIF stream if FIFO underruns (reset default). 1 = Forces “midscale” sample out the SPDIF stream if FIFO underruns.
SPAL	SPDIF ADC Loop Around: 0 = SPDIF transmitter is connected to the AC-LINK stream (reset default). 1 = SPDIF transmitter is connected to the digital ADC stream, not the AC-LINK.
INTS	INTERRUPT MODE SELECT: This bits selects the JS interrupt implementation path. 0 = Bit 0 SLOT 12 (Modem Interrupt) 1 = Slot 6 Valid Bit (MIC ADC Interrupt)
CHEN	Chain Enable: This bit enables chaining of a slave CODEC SDATA_IN stream into the ID0 Pin (45). 0 = Disable Chaining (Reset Default) 1 = Enable Chaining into ID0 Pin

REGM0	Master Codec Register Mask
REGM1	Slave 1 Codec Register Mask
REGM2	Slave 2 Codec Register Mask
SLOT16	Enable 16-Bit Slot Mode. SLOT16 makes all AC link slots 16 bits in length, formatted into 16 slots. This is a preferred mode for DSP serial port interfacing.

Miscellaneous Control Bits (Index 76h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
76h	Misc Control Bits	DACZ	X	MSPLT	X	DAM	X	FMXE	X	X	MADPD	X	MADST	VREFH	VREFD	MBG1	MBG0	0000h

MBG[1:0]	MIC Boost Gain Change Register: These two bits allow changing the MIC preamp gain from the nominal 20 dB gain. Note: This gain setting only takes effect while Bit D6 (M20) on the MIC Volume Register (0Eh) is set to 1. Otherwise the MIC boost block has a gain of 0 dB. 00 = 20 dB Gain (Reset Default) 01 = 10 dB Gain 10 = 30 dB Gain 11 = Reserved
VREFD	V_{REFOUT} Disable: Disables V_{REFOUT} placing it into High Zout mode. Note that this bit overrides the VREFH bit selection (see below). 0 = V_{REFOUT} Pin Is Driven by the Internal Reference (Reset Default) 1 = V_{REFOUT} Pin Is Placed into High Zout Mode
VREFH	V_{REFOUT} High: Changes V_{REFOUT} from 2.25 V to 3.70 V for MIC bias applications. 0 = V_{REFOUT} Pin Is set to 2.25 V Output (Reset Default) 1 = V_{REFOUT} Pin Is set to 3.70 V Output
MADST	Mixer ADC Status Bit: Indicates status of mixer digitizing ADC (L/R channels) 0 = Mixer ADC Not Ready 1 = Mixer ADC Is Ready
MADPD	Mixer ADC Power-Down: Controls power-down for mixer digitizing ADC. 0 = Mixer ADC Is Powered-On (Default) 1 = Mixer ADC Is Powered-Down
FMXE	Front DAC into Mixer Enable: Controls the Front (main) DAC to Mixer mute switches. 0 = Front DAC Outputs Are Allowed to Sum into the Mixer (Reset Default) 1 = Front DAC Outputs Are Muted into the Mixer (Blocked)
DAM	Digital Audio Mode: PCM DAC outputs bypass the analog mixer and are sent directly to the Codec output.
MSPLT	Mute Split: Allows separate mute control bits for master, Headphone, LINE_IN, CD, AUX, and PCM volume control Registers as well as Record Gain Register and mixer ADC volume. 0 = Both Left and Right Channel Mutes Are Controlled by Bit 15 in the Respective Registers (Reset Default) 1 = Bit 15 Affects Only the Left Channel Mute and Bit 7 Affects Only the Right Channel Mute
DACZ	DAC Zero-Fill: (versus repeat) if DAC is starved for data. 0 = When DAC Is Filled with Repeat Data 1 = When DAC Is Filled with Zeros (Reset Default)

Vendor ID Registers (Index 7Ch)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	4144h

S[7:0] This register is ASCII encoded to ‘A’

F[7:0] This register is ASCII encoded to ‘D’

Vendor ID Registers (Index 7Eh)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	5372h

T[7:0] This register is ASCII encoded to 'S'

REV[7:0] Vendor-specific revision number: The AD1981A assigns 71h to this field.

Table II. Codec ID and External Clock Selection

$\overline{ID1}$	$\overline{IDO}$	CODEC ID	CODEC CLOCKING SOURCE
1	1	(00) PRIMARY	24.576 MHz (Local Xtal or External into XTL_IN)
1	0	(01) SECONDARY	12.288 MHz (External into Bit_Clk)
0	1	(00) PRIMARY	48.000 MHz (External into XTL_IN)
0	0	(00) PRIMARY	14.31818 MHz (External into XTL_IN)

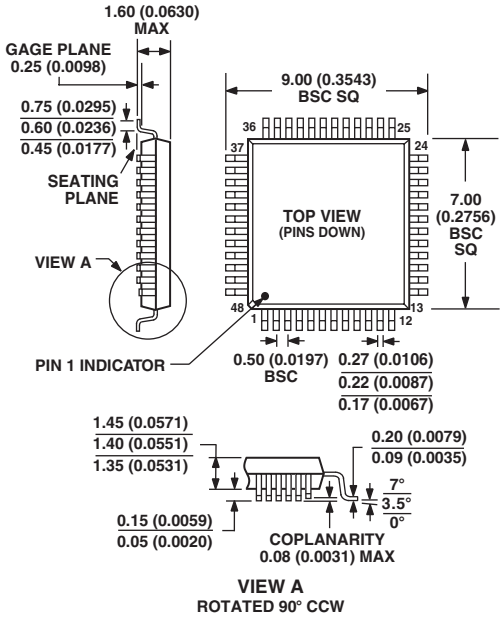
Note that the ID# Pins have weak internal pull-ups and are inverted internally.

OUTLINE DIMENSIONS

Dimensions shown in millimeters and (inches)

48-Lead Thin Plastic Quad (LQFP)

(ST-48)



CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

COMPLIANT TO JEDEC STANDARDS MS-026-BBC

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