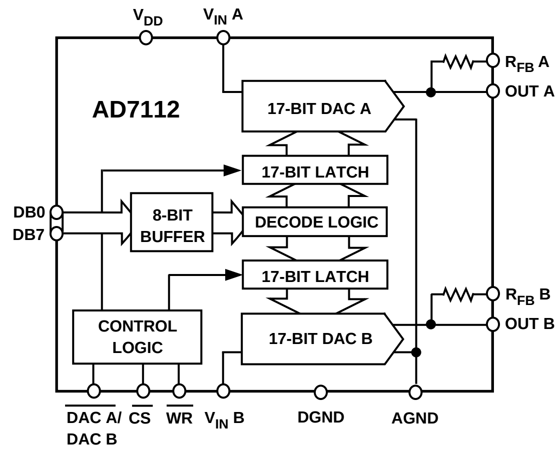
LC²MOS LOGDAC Dual Logarithmic D/A Converter

AD7112*

FEATURES
Dynamic Range: 88.5 dB
Resolution: 0.375 dB
On-Chip Data Latches for Both DACs
Four-Quadrant Multiplication
+5 V Operation
Pin Compatible with AD7528
Low Power

APPLICATIONS
Audio Attenuators
Sonar Systems
Function Generators

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The LOGDAC® AD7112 is a monolithic dual multiplying D/A converter featuring wide dynamic range and excellent DAC-to-DAC matching. Both DACs can attenuate an analog input signal over the range 0 dB to 88.5 dB in 0.375 dB steps. It is available in skinny 0.3" wide 20-pin DIPs and in 20-terminal surface mount packages.

The degree of attenuation in either channel is determined by the 8-bit word applied to the onboard decode logic. This 8-bit word is decoded into a 17-bit word which is then loaded into one of the 17-bit data latches, determined by $\overline{\text{DACA}}$/DACB. The fine step resolution over the entire dynamic range is due to the use of these 17-bit DACs.

The AD7112 is easily interfaced to a standard 8-bit MPU bus via an 8-bit data port and standard microprocessor control lines. It should be noted that the AD7112 is exactly pin-compatible with the AD7528, an industry standard dual 8-bit multiplying DAC. This allows an easy upgrading of existing AD7528 designs which would benefit both from the wider dynamic range and the finer step resolution offered by the AD7112.

The AD7112 is fabricated in Linear Compatible CMOS (LC²MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic.

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PRODUCT HIGHLIGHTS

1. DAC-to-DAC Matching: Since both of the AD7112 DACs are fabricated at the same time on the same chip, precise matching and tracking between the two DACs is inherent.
2. Small Package: The AD7112 is available in a 20-pin DIP and a 20-terminal SOIC package.
3. Fast Microprocessor Interface: The AD7112 has bus interface timing compatible with all modern microprocessors.

REV. 0

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AD7112–SPECIFICATIONS
(V_{DD} = +5 V ± 5%; OUT A = OUT B = AGND = DGND = 0 V; V_{IN} A = V_{IN} B = 10 V. Output amplifier AD712 except where noted. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	C Version[1] T_A = +25°C	C Version[1] T_A = T_{MIN}, T_{MAX}	B Version T_A = +25°C	B Version T_A = T_{MIN}, T_{MAX}	Units	Conditions/Comments
ACCURACY						
Resolution	0.375	0.375	0.375	0.375	dB	
Accuracy Relative to 0 dB Attenuation						Guaranteed Attenuation Ranges for Specified Step Sizes.
0.375 dB Steps:						
Accuracy ≤ ±0.17 dB	0 to 36	0 to 36	0 to 30	0 to 30	dB min	
Monotonic	0 to 54	0 to 54	0 to 48	0 to 48	dB min	
0.75 dB Steps:						
Accuracy ≤ ±0.35 dB	0 to 48	0 to 42	0 to 42	0 to 36	dB min	
Monotonic	0 to 72	0 to 66	0 to 72	0 to 60	dB min	
1.5 dB Steps:						
Accuracy ≤ ±0.7 dB	0 to 54	0 to 48	0 to 48	0 to 42	dB min	
Monotonic	Full Range	0 to 78	0 to 85.5	0 to 72	dB min	Full Range Is 0 dB to 88.5 dB.
3.0 dB Steps:						
Accuracy ≤ ±1.4 dB	0 to 66	0 to 54	0 to 60	0 to 48	dB min	
Monotonic	Full Range	Full Range	Full Range	Full Range	dB min	
6.0 dB Steps:						
Accuracy ≤ ±2.7 dB	0 to 72	0 to 60	0 to 60	0 to 60	dB min	
Monotonic	Full Range	Full Range	Full Range	Full Range	dB min	
Gain Error	±0.1	±0.15	±0.15	±0.2	dB max	Measured Using R_{FB} A, R_{FB} B. Both DAC Registers Loaded With All 0s.
Output Leakage Current OUT A, OUT B	±50	±400	±50	±400	nA max	
Input Resistance, V_{IN} A, V_{IN} B	9/15	9/15	9/15	9/15	kΩ min/max	Typically 12 kΩ.
Input Resistance Match	±1	±1	±2	±2	% max	
Feedback Resistance, R_{FB} A, R_{FB} B	9.3/15.7	9.3/15.7	9.3/15.7	9.3/15.7	kΩ min/max	
LOGIC INPUTS						
$\overline{CS}$, $\overline{WR}$, $\overline{DAC\ A}$/DAC B, DB0–DB7						
Input Low Voltage, V_{INL}	0.8	0.8	0.8	0.8	V max	
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	V min	
Input Leakage Current	±1	±10	±1	±10	μA max	
Input Capacitance[2]	10	10	10	10	pF max	
POWER REQUIREMENTS						
V_{DD}, Range[3]	4.75/5.25	4.75/5.25	4.75/5.25	4.75/5.25	V min/max	For Specified Performance.
	2	2	2	2	mA max	Logic Inputs = V_{IL} or V_{IH}
	2	2	2	2	mA max	Logic Inputs = 0 V or V_{DD}

NOTES
[1]Temperature range as follows: B, C Versions: –40°C to +85°C.
[2]Guaranteed by design, not production tested.
[3]The part will function with V_{DD} = 5 V ± 10% with degraded performance.

Specifications subject to change without notice.

TIMING SPECIFICATIONS[1] (V_{DD} = +5 V ± 5%; OUT A = OUT B = AGND = DGND = 0 V; V_{IN} A = V_{IN} B = 10 V)

Parameter		T_A = +25°C	T_A = –40°C to +85°C	Units	Conditions/Comments
$\overline{CS}$ to $\overline{WR}$ Setup Time	t_{CS}	0	0	ns min	See Figure 3.
$\overline{CS}$ to $\overline{WR}$ Hold Time	t_{CH}	0	0	ns min	
DAC Select to $\overline{WR}$ Setup Time	t_{AS}	4	4	ns min	
DAC Select to $\overline{WR}$ Hold Time	t_{AH}	0	0	ns min	
Data Valid to $\overline{WR}$ Setup Time	t_{DS}	55	55	ns min	
Data Valid to $\overline{WR}$ Hold Time	t_{DH}	10	10	ns min	
$\overline{WR}$ Pulse Width	t_{WR}	53	53	ns min	

NOTES
[1]Timing specifications guaranteed by design not production tested. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

Specifications subject to change without notice.

AC PERFORMANCE CHARACTERISTICS[1] (V_{DD} = +5 V ± 5%; OUT A = OUT B = AGND = DGND = 0 V; V_{IN} A = V_{IN} B = 10 V. Output amplifier AD712 except where noted.)

Parameter	T_A = +25°C	T_A = –40°C to +85°C	Units	Conditions/Comments
DC Supply Rejection Δ Gain/Δ V_{DD}	0.001	0.005	dB/% max	Δ V_{DD} = ± 5%. Input Code = 00000000
Digital-to-Analog Glitch Impulse	10	10	nV s typ	Measured with AD843 as output amplifier for input code transition 10000000 to 00000000.
Output Capacitance, $C_{OUT\ A}$, $C_{OUT\ B}$	50	50	pF max	
AC Feedthrough				
V_{IN} A to OUT A	–94	–90	dB max	V_{IN} A, V_{IN} B = 6 V rms at 1 kHz. DAC Registers loaded with all 1s.
V_{IN} B to OUT B	–94	–90	dB max	
Channel-to-Channel Isolation				
V_{IN} A to OUT B	–87	–87	dB typ	V_{IN} A = 6 V rms at 10 kHz sine wave, V_{IN} B = 0 V. DAC Registers loaded with all 0s.
V_{IN} B to OUT A	–87	–87	dB typ	V_{IN} B = 6 V rms at 10 kHz sine wave, V_{IN} A = 0 V. DAC Registers loaded with all 0s.
Digital Feedthrough	1	1	nV s typ	Measured with input code transitions of all 0s to all 1s.
Output Noise Voltage Density				
(30 Hz to 50 kHz)	15	15	nV/$\sqrt{Hz}$ typ	Measured between R_{FB} A and OUT A or between R_{FB} B and OUT B.
Total Harmonic Distortion	–91	–91	dB typ	V_{IN} A = V_{IN} B = 6 V rms at 1 kHz. DAC Registers loaded with all 0s.

NOTES
[1]Guaranteed by design, not production tested.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND or DGND	–0.3 V, +7 V
AGND to DGND	–0.3 V, V_{DD} + 0.3 V
Digital Inputs to DGND	–0.3 V, V_{DD} + 0.3 V
OUT A, OUT B to AGND	–0.3 V, V_{DD} + 0.3 V
V_{IN} A, V_{IN} B to AGND	±25 V
V_{RFB} A, V_{RFB} B to AGND	±25 V
Operating Temperature Range	
All Versions	–40°C to +85°C
Junction Temperature	+150°C
Storage Temperature	–65°C to +150°C
Power Dissipation, DIP	1 W
θ_{JA}, Thermal Impedance	102°C/W
Lead Temperature (Soldering, 10 secs)	+300°C
Power Dissipation, SOIC	1 W
θ_{JA}, Thermal Impedance	75°C/W
Lead Temperature (Soldering)	
Vapor Phase (60 secs)	215°C
Infrared (15 secs)	220°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7112 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TERMINOLOGY

RESOLUTION: Nominal change in attenuation when moving between two adjacent codes.

MONOTONICITY: The device is monotonic if the analog output decreases or remains constant as the wdigital code increases.

FEEDTHROUGH ERROR: That portion of the input signal which reaches the output when all digital inputs are high.

OUTPUT CAPACITANCE: Capacitance from OUT A or OUT B to ground.

GAIN ERROR: Gain error results from a mismatch between R_{FB} (the feedback resistance) and the R-2R ladder resistance. Its effect in a LOGDAC is to produce a constant additive attenuation error in dB over the whole range of the DAC.

ACCURACY: The difference (measured in dB) between the ideal transfer function as listed in Table I and the actual transfer function as measured with the device.

DIGITAL-TO-ANALOG GLITCH IMPULSE: The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-s or nV-s depending on whether the glitch is measured as a current or voltage signal. Glitch impulse is measured with V_{IN} = AGND.

ORDERING INFORMATION

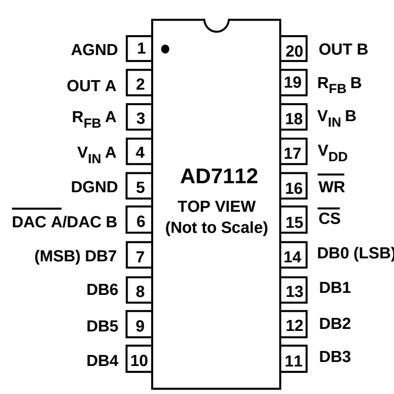
Model	Temperature Range	Specified Accuracy Range	Package Option*
AD7112BN	–40°C to +85°C	0 dB to 60 dB	N-20
AD7112CN	–40°C to +85°C	0 dB to 72 dB	N-20
AD7112BR	–40°C to +85°C	0 dB to 60 dB	R-20
AD7112CR	–40°C to +85°C	0 dB to 72 dB	R-20

*N = Plastic DIP; R = SOIC.

PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	AGND	Analog Ground.
2	OUT A	Current Output Terminal of DAC A.
3	R_{FB} A	Feedback Resistor for DAC A.
4	V_{IN} A	Reference Input to DAC A
5	DGND	Digital Ground.
6	$\overline{\text{DAC A}}$/DAC B	Selects Which DAC Can Accept Data from Input Port.
7–14	DB7–DB0	8 Data Inputs.
15	$\overline{\text{CS}}$	Chip Select Input, Active Low.
16	$\overline{\text{WR}}$	Write Input, Active Low.
17	V_{DD}	Power Supply Input 5 V ± 5%.
18	V_{IN} B	Reference Input to DAC B.
19	R_{FB} B	Feedback Resistor for DAC B.
20	OUT B	Current Output Terminal of DAC B.

PIN CONFIGURATION
DIP/SOIC



CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7112 consists of a dual 17-bit R-2R CMOS multiplying D/A converter with extensive digital logic. Figure 1 shows a simplified circuit of the D/A converter section of the AD7112. The logic translates the 8-bit binary input into a 17-bit word which is used to drive the D/A converter. Figure 2 shows a typical circuit configuration for the AD7112.

The transfer function for the circuit of Figure 2 is given by:

$$V_O = -V_{IN} \times 10\exp -\frac{0.375\,N}{20}$$

or

$$\left|\frac{V_O}{V_{IN}}\right| dB = -0.375\,N$$

where 0.375 is the step size (resolution) in dB and N is the input code in decimal for values 0 to 239. For $240 \le N \le 255$ the output is zero. Table I gives the output attenuation relative to 0 dB for all possible input codes.

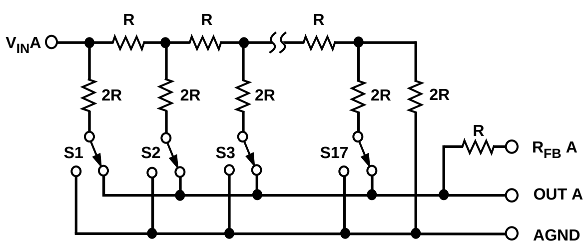
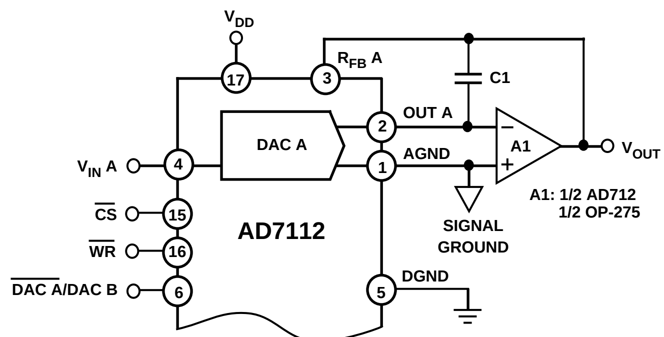


Figure 1. Simplified D/A Circuit of 1/2 AD7112

Figures 16 and 17 give a pictorial representation of the specified accuracy and monotonic ranges for all grades of the AD7112. High attenuation levels are specified with less accuracy than low attenuation levels. The range of monotonic behavior depends upon the attenuation step size used. To achieve monotonic operation over the entire 88.5 dB range, it is necessary to select input codes so that the attenuation step size at any point is consistent with the step size guaranteed for monotonic operation at that point.



NOTES
1. ONLY ONE DAC IS SHOWN FOR CLARITY.
2. DATA INPUT CONNECTIONS ARE OMITTED.
3. C1 PHASE COMPENSATION (5–15pF) MAY BE REQUIRED WHEN USING HIGH SPEED AMPLIFIER.

Figure 2. Typical Circuit Configuration

Table I. Ideal Attenuation in dB vs. Input Code

D7–D4 \ D3–D0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	0.000	0.375	0.750	1.125	1.500	1.875	2.250	2.625	3.000	3.375	3.750	4.125	4.500	4.875	5.250	5.625
0001	6.000	6.375	6.750	7.125	7.500	7.875	8.250	8.625	9.000	9.375	9.750	10.125	10.500	10.875	11.250	11.625
0010	12.000	12.375	12.750	13.125	13.500	13.875	14.250	14.625	15.000	15.375	15.750	16.125	16.500	16.875	17.250	17.625
0011	18.000	18.375	18.750	19.125	19.500	19.875	20.250	20.625	21.000	21.375	21.750	22.125	22.500	22.875	23.250	23.625
0100	24.000	24.375	24.750	25.125	25.500	25.875	26.250	26.625	27.000	27.375	27.750	28.125	28.500	28.875	29.250	29.625
0101	30.000	30.375	30.750	31.125	31.500	31.875	32.250	32.625	33.000	33.375	33.750	34.125	34.500	34.875	35.250	35.625
0110	36.000	36.375	36.750	37.125	37.500	37.875	38.250	38.625	39.000	39.375	39.750	40.125	40.500	40.875	41.250	41.625
0111	42.000	42.375	42.750	43.125	43.500	43.875	44.250	44.625	45.000	45.375	45.750	46.125	46.500	46.875	47.250	47.625
1000	48.000	48.375	48.750	49.125	49.500	49.875	50.250	50.625	51.000	51.375	51.750	52.125	52.500	52.875	53.250	53.625
1001	54.000	54.375	54.750	55.125	55.500	55.875	56.250	56.625	57.000	57.375	57.750	58.125	58.500	58.875	59.250	59.625
1010	60.000	60.375	60.750	61.125	61.500	61.875	62.250	62.625	63.000	63.375	63.750	64.125	64.500	64.875	65.250	65.625
1011	66.000	66.375	66.750	67.125	67.500	67.875	68.250	68.625	69.000	69.375	69.750	70.125	70.500	70.875	71.250	71.625
1100	72.000	72.375	72.750	73.125	73.500	73.875	74.250	74.625	75.000	75.375	75.750	76.125	76.500	76.875	77.250	77.625
1101	78.000	78.375	78.750	79.125	79.500	79.875	80.250	80.625	81.000	81.375	81.750	82.125	82.500	82.875	83.250	83.625
1110	84.000	84.375	84.750	85.125	85.500	85.875	86.250	86.625	87.000	87.375	87.750	88.125	88.500	88.875	89.250	89.625
1111	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE

INTERFACE LOGIC INFORMATION

DAC Selection

Both DAC latches share a common 8-bit port. The control input $\overline{\text{DAC A}}$/DAC B selects which DAC can accept data from the input port.

Mode Selection

Inputs $\overline{\text{CS}}$ and $\overline{\text{WR}}$ control the operating mode of the selected DAC. See the Mode Selection Table below.

Write Mode

When $\overline{\text{CS}}$ and $\overline{\text{WR}}$ are both low the DAC is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to activity on DB0–DB7.

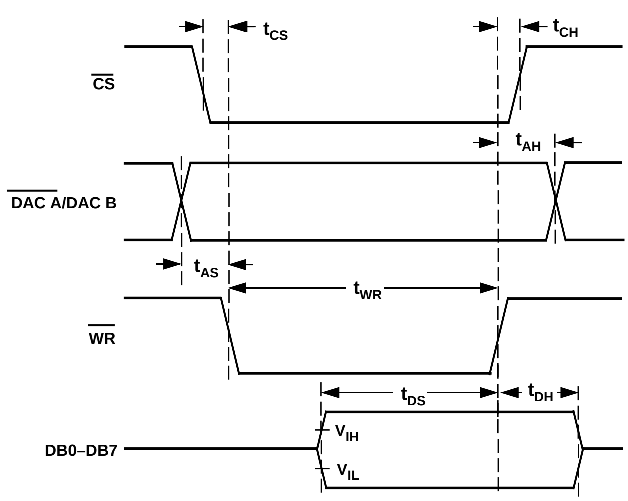
Hold Mode

The selected DAC latch retains the data which was present on DB0–DB7 just prior to $\overline{\text{CS}}$ and $\overline{\text{WR}}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches.

Mode Selection Table

$\overline{\text{DACA}}$/ DAC B	$\overline{\text{CS}}$	$\overline{\text{WR}}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low State, V_{IL}; H = High State, V_{IH}; X = Don't Care.



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF V_{DD}. $t_R = t_F = 20$ns.
2. CONTROL TIMING MEASUREMENT REFERENCE LEVEL = $(V_{IH} + V_{IL}) / 2$

Figure 3. Write Cycle Timing Diagram

DYNAMIC PERFORMANCE

The dynamic performance of the AD7112 will depend on the gain and phase characteristics of the output amplifier, together with the optimum choice of PC board layout and decoupling components. Circuit layout is most important if the optimum performance of the AD7112 is to be achieved. Most application problems stem from either poor layout, grounding errors, or inappropriate choice of amplifier. Ensure that the layout of the printed circuit board has the digital and analog lines separated as much as possible. Take care not to run any digital track alongside an analog signal track. Establish a single point analog ground (star ground) separate from the logic system ground. Place this ground as close as possible to the AD7112. Connect all analog grounds to this star ground, and also connect the AD7112 DGND to this ground. Do not connect any other digital grounds to this analog ground point. Low impedance analog and digital power supply common returns are essential for low noise and high performance of these converters, therefore the foil width of these tracks should be as wide as possible. The use of ground planes is recommended as this minimizes impedance paths and also guards the analog circuitry from digital noise.

It is recommended that when using the AD7112 with a high speed amplifier, a capacitor (C1) be connected in the feedback path as shown in Figure 2. This capacitor which should be between 5 pF and 15 pF, compensates for the phase lag introduced by the output capacitance of the D/A converter. Figures 4 and 5 show the performance of the AD7112 using the AD712, a high speed, low cost BiFET amplifier, and the OP275, a dual bipolar/JFET amplifier suitable for audio applications. The performance with and without the compensation capacitor is shown in both cases. For operation beyond 250 kHz, capacitor C1 may be reduced in value. This gives an increase in bandwidth at the expense of a poorer transient response as shown in Figure 7. In circuits where C1 is not included, the high frequency roll-off point is primarily determined by the characteristics of the output amplifier and not the AD7112.

Feedthrough and accuracy are sensitive to output leakage currents effects. For this reason it is recommended that the operating temperature of the AD7112 be kept as close to +25°C as is practically possible, particularly where the devices performance at high attenuation levels is important. A typical plot of leakage current vs. temperature is shown in Figure 11.

Some solder fluxes and cleaning materials can form slightly conductive films which cause leakage effects between analog input and output. The user is cautioned to ensure that the manufacturing process for circuits using the AD7112 does not allow such films to form. Otherwise the feedthrough, accuracy and maximum usable range will be affected.

STATIC ACCURACY PERFORMANCE

The D/A converter section of the AD7112 consists of a 17-bit R–2R type converter. To obtain optimum static performance at this level of resolution it is necessary to pay great attention to amplifier selection, circuit grounding, etc.

Amplifier input bias current results in a dc offset at the output of the amplifier due to current flowing in the feedback resistor R_{FB}. It is recommended that amplifiers with input bias currents of less than 10 nA be used (e.g., AD712) to minimize this offset.

Another error arises from the output amplifier's input offset voltage. The amplifier is operated with a fixed feedback resistance, but the equivalent source impedance (the AD7112 output impedance) varies as a function of the attenuation level. This has the effect of varying the noise gain of the amplifier thus creating a varying error due to amplifier offset voltage. It is recommended that an amplifier with less than 50 μV of input offset be used (such as the AD712 or ADOP07) in dc applications. Amplifiers with a large input offset voltage may cause audible thumps in audio applications due to dc output changes. The AD7112 accuracy is specified and tested using only the internal feedback resistor. Any gain error (i.e., mismatch of R_{FB} to the R–2R ladder) that may exist in the AD7112 D/A converter circuit results in a constant attenuation error over the whole range. The AD7112 accuracy is specified relative to 0 dB attenuation, hence gain trim resistors can be used to adjust $V_{OUT} = V_{IN}$ precisely (i.e., 0 dB attenuation) with input code 00000000. For further information on gain error refer to the "CMOS DAC Application Guide" which is available from Analog Devices, Publication Number G872b-8-1/89.

TYPICAL PERFORMANCE CHARACTERISTICS

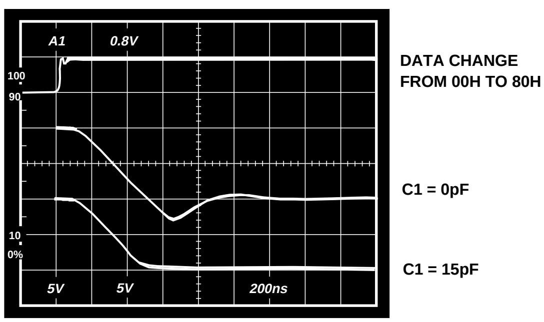


Figure 4. Response of AD7112 with AD712

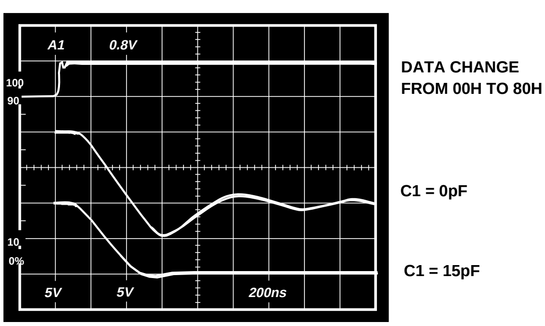


Figure 5. Response of AD7112 with OP275

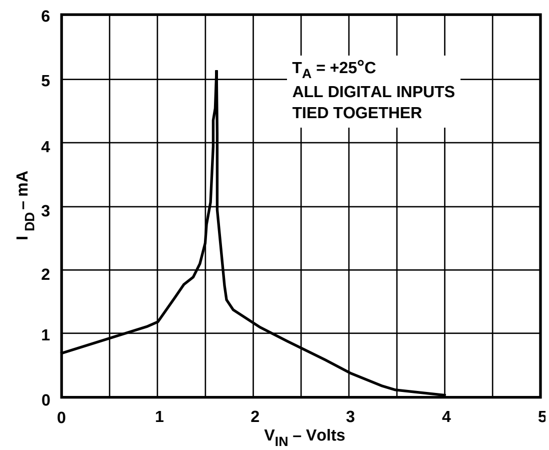


Figure 6. Supply Current vs. Logic Input Level

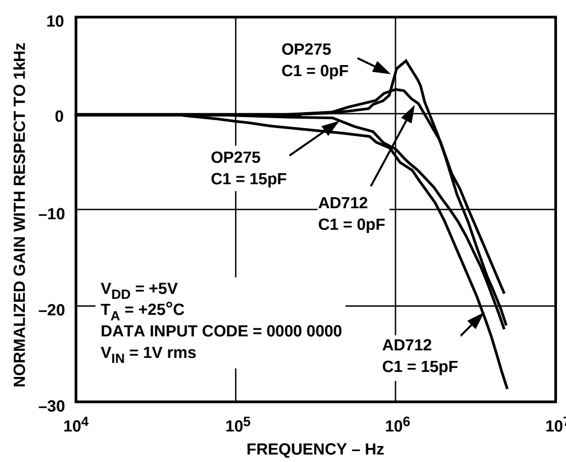


Figure 7. Frequency Response with AD712 and OP275

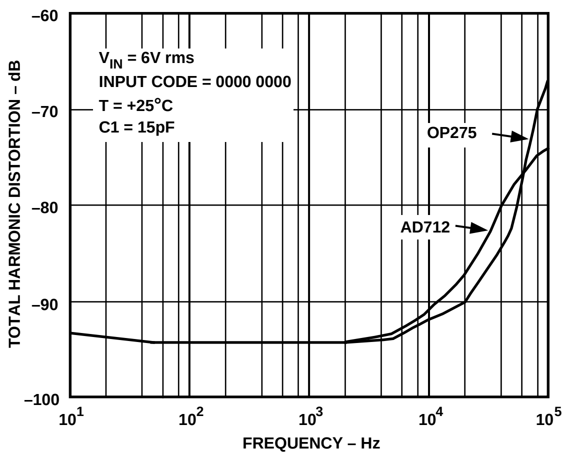


Figure 8. Distortion vs. Frequency

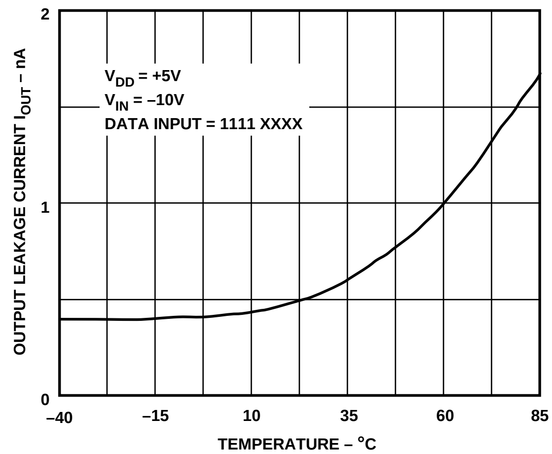


Figure 11. Output Leakage Current vs. Temperature

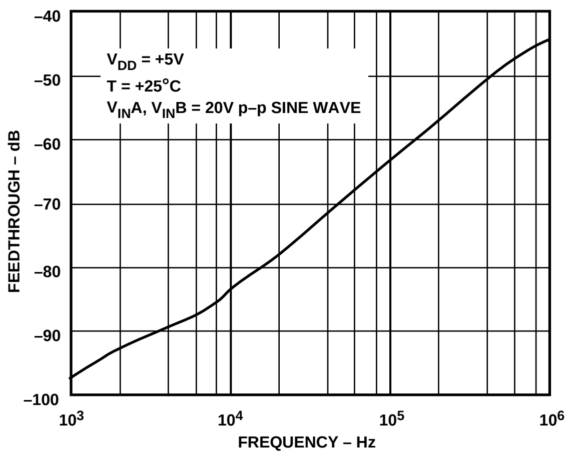


Figure 9. Feedthrough vs. Frequency

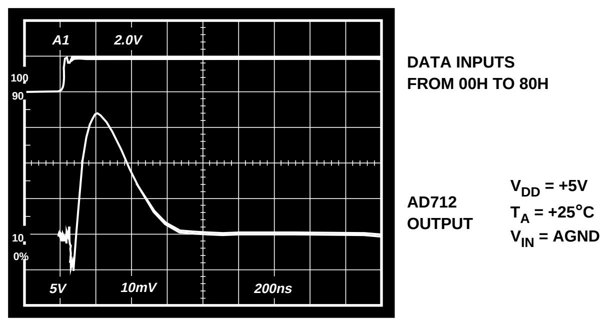


Figure 12. Digital-to-Analog Glitch Impulse

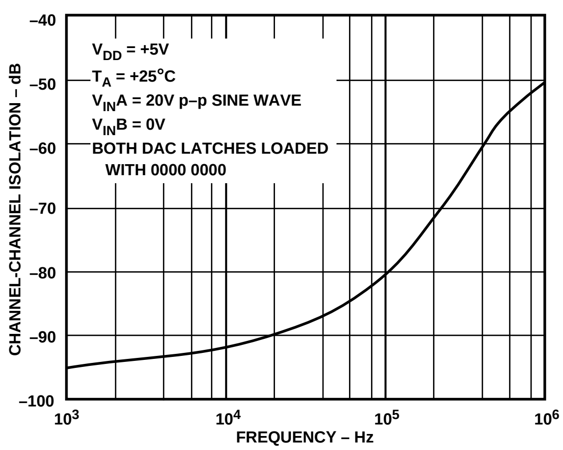


Figure 10. Channel-to-Channel Isolation vs. Frequency

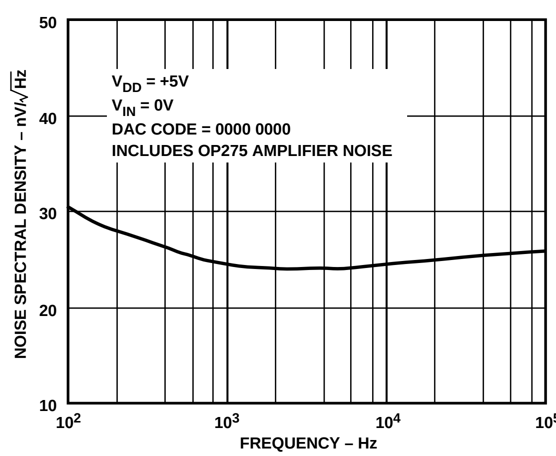


Figure 13. Noise Spectral Density vs. Frequency

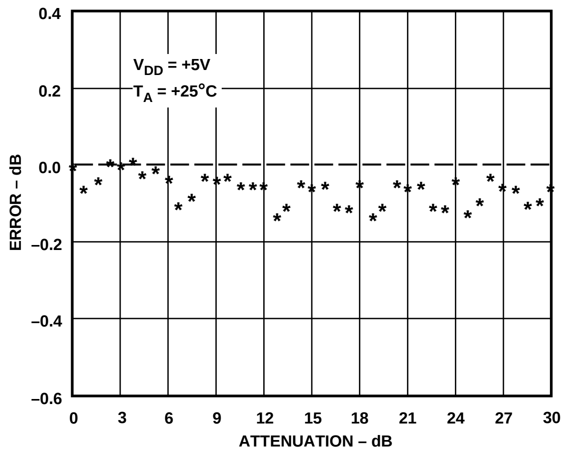


Figure 14. Typical Attenuation Error for 0.75 dB Steps

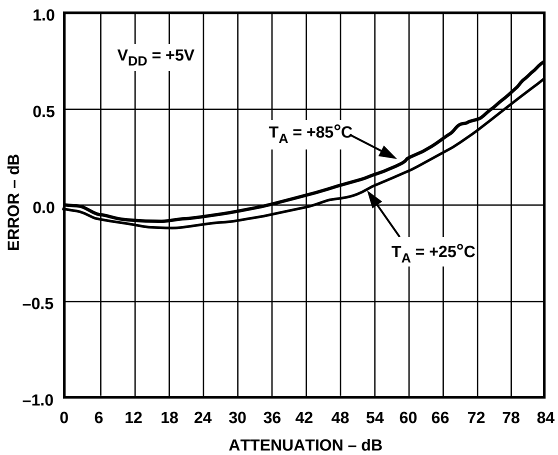


Figure 15. Typical Attenuation Error for 3 dB Steps vs. Temperature

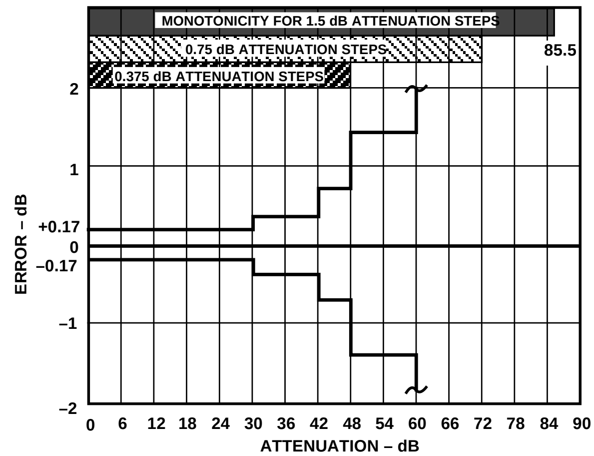


Figure 16. Accuracy Specification for B Grade Devices at T_A = +25°C

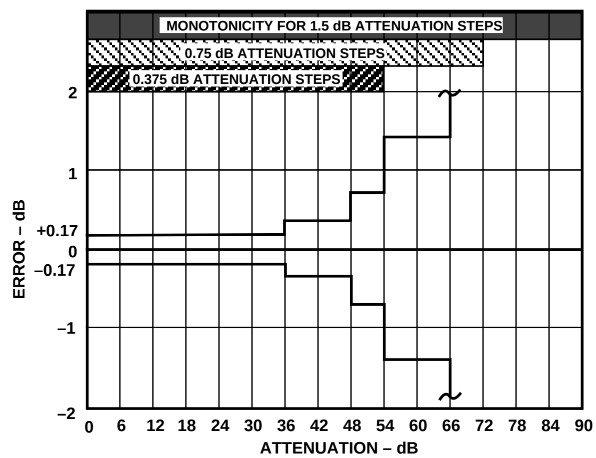


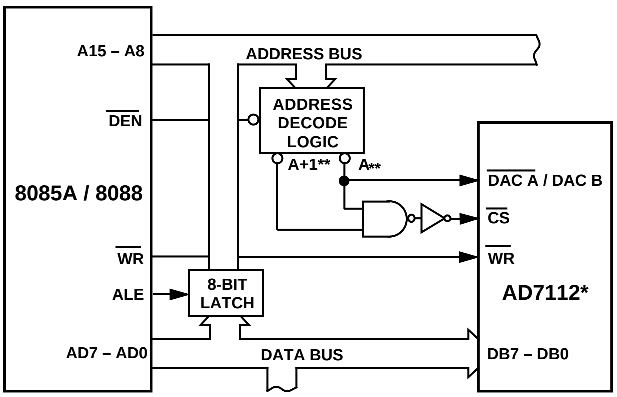
Figure 17. Accuracy Specification for C Grade Devices at T_A = +25°C

MICROPROCESSOR INTERFACING

Figures 18 to 20 show interfaces between the AD7112 and three popular 8-bit microprocessor systems, the MC68008, 8085A/8088 and the 8051. In the MC68008 and 8085/8088 interfaces, the AD7112 is memory mapped with separate addresses for each DAC.

AD7112-8085A/8088 INTERFACE

Figure 18 shows a connection diagram for interfacing the AD7112 to both the 8085A and the 8088 microprocessors. This scheme is also suited to the Z80 microprocessor, but the Z80 address/data bus does not have to be demultiplexed. The AD7112 is memory mapped with separate memory addresses for DAC A and DAC B.

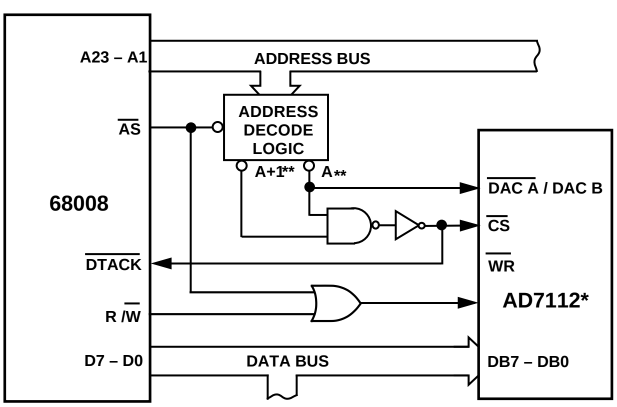


* ANALOG CIRCUITRY HAS BEEN OMITTED FOR CLARITY.
** A = DECODED ADDRESS FOR AD7112 DAC A
A+1 = DECODED ADDRESS FOR AD7112 DAC B

Figure 18. AD7112–8085A/8088 Interface Circuit

AD7112–68008 INTERFACE

Figure 19 shows a connection diagram for interfacing the AD7112 to the 68008 microprocessor. The AD7112 is again memory mapped with separate memory addresses for DAC A and DAC B.



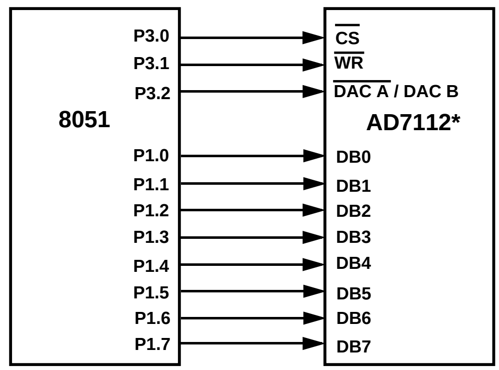
* ANALOG CIRCUITRY HAS BEEN OMITTED FOR CLARITY.
** A = DECODED ADDRESS FOR AD7112 DAC A
A+1 = DECODED ADDRESS FOR AD7112 DAC B

Figure 19. AD7112–68008 Interface Circuit

AD7112–8051 INTERFACE

Figure 20 shows a connection diagram between the AD7112 and the 8051 microprocessor. The AD7112 is port mapped in this interface. The loading structure is as follows: Data to be loaded to the DAC is output to Port 1: P3.0, P3.1 and P3.2 are bit addressable port lines and are used to control the DAC select, $\overline{CS}$ and $\overline{WR}$ inputs. A sample routine for writing to DAC A is shown below.

MOV A,DATA;	Data to be written is loaded to the accumulator.
CLR 3.2;	Select DAC A.
CLR 3.0;	Bring $\overline{CS}$ low.
CLR 3.1;	Bring $\overline{WR}$ low.
MOV A,P1;	Write data to DAC.
SET B 3.1;	Deactivate $\overline{WR}$.
SET B 3.0;	Deactivate $\overline{CS}$



* ANALOG CIRCUITRY OMITTED FOR CLARITY

Figure 20. AD7112–8051 Interface Circuit

APPLICATIONS

Automatic Gain Control

In an automatic gain control system an input signal is attenuated or amplified so that its average output level remains constant. The AD7112 D/A converter is used here as a variable gain or attenuation element that adjusts the output signal relative to the input level.

A feedback loop consisting of a detector, comparator, and up/down counter continuously adjusts the contents of the counter and hence the gain or attenuation of the circuit so that the signal level at the output remains constant and equal to the reference input signal. The negative feedback action of the loop ensures that the average output voltage of the automatic gain control system remains constant. Figure 21 shows a block diagram of a typical AGC control loop using 1/2 AD7112 as the gain/ attenuation element.

Whenever the input signal is outside the dynamic range of the programmable gain element in the AGC loop, there should be a stable, well defined input output relationship.

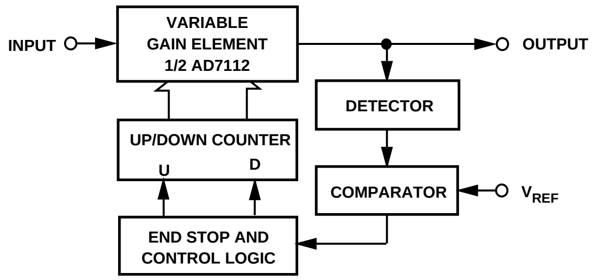


Figure 21. Automatic Gain Control System

Programmable State Variable Filter

The AD7112 with its multiplying capability and fast settling time is ideal for many types of signal conditioning applications. The circuit of Figure 22 shows its use in a state variable filter design. This type of filter has three outputs: low pass, bandpass and high pass. The particular version shown in Figure 22 uses two AD7112 to control the critical parameters f_0, Q and A_0. Instead of several fixed resistors, the circuit uses the DAC equivalent resistances as circuit elements. Thus, R1 in Figure 22 is controlled by the 8-bit word loaded to DAC A1 of the AD7112. This is also the case with R2, R3 and R4.

DAC Equivalent Resistance,

$$R_{EQ} = \frac{R_{DAC}}{10 \times EXP\,(-0.375 \times N/20)}$$

where:

R_{DAC} is the DAC ladder resistance.

N is the DAC code in Decimal ($0 \leq N \leq 240$).

DACs A1 and B1 control the gain and Q of the filter characteristic while DACs A2 and B2 control the cutoff frequency.

Circuit equations:

C1 = C2, R3 = R4, R7 = R8.

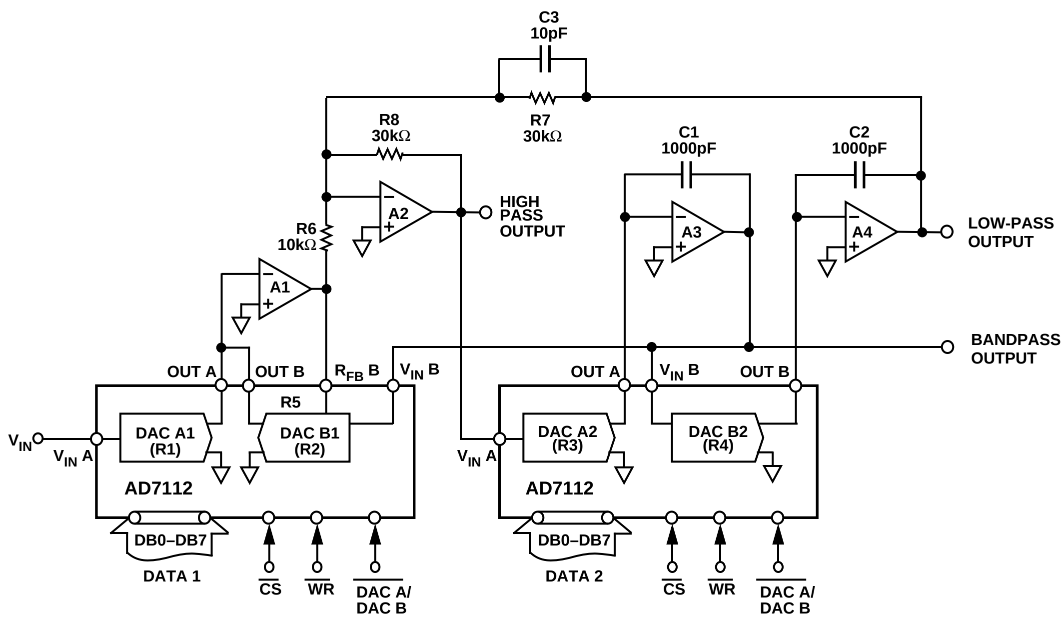
Resonant frequency, $f_0 = 1/(2\,\pi\, R3C1)$.

Quality factor, $Q = (R6/R8) \times (R2/R_{FBB1})$.

R_{FBB1} is the feedback resistance of DAC B1 in Figure 22

Bandpass Gain, $A_0 = -R2/R1$.

Programmable range for component values shown is f_0 = 0 kHz to 15 kHz and Q = 0.3 to 4.5.



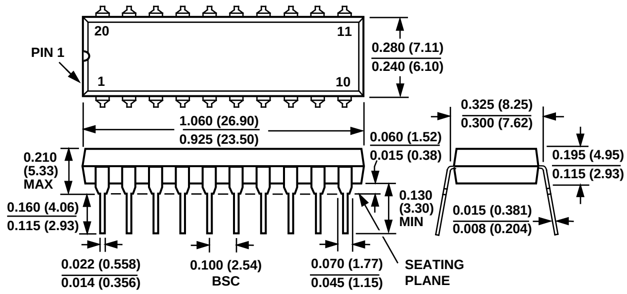
NOTES
1. A1, A2, A3, A4 : 1/4 x AD713
2. C3 IS A COMPENSATION CAPACITOR TO ELIMINATE Q AND GAIN VARIATIONS CAUSED BY AMPLIFIER GAIN BANDWIDTH LIMITATIONS

Figure 22. Programmable State Variable Filter

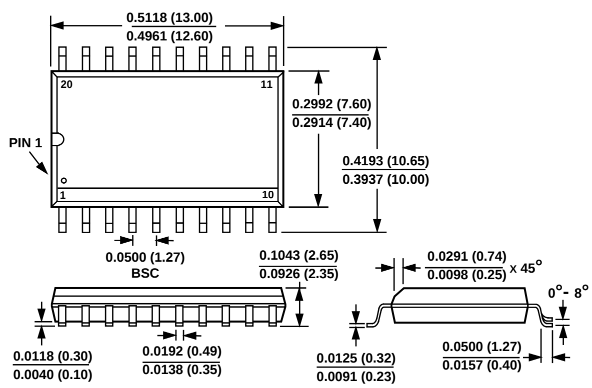
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

20-Pin Plastic DIP (N-20)



20-Pin SOIC (R-20)



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