High Frequency Divider/PLL Synthesizer

ADF4007

FEATURES

7.5 GHz bandwidth
Maximum PFD frequency of 120 MHz
Divide ratios of 8, 16, 32, or 64
2.7 V to 3.3 V power supply
Separate charge pump supply (V_P) allows extended tuning voltage in 3 V systems
R_{SET} contol of charge pump current
Hardware power-down mode

APPLICATIONS

Satellite communications
Broadband wireless access
CATV
Instrumentation
Wireless LANs

GENERAL DESCRIPTION

The ADF4007 is a high frequency divider/PLL synthesizer that can be used in a variety of communications applications. It can operate to 7.5 GHz on the RF side and to 120 MHz at the PFD. It consists of a low noise digital PFD (phase frequency detector), a precision charge pump, and a divider/prescaler. The divider/ prescaler value can be set by two external control pins to one of four values (8, 16, 32, or 64). The reference divider is permanently set to 2, allowing an external REF_{IN} frequency of up to 240 MHz.

A complete PLL (phase-locked loop) can be implemented if the synthesizer is used with an external loop filter and a VCO (voltage controlled oscillator). Its very high bandwidth means that frequency doublers can be eliminated in many high frequency systems, simplifying system architecture and reducing cost.

FUNCTIONAL BLOCK DIAGRAM

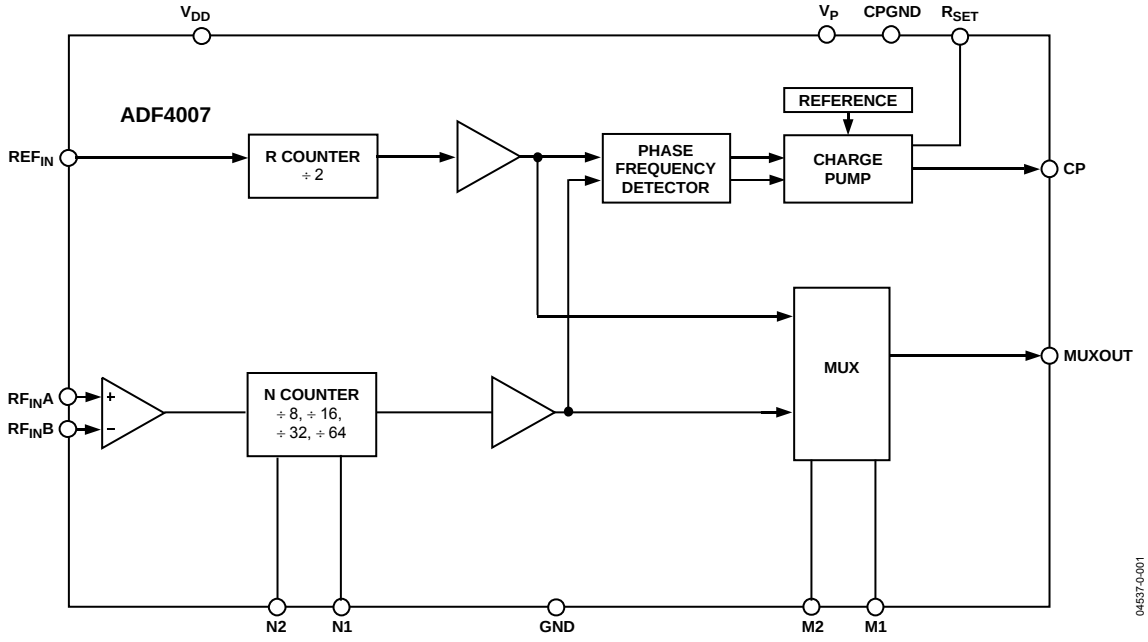

Figure 1.

Rev. 0

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TABLE OF CONTENTS

REVISION HISTORY

Revision 0: Initial Version

SPECIFICATIONS

$AV_{DD} = DV_{DD} = 3\ V \pm 10\%$, $AV_{DD} \le V_P \le 5.5\ V$, AGND = DGND = CPGND = 0 V, $R_{SET} = 5.1\ k\Omega$, dBm referred to 50 Ω, $T_A = T_{MAX}$ to T_{MIN}, unless otherwise noted.

Table 1.

Parameter	B Version[1]	Unit	Test Conditions/Comments
RF CHARACTERISTICS			
RF Input Frequency (RF_{IN})	1.0/7.0	GHz min/max	RF input level: +5 dBm to −10 dBm
RF Input Frequency	0.5/7.5	GHz min/max	RF input level: +5 dBm to −5 dBm
			For lower frequencies, ensure that slew rate (SR) > 560 V/µs
REF_{IN} CHARACTERISTICS			
REF_{IN} Input Sensitivity	0.8/V_{DD}	V p-p min/max	Biased at $AV_{DD}/2$[2]
REF_{IN} Input Frequency	20/240	MHz min/max	For f < 20 MHz, use square wave (slew rate > 50 V/µs)
REF_{IN} Input Capacitance	10	pF max	
REF_{IN} Input Current	±100	µA max	
PHASE DETECTOR			
Phase Detector Frequency[3]	120	MHz max	
MUXOUT			
MUXOUT Frequency[3]	200	MHz max	$C_L = 15$ pF
CHARGE PUMP			
I_{CP} Sink/Source	5.0	mA typ	With $R_{SET} = 5.1\ k\Omega$
Absolute Accuracy	2.5	% typ	With $R_{SET} = 5.1\ k\Omega$
R_{SET} Range	3.0/11	kΩ typ	
I_{CP} Three-State Leakage	10	nA max	$T_A = 85°C$
Sink and Source Current Matching	2	% typ	$0.5\ V \le V_{CP} \le V_P - 0.5\ V$
I_{CP} vs. V_{CP}	1.5	% typ	$0.5\ V \le V_{CP} \le V_P - 0.5\ V$
I_{CP} vs. Temperature	2	% typ	$VCP = V_P/2$
LOGIC INPUTS			
V_{IH}, Input High Voltage	1.4	V min	
V_{IL}, Input Low Voltage	0.6	V max	
I_{INH}, I_{INL}, Input Current	±1	µA max	$T_A = 25°C$
C_{IN}, Input Capacitance	10	pF max	
LOGIC OUTPUTS			
V_{OH}, Output High Voltage	$V_{DD} - 0.4$	V min	$I_{OH} = 100\ \mu A$
V_{OL}, Output Low Voltage	0.4	V max	$I_{OL} = 500\ \mu A$
POWER SUPPLIES			
AV_{DD}	2.7/3.3	V min/max	
DV_{DD}	AV_{DD}		
V_P	AV_{DD}/5.5	V min/max	$AV_{DD} \le V_P \le 5.5\ V$
I_{DD}[4] ($AI_{DD} + DI_{DD}$)	17	mA max	15 mA typ
I_P	2.0	mA max	$T_A = 25°C$
NOISE CHARACTERISTICS			
Normalized Phase Noise Floor[5]	−219	dBc/Hz typ	

[1] Operating temperature range (B version) is −40°C to +85°C.
[2] AC coupling ensures $AV_{DD}/2$ bias. See Figure 13 for typical circuit.
[3] Guaranteed by design. Characterized to ensure compliance.
[4] $T_A = 25°C$; $AV_{DD} = DV_{DD} = 3\ V$; N = 64; $RF_{IN} = 7.5\ GHz$.
[5] The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO, PN_{TOT}, and subtracting 20logN (where N is the N divider value) and 10logF_{PFD}. $PN_{SYNTH} = PN_{TOT} - 10\log F_{PFD} - 20\log N$. The in-band phase noise (PN_{TOT}) is measured using the HP8562E Spectrum Analyzer from Agilent.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
AV_{DD} to GND[1]	−0.3 V to +3.6 V
AV_{DD} to DV_{DD}	−0.3 V to +0.3 V
V_P to GND	−0.3 V to +5.8 V
V_P to AV_{DD}	−0.3 V to +5.8 V
Digital I/O Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to GND	−0.3 V to V_P + 0.3 V
REF_{IN}, $RF_{IN}A$, $RF_{IN}B$ to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
CSP θ_{JA} Thermal Impedance	122°C/W
Lead Temperature, Soldering	
Vapor Phase (60 s)	215°C
Infrared (15 s)	220°C
Transistor Count	
CMOS	6425
Bipolar	303

[1] GND = AGND = DGND = 0 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance RF integrated circuit with an ESD rating of <2 kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

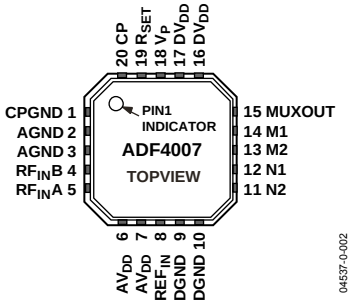


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	CPGND	Charge Pump Ground. The ground return path of the charge pump.
2, 3	AGND	Analog Ground. The ground return path of the prescaler.
4	$RF_{IN}B$	Complementary Input to the RF Prescaler. This point must be decoupled to the ground plane with a small bypass capacitor, typically 100 pF.
5	$RF_{IN}A$	Input to the RF Prescaler. This small signal input is ac-coupled to the external VCO.
6, 7	AV_{DD}	Analog Power Supply. This pin can range from 2.7 V to 3.3 V. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin. AV_{DD} must be the same value as DV_{DD}.
8	REF_{IN}	Reference Input. A CMOS input with a nominal threshold of $V_{DD}/2$ and a dc equivalent input resistance of 100 kΩ. This input can be driven from a TTL or CMOS crystal oscillator, or it can be ac-coupled.
9, 10	DGND	Digital Ground.
11, 12	N2, N1	These two bits set the N value. See Table 4.
13, 14	M2, M1	These two bits set the status of MUXOUT and PFD polarity. See Table 5.
15	MUXOUT	This multiplexer output allows either the N divider output or the R divider output to be accessed externally.
16, 17	DV_{DD}	Digital Power Supply. This pin can range from 2.7 V to 3.3 V. Decoupling capacitors to the digital ground plane should be placed as close as possible to this pin. DV_{DD} must be the same value as AV_{DD}.
18	V_P	Charge Pump Power Supply. This pin should be greater than or equal to V_{DD}. In systems where V_{DD} is 3 V, it can be set to 5 V and used to drive a VCO with a tuning range of up to 5 V.
19	R_{SET}	Connecting a resistor between this pin and CPGND sets the maximum charge pump output current. The nominal voltage potential at the R_{SET} pin is 0.66 V. The relationship between I_{CP} and R_{SET} is $$I_{CPMAX} = \frac{25.5}{R_{SET}}$$ Therefore, if R_{SET} = 5.1 kΩ, then I_{CP} = 5 mA.
20	CP	Charge Pump Output. When enabled, this pin provides $\pm I_{CP}$ to the external loop filter, which in turn drives the external VCO.

Table 4. N Truth Table

N2	N1	N Value
0	0	8
0	1	16
1	0	32
1	1	64

Table 5. M Truth Table

M2	M1	Operation	
0	0	CP:	Active
		MUXOUT:	V_{DD}
		PFD polarity:	+ve
0	1	CP:	Three-state
		MUXOUT:	R divider output
		PFD polarity:	+ve
1	0	CP:	Active
		MUXOUT:	N divider output
		PFD polarity:	+ve
1	1	CP:	Active
		MUXOUT:	GND
		PFD polarity:	−ve

TYPICAL PERFORMANCE CHARACTERISTICS

Table 6. S-Parameter Data for the RF Input

Frequency[1]	MagS11	AngS11
0.60000	0.87693	−19.9279
0.70000	0.85834	−23.5610
0.80000	0.85044	−26.9578
0.90000	0.83494	−30.8201
1.00000	0.81718	−34.9499
1.10000	0.80229	−39.0436
1.20000	0.78917	−42.3623
1.30000	0.77598	−46.3220
1.40000	0.75578	−50.3484
1.50000	0.74437	−54.3545
1.60000	0.73821	−57.3785
1.70000	0.72530	−60.6950
1.80000	0.71365	−63.9152
1.90000	0.70699	−66.4365
2.00000	0.70380	−68.4453
2.10000	0.69284	−70.7986
2.20000	0.67717	−73.7038
2.30000	0.67107	−75.8206
2.40000	0.66556	−77.6851
2.50000	0.65640	−80.3101
2.60000	0.63330	−82.5082
2.70000	0.61406	−85.5623
2.80000	0.59770	−87.3513
2.90000	0.56550	−89.7605
3.00000	0.54280	−93.0239
3.10000	0.51733	−95.9754
3.20000	0.49909	−99.1291
3.30000	0.47309	−102.208
3.40000	0.45694	−106.794
3.50000	0.44698	−111.659
3.60000	0.43589	−117.986
3.70000	0.42472	−125.620
3.80000	0.41175	−133.291
3.90000	0.41055	−140.585
4.00000	0.40983	−147.970
4.10000	0.40182	−155.978
4.20000	0.41036	−162.939
4.30000	0.41731	−168.232
4.40000	0.43126	−174.663
4.50000	0.42959	−179.797
4.60000	0.42687	174.379
4.70000	0.43450	171.537
4.80000	0.42275	167.201
4.90000	0.40662	163.534
5.00000	0.39103	159.829
5.10000	0.37761	157.633
5.20000	0.34263	152.815
5.30000	0.30124	147.632
5.40000	0.27073	144.304
5.50000	0.23590	138.324
5.60000	0.17550	131.087
5.70000	0.12739	124.568
5.80000	0.09058	119.823
5.90000	0.06824	114.960
6.00000	0.04465	84.4391
6.10000	0.04376	34.2210
6.20000	0.06621	4.70571
6.30000	0.08498	−12.6228
6.40000	0.10862	−26.6069
6.50000	0.12161	−38.5860
6.60000	0.12917	−47.1990
6.70000	0.12716	−55.8515
6.80000	0.11678	−63.0234
6.90000	0.10533	−66.9967
7.00000	0.09643	−75.4961
7.10000	0.08919	−89.2055
7.20000	0.08774	−103.786
7.30000	0.09289	−127.153
7.40000	0.10803	−150.582
7.50000	0.13956	−170.971

[1]Frequency unit: GHz; parameter type: s; data format: MA; keyword: R; impedance: 50.

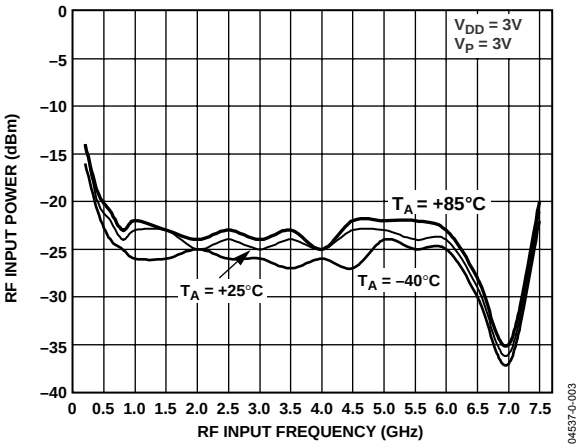


Figure 3. Input Sensitivity

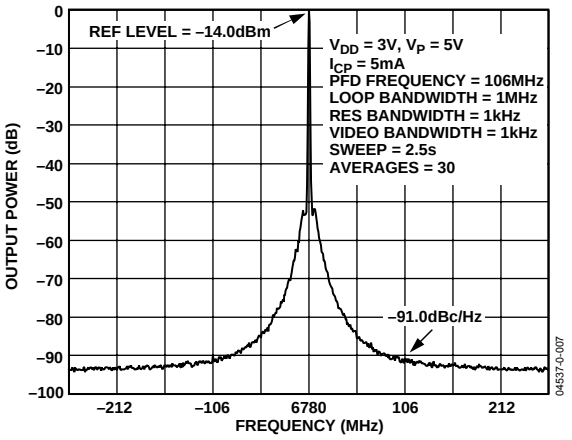


Figure 6. Reference Spurs (6.78 GHz RF_{OUT}, 106 MHz PFD, and 1 MHz Loop Bandwidth)

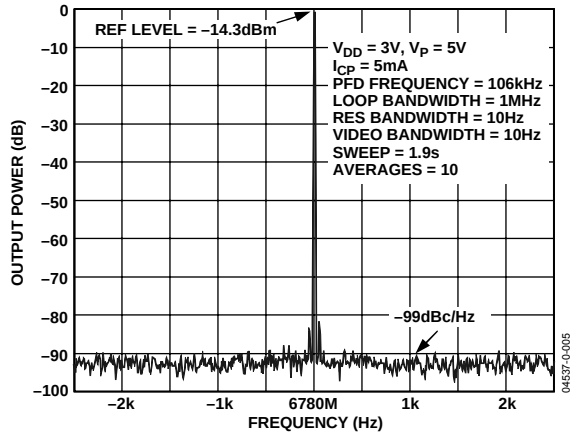


Figure 4. Phase Noise (6.78 GHz RF_{OUT}, 106 MHz PFD, and 1 MHz Loop Bandwidth)

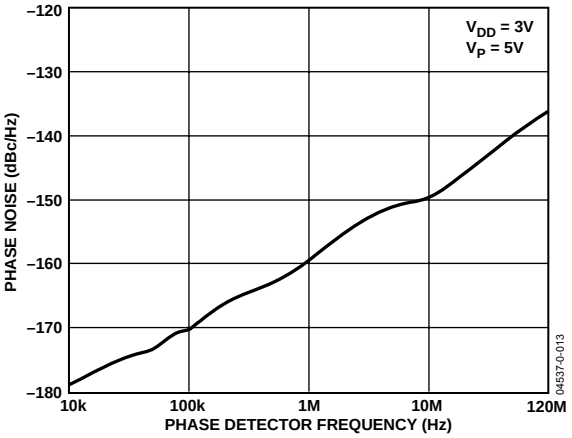


Figure 7. Phase Noise (Referred to CP Output) vs. PFD Frequency

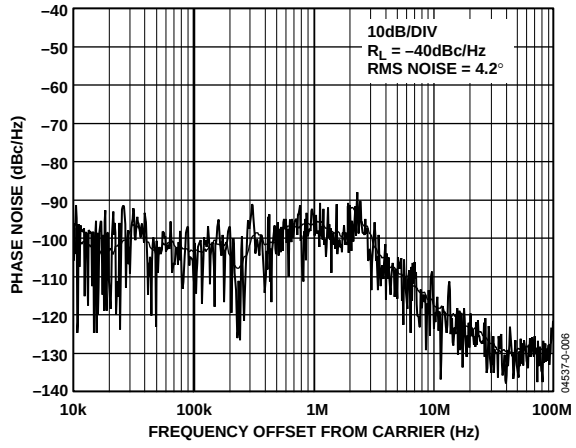


Figure 5. Integrated Phase Noise (6.78 GHz RF_{OUT}, 106 MHz PFD, and 1 MHz Loop Bandwidth)

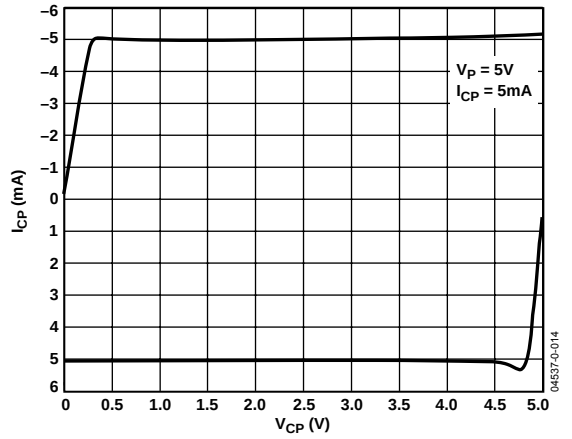


Figure 8. Charge Pump Output Characteristics

THEORY OF OPERATION

REFERENCE INPUT SECTION

The reference input stage is shown in Figure 9. SW1 and SW2 are normally closed switches. SW3 is normally open. When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REF_{IN} pin on power-down.

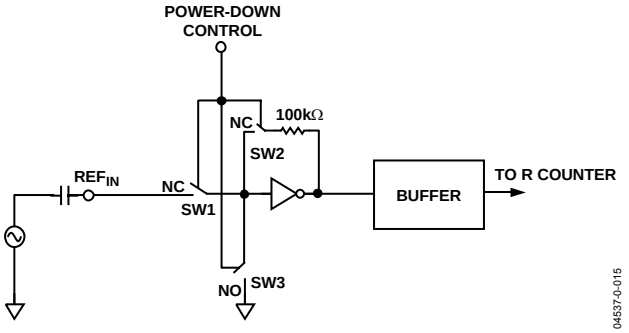


Figure 9. Reference Input Stage

RF INPUT STAGE

The RF input stage is shown in Figure 10 . It is followed by a 2-stage limiting amplifier to generate the CML clock levels needed for the prescaler.

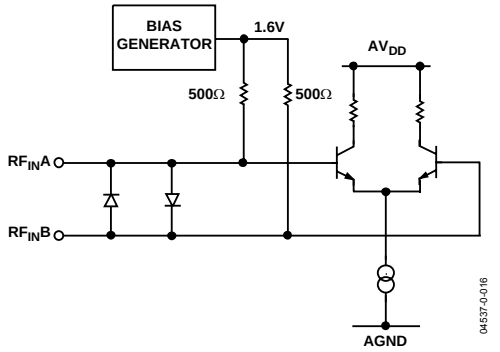


Figure 10. RF Input Stage

PRESCALER P

The prescaler, operating at CML levels, takes the clock from the RF input stage and divides it down to a manageable frequency for the PFD. The prescaler can be selected to be either 8, 16, 32, or 64, and is effectively the N value in the PLL synthesizer. The terms N and P are used interchangeably in this data sheet. N1 and N2 set the prescaler values. The prescaler value should be chosen so that the prescaler output frequency is always less than or equal to 120 MHz, the maximum specified PFD frequency. Thus, with an RF frequency of 4 GHz, a prescaler value of 64 is valid, but a value of 32 or less is not valid.

$$f_{VCO} = [N] \times \frac{f_{REFIN}}{2}$$

R COUNTER

The R counter is permanently set to 2. It allows the input reference frequency to be divided down by 2 to produce the reference clock to the phase frequency detector (PFD).

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R counter and the N counter (prescaler, P) and produces an output proportional to the phase and frequency difference between them. Figure 11 is a simplified schematic. The PFD includes a fixed, 3 ns delay element that controls the width of the antibacklash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and minimizes phase noise and reference spurs.

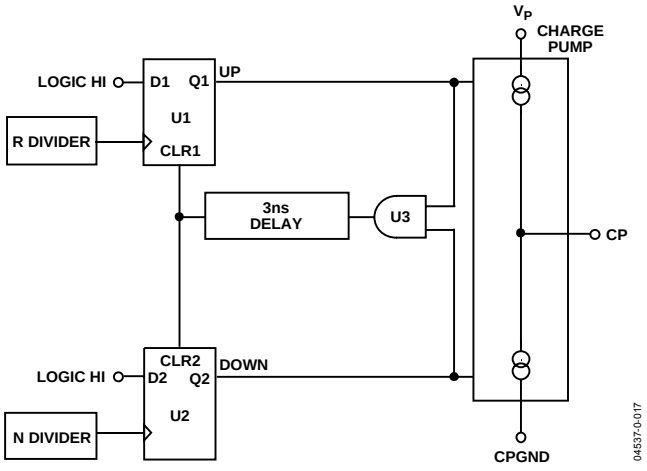


Figure 11. PFD Simplified Schematic and Timing (In Lock)

MUXOUT

The output multiplexer on the ADF4007 allows the user to access various internal points on the chip. The state of MUXOUT is controlled by the M2 and M1 pins. Figure 12 shows the MUXOUT section in block diagram form.

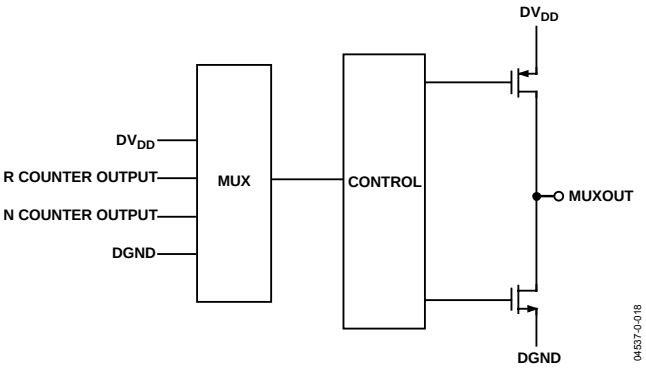


Figure 12. MUXOUT Circuit

PFD Polarity

The PFD polarity is set by the state of M2 and M1 pins as given in the Table 5. The ability to set the polarity allows the use of VCOs with either positive or negative tuning characteristics. For standard VCOs with positive characteristics (output frequency increases with increasing tuning voltage), the polarity should be set to positive. This is accomplished by tying M2 and M1 to a logic low state.

CP Output

The CP output state is also controlled by the state of M2 and M1. It can be set either to active (so that the loop can be locked) or to three-state (open the loop). The normal state is CP output active.

APPLICATIONS

FIXED HIGH FREQUENCY LOCAL OSCILLATOR

Figure 13 shows the ADF4007 being used with the HMC358MS8G VCO from Hittite Microwave Corporation to produce a fixed-frequency LO (local oscillator), which could be used in satellite or CATV applications. In this case, the desired LO is 6.7 GHz.

The reference input signal is applied to the circuit at $FREF_{IN}$ and, in this case, is terminated in 50 Ω. Many systems would have either a TCXO or an OCXO driving the reference input without any 50 Ω termination. To bias the REF_{IN} pin at $AV_{DD}/2$, ac coupling is used. The value of the coupling capacitor used depends on the input frequency. The equivalent impedance at the input frequency should be less than 10 Ω. Given that the dc input impedance at the REF_{IN} pin is 100 kΩ, less than 0.1% of the signal is lost.

The charge pump output of the ADF4007 drives the loop filter. In calculating the loop filter component values, a number of items need to be considered. In this example, the loop filter was designed so that the overall phase margin for the system is 45°.

Other PLL system specifications are as follows:

K_D = 5 mA
K_V = 100 MHz/V
Loop Bandwidth = 300 kHz
F_{PFD} = 106 MHz
N = 64

All these specifications are needed and used with the ADIsimPLL to derive the loop filter component values shown in Figure 13.

The circuit in Figure 13 gives a typical phase noise performance of −100 dBc/Hz at 10 kHz offset from the carrier. Spurs are heavily attenuated by the loop filter and are below −90 dBc.

The loop filter output drives the VCO, which, in turn, is fed back to the RF input of the PLL synthesizer and also drives the RF output terminal. A T-circuit configuration provides 50 Ω matching between the VCO output, the RF output, and the RF_{IN} terminal of the synthesizer.

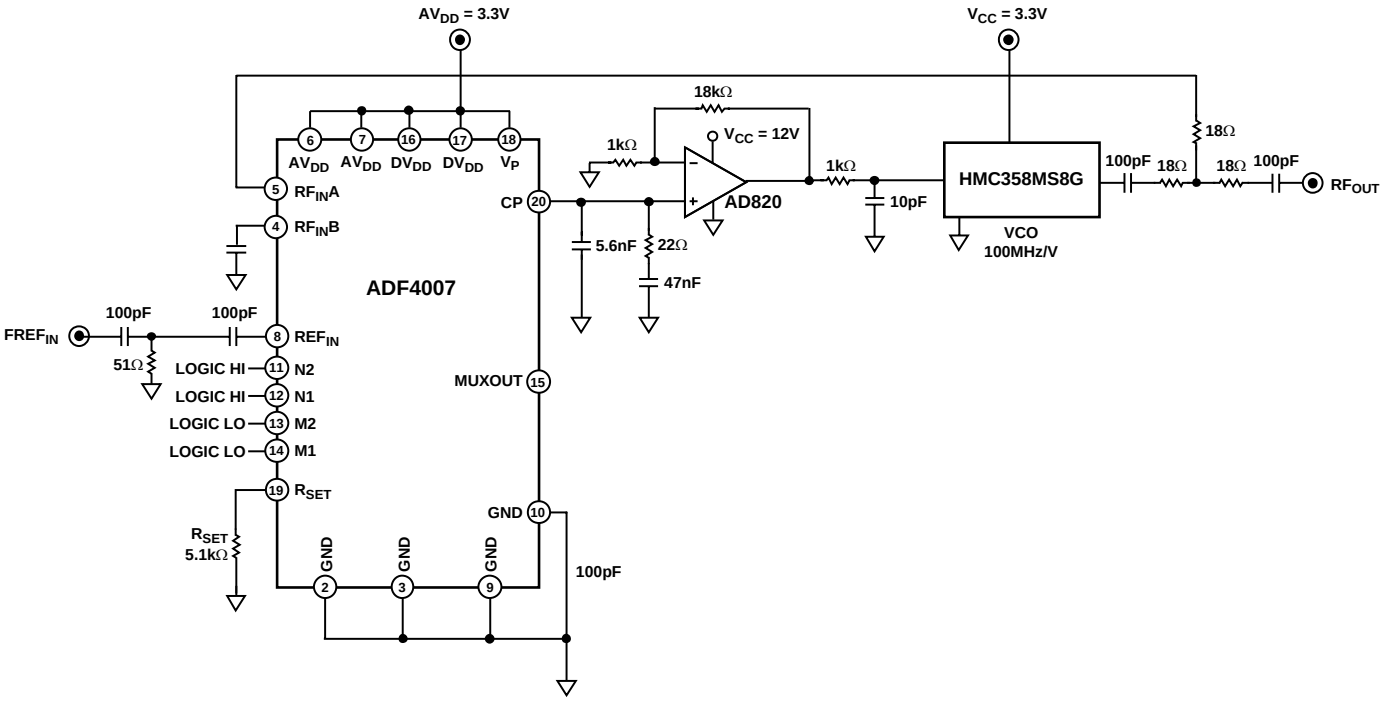


Figure 13. 6.78 GHz Local Oscillator Using the ADF4007

USING THE ADF4007 AS A DIVIDER

In addition to its use as a standard PLL synthesizer, the ADF4007 can also be used as a high frequency counter/divider with a value of 8, 16, 32, or 64.This can prove useful in a wide variety of applications where a higher frequency signal is readily available. Figure 14 shows the ADF4007 used in this manner with the ADF4360-7.

This part is an integrated synthesizer and VCO, in this case operating over a range of 1200 MHz to 1500 MHz. With divide-by-8 chosen in the ADF4007 (N2 = 0, N1 = 0), the output range is 150 MHz to 187.50 MHz.

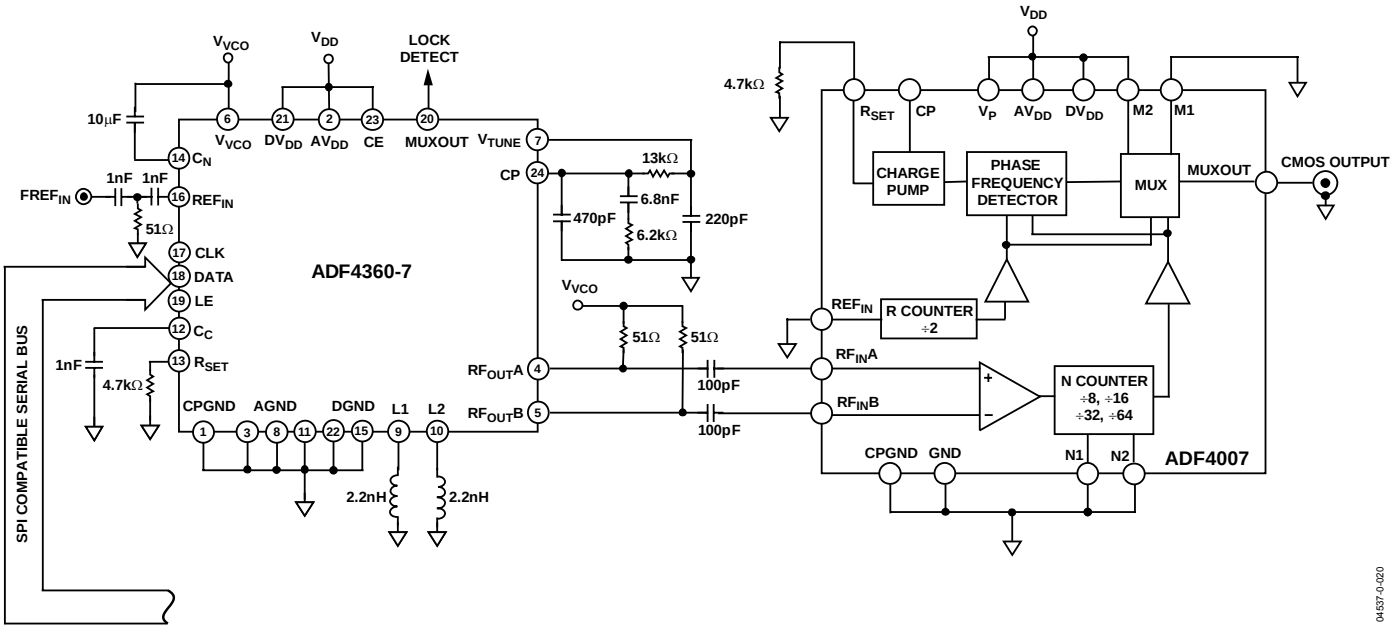


Figure 14. Using the ADF4007 to Divide-Down the Output of the ADF4360-7

PCB DESIGN GUIDELINES FOR CHIP SCALE PACKAGE

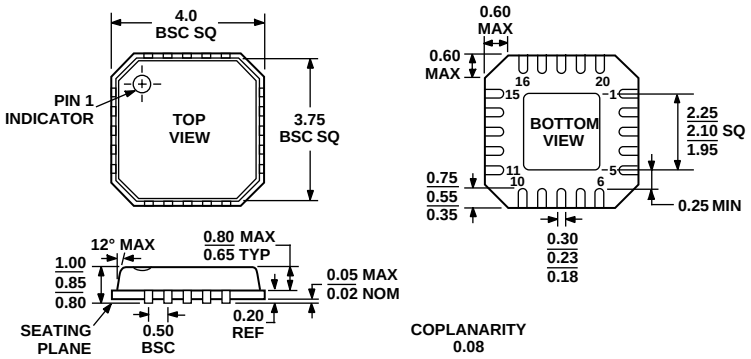
The lands on the chip scale package (CP-20) are rectangular. The printed circuit board pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad to ensure that the solder joint size is maximized.

The bottom of the chip scale package has a central thermal pad. The thermal pad on the printed circuit board should be at least as large as this exposed pad. The printed circuit board should have a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern to ensure that shorting is avoided.

Thermal vias may be used on the printed circuit board thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated in the thermal pad at 1.2 mm pitch grid. The via diameter should be between 0.30 mm and 0.33 mm, and the via barrel should be plated with 1 oz. copper to plug the via.

The user should connect the printed circuit board thermal pad to AGND.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-1

Figure 15. 20-Lead Frame Chip Scale Package [LFCSP]
(CP-20)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADF4007BCP	−40°C to + 85°C	20-lead frame chip scale package (LFCSP)	CP-20
ADF4007BCP−REEL	−40°C to + 85°C	20-lead frame chip scale package (LFCSP)	CP-20
ADF4007BCP−REEL7	−40°C to + 85°C	20-lead frame chip scale package (LFCSP)	CP-20

CP = chip scale package.

NOTES

NOTES

D04537–0–2/04(0)