System-Management IC with Programmable Quad Voltage Monitoring and Supervisory Functions

Preliminary Technical Data

AD5100

FEATURES

- **Two Device-Enabling Outputs with Six Programmable Monitoring Inputs (Table 1)**
  - **Two 30V Monitoring Inputs with Shutdown Control of External Devices:**
    - **Programmable Over-voltage, Under-voltage, Turn-on, Turn-off Thresholds, and Shutdown timings**
    - **Shutdown Warning with Fault Detection**
  - **Two 5V Monitoring Inputs with Reset Control of External Devices:**
    - **Programmable Reset Thresholds and Hold Time**
  - **Two Supervisory Functions:**
    - **Watchdog Reset Controller with Programmable Timeout and Selectable Floating Input**
    - **Manual Reset Control for External Devices**
- **Digital Interface and Programmability:**
  - **I²C® Compatible Interface**
  - **OTP[1] for Permanent Threshold and Timing Settings**
  - **OTP Overwritten Capable for Dynamic Adjustments**
  - **Power Up by Edge Triggered Signal**
  - **Power Down by I²C Software**
- **Operating Range:**
  - **Supply Voltage 6.0V to 30V**
  - **Temp Range -40°C to +125°C**
  - **Low Shutdown Current: 10µA**
- **High-Voltage-Input Anti-migration Shielding Pinouts**

APPLICATIONS

- **Automotive Systems**
- **Network Equipment**
- **Computers, Controllers, and Embedded Systems**

GENERAL DESCRIPTION

The AD5100 is a programmable system-management IC that combines 4-channel of voltage monitoring and a watchdog supervision that can be used to shutdown external supplies, reset processors, or disable any other system electronics when the systems malfunction. The AD5100 can also be used to protect system under faulty condition of improper devices power up sequencing. The AD5100 can monitor two 30V inputs with shutdown and reset controls, one 2.5V-5.0V and one 0.9V-3.3V monitoring inputs with reset control, a robust watchdog reset controller. Most monitoring input thresholds and timing settings can be programmed on the fly or permanently set in the factory with the OTP feature.

The AD5100 is versatile for system-monitoring applications where critical µP, DSP, and embedded systems operate under harsh conditions such as automotive, industrial, or communications network environments.

The AD5100 is available in compact QSOP-16 and can operate in an extended automotive temperature range from -40°C to +125°C.

[1].One Time Programmable EPROM – Unlimited Adjustment Before OTP Execution.
[2] With Programmable Threshold and Programmable Delay.

Table 1. AD5100 General Inputs and Output Information

Input	Monitoring Range[2]	Shutdown Control	Reset Control	Fault Detection
V_{1MON}	6 – 30 V	√	√	√
V_{2MON}	3 – 30 V	√	√	√
V_{3MON}	2.5 – 5.0 V		√	√
V_{4MON}	0.9 – 3.3 V		√	√
WDI	0 – 5 V	√	√	
$\overline{MR}$	0 – 5 V		√	

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FUNCTIONAL BLOCK DIAGRAM

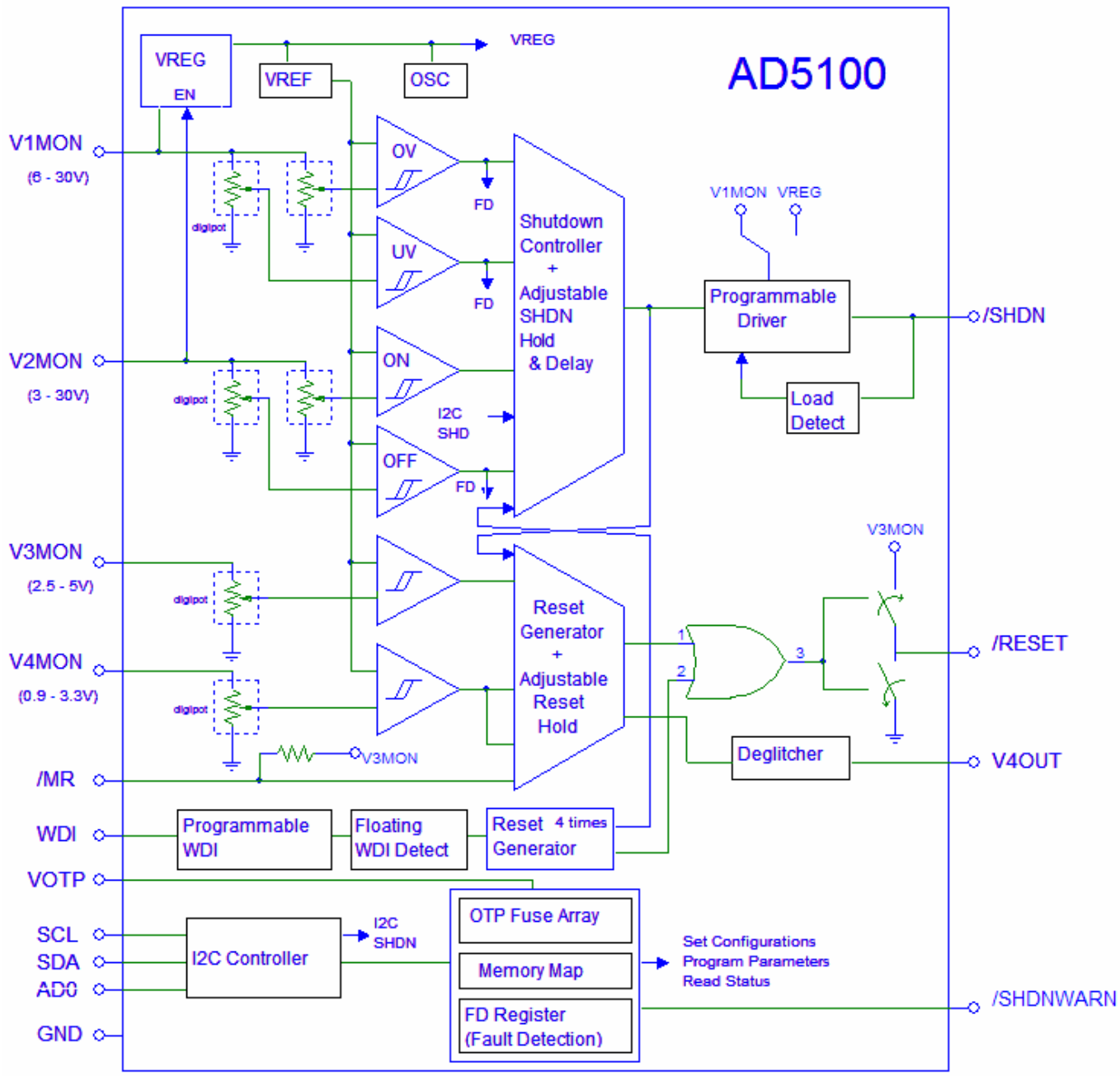


Figure 1. Functional Block Diagram

Electrical Characteristics

$6V \le V_{1MON} \le 30V$ and $3V \le V_{2MON} \le 30V$, $-40°C \le T_A \le +125°C$, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
HIGH-VOLTAGE MONITORING INPUTS V_{1MON}, V_{2MON} AND $\overline{SHDN}$, $\overline{SHDNWARN}$ OUTPUT						
Input Resistance	R_{IN_V1MON}, R_{IN_V2MON}			60		KΩ
V_{1MON}						
OV, UV Threshold Tolerance	ΔOV, ΔUV	T_A = 25°C	-1.5		+1.5	%
(Figure 5 and Table 5a)		T_A = -40°C to 85°C	-2		+2	%
		T_A = -40°C to 125°C	-3		+3	%
Hysteresis				1.5		%
Programmable Shutdown Hold Time Tolerance	Δt_{1SD_HOLD}	Does not apply to code 0x7	-10		+10	%
(Figure 5 and Table 6a)						
Programmable Shutdown Delay Tolerance	Δt_{1SD_DELAY}	Does not apply to code 0x7	-10		+10	%
(Figure 4 and Table 6a)						
Fault Detection Delay	t_{FD_DELAY}			70		µs
Glitch-Immune Time	t_{GLITCH}			50		µs
V_{2MON}						
On, Off Threshold Tolerance[2]	ΔOn, ΔOff	T_A = 25°C	-1.5		+1.5	%
(Figure 5 and Table 5a)		T_A = -40°C to 85°C	-2		+2	%
		T_A = -40°C to 125°C	-3		+3	%
Hysteresis				1.5		%
Turn-On Programmable SHDN Hold Time Tolerance	Δt_{2SD_HOLD}	Does not apply to code 0x7	-10		+10	%
(Figure 5 and Table 6a)						
Turn-Off Programmable SHDN Delay Time Tolerance	Δt_{2SD_DELAY}	Does not apply to code 0x7	-10		+10	%
(Figure 5 and Table 6a)						
Fault Detection Delay	t_{FD_DELAY}	V_{2MON_OFF} only		70		µs
Glitch Immune Time	t_{GLITCH}			50		µs
$\overline{SHDN}$						
$\overline{SHDN}$ Output High	V_{OH}	V_{RAIL}=V_{REG}, I_{SOURCE}=40uA	2.4			V
$\overline{SHDN}$ Output High	V_{OH}	V_{RAIL}=V_{1MON}, I_{SOURCE}=600uA	V_{1MON}-0.5			V
$\overline{SHDN}$ Output Low	V_{OL}	I_{SINK}=1.6mA			0.4	V
$\overline{SHDN}$ Output Low	V_{OL}	V_{1MON}=12V, I_{SINK}=40mA		1.7	3	V
$\overline{SHDN}$ Sink Current	I_{SINK}	V_{1MON}=12V, $\overline{SHDN}$ forced to 12V		10	15	mA
$\overline{SHDNWARN}$ (Open Drain Output)						
$\overline{SHDNWARN}$ Inactive Leakage Current	$I_{OH\_SHDNWARN}$			1		µA
$\overline{SHDNWARN}$ Active	$V_{OL\_SHDNWARN}$	Isink = 3mA			0.4	V
LOW-VOLTAGE MONITORING INPUTS V_{3MON}, V_{4MON} AND $\overline{RESET}$ OUTPUT						
Voltage Range	V_{3MON}, V_{4MON}		-0.3		5.5	V
Input Resistance	R_{IN_V1MON}, R_{IN_V2MON}			50		KΩ
V_{3MON}, V_{4MON}						
V_{3MON} Threshold Tolerance	ΔV_{3MON}	T_A = 25°C	-1.5		+1.5	%
(Figure 6 and Table 5a)		T_A = -40°C to 85°C	-2		+2.7	%
		T_A = -40°C to 125°C	-3		+3.5	%
V_{3MON} Hysteresis	$V_{3\_HYSTERESIS}$			1.5		%

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
V_{4MON} Threshold Tolerance	ΔV_{4MON}	T_A = 25°C	-2.5		+2.5	%
(Figure 7 and Table 5a)		T_A = -40°C to 85°C	-3		+3	%
		T_A = -40°C to 125°C	-3.5		+3.5	%
V_{4MON} Hysteresis	$V_{4\_HYSTERESIS}$			6		%
Reset Hold Time Tolerance (Figures 6, 7, and Table 6a)	Δt_{RS_HOLD}	Does not apply to codes 0x6 and 0x7	-10		+10	%
$V_{3,4MON}$–to-$\overline{RESET}$ Delay	t_{RS_DELAY}			70		µs
$\overline{RESET}$ Output Voltage	V_{OH}	$V_{3MON} \geq$ 4.38V, I_{SOURCE} = 120uA	V_{3MON}-1.5			V
		2.7V < $V_{3MON} \leq$ 4.38V, I_{SOURCE} = 30uA	0.8xV_{3MON}			V
		2.3V < $V_{3MON} \leq$ 2.7V, I_{SOURCE} = 20uA	0.8xV_{3MON}			V
		1.8V $\leq V_{3MON} \leq$ 2.3V, I_{SOURCE} = 8uA	0.8xV_{3MON}			V
	V_{OL}	V_{3MON} > 4.38V, I_{SINK} = 3.2mA			0.4	V
		V_{3MON} < 4.38V, I_{SINK} = 1.2mA			0.3	V
$\overline{RESET}$ Output Short-Circuit Current[3]	I_{SOURCE}	$\overline{RESET}$ = 0, V_{3MON} = 5.5V			800	µA
		$\overline{RESET}$ = 0, V_{3MON} = 3.6V			400	µA
Glitch Immune Time	t_{GLITCH}			50		µs
V_{4OUT} Maximum Output	V_{4OUT_MAX}	Open Drain			5.5	V
V_{4OUT} Propagation Delay	t_{V4OUT_Delay}			70		µs
V_{4OUT} Maximum Frequency	f_{V4OUT}	Apply to $\overline{RESET}$ disabled only		10		KHz
WDI (WATCHDOG INPUT)						
WDI Programmable-Timeout Tolerance	Δt_{WD}		-10		+10	%
(Figure 8 and Table 6a)						
WDI Pulse Width	t_{WDI}		50			ns
Watchdog-Initiated $\overline{RESET}$ Pulse Width	t_{WDR}	When no WDI		t_{WD}/50		ms
Watchdog-Initiated $\overline{SHDN}$	t_{WD_SHDN}	When no WDI activity > 4 t_{WD}		1		s
WDI Input Voltage	V_{IL_WD}				0.3xV_{3MON}	V
	V_{IH_WD}		0.7xV_{3MON}			V
WDI Input Current		WDI = V_{3MON}, time average			160	µA
		WDI = 0, time average	-20			µA
$\overline{MR}$ (**MANUAL RESET) INPUT**						
$\overline{MR}$ Input Voltage	V_{IL_MR}				0.3*V_{3MON}	V
	V_{IH_MR}		0.7*V_{3MON}			V
$\overline{MR}$ Pulse Width	t_{MR}		1			µs
$\overline{MR}$ Deglitching	t_{MR_GLITCH}			100		ns
$\overline{MR}$ -to-Reset Delay	t_{MR_DELAY}			1		µs
$\overline{MR}$ Pullup Resistance (internal to V3MON)				50		KΩ
Reset Hold-Time Tolerance (Figure 9 and Table 6a)	Δt_{RS_HOLD}	Do not apply to codes 0x6 and 0x7	-10		+10	%
SERIAL INTERFACES						
Input Logic High (SCL, SDA)[4]	V_{IH}	External Rpull-up = 2.2kΩ	2.0		5.5	V
Input Logic Low (SCL, SDA)	V_{IL}	External Rpull-up = 2.2kΩ	0		0.8	V
Output Logic High (SDA)	V_{OH}	V_{RAIL} = 3.3V, External Rpull-up = 2.2kΩ	3.0		3.3	V
Output Logic Low (SDA)	V_{OL}	V_{RAIL} = 3.3V, External Rpull-up = 2.2kΩ	0		0.4	V
Input Capacitance	C_I			5		pF
POWER SUPPLY						
Supply Voltage Range	V_{1MON}		6.0		30	V

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
Sleep Mode Supply Current	I_{SLEEP_V1MON}	V_{2MON} = 0 V			10	µA
Active Mode Supply Current	I_{POWER_V1MON}	V_{2MON} = 12 V			3	mA
		V_{2MON} Edge Triggered Mode Selected			3	mA
Device Power On Threshold	V2MON,IH		2.2			V
	V2MON,IL				0.4	V
Device Power Up V2MON Minimum Pulse Width (Figure 14)	t_{V2MON_PW}		4			ms
Device Power Down Delay		V2MON < 0.4V (Normal Mode)		2		s
		I2C Initiated Power Down		10		µs
OTP Supply Voltage[6]	V_{OTP}	For OTP only	6		6.5	V
OTP Supply Current	I_{VOTP}	For OTP only	200			mA
OTP Settling Time[7]	t_{S_OTP}			12		ms
TIMING CHARACTERISTICS [8]						
Parameter Adjustment Time	t_{S1}			1		µs
I2C Interface Timing Characteristics						
SCL Clock Frequency	f_{SCL}				400	KHz
t_{BUF} Bus Free Time between Start and Stop	t_1		1.3			µs
$t_{HD;STA}$ Hold Time after (Repeated) START condition. After this period, the first clock is generated	t_2		0.6			µs
t_{LOW} Low Period of SCL Clock	t_3		1.3			µs
t_{HIGH} High Period of SCL Clock	t_4		0.6		50	µs
$t_{SU;STA}$ Setup Time for Start Condition	t_5		0.6			µs
$t_{HD;DAT}$ Data Hold Time	t_6				0.9	µs
$t_{SU;DAT}$ Data Setup Time	t_7		0.1			µs
t_F Fall Time of Both SDA and SCL Signals	t_8				0.3	µs
t_R Rise Time of Both SDA and SCL Signals	t_9				0.3	µs
$t_{SU;STO}$ Setup Time for Stop Condition	t_{10}		0.6			µs

Notes:
1. Represent typical values at 25°C, V_{1MON} = 12 V, and V_{2MON} = 12 V.
2. Does not apply if V_{2MON} is a digital signal.
3. The $\overline{\text{RESET}}$ short-circuit current is the maximum pullup current when $\overline{\text{RESET}}$ is driven low by a µP bidirectional reset pin.
4. It is typical for the SCL and SDA have resistors to be pulled up to V_{3MON}. However, care must be taken to ensure that the minimum V_{IH} is met when the SCL and SDA are driven directly from a low voltage logic controller without pull-up resistors.
5. Initial V_{2MON} ON minimum remains as 2.2V but the -0.3V to 30V specifications apply afterwards.
6. V_{OTP} can be furnished by Factory 6V power supply, rather than on-board power supply, when performing factory programming. A 10uF tantalum capacitor is required on V_{OTP} during operation regardless of whether the OTP fuses are programmed.
7. The OTP settling time occurs only once if OTP function is used.
8. Guaranteed by design and not subject to production test.

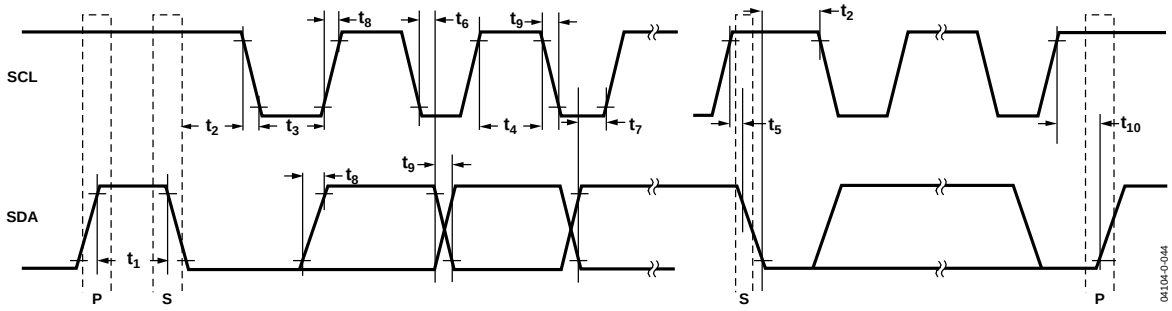


Figure 2. Digital Interface Timing Diagram

Absolute Maximum Ratings

Table 3.

Parameter	Rating
V_{1MON} to GND	−0.3 V, +33 V
V_{2MON} to GND	−0.3 V, +33 V
V_{3MON} to GND	−0.3 V, +7 V
V_{4MON} to GND	−0.3 V, +7 V
V_{OTP} to GND	−0.3 V, +7 V
Digital Input Voltage to GND ($\overline{MR}$, WDI, SCL, SDA, AD0)	0 V, +7V
Digital Output Voltage to GND ($\overline{RESET}$,$V_{4OUT,}$ $\overline{SHDNWARN}$)	0 V, +7V
Digital Output Voltage to GND ($\overline{SHDN}$)	0 V, +33V
Operating Temperature Range	−40°C to +125°C
HBM ESD (All Pins)	2KV
Maximum Junction Temperature ($T_J$max)	140°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 s – 30 s)	245°C
Thermal Resistance Junction-to-Ambient[1] θ_{JA}	105°C/W
Thermal Resistance Junction-to-Case θ_{JC}	39°C/W

[1] Package power dissipation = ($T_J$max – T_A) / θ_{JA}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTION

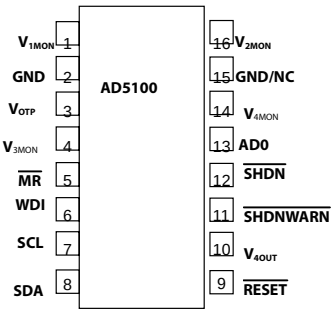


Figure 3a. AD5100 Pin Configuration

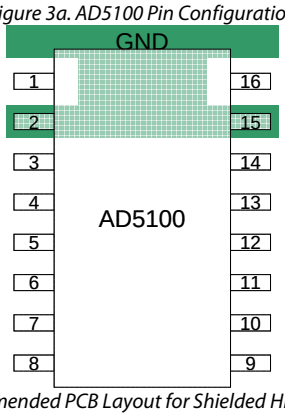


Figure 3b. Recommended PCB Layout for Shielded High-Voltage Inputs

Table 4. AD5100 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{1MON}	High-voltage monitoring input. AD5100 internal supply is derived from V_{1MON}..
2	GND	Ground.
3	V_{OTP}	One-time supply voltage for EPROM. Can be floating when it is not performing fuse programming
4	V_{3MON}	Low-voltage monitoring-input
5	$\overline{MR}$	Manual-Reset Input. Active-low.
6	WDI	Watch-Dog Input.
7	SCL	I2C Serial-Input Register Clock. If it is driven directly from a logic driver without the pull-up resistor, ensure that V_{IH} min is 3.3V.
8	SDA	I2C Serial Data Input/Output. If it is driven direct from a logic driver without the pull-up resistor, ensure that V_{IH} min is 3.3V.
9	$\overline{RESET}$	$\overline{RESET}$, Push-Pull Output with rail voltage of V_{3MON}
10	V_{4OUT}	Open-drain output. Triggered by V_{4MON}
11	$\overline{SHDNWARN}$	Shutdown Warning. Active-Low, Open-drain output.
12	$\overline{SHDN}$	Shutdown output. Push-Pull Output with selectable rail voltage of V_{1MON} or V_{REG} . 30V maximum
13	AD0	I2C Slave-Address Configuration.
14	V_{4MON}	Low-voltage monitoring Input.
15	GND/NC	Ground/No Connect. Can be grounded or left floating but do not connect to any other potentials.
16	V_{2MON}	High-voltage monitoring input. It is also the internal-supply-voltage enabling input.

Table 5a. Available Programmable-Threshold at T_A = 25 °C (All values are typical ratings; see Table 2 for tolerances)

V_{1MON} OV Threshold	V_{1MON} UV Threshold	V_{2MON} ON Threshold	V_{2MON} OFF Threshold	V_{3MON} Threshold	V_{4MON} Threshold
7.92	6.00	3.00	3.00	2.32	Disabled*
9.00	6.49	3.30	3.30	2.64	0.86
9.90	6.95	4.50	4.50	2.93	1.15
11.00	7.47	4.77	4.77	3.10	1.37
12.00	7.92	6.00	6.00	4.36*	1.43
13.20	8.43*	6.49	6.49	4.65	1.66
14.14	9.00	6.95	6.95*	4.75	2.30
15.23	9.43	7.47*	7.47	4.97	3.10
15.84	9.90	7.92	7.92	Reserved	Reserved
17.22	10.42	8.43	8.43	Reserved	Reserved
18.00*	11.00	9.00	9.00	Reserved	Reserved
18.86	11.65	9.43	9.43	Reserved	Reserved
19.80	12.00	9.90	9.90	Reserved	Reserved
22.00	12.38	15.23	15.23	Reserved	Reserved
24.75	13.20	19.80	19.80	Reserved	Reserved
28.29	13.66	24.75	Rising Edge Trigger/Pseudo CAN Wake Up Mode	Reserved	Reserved

* Default. V_{1MON_OV} must be > V_{1MON_UV}. V_{2MON_OFF} will be ignored if > V_{2MON_ON} but V_{2MON_OFF} cannot be = V_{2MON_ON}.

Table 5b. Look Up Table of Programming Code versus Typical Thresholds Shown in Table 5a

Code	V_{1MON} OV Threshold	V_{1MON} UV Threshold	V_{2MON} ON Threshold	V_{2MON} OFF Threshold	V_{3MON} Threshold	V_{4MON} Threshold
0000	18.00*	8.43*	7.47*	6.95*	4.36*	Disabled*
0001	18.86	7.92	6.95	7.47	4.65	0.86
0010	15.84	9.43	6.49	6.00	4.75	1.15
0011	17.22	9.00	6.00	6.49	4.97	1.37
0100	24.75	6.49	4.77	4.50	2.32	1.43
0101	28.29	6.00	4.50	4.77	2.64	1.66
0110	19.80	7.47	3.30	3.00	2.93	2.30
0111	22.00	6.95	3.00	3.30	3.10	3.10
1000	9.90	12.38	24.75	19.80	Reserved	Reserved
1001	11.00	12.00	19.80	Rising Edge Trigger/Pseudo CAN Wake Up Mode	Reserved	Reserved
1010	7.92	13.66	15.23	9.90	Reserved	Reserved
1011	9.00	13.20	9.90	15.23	Reserved	Reserved
1100	14.14	10.42	9.43	9.00	Reserved	Reserved
1101	15.23	9.90	9.00	9.43	Reserved	Reserved
1110	12.00	11.65	8.43	7.92	Reserved	Reserved
1111	13.20	11.00	7.92	8.43	Reserved	Reserved

Table 6a. Available Programmable Hold Time and Delay (All values are typical ratings; see Table 2 for tolerances)

t_{1SD_HOLD} (ms)	t_{1SD_DELAY} (ms)	t_{2SD_HOLD} (ms)	t_{2SD_DELAY} (ms)	t_{RS_HOLD} (ms)	t_{WD} (ms)
0.07	0.07	0.07	0.07	0.1	100
20	50	10*	50	1	250
40	100	20	100*	15	500
60	200	30	200	30	750
80	400	40	400	50	1000
100	800	50	800	100	1250
150	1000	100	1000	150	1500*
200*	1200*	200	1200	200*	2000

* Default

Table 6b. Look Up Table of Programming Code versus Typical Timings Shown in Table 6a

Code	t_{1SD_HOLD} (ms)	t_{1SD_DELAY} (ms)	t_{2SD_HOLD} (ms)	t_{2SD_DELAY} (ms)	t_{RS_HOLD} (ms)	t_{WD} (ms)
000	200*	1200*	10*	100*	200*	1500*
001	150	1000	20	50	150	2000
010	100	800	30	200	100	1250
011	80	400	40	400	50	1000
100	60	200	50	800	30	750
101	40	100	100	1000	15	500
110	20	50	200	1200	1	250
111	0.07	0.07	0.07	0.07	0.1	100

* Default

THEORY OF OPERATION

The AD5100 is a Programmable System Management IC that has four channels of monitoring inputs. Two inputs have high voltage (30V) capability. For example if the AD5100 is used in the automotive application, the V_{1MON} (Monitoring Input 1) should be the battery and the V_{2MON} should either be the ignition switch or the pseudo CAN bus wake up signal input. Two other inputs, V_{3MON} and V_{4MON}, are low voltage for 0.9V, 1.8V, 2.5V, 3.3V, or 5V monitoring. The two high voltage inputs control the shutdown signal, $\overline{SHDN}$, while the two low voltage inputs control the reset signal, $\overline{RESET}$. The $\overline{SHDN}$ and $\overline{RESET}$ are both disabling functions for the external devices. The differences are output levels and driving capabilities that will be described later. In some cases the $\overline{SHDN}$ and $\overline{RESET}$ may be used interchangeably. The WDI (Watchdog) and $\overline{MR}$ (Manual Reset) inputs also control $\overline{RESET}$ output for external digital processor. Figure 4 shows the general flow chart and Table 7 summarizes the AD5100 functions and features.

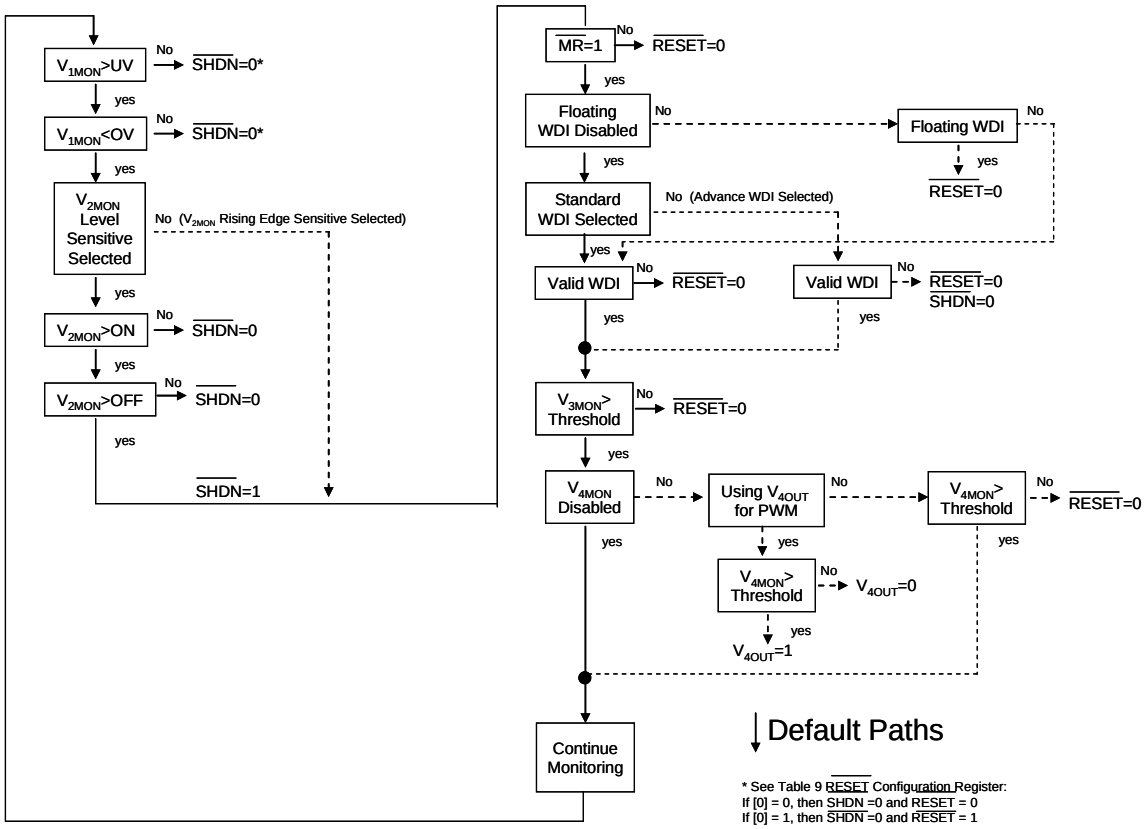


Figure 4. General Flow Chart

Table 7. AD5100 Functions and Features

Input	Monitoring Range	Shutdown Control	Reset Control	Fault Detection	Functions and Features	If Not Used
V_{1MON}	6 – 30 V	√	√	√	Over/Under Voltage	Does not apply
V_{2MON}	3 – 30 V	√	√	√	On/Off Voltage CAN Bus Wake Up	Tie to V_{1MON}, Min Input
V_{3MON}	2.5 – 5.0 V		√	√		Connect to VOTP and Threshold to Minimum
V_{4MON}	0.9 – 3.3 V		√	√	Additional Output	Select Disable in Threshold
WDI	0 – 5 V	√	√		Standard, Advance, or Watchdog Selectable	Leave Floating

$\overline{MR}$	0 – 5 V	√	Highest Prority on Other Inputs	Leave Floating

Monitoring Inputs

V_{1MON}

V_{1MON} is a high-voltage monitoring input that controls the $\overline{SHDN}$ and $\overline{RESET}$ functions of the external devices. In addition, it also provides a shutdown warning to the system. V_{1MON} monitors inputs from 6V to 30V. It has a 16-level programmable over-voltage, under-voltage (OV,UV) shutdown threshold with an 8-step 0.05ms-200ms shutdown hold time and 0.05ms-1200ms shutdown delay. The shutdown hold time means that the shutdown of the external device is held until the programmed-time is reached. On the other hand, the shutdown delay means that shuting down the external device is delayed until the programmed-time is reached.

The OV threshold chosen must be greater than the UV threshold. When the shutdown is triggered either because the input has reached OV or UV threshold, such fault condition will be temporarily recorded in the Fault Detection Register. The $\overline{SHDNWARN}$ output will transition low for signaling before shutdown occurs. The occurance of Shutdown is depending on how long the shutdown programmed-delay is set relative to the $\overline{SHDNWARN}$ propagation delay, this feature attempts to allow the system to finish any critical house keeping tasks before shuting down the external device. The V_{1MON}, shutdown, and shutdown warning timing diagrams are shown in Figure 5. The ranges of OV and UV Thresholds are shown in Table 5a and the programming codes of the selected-thresholds are found in Table 5b. The defaulted OV threshold is 18.00V and UV threshold is 8.43V. Simarily, the ranges of shutdown hold and delay times are shown in Table 6a and the programming codes of the selected-timings are found in Table 6b. The defaulted shutdown hold time is 200ms delay time is 1200ms.

The voltage at V_{1MON} provides the power for the AD5100 but valid signal at V_{2MON} must be present before the internal V_{REG} starts operation. Details will be explained in the power section.

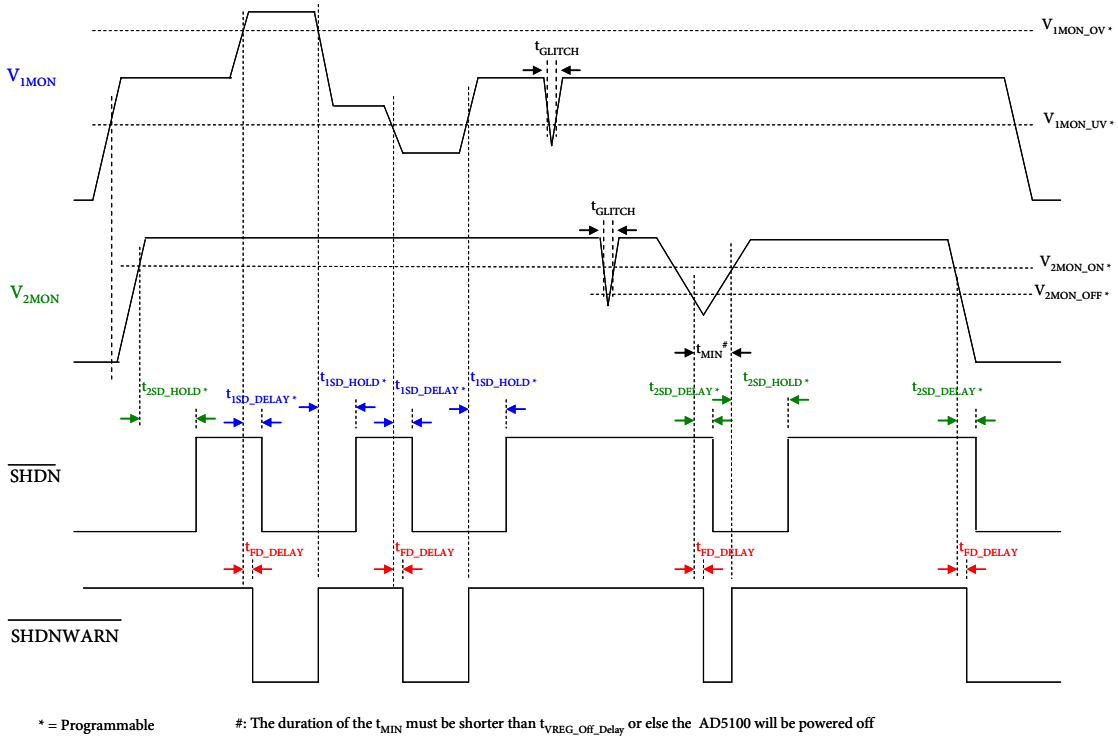


Figure 5. V_{1MON} and V_{2MON} Shutdown Timing Diagrams (Note $\overline{RESET}$ follows $\overline{SHDN}$).

The V_{1MON} pin is monitored by two comparators, one for over-voltage, and one for under-voltage detection. Both are designed with 1.5% hysteresis.

When the V_{1MON} n input goes above the programmed OV threshold, the comparator will become active immediately, indicating an OV condition has occurred. Due to hysteresis, the V_{1MON} input must be brought below the programmed OV threshold by 1.5% before the comparator will be in-active, indicating the OV condition has gone away, see Figure 6.

When the V_{1MON} input drops below the programmed UV threshold, the comparator will become active immediately, indicating a UV condition has occurred. Similarly due to hysteresis, the V_{1MON} input must be brought above the programmed UV threshold by 1.5% before the comparator will be in-active, indicating the UV condition has gone away. Both V1mon comparators are used (in conjunction with hold and delay timers) to control the $\overline{SHDN}$ and $\overline{RESET}$ pins.

V_{1MON} exhibits typical input resistance of 60KΩ that users should account the loading effect.

The default V_{1MON} OV and UV thresholds are 18.00V and 8.43V respectively. The default V_{1MON} Shutdown Hold time and Shutdown Delay are 200ms and 1200ms respectively. User should refer to Tables 5b and 6b if they want to program different settings.

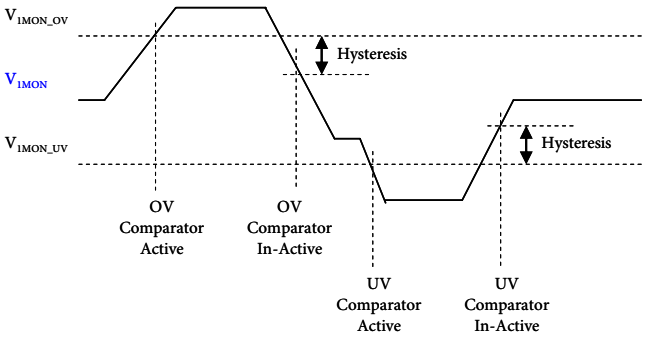


Figure 6. V_{1MON} Hysteresis.

V_{2MON}

V_{2MON} is a high-voltage monitoring input that controls the $\overline{SHDN}$ and $\overline{RESET}$ functions of the external devices. V_{2MON} monitors inputs from 3V to 30V. It has a 16-level programmable Turn-on, Turn-off (ON,OFF) hysteresis threshold with an 8-step 0.05ms-200ms shutdown hold time and 0.05ms-1200ms shutdown delay.

By default, V_{2MON} is level-sensitive that the ON and OFF thresholds are both monitored. The ON threshold chosen must be greater than the OFF threshold. When the shutdown function is triggered by the input reaching V_{2MON_OFF} threshold, such fault condition will be temporarily recorded in the Fault Detection Register. The $\overline{SHDNWARN}$ output will transition low for signaling before shutdown occurs. The occurance of shutdown is depending on how long the shutdown programmed-delay is set relative to the $\overline{SHDNWARN}$ propagation delay, this feature attempts to allow the system to finish any critical house keeping tasks before shuting down the external device. The V_{2MON}, shutdown, and shutdown warning pins timing diagrams are also shown in Figure 5. The ranges of ON and OFF Thresholds are shown in Tables 5a and the programming codes of the selected-thresholds are found in Table 5b. The defaulted ON threshold is 7.47V and OFF threshold is 6.95V. Simarily, the ranges of shutdown hold and delay times are shown in Table 6a and the programming codes of the selected-timings are found in Table 6b. The defaulted shutdown hold time is 10ms and delay time is 100ms.

V_{2MON_OFF} will be ignored if $V_{2MON\_OFF} > V_{2MON\_ON}$ but V_{2MON_OFF} cannot be = V_{2MON_ON}.

If the V_{2MON} is selected with Rising Edge Triggered, only the ON threshold is monitored and the OFF Threshold is ignored.

The voltage at V_{1MON} provides the power for the AD5100 but valid signal at V_{2MON} must be present before the internal V_{REG} starts operation. Details will be explained in the power section.

The V_{2MON} pin is monitored by 2 comparators, 1 for turn-on, and 1 for turn-off detection in the level sensitive power-up mode. Both are designed with 1.5% hysteresis. On the other hand, the turn-on monitoring comparator is used only if the rising edge trigger power-up mode is selected.

When the V_{2MON} input goes above the programmed Ton threshold, the comparator will become active immediately, indicating an OV condition has occurred. Due to hysteresis, the V_{2MON} input must be brought below the programmed threshold by 1.5% before the comparator will be in-active, indicating the OV condition has gone away, see Figure 7.

When the V_{2MON} input drops below the programmed threshold, the comparator will become active immediately, indicating a UV condition has occurred. Similarly due to hysteresis, the V_{2MON} input must be brought above the programmed threshold by 1.5% before the comparator will be in-active, indicating the UV condition has gone away.

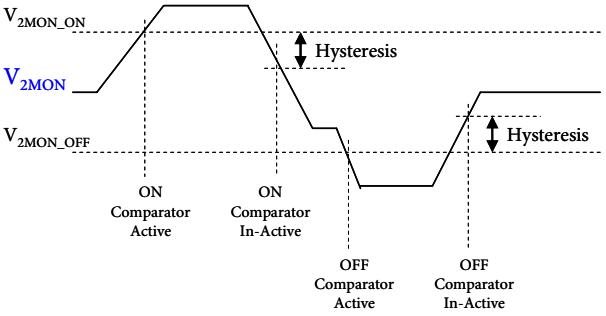


Figure 7. V_{2MON} Hysteresis.

V_{2MON} exhibits typical input resistance of 60KΩ that users should account the loading effect.

The default V_{2MON} ON and OFF thresholds are 7.47V and 6.95V respectively. The default V_{2MON} Shutdown Hold time and Shutdown Delay are 10ms and 100ms respectively. User should refer to Tables 5b and 6b if they want to program different settings.

V_{3MON}

V_{3MON} is a low-voltage monitoring input that controls the $\overline{RESET}$ function of an external device. V_{3MON} monitors inputs from 2.5V to 5.5V. It has an 8-step programmable reset threshold with an 8-step 0.1ms-200ms reset hold time. The reset hold time means that the reset of the external device is held until the programmed-time is reached. The V_{3MON} and reset timing diagrams are shown in Figure 8. The range of thresholds is shown in Table 5a and the programming code of the selected-threshold is found in Table 5b. The defaulted monitoring threshold is 4.36V. Similarly, the range of reset hold time is shown in Tables 6a and the programming code of the selected-timing is found in Table 6b. The defaulted reset hold time is 200ms.

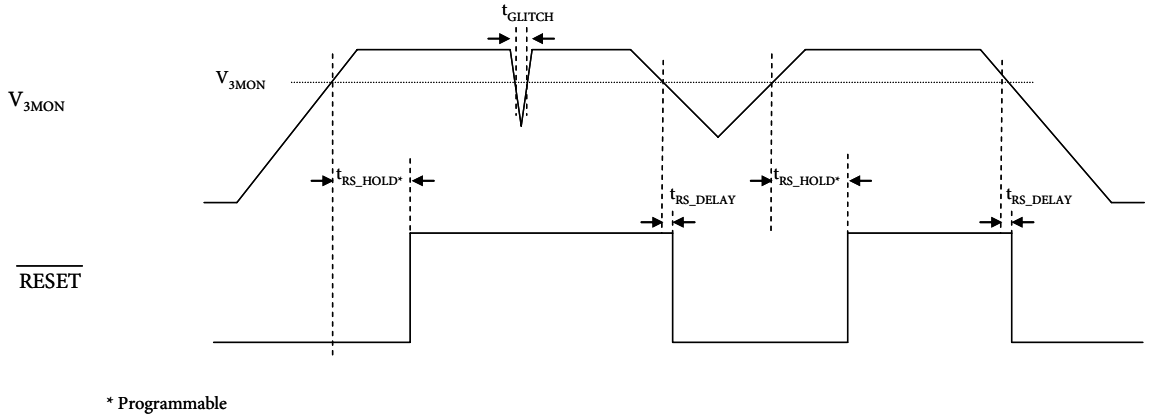


Figure 8. V_{3MON} $\overline{RESET}$ Timing Diagrams

The V_{3MON} pin is monitored by a comparator to detect an under-voltage condition. It is designed with 1.5% hysteresis. When the V_{3MON} input drops below the programmed UV threshold, the comparator will become active immediately, indicating a UV condition has occurred. Due to hysteresis, the V_{3MON} input must be brought above the programmed UV threshold by 1.5% before the comparator will be in-active, indicating the UV condition has gone away, see Figure 9.

The V_{3MON} comparator is used (in conjunction with a hold timer) to control the $\overline{RESET}$ pin.

V_{3MON} exhibits typical input resistance of 50KΩ that users should account the loading effect.

The $\overline{MR}$ input has an internal resistor pull-up toV_{3MON}. The $\overline{RESET}$ output are push-pull configured between V_{3MON} and GND.

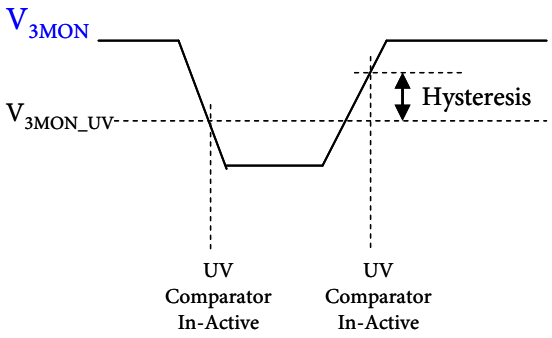
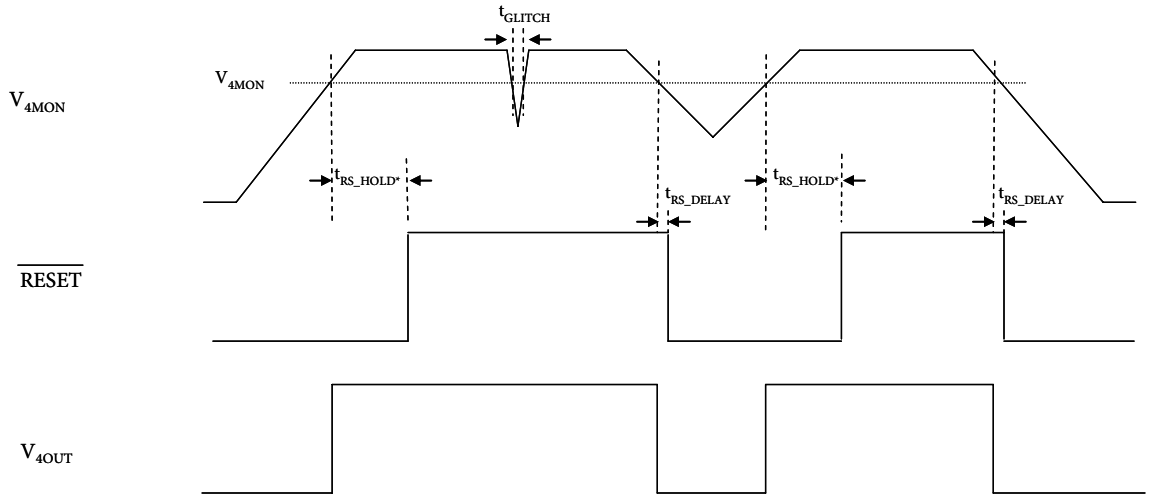


Figure 9. V_{3MON} Hysteresis.

The default V_{3MON} threshold is 4.36V. User should refer to Table 5b if they want to program different setting.

V_{4MON}

V_{4MON} is the lowest voltage monitoring input that controls the $\overline{RESET}$ function of an external device or provides a comparator output, V_{4OUT}. V_{4MON} monitors input from 0.9V to 3.3V. It has an 8-step programmable reset threshold with an 8-step 0.1ms to 200ms reset hold time. The V_{4MON}, reset, and V_{4OUT} timing diagrams are shown in Figure 10. The range of thresholds is shown in Table 5a and the programming code of the selected-threshold is found in Tables 5b. The defaulted monitoring threshold is Disabled. Similarly, the range of reset hold time is shown in Tables 6a and the programming code of the selected-timing is found in Table 6b.



•Programmable
Most Applications using V_{4OUT} require disabling of V_{4MON} triggered reset

Figure 10. V_{4MON}, $\overline{RESET}$, and V_{4OUT} Timing Diagrams

The V_{4MON} pin is monitored by a comparator to detect an under-voltage condition. It is designed with 6% hysteresis.

When the V_{4MON} input drops below the programmed UV threshold, the comparator will become active immediately, indicating a UV condition has occurred. Due to hysteresis, the V_{4MON} input must be brought above the programmed UV threshold by 6% before the comparator will be in-active, indicating the UV condition has gone away, See Figure 11.

The V_{4MON} comparator is used to control the V_{4OUT} pin and also (in conjunction with a hold timer) to control the RESET pin.

V_{4MON} exhibits typical input resistance of 50KΩ that users should account the loading effect.

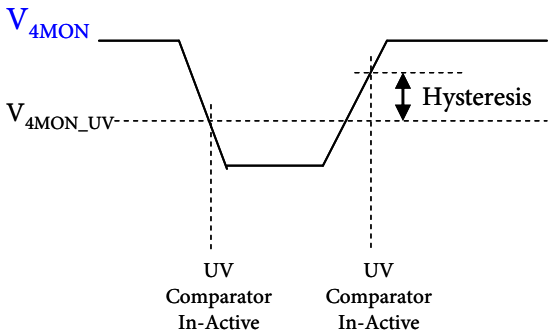


Figure 11. V_{4MON} Hysteresis.

The default V_{4MON} is Disabled. User should refer to Table 5b if they want to program a different setting.

Watchdog Input

The Watch-Dog Input (WDI) circuit attempts to reset the system to a known good state if a software or hardware glitch renders the system processor inactive for a duration that is longer than the timeout period. There is an 8-step programmable timeout period from 100ms to 2000ms.The watchdog circuit is independent of the CPU clock that the watchdog is monitoring.

Watchdog is disabled during power-up. WDI starts monitoring once the $\overline{\text{RESET}}$ is high. Unique to AD5100, it provides a Standard or Advance Watchdog monitoring function. In the defaulted Standard Watchdog mode, if WDI remains either high or low for longer than the timeout period, a reset pulse is generated in an attempt to allow the system processor to re-establish the WDI signal. The reset pulses continue indefinitely until a valid watchdog signal, a rising or falling edge signal at the WDI, is received. The internal watchdog timer clears whenever reset is asserted. The Standard WDI and $\overline{\text{RESET}}$ timing diagrams are shown in Figure 12.

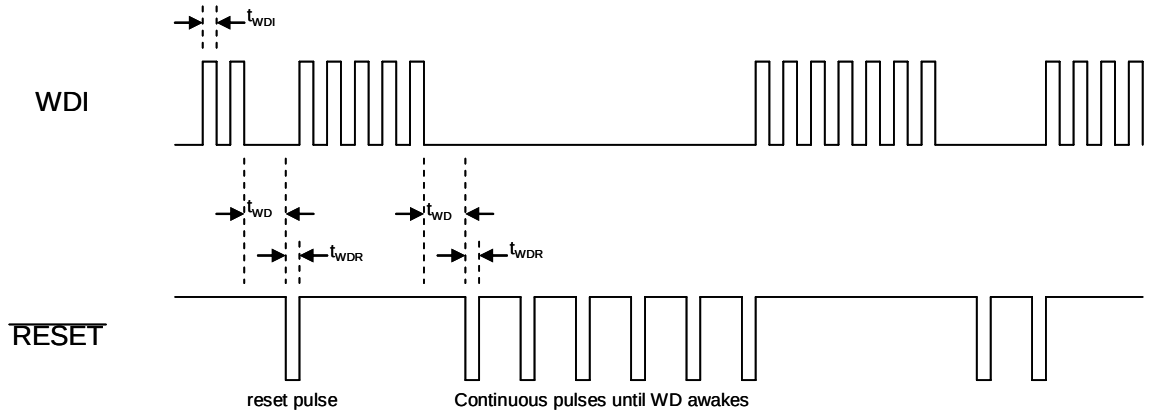


Figure 12. Standard Watchdog – Pulsing Reset Until Watchdog Awakes.

On the other hand, the AD5100 can be programmed to an Advance Watchdog mode such that when the watchdog remains inactive longer than three times the watchdog timeout period, at the forth time the $\overline{\text{SHDN}}$ and $\overline{\text{RESET}}$ will be asserted and released after 1 second. These actions repeat indefinitely, unless it is interferred by the user, if the processor is not responding. The Advance WDI and $\overline{\text{RESET}}$ timing diagrams are shown in Figure 13.

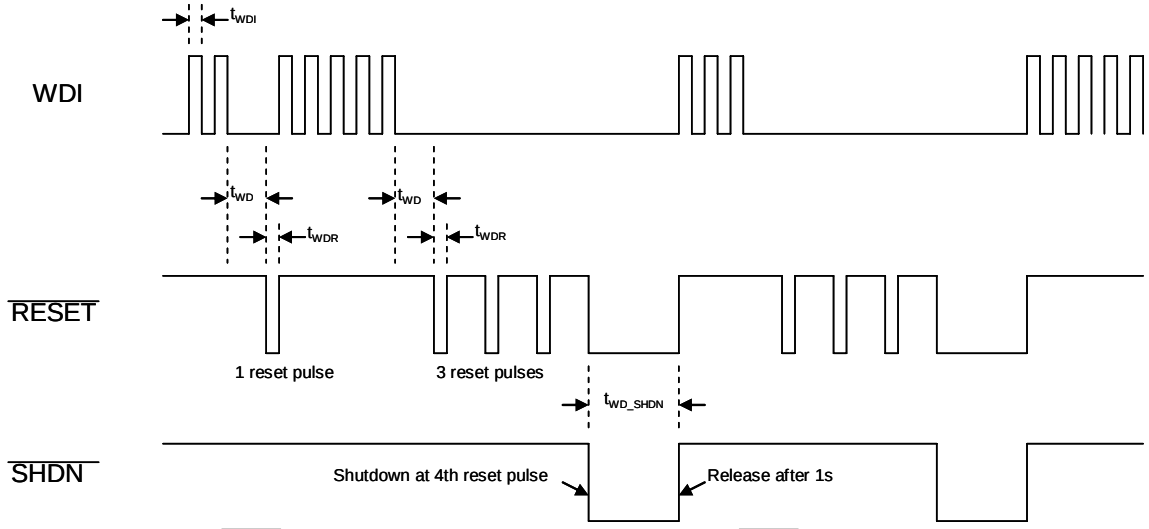


Figure 13. Advance Watchdog – $\overline{\text{SHDN}}$ Asserted After Three Trials of Reseting the Watchdog. $\overline{\text{SHDN}}$ Released After 1 second and the cycle repeats.

The range of Watchdog Timeout is shown in Table 6a and the programming code of the selected-timeout is found in Table 6b. The default timeout is 1500ms.

If WDI is floating, the watchdog is disabled by default. However, floating watchdog can be enabled through I2C

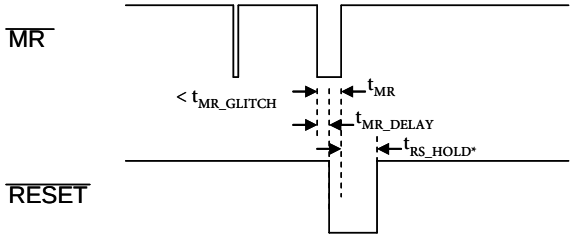
programming such that a broken WDI connection or any unusual condition that makes WDI float will trigger the reset.

Enabling or disabling floating WDI can be changed dynamically provided that the OTP fuse of such function is not programmed or the OTP overriden function is selected.

Manual Reset

Manual Reset $\overline{MR}$ is active low and it has an internal pull-up resistor to V_{3MON}. $\overline{MR}$ can be driven from a CMOS logic signal. The $\overline{MR}$ and $\overline{RESET}$ timing diagrams are shown in Figure 14. $\overline{MR}$ has the highest priority in triggering the $\overline{RESET}$ over any other monitoring inputs.

The default Watchdog Timeout is 1500ms. User should refer to Table 6b if they want to program a different setting.



•Programmable

Figure 14. Manual Reset Timing Diagrams

Outputs

Shutdown Generator

The shutdown output, $\overline{SHDN}$, is triggered by the abnormal inputs of V_{1MON} or V_{2MON}. It can also be the result of a failed watchdog input. $\overline{SHDN}$ control can also be asserted low by users through I2C programming at anytime.

To be explicit, the shutdown generator asserts a logic-low $\overline{SHDN}$ signal based on the following conditions:

1. During power-up.
2. When V_{1MON} goes over or under the threshold, Figure 5.
3. When V_{2MON} is below the turn-on threshold during the rising edge or the turn-off threshold during the falling edge in the default level sensitive mode, Figure 5.
4. When the external monitoring processor cannot issue the necessary WDI signal and an Advanced WDI mode is selected, Figures 8 and 9.
5. I2C programmed-shutdown.

The $\overline{SHDN}$ signal is released after the programmable hold time. The $\overline{SHDN}$ output is push-pull configured with I^2C selectable rail voltage of either V_{1MON} in default or internal V_{REG}. Figure 15 shows the $\overline{SHDN}$ output configurations, Pull-down resistor R1 ensures $\overline{SHDN}$ is pulled to ground when the AD5100 is not powered. When AD5100 is powered, M2a and M2b are both on. M2a has relatively lower impedance than M2b and R1 that the $\overline{SHDN}$ remains low at shutdown. When the AD5100 settles, sw1 will be on. M1 is stronger than M2a that $\overline{SHDN}$ will be pulled to the rail that makes AD5100 out of the shutdown mode.

The AD5100 is likely be used to monitor and control power regulators in some applications where some regulators have the input and enable pins next to each other in fine pitch that may pose reliability concern under some abnormal conditions. To prevent this may happen, the AD5100 shutdown output features a smart-load detection that ensures the shutdown to respond for maximum protection. For example, if the car battery has not been started for an extensive period of time and a resistive dendrite may have formed across the $\overline{SHDN}$ and the battery terminal (V_{1MON}), the dendrite will be blown immediately as the M2a is designed with adequate current sinking capability and remains in the on position to offer such protection. In another situation where the $\overline{SHDN}$ pin may be hard-shorted to any sub-30V source, the short-circuit detector will open sw2 and therefore limit the current by the high impedance M2b.

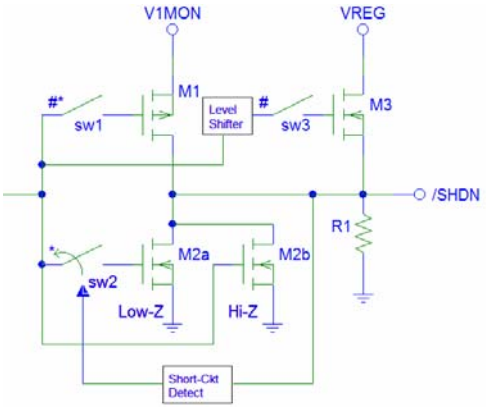


*Figure 15. Shutdown Output. # = I^2C Selectable, * = Default.*

Reset Generator

The Reset output, $\overline{RESET}$, is triggered by the abnormal input of V_{3MON} or V_{4MON}. $\overline{RESET}$ activation can also be the result of the processor that is not generating the proper watchdog signal or the Manual Reset is triggered.

To be explicit, the Reset generator asserts a logic-low $\overline{RESET}$ signal based on the following conditions

1. During power up
2. When V_{3MON} drops below the threshold, Figure 8.
3. When V_{4MON} drops below the threshold, Figure 10.
4. When $\overline{SHDN}$ output is asserted, Figures 5 and 13.
5. When the external monitoring processor cannot issue the necessary WDI signal, Figures 12 and 13.
6. When $\overline{MR}$ is asserted, Figure 14.

The $\overline{RESET}$ signal is asserted and maintained except when it is triggered by the WDI that will be described in the watchdog section. The $\overline{RESET}$ signal is released after the programmable hold time.

As shown in Figure 16, The $\overline{RESET}$ output is push-pull configured with the the rail voltage of V_{3MON}.

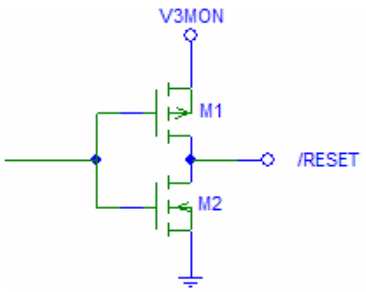


Figure 16. Reset Output.

Fault Detection with Shutdown Warning

An early shutdown warning is available for the system processor to identify the source of failure and take appropriate action before shuting down the external devices. Whenever the voltage at V_{1MON} is detected as over-voltage or under-voltage, or the voltage at V_{2MON} falls below the threshold, $\overline{SHDNWARN}$ outputs a logic 0. If the processor sees a logic-low on this pin, the processor may issue an I2C read command to identify the cause of failure reported in the Fault Detect/Status Register. The processor may store the information in the external EEPROM as a record of failure history.

V_{4OUT}

V_{4OUT} is an open-drain output triggered by V_{4MON} wth minimum propogation delay and the programmable delay does not apply. V_{4OUT} can be used as a PWM control over an external device or used as a monitoring signal. Most applications using V_{4OUT} require disabling V_{4MON} triggered reset with an I2C command.

Power Requirements

Internal Power

The AD5100 internal power V_{REG} is derived from V_{1MON} and V_{2MON} is used to turn AD5100 on and off with a different behavior depending on the V_{2MON} monitoring mode selection. By default, in the V_{2MON} level sensitive mode, the AD5100 turns on when the voltage at V_{2MON} rises above the logic threshold V_{2MON_ON}, When V_{2MON} falls below the logic threshold V_{2MON_OFF}, AD5100 will trun off 2 seconds after $\overline{SHDN}$ is deasserted. Note that AD5100 requries 5 us to start up and that V_{1MON} must be applied before V_{2MON}. The extension of the AD5100 turn-off attempts to allow the system to complete any housekeeping tasks before the system is powered off. Figure 17 shows the defaulted V_{2MON} and V_{REG} waveforms.

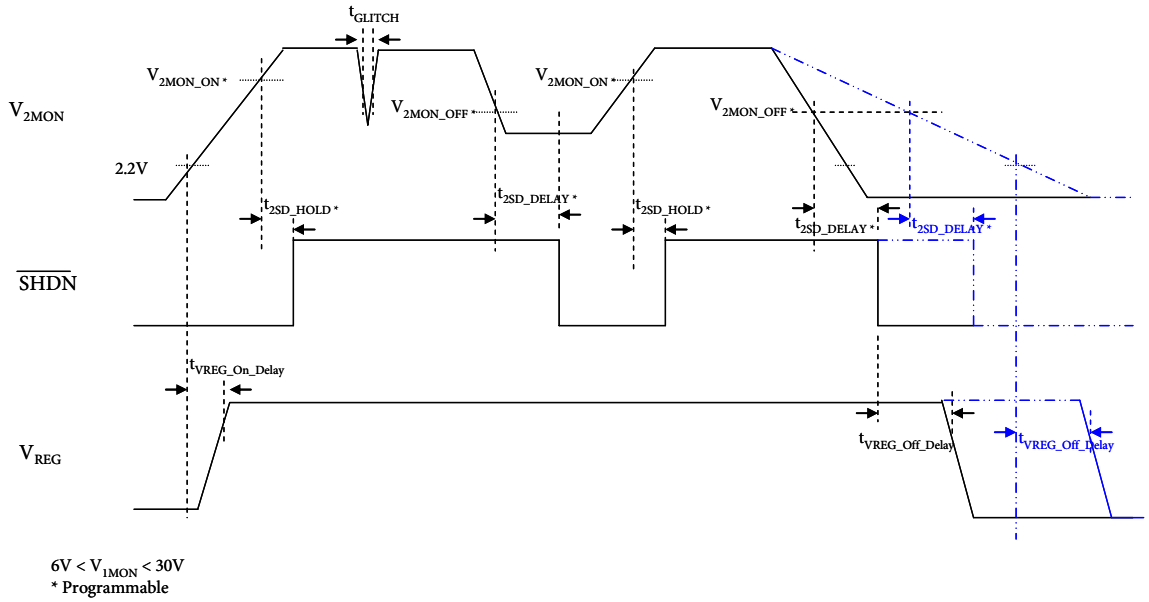


Figure 17. Internal Power V_{REG} versus V_{2MON} Timing Diagrams (Default)

If the Pulse-Sensitive V_{2MON} Mode is selected instead, the AD5100 will not turn off when V_{2MON} returns to a logic low. In this mode, once the part has been powered on, it can only be power-down by an I2C power down instruction or by eliminating the supply on V_{1MON} pin. This feature is for the applications that use a wake up signal.

V_{OTP}

A 6V supply voltage is needed only during OTP fuse programming. This voltage should be provided by an external source during factory programming and should have 6V/200mA driving capability. The OTP programming duration depends on the numbers of programming fuses with maximum duration of 10ms. V_{OTP} is not required for normal operation. The V_{OTP} has dual functions, it is used for programming the non-volatile memory fuse arrays as well as serving as a compensation network for internal power stability. As a result, a bypass capacitor must be connected at V_{OTP} pin at all times. A low ESR 10uF tantalum capacitor is recommended.

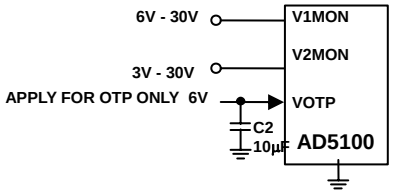


Figure 18. Power Supply Requirement

AD5100 achieves the OTP function through blowing internal fuses. Users should always apply the 6 V one-time program voltage requirement at the first fuse programming attempt. Failure to comply with this requirement may lead to a change in the fuse structures, rendering programming inoperable.

Care should be taken when SCL and SDA are driven from a low voltage logic driver.

Poor PCB layout introduces parasitic inductance that may affect the fuse programming voltage droop. Therefore, it is mandatory that a 10µF tantalum capacitor be placed as close as possible to the V_{OTP} pin. The value and the type of C2 chosen are important. It should provide both a fast response and larger supply current handling with minimum supply droop during programming, see Figure 18.

Protection

Over-Current Protection

If the V_{1MON} is shorted internally in the AD5100 to GND, the short-circuit protection kicks in and limits subsequent current to 150mA in normal operation or 50mA when the V_{OTP} is executed.

Thermal Shutdown

When the AD5100 junction temperature is near the junction temperature limit, it will automatically shutdown and cut out the power from V_{1MON}. The part will resume operational when the device junction temperature returns to normal.

For automotive applications, proper external protections on the AD5100 are needed in order to ensure reliable operation. The V_{1MON} will likely be used for battery monitoring. The V_{2MON} will likely be used for ignition switch or other critical inputs. As a result, these inputs may need additional protections such as EMI, loaddump, and ESD protections. In addition, battery input also requires reverse battery protection and short circuit fuse protection, see Figure 19.

ESD Protection

It is common to require a contact rating of ±8kV and a non-contact or air rating of ±15kV ESD protection for the automotive electronics. As a result, a ESD rated protection device must be used such as MMBV27VCL, a dual 40W TVS (Transient Voltage Suppressor) at the V_{1MON} and V_{2MON}.

Load Dump Protection

A load dump is a severe overvoltage surge that occurs when the car battery is being disconnected from a spinning alternator and the resulting long-duration, high-voltage surge introduced into the supply line. As a result, external load dump protection is recommended. Typically the load dump overvoltage lasts for few hundreds millisecond and peaks at around 40V to 70V while current can be as high as 1A. As a result, a load dump rated TVS D1 and D2 such as SMCJ17 are used to handle the surge energy. A series R is an in-line current limiting resistor, it should be adequate to limit the current without significant drop and yet small enough to not affect the input monitoring accuracy drop

Reverse Battery Protection

Reverse battery protection can be provided by a regular diode if the battery monitoring accuracy can be relaxed. Otherwise, a 60V P-Ch Power MOSFET, like NDT2955, can be used. Because of the MOSFET internal diode, the battery will first conduct through P1's body diode, as soon as the voltage reaches its source terminal, the voltage divider provides adequate gate-to-source voltage to turn on P1 and the voltage drop across the FET will be negligible. The resistor divider values are chosen such that the P1's maximum V_{GS} is not violated and the current drawn through the battery is only a few µA.

EMI Protection

For EMI protection, ferrite bead or EMC rated inductor such as DR331-7-103 can be used.

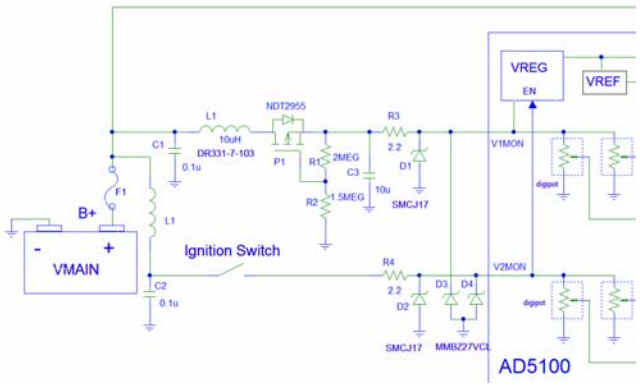


Figure 19. Protection Circuits

Digital Interface

All programmable parameters are set through a 2-wire I²C protocol with read/write access to the registers. All programmable parameters can be set permanently by blowing the OTP fuses at users' factories. Analog Devices offers device programming software, which effectively replaces the need for external I²C controllers or host processors for OTP programming in the factories.

SCL
Serial Input Register Clock Pin. Shifts in one bit at a time on positive clock edges. External 1k-2.2kΩ pull-up resistor is needed. The pull-up resistor should tie to V_{3MON} if it is used to monitor a sub-5V source.

SDA
Serial Data Input/Output Pin. Shifts in one bit at a time on positive clock edges. MSB loaded first. External 1k-2.2kΩ pull-up resistor is needed. The pull-up resistor should tie to V_{3MON} if it is used to monitor a sub-5V source.

AD0
I2C Slave Address Pin. AD5100 is a slave device that will communicate with a master if the AD0 bit in the protocol matches with the logic state of the AD5100's AD0 pin. Table 8 and Figure 20 show the example with two AD5100 devices operate on the same serial bus independently.

Table 8. Slave Address Decoding Scheme

AD0 Programming Bit	AD0 Device Pin	Device Addressed
0	0V	0x2E (U1)
1	5V	0x2F (U2)

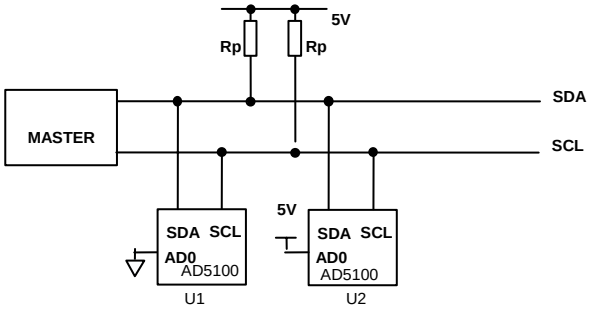


Figure 20. Two AD5100 Devices on One Bus

The master-device output bus-line drivers are open-drain pull-downs in a fully I²C compatible interface.

AD5100 Register Map

Table 9 outlines the Address Pointer Registers used to configure and control all parameters and functions in the AD5100. Table 10 shows the Address Pointer Register Structure. Table 9 also outlines if registers are writable, readable, or permanently settable. All registers are single-port, meaning they have the same address for read and write operations. The AD5100 ships from its manufacturing factory with default power-up values as listed in the last column. The user can experiment with different settings in the various threshold, delay and configuration registers. Once enough evaluation is done, the user can program their own power-up default values via a one time program (OTP) feature. When all desired settings have been programmed (or the user is satisfied with the manufacturers defaults), a lock-out bit can be set to prevent further/erroneous settings from being programmed.

Some users will use the AD5100 as a 'set and forget' device, i.e. program some default values and never need to change these over the life of the application. However some users will require 'On the Fly' flexibility, i.e. the ability to change settings to values other than those they choose as their defaults. An additional feature of the AD5100 is the ability to temporarily over-ride the OTP executed settings and still allows users to program the parts dynamically in the field. All over-ride values will revert back to OTP executed settings once the AD5100 is power cycled.

Register Writing, Reading, OTP & Over-Ride are explained later in the I2C section.

Table 9. AD5100 Register Map

Register Address	Read / Write	Permanently settable	Register Name & Bit Description	Pre-OTP Power On Default [1]
0x01	R/W	Y	**V_{1MON} Over-Voltage Threshold**	0x00
			[3:0] – 4 bits used to program V_{1MON} OV Threshold	(18.00 V)
			[7:4] – Reserved	
0x02	R/W	Y	**V_{1MON} Under-Voltage Threshold**	0x00
			[3:0] – 4 bits used to program V_{1MON} UV Threshold	(8.43 V)
			[7:4] – Reserved	
0x03	R/W	Y	**V_{2MON} Turn-On Threshold**	0x00
			[3:0] – 4 bits used to program V_{2MON} TON Threshold	(7.47 V)
			[7:4] – Reserved	
0x04	R/W	Y	**V_{2MON} Turn-Off Threshold**	0x00
			[3:0] – 4 bits used to program V_{2MON} TOFF Threshold	(6.95 V)
			[7:4] – Reserved	
0x05	R/W	Y	**V_{3MON} $\overline{\text{RESET}}$ Threshold**	0x00
			[2:0] – 3 bits used to program V_{3MON} $\overline{\text{RESET}}$ Threshold	(4.36 V)
			[7:3] – Reserved	
0x06	R/W	Y	**V_{4MON} $\overline{\text{RESET}}$ Threshold**	0x00
			[2:0] – 3 bits used to program V_{4MON} $\overline{\text{RESET}}$ Threshold	(Disabled)
			[7:3] – Reserved	
0x07	R/W	Y	**V_{1MON} OV/UV Triggered $\overline{\text{SHDN}}$ Hold**	0x00
			[2:0] – 3 bits used to program V_{1MON} OV/UV Triggered $\overline{\text{SHDN}}$ Hold time	(200 mS)
			[7:3] – Reserved	
0x08	R/W	Y	**V_{1MON} OV/UV Triggered $\overline{\text{SHDN}}$ Delay**	0x00
			[2:0] – 3 bits used to program V_{1MON} OV/UV Triggered $\overline{\text{SHDN}}$ Delay time	(1200 mS)
			[7:3] – Reserved	
0x09	R/W	Y	**V_{2MON} Turn-On Triggered $\overline{\text{SHDN}}$ Hold**	0x00
			[2:0] – 3 bits used to program V_{2MON} TON Triggered $\overline{\text{SHDN}}$ Hold time	(10 mS)
			[7:3] – Reserved	
0x0A	R/W	Y	**V_{2MON} Turn-Off Triggered $\overline{\text{SHDN}}$ Delay**	0x00
			[2:0] – 3 bits used to program V_{2MON} TOFF Triggered $\overline{\text{SHDN}}$ Delay time	(100 mS)
			[7:3] – Reserved	
0x0	R/	Y	**$\overline{\text{RESET}}$ Hold**	0x00

B	W		[2:0] – 3 bits used to program $\overline{\text{RESET}}$ Hold time	(200 mS)
			[7:3] – Reserved	
0x0C	R/W	Y	**Watchdog Timeout**	0x00
			[2:0] – 3 bits used to program Watchdog timeout time	(1500 mS)
			[7:3] – Reserved	
0x0D	R/W	Y	**$\overline{\text{RESET}}$ Configuration**	0x00
			[0] – 0 - $\overline{\text{RESET}}$ is active when $\overline{\text{SHDN}}$ is active	
			1 - $\overline{\text{RESET}}$ is not active when $\overline{\text{SHDN}}$ is active	
			[1] – Reserved	
			[2] – 0 - Enable V_{4MON} over threshold to cause $\overline{\text{RESET}}$	
			1 - Prevent V_{4MON} over threshold to cause $\overline{\text{RESET}}$ (For V_{4OUT} Application)	
			[3] – 0 - Prevent floating WDI to cause $\overline{\text{RESET}}$	
			1 - Enable floating WDI to cause $\overline{\text{RESET}}$	
			[7:4] – Reserved	
0x0E	R/W	Y	**$\overline{\text{SHDN}}$ Rail Voltage Configuration**	0x00
			[2:0] – Reserved	
			[3] – 0 - $\overline{\text{SHDN}}$ rail = V_{1MON}	
			1 - $\overline{\text{SHDN}}$ rail = Vreg	
			[7:4] – Reserved	
0x0F	R/W	Y	**Watchdog Mode**	0x00
			[2:0] – Reserved	
			[3] – 0 – Standard Mode	
			1 – Advanced Mode	
			[7:4] – Reserved	
0x15	R/W	Y	**Program Lock Fuse (Inhibit Further Programming)**	0x00
			[2:0] – Reserved	
			[3] – 0 – Fuse Programming allowed	
			1 – Fuse Programming Disabled	
			[7:4] – Reserved	
0x16	R/W	N	**Special Functions 1**	0x00
			[0] – 0 – OTP Enable A Inactive	
			1 – OTP Enable A Active	
			[1] – 0 - OTP Enable B Inactive	
			1 - OTP Enable B Active	
			[2] – 0 – Software assertion of $\overline{\text{SHDN}}$ Inactive	

			1 – Software assertion of $\overline{SHDN}$ Active	
			[3] – 0 - Over-ride of permanent settings Inactive	
			1 - Over-ride of permanent settings Active	
			[7:4] – Reserved	
0x17	R/W	N	**Special Functions 2**	0x00
			[0] – 0 – Software Power-down of AD5100 Inactive	
			1 – Software Power-down of AD5100 Active(2)	
			[7:1] – Reserved	
0x18	R/W	N	**Disable Special Functions (3)**	0x00
			[0] – 0 – Allow Over-ride Function	
			1 – Disable Further Over-ride Function	
			[1] – 0 – Allow OTP Function	
			1 – Disable OTP Function	
			[2] – 0 – Allow Manufacturer Test-modes	
			1 – Disable Manufacturer Test-modes	
			[3] – 0 – Allow Software power-down Function	
			1 - Disable Software power-down Function	
			[4] – 0 – Allow Software assertion of $\overline{SHDN}$ Function	
			1 – Disable Software assertion of $\overline{SHDN}$ Function	
			[7:5] – Reserved	
0x19	R-only	N	**Fault Detect & Status Register**	0x00
			[3:0] – These 4 level triggered bits indicate the current state of the comparators monitoring the V_{1MON} and V_{2MON} input pins.	
			[0] – A '1' indicates V_{2MON} input < V_{2MON} OFF Threshold	
			[1] – A '1' indicates V_{2MON} input > V_{2MON} ON Threshold	
			[2] – A '1' indicates V_{1MON} input < V_{1MON} UV Threshold	
			[3] – A '1' indicates V_{1MON} input > V_{1MON} OV Threshold	
			[6:4] – These are Fault Detection bits can be decoded to indicate one or more conditions were present when a $\overline{SHDN}$ event occurred. These bits are edge triggered.	
			000 – None	
			001 – V_{1MON} UV only	
			010 – V_{1MON} OV only	
			011 – Never Occur	
			100 – V_{2MON} Below OFF only	
			101 – V_{1MON} UV AND V_{2MON} Below OFF Both Occur	
			110 – V_{1MON} OV AND V_{2MON} Below OFF Both Occur	

	111 – Never Occur
	[7] – Reserved

Notes
1. Values AD5100 has when shipped from manufacturer's factory.
2. V_{2MON} must be 0V for Software Power down.
3. These register bits are set only. To clear them the AD5100 must be power cycled. In some cases the AD5100 may be connected to an I²C bus with lots of activity. Setting these bits is an added means of ensuring any erroneous activity on the bus does not cause AD5100 special functions to become active.

I2C Serial Interface

Control of the AD5100 is accomplished via an I²C compatible serial bus. The AD5100 is connected to this bus as a slave device (the AD5100 has no master capabilities).

The AD5100 has a 7-bit slave address. The six MSBs are 010111 and the LSB is determined by the state of the A0 pin. Therefore when A0 is low, the AD5100 slave address is 01011110 and 0101111 otherwise. Therefore the A0 pin allows the user to connect two AD5100s to the same I²C bus provided the two devices comply with the configurations shown in Figure 20.

The 2-wire serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, which is when SDA goes from high-to-low while SCL is high. The following byte is the slave address byte, which consists of the 7-bit slave address followed by an R/$\overline{W}$ bit which determines whether data is read from or written to the slave device
2. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an Acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL.
3. When all data bits have been read or written, a STOP condition is established by the master. A STOP condition is defined as a low-to-high transition on the SDA line while SCL is high. In write mode, the master pulls the SDA line high during the 10th clock pulse to establish a STOP condition. In the read mode, the master issues a no Acknowledge for the 9th clock pulse, (i.e., the SDA line remains high). The master then brings the SDA line low before the 10th clock pulse and then high during the 10th clock pulse to establish a STOP condition.

Writing Data to AD5100

When writing data to the AD5100, the user begins by writing an address byte followed by the R/$\overline{W}$ bit set to '0'. The AD5100 will acknowledge (if the correct address byte is used) by pulling the SDA line low during the 9th clock pulse. The user then

For the AD5100, write operations contain either one or two bytes, while read operations contain one byte. The AD5100 makes use of an **Address Pointer Register**. The Address Pointer Register does not have and does not require an address, because it is the register to which the first data byte of every write operation is written automatically. This data byte is an address pointer that sets up one of the other registers for the second byte of the write operation or for a subsequent read operation. Table 10 shows the structure of the Address Pointer Register. Bits [6:0] signify the address of the register that is to be written to or read from. Bit [7] is used when OTP mode is invoked (use of this bit is explained later in the OTP section), and should be '0' for normal write/read operations.

Table 10 – Address Pointer Register Structure

Bit #	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Function	OTP En	AP6	AP5	AP4	AP3	AP2	AP1	AP0

follows with two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the Address Pointer Register. The second byte is the data to be written to the internal data register. After each byte the AD5100 acknowledges by pulling the SDA line low during the 9th clock pulse. Figure 21 illustrated this operation.

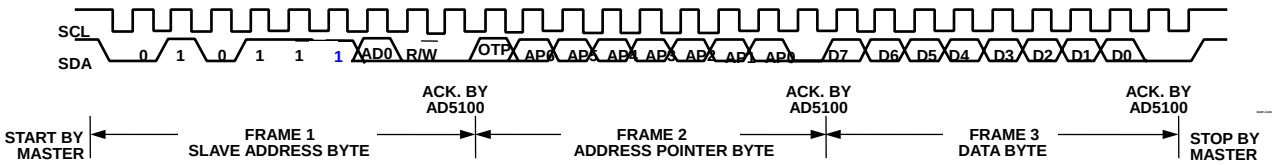


Figure 21 – Writing a register address to the Address Pointer Register, then writing data to the selected register

Reading Data from AD5100

When reading data from an AD5100 register there are two possibilities:

1. If the AD5100's Address Pointer Register value is unknown or not at the desired value, it is first necessary to set it to the correct value before data can be read from the desired data register. This is done by performing a write to the AD5100 as before, but only a value containing the register address is sent, because data is not to be written to the register. This is shown in Figure 22. A read operation is then performed consisting of the serial bus address, R/$\overline{W}$ bit set to '1', followed by the data byte from the data register. This is shown in Figure 23.
2. If the address pointer is known to be already at the desire address, data can be read from the corresponding data register without first writing to the Address Pointer Register.

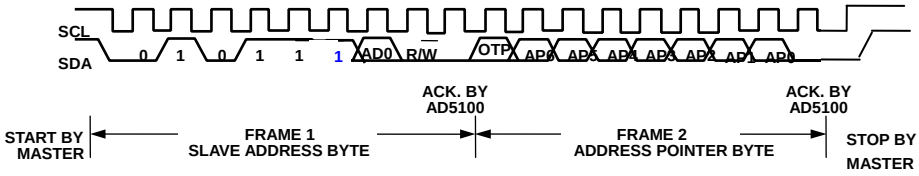


Figure 22. Dummy Write to set proper Address Pointer.

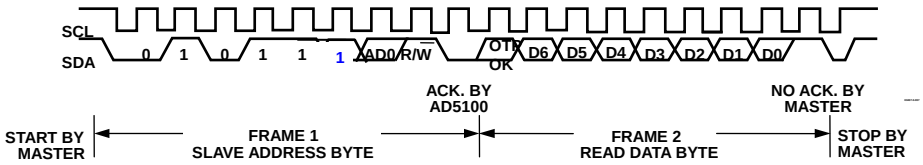


Figure 23. Read Data from the Address Pointer Register.

Table 11 shows the read-back data byte structure. Bits [6:0] contain the data from the register just read. Bit [7] only has significance when OTP mode is being used, and should be ignored for normal read operations. The majority of AD5100's registers are 4-bits wide, with only the Status/FDR Register and disable Special Function Register by 7 bit and 5 bits wide respectively.

Table 11 – Read-Back Data Byte Structure

Bit #	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Function	OTP Okay	D6	D5	D4	D3	D2	D1	D0

Permanent Setting of AD5100 Registers (OTP Function)

When the user wants to permanently program settings to the AD5100, the one time program (OTP) function is invoked. To complete a permanent program cycle for a particular register, the following sequence should be used:

1. Set bit [0] in register 0x16 using a normal write operation
2. Set bit [1] in register 0x16 using a normal write operation
3. Apply a 6V (200mA) voltage source to the OTP pin. This provides the current for the programming cycle.
4. Write the desired permanent data to the register of choice, using a write operation with the OTP bit set to '1' in the Address Pointer byte.

When the write cycle has been completed, the user should allow minimum of 30ms for the AD5100 to perform the permanent setting of the internal register. The user has the opportunity to check whether the AD5100 programmed correctly by performing a read cycle, and monitoring the state of bit [7] (**OTP Okay**).

OTP Okay = 1 indicates the AD5100 programmed correctly

OTP Okay = 0 indicates the AD5100 programmed incorrectly

Note: Read-back of the **OTP Okay** bit is only available for the read cycle following immediately after the program cycle. If a write or read of a different register is done immediately after the program cycle, then the opportunity for verifying if the programming was successful will have been missed. Figure 24 shows the recommended way of performing a program then read-back and verify of the V_{1MON} Over-Voltage Register, (assuming steps 1-3 above have already been done).

Programming Sequence	S	0x5C	A	0x01	A	0x8F	A	P	Delay	S	0x5D
Comment	Start	Slave Address + Write	Ack	Set V_{1MON} OV Threshold	Ack	OTP at setting 15	Ack	Stop	Wait for 30ms	Start	Slave Address + Read

Figure 24. Example of Executing OTP and a Successful Validation

When all default registers have been programmed, the lock bit should be set. User programmed defaults won't become active until the first power cycle after the lock bit is set. Programming the lock bit is done in exactly the same manner as all other registers.

Temporary Over-Ride of Default Settings (Over-Ride Function)

As stated previously in the register map section, even with the lock bit set, it is possible to temporarily over-ride the default values of any of the permanently programmable registers. To Over-Ride a permanent setting in a particular register, the following sequence should be used:

1. Set bit [3] in register 0x16 (Special Functions 1)
2. Write the desired temporary data to the register of choice

While the Over-Ride bit is set in register 0x18, the user may over-ride any registers they wish by simply writing to them with new data.

To revert an over-ridden register back to its default setting, the following sequence should be used:

1. Clear bit [3] in register 0x16
2. Write a dummy byte to the register of choice

Clearing the Over-Ride bit in register 0x18 does not cause all over-ridden registers to revert back to their defaults at the same time. For example, imagine the user had over-ridden registers 0x01, 0x02 & 0x03. If the user now cleared the Over-Ride bit in register 0x16 and wrote a dummy byte to register 0x01, it would revert back to its default value. However registers 0x02 & 0x03 would still contain their Over-Ride data. To revert both registers back to their defaults, the user must write dummy data to each register individually.

Power cycling the AD5100 will also revert all registers back to their programmed defaults.

Controlling the AD5100

There are two ways to control the AD5100. Users can apply the AD5100 evaluation software for one time programming the devices in the factory without ever reprogramming the parts in the fields. They can also design or make use of the on-board I^2C controllers for programming the AD5100. The later is necessary for any dynamic or field programming applications.

APPLICATIONS

Car Battery and Infotainment System Supply Monitoring

The AD5100 has two high-voltage monitoring inputs with shutdown and reset controls over external devices. For example, the V_{1MON} and V_{2MON} can be used to monitor the signals from a car battery and an ignition key in an automobile, respectively. Such application is shown in Figure 25. The shutdown output can be connected to the shutdown pin of an external regulator to prevent false conditions such as a weak battery or overcharging battery by an alternator. The reset output can be used to reset the processor in the event of a hardware or software malfunction. An example of the input and output responses of this circuit is shown in Figure 26.

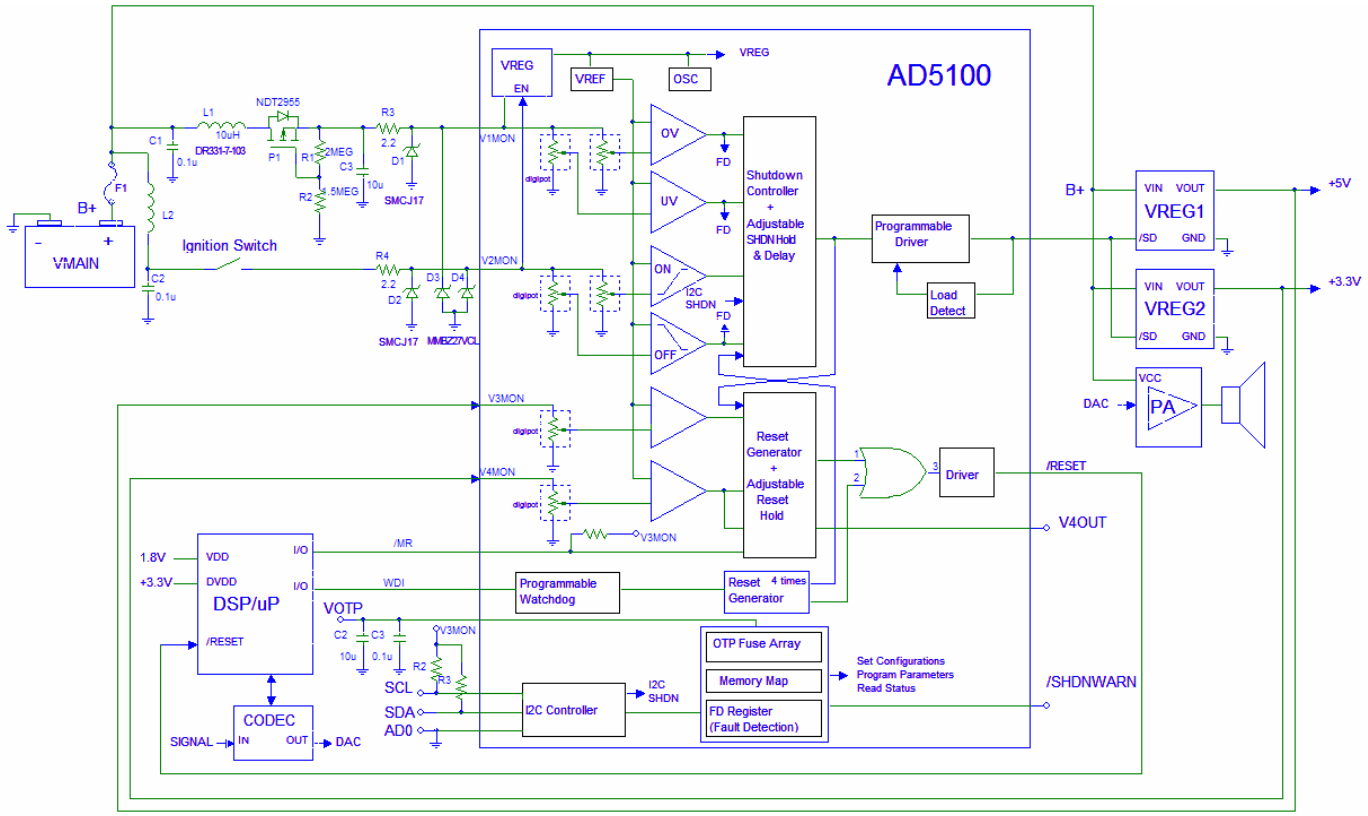


Figure 25. Typical DSP in Car Infotainment Application.

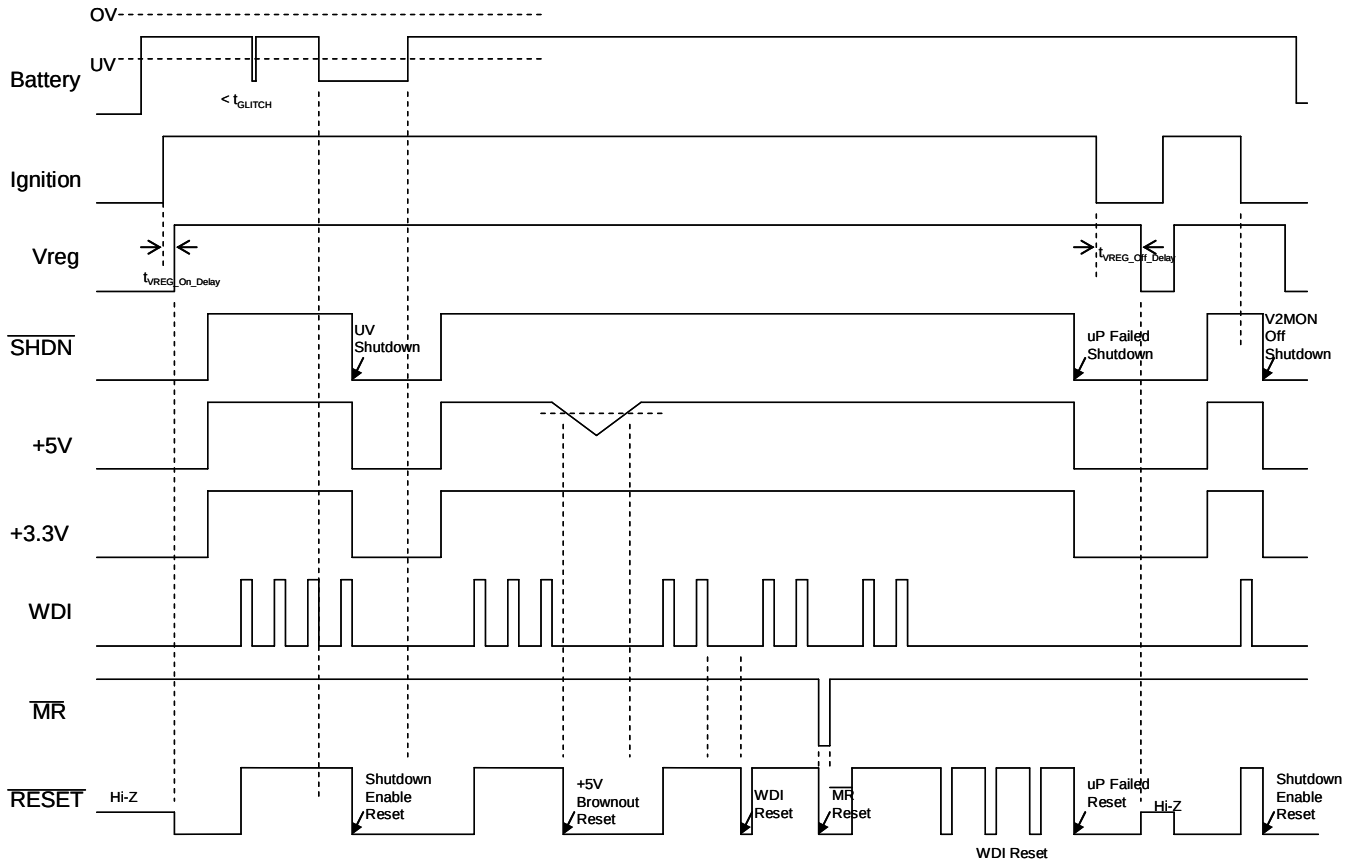


Figure 26. Examples of $\overline{\text{SHDN}}$ *and* $\overline{\text{RESET}}$ *Responses of circuit shown in Figure 25.*

Battery Monitoring with Fan Control

V_{4MON} can be used with V_{4OUT} intandem to form a simple PWM control circuit. For example as shown in Figure 27, when a temperature sensor output connects to the V_{4MON} input, with the proper threshold level set, V_{4OUT} outputs high whenever the temperature goes above the threshold. This turns on the FET switch which activates the fan. When Vtemp drops below the threshold, V_{4OUT} decreases which turns off the fan.

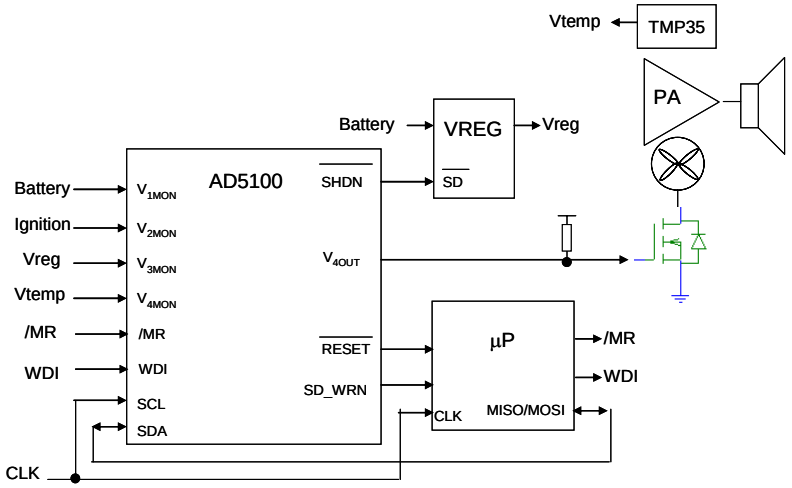


Figure 27. Power Amp Monitoring and Fan Control

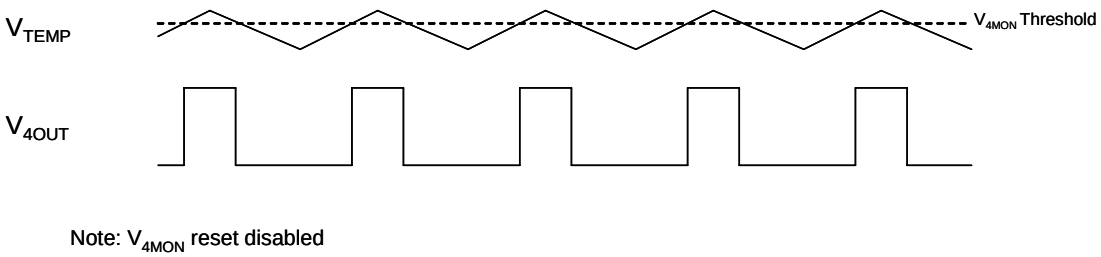


Figure 28. V_{4OUT} with respect to Vtemp withV_{4MON} reset disabled in circuit shown in Figure 27.

Battery State of Charge Indicator and Shutdown Early Warning Monitoring

In the automotive application, the system designer may set the battery threshold to the lowest level in order to allow an automobile to start at the worst case condition. If the battery remains at the low voltage level, it is indeed a poor battery. However, there is no way to warn the driver. As a result, the system designer may use V_{4OUT} as the battery warning indicator. By stepping down the battery voltage monitored at V_{4MON}, the LED is lit which gives a battery replacement warning. The circuit is shown in Figure 29.

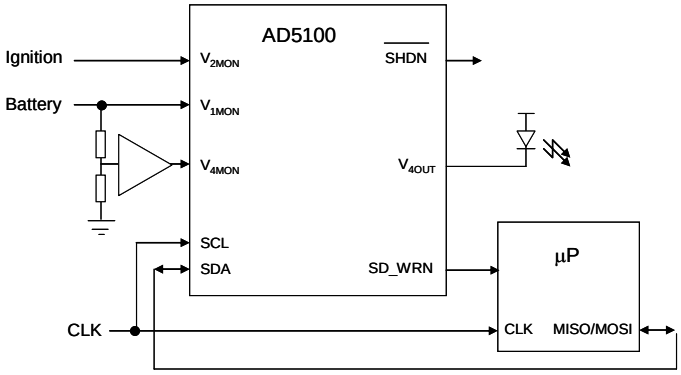


Figure 29. Battery State of Charge Indication

Psuedo CAN Bus Wake Up Mode

Using the AD5100 as indicated in Figure 30, the microprocessor can control its own power down sequence using the CAN Bus wake up signal. The operator must select the last setting 'Rising Edge Trigger/CAN wake up mode' in the V_{2MON} Turn Off Threshold parameter (The I2C write command is S 01011100 A 00000100 A 00001001 A P).

Now when the rising edge of the CAN Bus wake up signal is detected by V_{2MON}, the AD5100 is powered up with shutdown pulls high. The external regulator is turned on to supply power to the microprocessor. A reset pulse train will be generated at the reset output if there is no watchdog activity. The pulse continues until the correct watchdog signal appears at the AD5100 WDI pin. The shutdown pin remains high as long as the AD5100 continues to receive the correct watchdog signal.

When the microprocessor finishes its housekeeping tasks or powers down the software rountine, it stops sending a watchdog signal. In response, the AD5100 generates a reset. The shutdown pin will be pulled low 2 seconds after and the regulator output drops to 0V, which shuts down the microprocessor. At that point, the AD5100 goes into sleep mode.

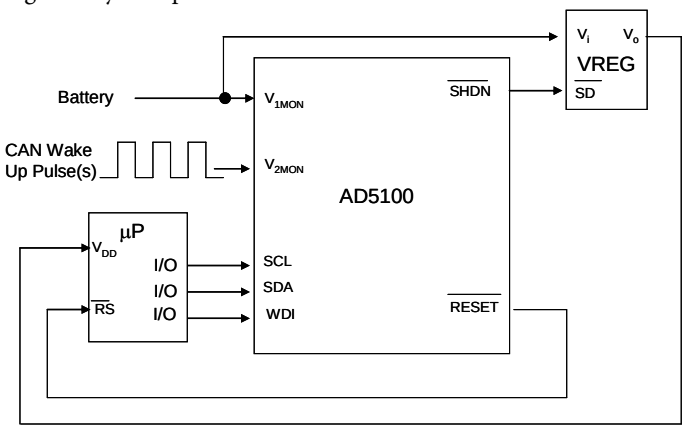
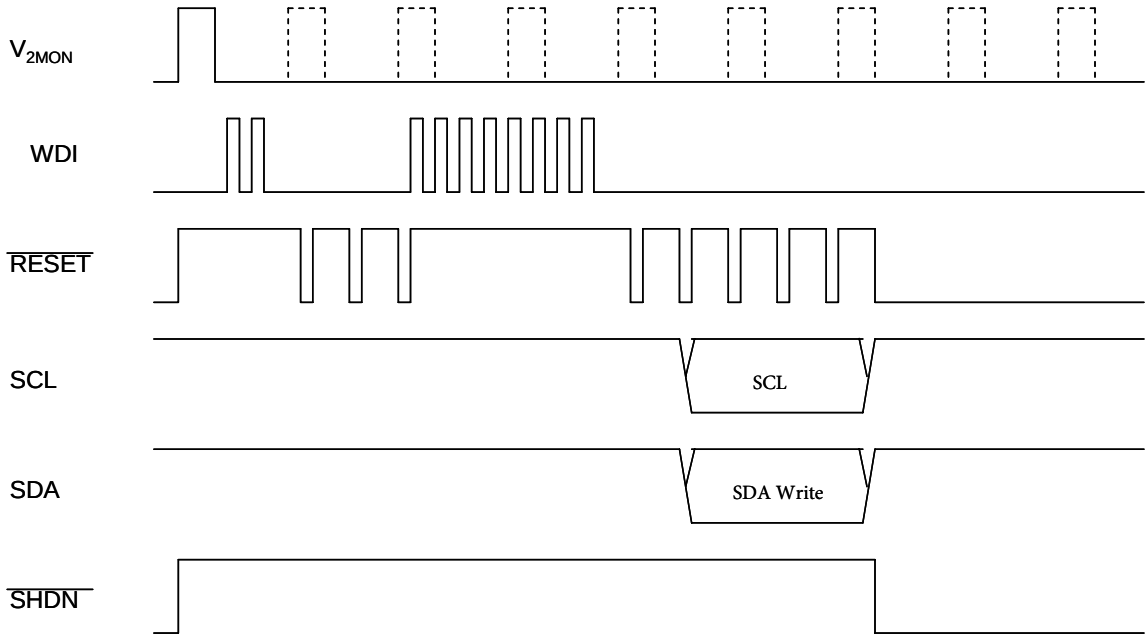


Figure 30. CAN Wake Up Mode



Notes
•6V < V_{1MON} < 30V
•Select V_{2MON_OFF} = Rising Edge Trigger/CAN wake up mode

Figure 31. CAN Bus operation of circuit shown in Figure 30.

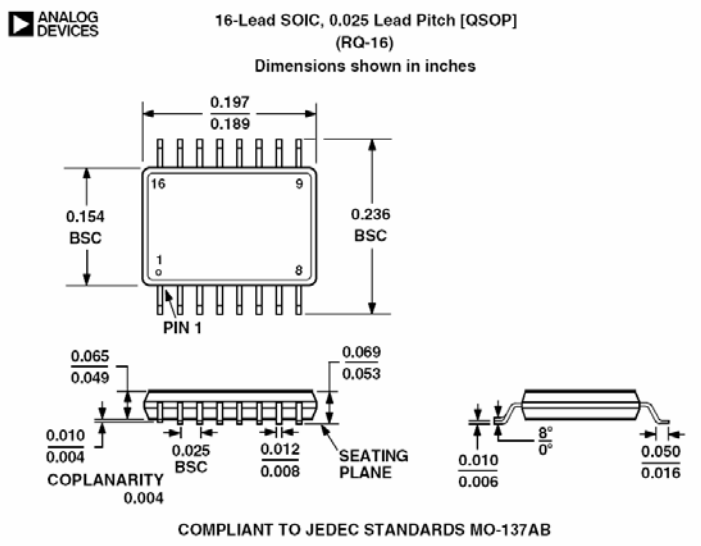


Figure 32. QSOP-16 Mechanical Dimension

ORDERING GUIDE

Model	Temperature Range	Package Code	Package Description	Full Container Quantity	Branding
AD5100YRQZ-RL7[1]	–40°C to +125°C	RQ-16	QSOP-16	1,000	TBD
A AD5100YRQZ[1]	–40°C to +125°C	RQ-16	QSOP-16	98	TBD
AD5100EVAL			Evaluation Board	1	

[1] Z = Pb-free part.

PR05692-0-2/06(PrJ)