F-MOD - 250 MHz to 4000 MHz Quadrature Modulator Family

Preliminary Technical Data

ADL5370/1/2/3/4

FEATURES

Output frequency range: 250 MHz to 4000 MHz
Modulation bandwidth: 700 MHz (3 dB)
1 dB output compression: 12 dBm @ 2140 MHz
Noise floor: -158 dBm/Hz
Sideband Suppression: < -40 dBc
LO Leakage: < - 40 dBm
Single supply: 4.75 V to 5.5 V
24-Lead LFCSP package

APPLICATIONS

Cellular/PCS communication systems infrastructure
WCDMA/CDMA2000/GSM/EDGE, WiMax
Wi-Max/broadband wireless access systems

FUNCTIONAL BLOCK DIAGRAM

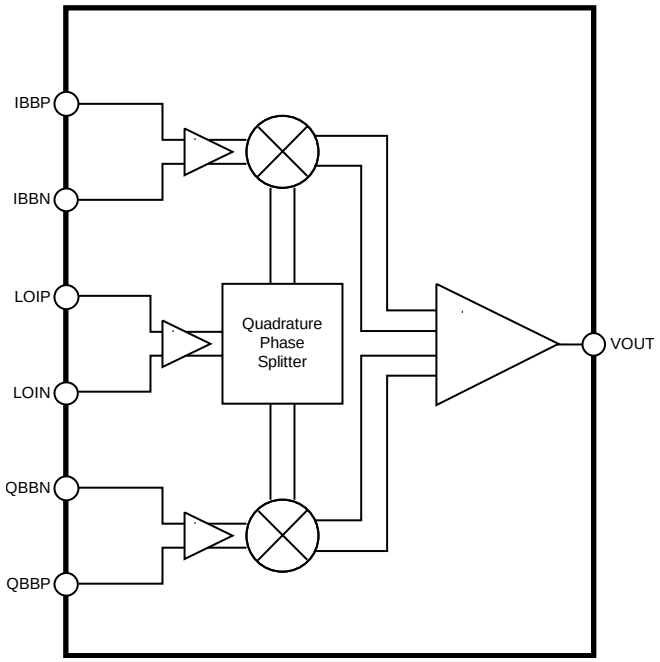

Figure 1.

PRODUCT DESCRIPTION

The F-MOD family of monolithic, RF quadrature modulators is designed for use from 250 MHz to 4000 MHz. Excellent phase accuracy and amplitude balance enable high performance direct RF modulation for communication systems.

The F-MOD family can be used as direct-to-RF modulators in digital communication systems such as GSM, CDMA, and WCDMA base stations, and QPSK or QAM broadband wireless access transmitters. A 700 MHz 3 dB baseband bandwidth makes it ideal in broadband Zero-IF or Low-IF-to-RF applications and in broadband Digital Pre-Distortion transmitters.

The F-MOD family is fabricated using Analog Devices' advanced Silicon-Germanium bipolar process, and are available in a 24-lead exposed-paddle LFCSP package. Performance is specified over a –40°C to +85°C temperature range.

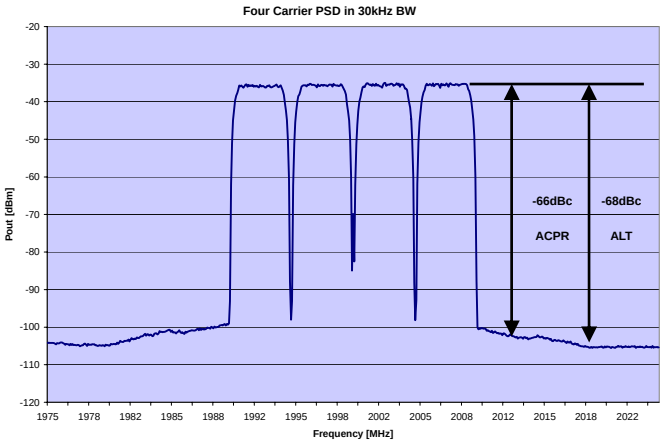

Figure 2. ADL5372 Four Carrier WCDMA Spectrum @ 2 GHz, -14.5 dBm per Carrier

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SPECIFICATIONS

Table 1. V_S = 5 V; Ambient Temperature (T_A) = 25°C; LO = 0 dBm[1]; I/Q inputs = 1.4 V p-p differential sine waves in quadrature on a 500 mV dc bias; baseband frequency = 1 MHz, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Unit
Operating Frequency Range	Frequency Range covered by F-Mod family				MHz
	Low Frequency		250		
	High Frequency		4000		MHz
ADL5370	LO = 450 MHz				
Operating Frequency Range	Range over which Uncompensated Sideband Suppression < -30 dBc				
	Low Frequency		250		MHz
	High Frequency		1300		MHz
Output Power	V_{IQ}=1.4V pp differential		5.6		dBm
Output P1 dB			10.5		dBm
Carrier Feedthrough			-54.6		dBm
Sideband Suppression			-43.4		dBc
Second Harmonic	$P_{OUT} – (F_{LO} + (2 \times F_{BB}))$, P_{OUT} = 7 dBm		-59.8		dBc
Third Harmonic	$P_{OUT} – (F_{LO} + (3 \times F_{BB}))$, P_{OUT} = 7 dBm		-54.8		dBc
Output IP3	$F1_{BB}$ = 3 MHz, $F2_{BB}$ = 4 MHz, P_{OUT} = -2 dBm per tone		23		dBm
Noise Floor	Baseband inputs biased to 500 mV; P_{LO} = +0 dBm		-156		dBm/Hz
GSM	F_{LO} = 380 MHz, 6 MHz carrier offset, P_{OUT} = +6 dBm, P_{LO} = +3 dBm		-154		dBc/Hz
ADL5371	LO = 900 MHz				
Operating Frequency Range	Range over which Output P1dB > 10 dBm				
	Low Frequency		700		MHz
	High Frequency		1300		MHz
Output Power	V_{IQ}=1.4Vpp differential		6.8		dBm
Output P1 dB			13.5		dBm
Carrier Feedthrough			-52.2		dBm
Sideband Suppression			-61.7		dBc
Second Harmonic	$P_{OUT} – (F_{LO} + (2 \times F_{BB}))$, P_{OUT} = 7 dBm		-56.8		dBc
Third Harmonic	$P_{OUT} – (F_{LO} + (3 \times F_{BB}))$, P_{OUT} = 7 dBm		-51.1		dBc
Output IP3	$F1_{BB}$ = 3 MHz, $F2_{BB}$ = 4 MHz, P_{OUT} = -2 dBm per tone		26		dBm
Noise Floor	Baseband inputs biased to 500 mV; P_{LO} = +6 dBm		-156		dBm/Hz
GSM	F_{LO} = 885 MHz, 6 MHz carrier offset, P_{OUT} = +7 dBm, P_{LO} = +6 dBm		-158		dBc/Hz
ADL5372	LO = 1900 MHz, 2140 MHz				
Operating Frequency Range	Range over which Output P1dB > 10 dBm				
	Low Frequency		1600		MHz
	High Frequency		2400		MHz
Output Power	V_{IQ}=1.4Vpp differential		6.4		dBm
Output P1 dB			12		dBm
Carrier Feedthrough			-44		dBm
Sideband Suppression			-41.5		dBc
Second Harmonic	$P_{OUT} – (F_{LO} + (2 \times F_{BB}))$, P_{OUT} = 7 dBm		-48		dBc
Third Harmonic	$P_{OUT} – (F_{LO} + (3 \times F_{BB}))$, P_{OUT} = 7 dBm		-49		dBc
Output IP3	$F1_{BB}$ = 3 MHz, $F2_{BB}$ = 4 MHz, P_{OUT} = -2 dBm per tone		26		dBm
Noise Floor	Baseband inputs biased to 500 mV; P_{LO} = +6 dBm		-158		dBm/Hz
WCDMA	Single Carrier WCDMA, 20 MHz Carrier Offset, Pout=-10 dBm, P_{LO}= 0 dBm		-156		dBm/Hz
GSM	F_{LO} = 1900 MHz, 6 MHz carrier offset, P_{OUT} = +9dBm, P_{LO} = +6 dBm		-158		dBc/Hz
WCDMA ACPR	Single Carrier, Test Model 1-64, Pout = -10 dBm, P_{LO} = 0 dBm		-75		dBc
	Four Carrier, Test Model 1-64, Pout (total) = -10 dBm, P_{LO} = 0 dBm		-65		dBc

Parameter	Conditions	Min	Typ	Max	Unit
ADL5373	LO = 2500 MHz				
Operating Frequency Range					
	Low Frequency (3dB Bandwidth)		2300		MHz
	High Frequency		3000		MHz
Output Power	V_{IQ}=1.4Vpp differential		6.5		dBm
Output P1 dB			13		dBm
Carrier Feedthrough			-34.5		dBm
Sideband Suppression			-33.3		dBc
Second Harmonic	$P_{OUT} - (F_{LO} + (2 \times F_{BB}))$, P_{OUT} = 7 dBm		-48.8		dBc
Third Harmonic	$P_{OUT} - (F_{LO} + (3 \times F_{BB}))$, P_{OUT} = 7 dBm		-45.4		dBc
Output IP3	$F1_{BB}$ = 3 MHz, $F2_{BB}$ = 4 MHz, P_{OUT} = -3 dBm per tone		25		dBm
Noise Floor	Baseband inputs biased to 500 mV, P_{LO} = +6 dBm		156		dBm/Hz
ADL5374	LO = 3500 MHz				
Operating Frequency Range					
	Low Frequency (3 dB Bandwidth)		2800		MHz
	High Frequency		4000		MHz
Output Power	V_{IQ}=1.4Vpp differential		4.8		dBm
Output P1 dB			11		dBm
Carrier Feedthrough			-32.1		dBm
Sideband Suppression			-35.9		dBc
Second Harmonic	$P_{OUT} - (F_{LO} + (2 \times F_{BB}))$, P_{OUT} = 7 dBm		-36.9		dBc
Third Harmonic	$P_{OUT} - (F_{LO} + (3 \times F_{BB}))$, P_{OUT} = 7 dBm		-43.1		dBc
Output IP3	$F1_{BB}$ = 3 MHz, $F2_{BB}$ = 4 MHz, P_{OUT} = -3 dBm per tone		21.5		dBm
Noise Floor	Baseband inputs biased to 500 mV, P_{LO} = +6 dBm		155		dBm/Hz
LO INPUTS					
LO Drive Level[1]	Characterization performed at typical level	-3	0	3	dBm
Nominal Impedance			50		Ω
Input Return Loss				-10	dB
BASEBAND INPUTS	Pins IBBP, IBBN, QBBP, QBBN				
I and Q Input Bias Level		400	500	600	mV
Bandwidth (3 dB)			700		MHz
POWER SUPPLIES	Pins VPS1 and VPS2				
Voltage		4.75		5.5	V
Supply Current	ADL5370		210		
	ADL5371, ADL5372, ADL5373, ADL5374		175		mA

Notes

1 LO drive in excess of +3 dBm can be provided to further reduce noise at 6 MHz and 20 MHz carrier offsets in GSM and WCDMA applications respectively.

ABSOLUTE MAXIMUM RATINGS

Table 2. F-MOD Absolute Maximum Ratings

Parameter	Rating
Supply Voltage VPOS	5.5 V
IBBP, IBBN, QBBP, QBBN	0 V, 2.5 V
LOIP and LOIN	10 dBm
Internal Power Dissipation	800 mW
θ_{JA} (Exposed Paddle Soldered Down)	30°C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

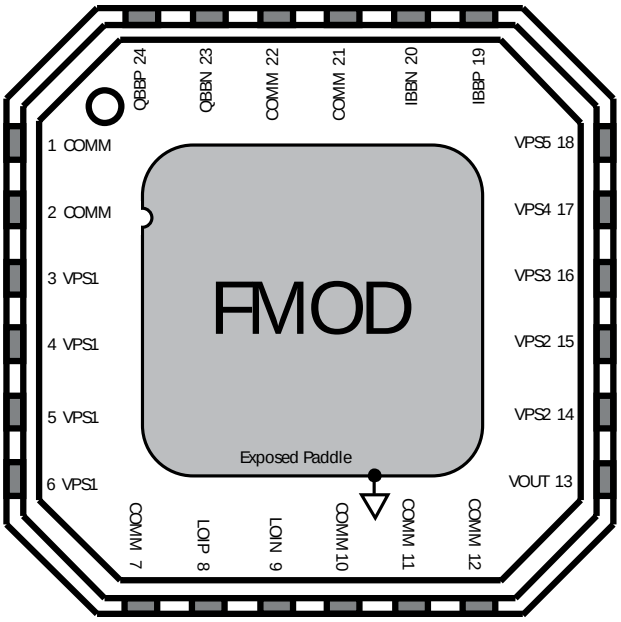

Figure 2.

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1,2,7,10,11,12,21,22	COMM	Input Common Pins. Connect to ground plan via a low impedance path
3,4,5,6,14,15,16,17,18	VPS1,VPS2, VPS3,VPS4,VPS5	Positive Supply Voltage pins. All pins should be connected to the same supply. To ensure adequate external bypassing, connect 0.1 µF capacitors between each pin and ground. Adjacent power supply pins of the same name can share one capacitor (see evaluation board schematic).
19,20,23,24	IBBP,IBBN, QBBN,QBBP	Differential In-Phase and Quadrature Baseband Inputs. These high impedance inputs must be dc-biased to approximately 500 mV dc, and must be driven from a low impedance source. Nominal characterized ac signal swing is 700 mV p-p on each pin. This results in a differential drive of 1.4 V p-p with a 500 mV dc bias. These inputs are not self-biased and must be externally biased.
8,9	LOIP, LOIN	50 Ω Single-Ended Local Oscillator Input. Internally dc-biased. Pins must be ac-coupled. AC-couple LOIN to ground and drive LO through LOIP.
13	VOUT	Device Output. Single-ended, 50 Ω internally biased RF output. Pin must be ac-coupled to the load.
	Exposed Paddle	Connect to ground plan via a low impedance path

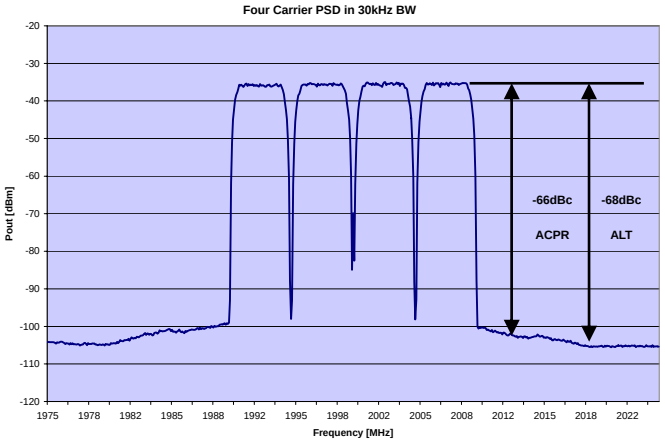

Figure 3. ADL5372 Four Carrier WCDMA Spectrum (Test Model 1-64) @ 2 GHz, -14.5 dBm per Carrier, ACPR = -66 dBc, Zero IF

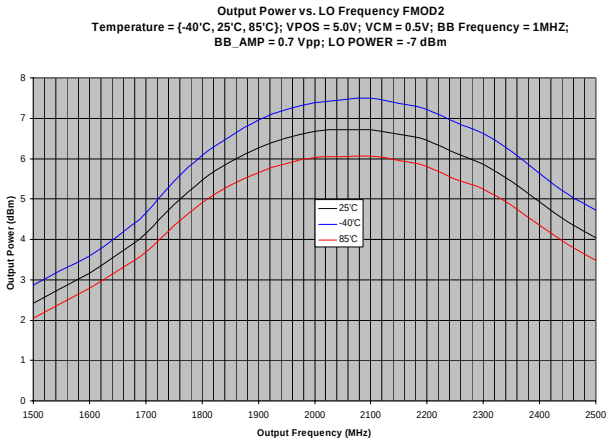

Figure 6. ADL5372 Output Power vs. Frequency and Temperature. Baseband drive is 1.4 Vpp differential

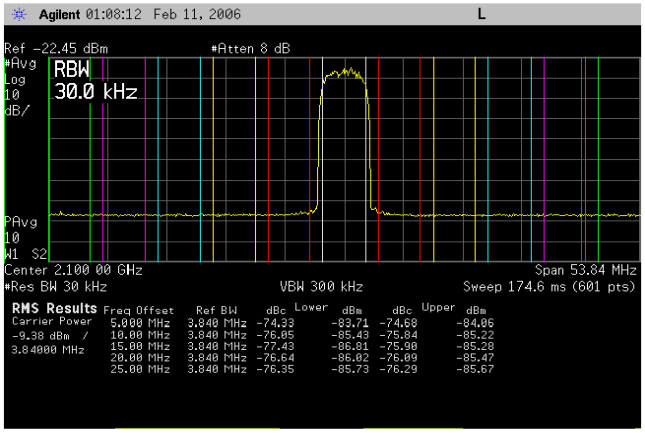

Figure 4. ADL5372 Single Carrier WCDMA Spectrum(Test Model 1-64) @ 2.1 GHz, Pout = -9.4 dBm, ACPR = -75 dBc, Baseband drive from AD9779 Dual DAC, Zero IF

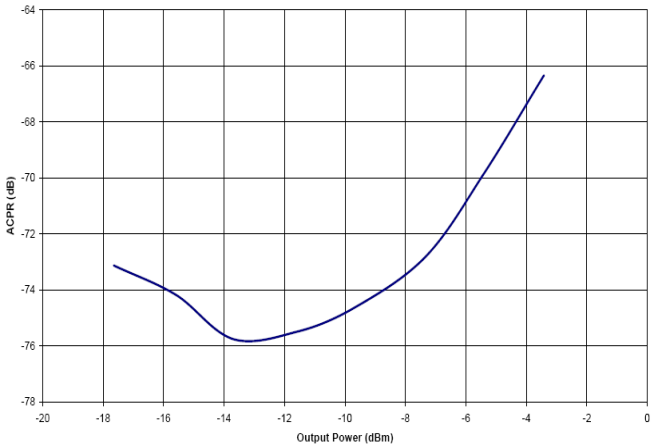

Figure 7. ADL5372 WCDMA Single Carrier 64-Users ACPR versus Output Power at 2140 MHz, Plo=+3dBm, Zero IF

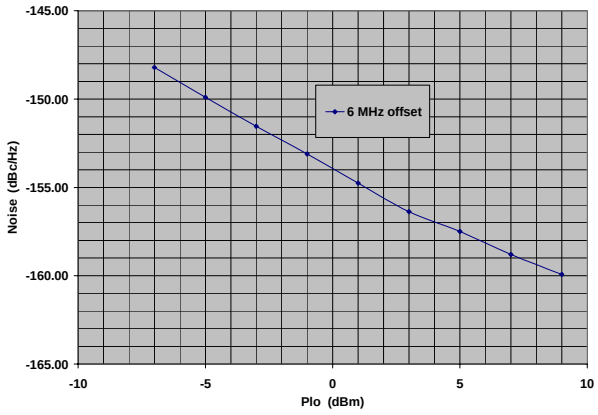

Figure 5. ADL5371 GSM Noise at 900 MHz vs. LO Drive, 6 MHz Carrier Offset. Pout = +5 dBm

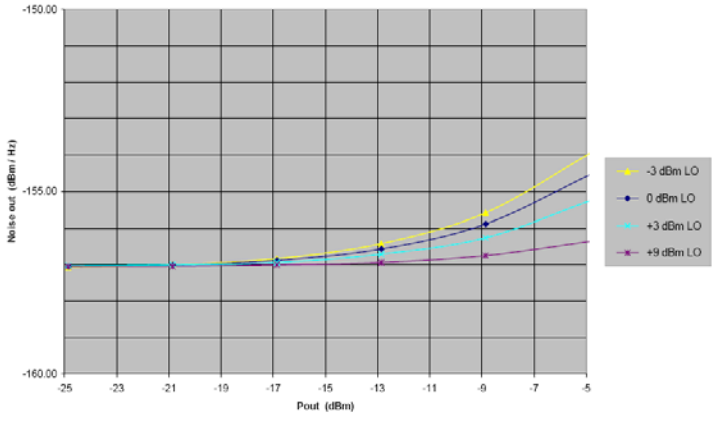

Figure 4. ADL5372 Single Carrier WCDMA Noise at 1.96 GHz, 50-MHz carrier offset,Test Model 1-64, Zero IF

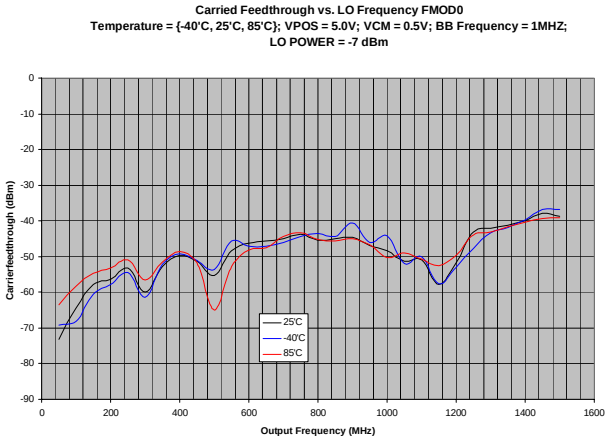

Figure 9. ADL5370 Uncalibrated Carrier Feed through

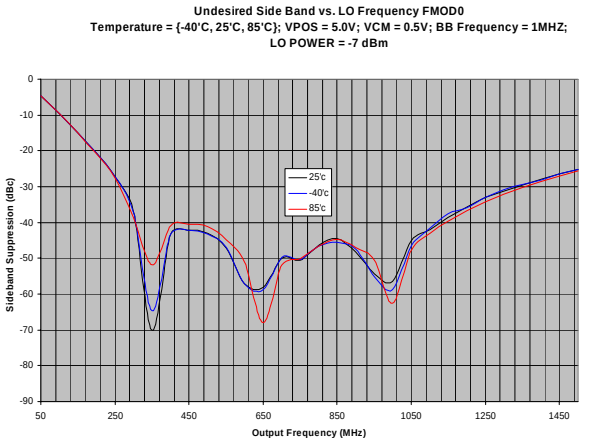

Figure 10. ADL5370 Uncalibrated Undesired Side band

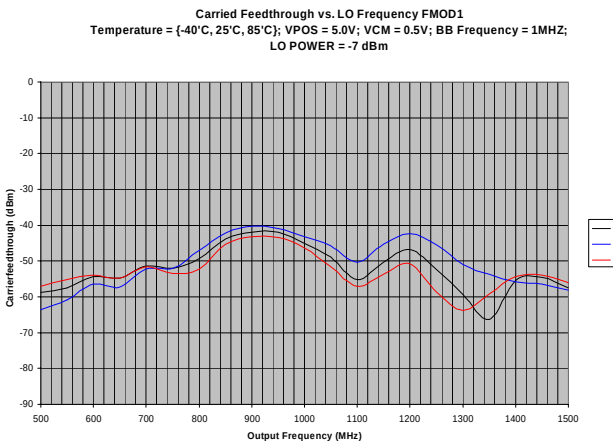

Figure 11. ADL5371 Uncalibrated Carrier Feed through

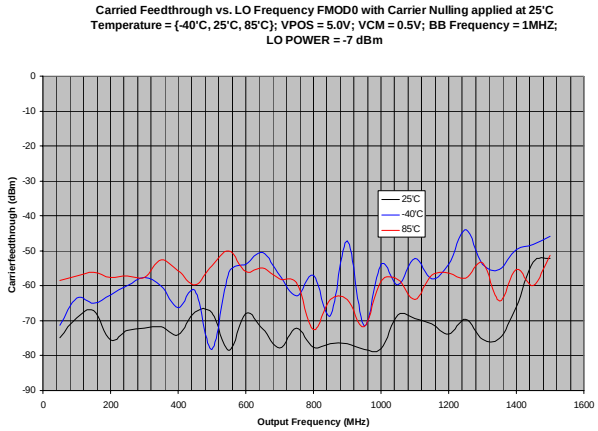

Figure 12. ADL5370 Carrier Feed through with Nulling at 25C

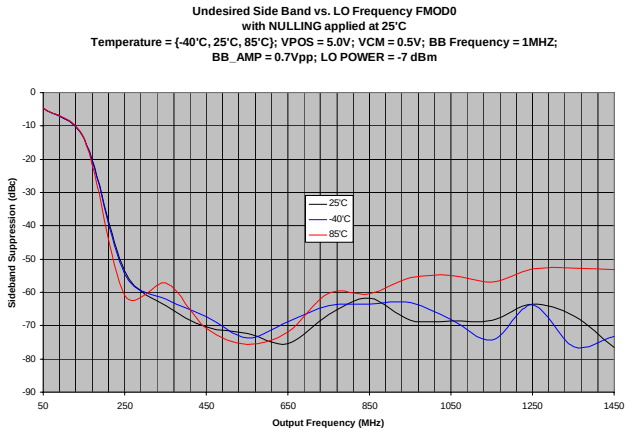

Figure 13. ADL5370 Undesired Sideband with Nulling at 25C

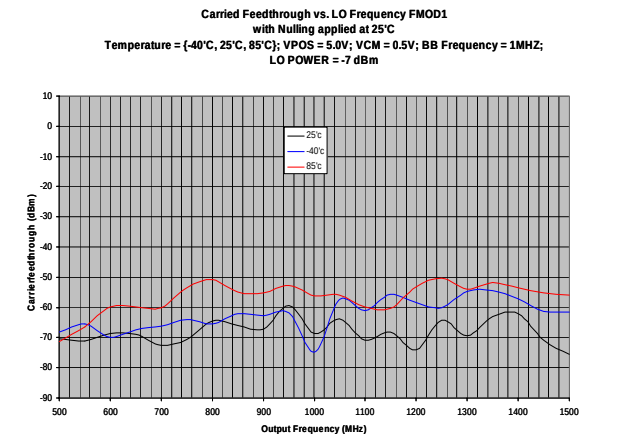

Figure 14. ADL5371 Carrier Feed through with Nulling at 25C

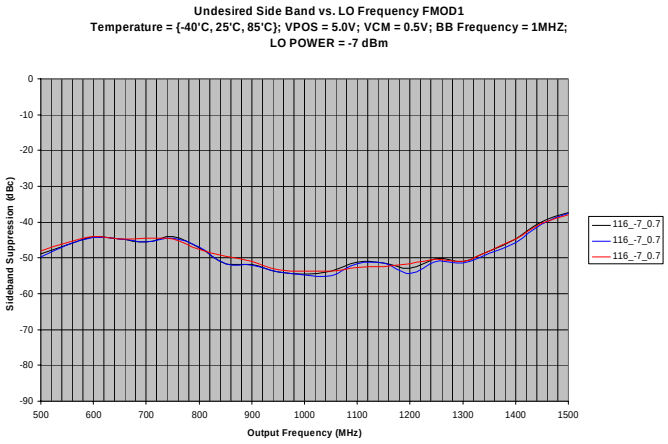

Figure 15. ADL5371 Uncalibrated Undesired Side band

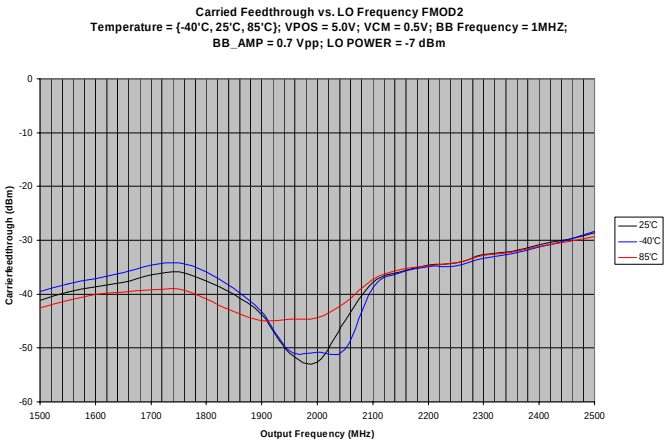

Figure 16. ADL5372 Uncalibrated Carrier Feed through

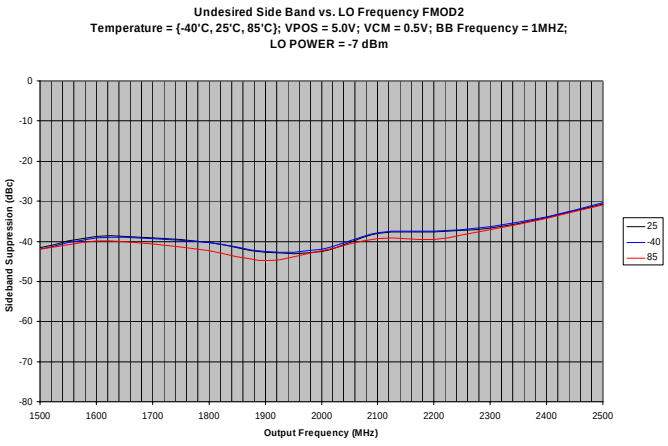

Figure 17. ADL5372 Uncalibrated Undesired Side band

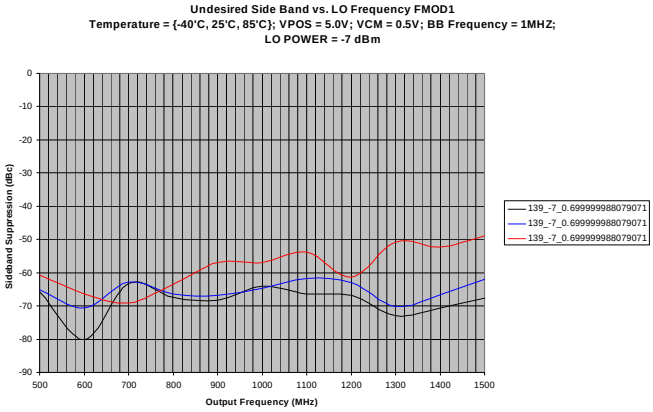

Figure 18. ADL5371 Undesired Sideband with Nulling at 25C

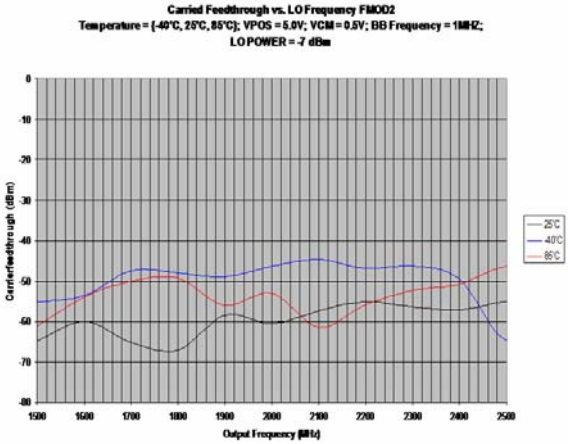

Figure 19. ADL5372 Carrier Feed through with Nulling at 25C

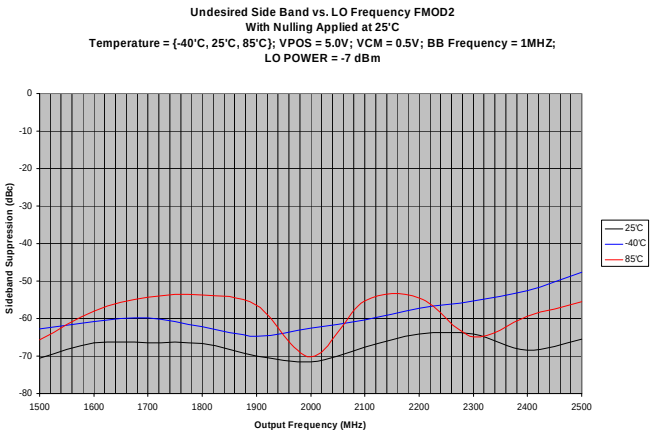

Figure 20. ADL5372 Undesired Sideband with Nulling at 25C

BASIC CONNECTIONS

Refer to the evaluation board schematic for the basic connections for operating the F-MOD family.

A single power supply of between 4.75 V and 5.5 V is applied to pins VPS1 and VPS2 and VPS3. All the VPS pins must be connected to the same potential. Adjacent pins of the same name can be tied together and decoupled with a 0.1 uF capacitor. These capacitors should be located as close as possible to the device.

All the COMM pins should be tied to the same ground plane through low impedance paths. The exposed paddle on the under side of the package should also be soldered to a low impedance ground plane. If multiple ground planes exist on the circuit board, these should be stitched together with multiple (typically 9) vias to enhance thermal and electrical performance.

The baseband inputs QBBP, QBBN, IBBP and IBBN must be driven from a differential source. The nominal drive level of 1.4 Vpp differential (700 mVpp on each pin) should be biased at 500 mV.

A Single–ended Local Oscillator signal should be applied to the LOIP pin through an ac-coupling capacitor. The recommended LO drive power is 0 dBm. The LO return pin, LOIN, should be ac-coupled to ground though a low impedance path.

The RF output is available at the VOUT pin (Pin 7). This pin must also be ac-coupled. Both LOIP and VOUT have nominal broadband input and output impedances of 50 Ω and do not need further external matching.

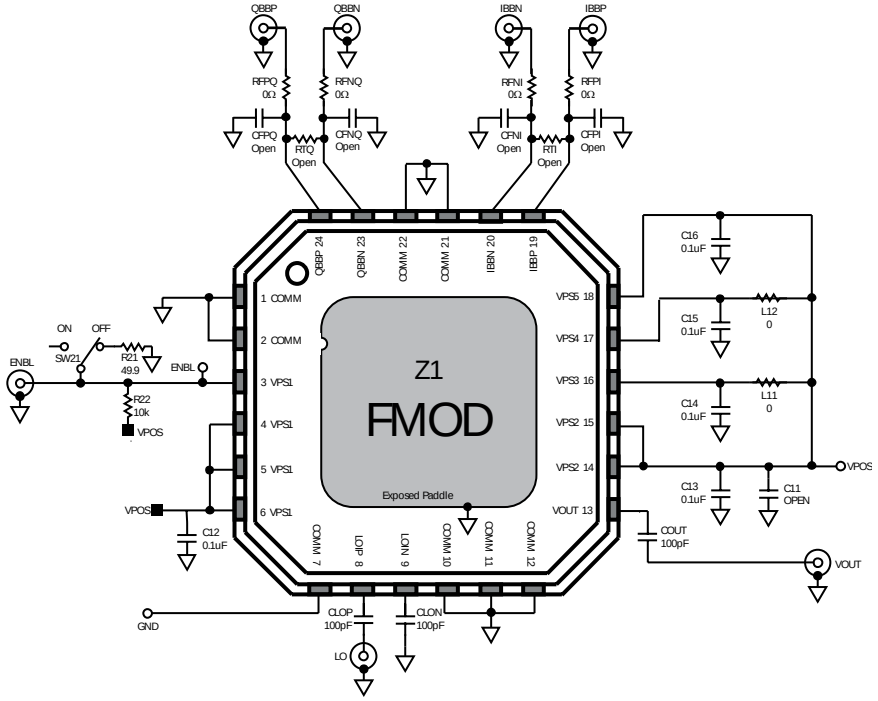

Figure 5. F-MOD Evaluation Board Schematic.

EVALUATION BOARD

Populated RoHS-compliant evaluation boards are available for the F-MOD family (see Ordering Guide for evaluation board part numbers). Each device has an exposed paddle underneath the package, which must be soldered to the board. The evaluation board is designed without any components on the underside of the board so that heat may be applied to the underside for easy removal and replacement of the F-MOD.

Note that the evaluation board pcb design includes an Enable Output SMA connector (ENOP) and switch (SW21) which connect ground or supply to pin 3. Since the F-MOD family does not support the Enable Output function (pin 3 is a power supply pin), SW21 should be placed in the ON position. This connects pin 3 to supply.

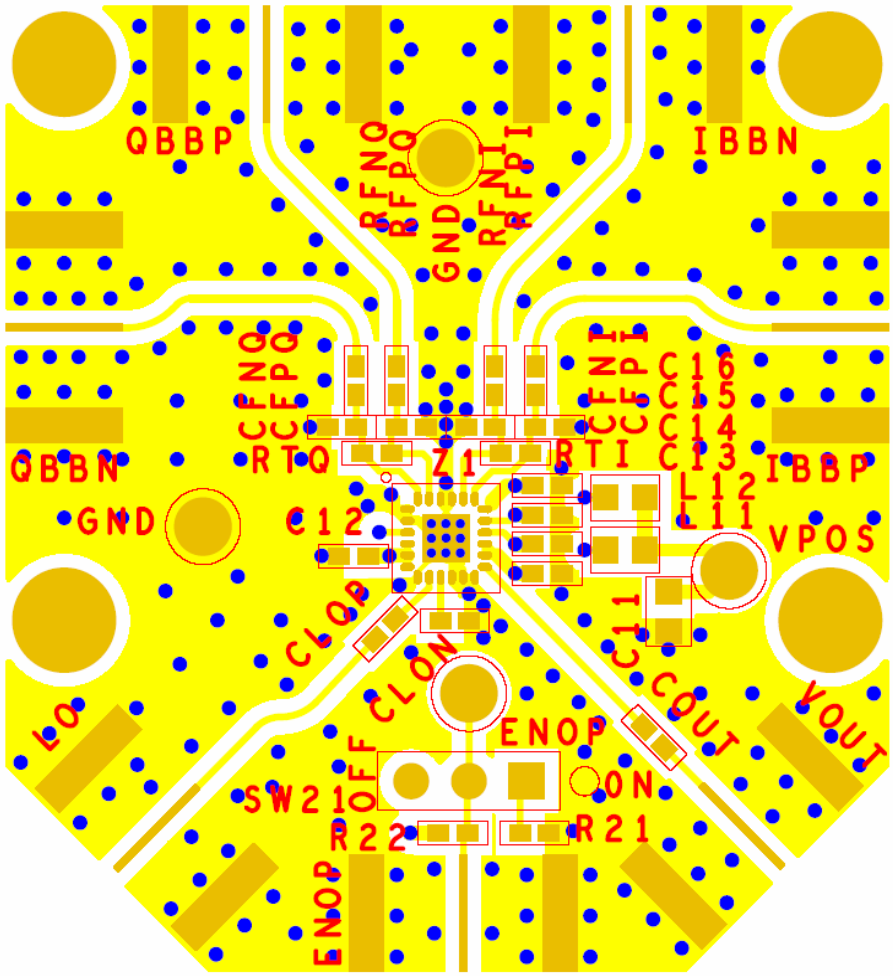

Figure 6. Evaluation Board Layout, Top Layer.

Table 4. Evaluation Board Configuration Options

Component	Function	Default Condition
VPOS, GND	Power Supply and Ground Clip Leads	Not applicable
SW21, ENOP SMA Connector	Enable Output Function (not supported in F-Mod family)	SW21 = ON (connects pin 3 (VPS1) to supply)
RFPI,RFNI,RFPQ,RFNQ,	Baseband Input Filters: These components can be used to implement a low-pass filter for the baseband signals.	RFNQ, RFPQ, RFNI RFPI = 0 Ω (0402)
CFPI, CFNI, CFPQ,CFNQ,		CFNQ,CFPQ,CFNI,CFPI = Open (0402)
RTQ, RTI,		RTQ, RTI = Open (0402)

OUTLINE DIMENSIONS

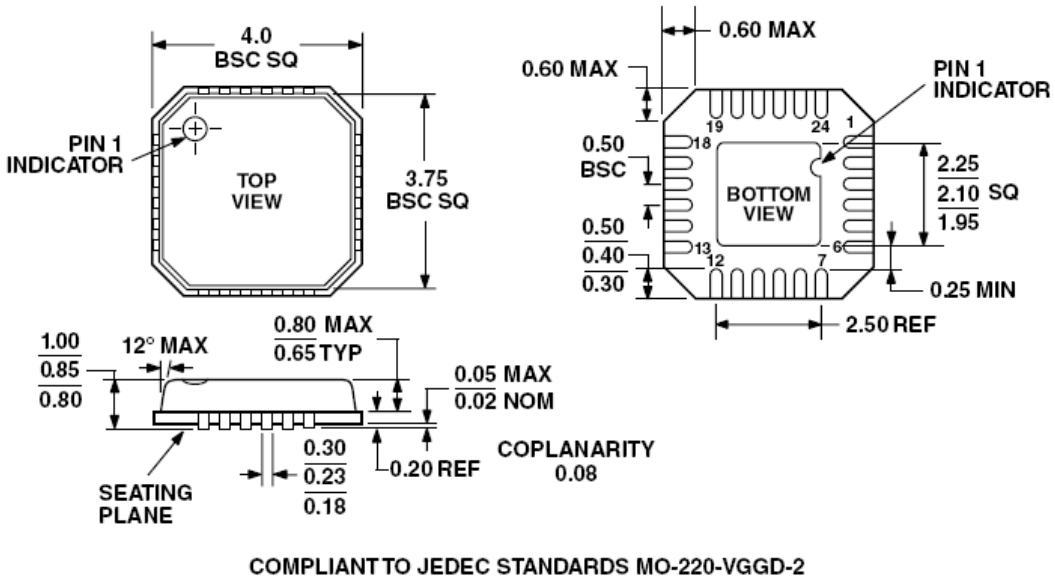

Figure 7. 24-Lead LFCSP with exposed paddle. Dimensions shown in millimeters

PR06117-0-4/06(PrG)

ORDERING GUIDE

Model	Temperature Range (°C)	Package Description	Package Option
ADL5370ACPZ-R7[1]	–40 to +85	7" Tape and Reel	
ADL5370ACPZ-WP[1]	–40 to +85	Waffle Pack	
ADL5370-EVALZ[1]		Evaluation Board	
ADL5371ACPZ-R7[1]	–40 to +85	7" Tape and Reel	
ADL5371ACPZ-WP[1]	–40 to +85	Waffle Pack	
ADL5371-EVALZ[1]		Evaluation Board	
ADL5372ACPZ-R7[1]	–40 to +85	7" Tape and Reel	
ADL5372ACPZ-WP[1]	–40 to +85	Waffle Pack	
ADL5372-EVALZ[1]		Evaluation Board	
ADL5373ACPZ-R7[1]	–40 to +85	7" Tape and Reel	
ADL5373ACPZ-WP[1]	–40 to +85	Waffle Pack	
ADL5373-EVALZ[1]		Evaluation Board	
ADL5374ACPZ-R7[1]	–40 to +85	7" Tape and Reel	
ADL5374ACPZ-WP[1]	–40 to +85	Waffle Pack	
ADL5374-EVALZ[1]		Evaluation Board	
ADL5375ACPZ-R7[1]	–40 to +85	7" Tape and Reel	
ADL5375ACPZ-WP[1]	–40 to +85	Waffle Pack	
ADL5375-EVALZ[1]		Evaluation Board	

[1] Z indicates Pb-free