Rail-to-Rail, Very Fast, 2.5 V to 5.5 V, Single-Supply LVDS Comparators

Preliminary Technical Data

ADCMP604/ACMP605

FEATURES

10 mV sensitivity rail to rail at V_{CC} = 2.5 V
Input common-mode voltage from −0.2 V to V_{CC} + 0.2 V
Low glitch LVDS-compatible output stage
1.5 ns propagation delay
35 mW at 2.5 V
Shutdown pin
Single-pin control for programmable hysteresis and latch
Power supply rejection >60 dB
−40C° to +125C° operation

APPLICATIONS

High speed instrumentation
Clock and data signal restoration
Logic level shifting or translation
Pulse spectroscopy
High speed line receivers
Threshold detection
Peak and zero-crossing detectors
High speed trigger circuitry
Pulse-width modulators
Current-/voltage-controlled oscillators
Automatic test equipment (ATE)

FUNCTIONAL BLOCK DIAGRAM

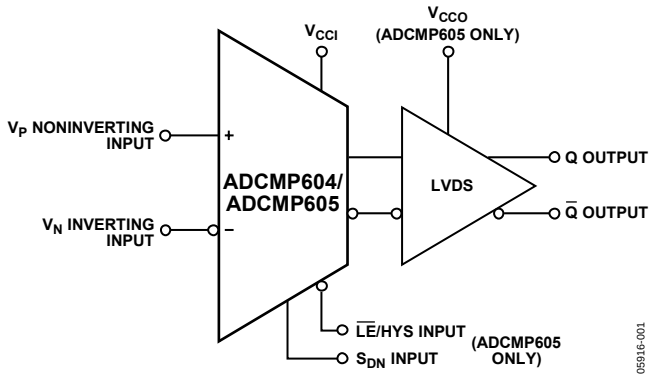

Figure 1.

GENERAL DESCRIPTION

The ADCMP604 and ADCMP605 are very fast comparators fabricated on Analog Devices' proprietary XFCB2 process. These comparators are exceptionally versatile and easy to use. Features include an input range from V_{EE} − 0.5 V to V_{CC} + 0.5 V, low noise, LVDS-compatible output drivers, and TTL/CMOS latch inputs with adjustable hysteresis and/or shutdown inputs.

The devices offer 1.5 ns propagation delays with 1 ps RMS random jitter (RJ). Overdrive and slew rate dispersion are typically less than 50 ps. A flexible power supply scheme allows the devices to operate with a single +2.5 V positive supply and a −0.5 V to +3.0 V input signal range up to a +5.5 V positive supply with a −0.5 V to +6V input signal range.

Split input/output supplies, with no sequencing restrictions on the ADCMP605, support a wide input signal range with greatly reduced power consumption.

The LVDS-compatible output stage is designed to drive any standard LVDS input. The comparator input stage offers robust protection against large input overdrive, and the outputs do not phase reverse when the valid input signal range is exceeded. High speed latch and programmable hysteresis features are also provided in a unique single-pin control option.

The ADCMP604 is available in a 6-lead SC70 package. The ADCMP605 is available in a 12-lead LSCFP package.

Rev. PrA

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REVISION HISTORY

2/06—Revision PrA: Preliminary Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{CCI} = V_{CCO} = 3.0 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DC INPUT CHARACTERISTICS						
Voltage Range	V_P, V_N	V_{CC} = 2.5 V to 5.5 V	−0.5		V_{CC} + 0.5 V	V
Common-Mode Range		V_{CC} = 2.5 V to 5.5 V	−0.2		V_{CC} + 0.2 V	V
Differential Voltage		V_{CC} = 2.5 V to 5.5 V			V_{CC}	V
Offset Voltage	V_{OS}		−5.0		+5.0	mV
Bias Current	I_P, I_N		−5.0	±2	+5.0	µA
Offset Current			−2.0		+2.0	µA
Capacitance	C_P, C_N			TBD		pF
Resistance, Differential Mode		0.1 V to V_{CC}		100		kΩ
Resistance, Common Mode		−0.5 V to V_{CC} + 0.5 V		100		kΩ
Active Gain	A_V			62		dB
Common-Mode Rejection	CMRR	V_{CCI} = 2.5 V, V_{CCO} = 2.5 V, V_{CM} = −0.2 V to 2.7 V		50		dB
		V_{CCI} = 5.5 V, V_{CCO} = 5.5 V, V_{CM} = −0.2 V to 5.7 V		60		dB
Hysteresis		R_{HYS} = ∞		0.1		mV
LATCH ENABLE PIN CHARACTERISTICS						
ADCMP604 only						
V_{IH}		Hysteresis is shut off	2.0		V_{CC}	V
V_{IL}		Latch mode guaranteed	−0.2	0.4	0.8	V
I_{IH}		V_{IH} = V_{CCO} + 0.2 V			0.2	mA
I_{OL}		V_{IL} = 0.4 V			−0.2	mA
HYSTERESIS MODE AND TIMING						
Hysteresis Mode Bias Voltage		Current sink 0 µA	1.145	1.25	1.35	V
Minimum Resistor Value		Hysteresis = 16 mV	150			kΩ
Latch Setup Time	t_S	V_{OD} = 100 mV		2		ns
Latch Hold Time	t_H	V_{OD} = 100 mV		5		ns
Latch to Output Delay	t_{PLOH}, t_{PLOL}	V_{OD} = 100 mV		1.5		ns
Latch Minimum Pulse Width	t_{PL}	V_{OD} = 100 mV		2		ns
SHUTDOWN PIN CHARACTERISTICS						
ADCMP605						
V_{IH}		Comparator is operating	2.0		V_{CCO}	V
V_{IL}		Shutdown guaranteed	−0.2	0.4	0.6	V
I_{IH}		V_{IH} = V_{CC}			0.3	mA
I_{OL}		V_{IL} = 0 V			−0.3	mA
Sleep Time	t_{SD}	I_{CC} < TBD		50		ns
Wake-Up Time	t_H	V_{OD} = 10 mV, output valid		80		ns
DC OUTPUT CHARACTERISTICS		V_{CCO} = 2.5 V to 5.5 V				
Differential Output Voltage Level	V_{OD}	R_{LOAD} = 100 Ω	245	350	445	mV
ΔV_{OD}	ΔV_{OD}	R_{LOAD} = 100 Ω			50	mV
Common-Mode Voltage	V_{OC}	R_{LOAD} = 100 Ω	1.125		1.375	V
P-P Common-Mode Output	$V_{OC(pp)}$	R_{LOAD} = 100 Ω			50	mV

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
AC PERFORMANCE						
Propagation Delay	t_{PD}	V_{CC} = 2.5 V to 5.5 V, V_{OD} = 5 mV		2		ns
		V_{CCO} = 2.5 V/5.5 V, V_{OD} = 200 mV		1.5		ns
Propagation Delay Skew—Rising to Falling Transition		V_{OD} = 5 mV		50		ps
Overdrive Dispersion		10 mV < V_{OD} < 2.5 V		300		ps
		5 mV < V_{OD} < 2.5 V		500		ps
Slew Rate Dispersion		.05 V/ns to 2.5 V/ns		75		ps
Pulse Width Dispersion		2 ns to 20 ns				
10% – 90% Duty Cycle Dispersion		1 V/ns, V_{CM} = 2.5 V		1		ps
Common-Mode Dispersion		V_{CM} = 0.2 V to V_{CC} + 0.2 V		200		ps
Toggle Rate		>50% output swing		TBD		Gbps
Deterministic Jitter	DJ	V_{OD} = 200 mV, 5 V/ns		TBD		ns
TTL/CMOS Outputs		$PRBS^{31}$ – 1 NRZ, 0.25 GPS				
RMS Random Jitter	RJ	V_{OD} = 200 mV, 5 V/ns		TBD		ps
		$PRBS^{31}$ – 1 NRZ, 0.525 GPS				
Minimum Pulse Width	PW_{MIN}	$\Delta t_{PD}/\Delta PW$ < 35 ps		2		ns
Rise Time	t_R	10% to 90%		1		ns
Fall Time	t_F	10% to 90%		1		ns
Output Skew	T_{SKEW}	@50%		25		ps
POWER SUPPLY						
Input Supply Voltage Range	V_{CCI}		2.5		5.5	V
Output Supply Voltage Range	V_{CCO}		2.5		5.5	V
Positive Supply Differential (ADCMP605)	$V_{CCI} - V_{CCO}$	Operating	−3		+3	V
Positive Supply Differential (ADCMP605)	$V_{CCI} - V_{CCO}$	Nonoperating	−5.5		+5.5	V
Positive Supply Current	I_{VCC}	V_{CC} = 2.5 V to 5.5 V		17		mA
Input Section Supply Current (ADCMP605)	I_{VCCI}	V_{CCI} = 5.5 V to 2.5 V		0.8		mA
Output Section Supply Current (ADCMP605)	I_{VCCO}	V_{CCO}= 5.5 V to 2.5 V		16		mA
Power Dissipation	P_D	V_{CC} = 2.5 V		42		mW
(ADCMP605)	P_D			100		mW
Power Supply Rejection	PSRR	V_{CCI} = 2.5 V to 5 V		−50		dB

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltages	
Input Supply Voltage (V_{CCI} to GND)	−0.5 V to +6.0 V
Output Supply Voltage (V_{CCO} to GND)	−0.5 V to +6.0 V
Positive Supply Differential ($V_{CCI} - V_{CCO}$)	−6.0 V to +6.0 V
Input Voltages	
Input Voltage	−0.5 V to V_{CCI} + 0.5 V
Differential Input Voltage	±(V_{CCI} + 0.5 V)
Maximum Input/Output Current	±50mA
Shutdown Control Pin	
Applied Voltage (HYS to GND)	−0.5 V to Vcco + 0.5 V
Maximum Input/Output Current	±50 mA
Latch/Hysteresis Control Pin	
Applied Voltage (HYS to GND)	−0.5 V to V_{CCO} + 0.5 V
Maximum Input/Output Current	±50 mA
Output Current	±50 mA
Temperature	
Operating Temperature, Ambient	−40°C to +125°C
Operating Temperature, Junction	150°C
Storage Temperature Range	−65°C to +150°C

Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}[1]	Unit
ADCMP604 SC70 6-lead	TBD	°C/W
ADCMP605 LSCFP 12-lead	62	°C/W

[1] Measurement in still air.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

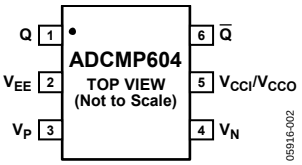

Figure 2. ADCMP604 Pin Configuration

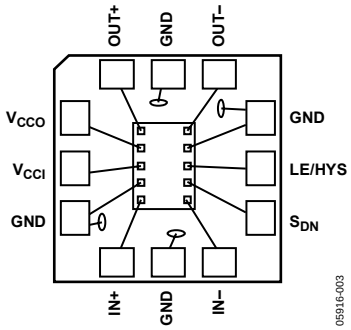

Figure 3. ADCMP605 Pin Configuration

Table 4. ADCMP604 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	Q	Noninverting Output. Q is at logic high if the analog voltage at the noninverting input, V_P, is greater than the analog voltage at the inverting input, V_N.
2	V_{EE}	Negative Supply Voltage.
3	V_P	Noninverting Analog Input.
4	V_n	Inverting Analog Input.
5	V_{CCI}/V_{CCO}	VCCI and VCCO Shared Pin.
6	$\overline{Q}$	Inverting Output. $\overline{Q}$ is at logic low if the analog voltage at the noninverting input, V_P, is greater than the analog voltage at the inverting input, V_N.

Table 5. ADCMP605 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{CCO}	Output Section Supply.
2	V_{CCI}	Input Section Supply.
3	V_{EE}	Negative Supply Voltage.
4	V_P	Noninverting Analog Input.
5	V_{EE}	Negative Supply Voltage.
6	V_N	Inverting Analog Input.
7	S_{DN}	Shutdown. Drive this pin low to shutdown the device.
8	LE/HYS	Latch/Hysteresis Control. Bias with resistor or current source for hysteresis; drive TTL low to latch.
9	V_{EE}	Negative Supply Voltage.
10	$\overline{Q}$	Inverting Output. $\overline{Q}$ is at logic low if the analog voltage at the noninverting input, V_P, is greater than the analog voltage at the inverting input, V_N, provided the comparator is in compare mode.
11	V_{EE}	Negative Supply Voltage.
12	Q	Noninverting Output. Q is at logic high if the analog voltage at the noninverting input, V_P, is greater than the analog voltage at the inverting input, V_N, provided the comparator is in compare mode.
Heat Sink Paddle	V_{EE}	The metallic back surface of the package is electrically connected to V_{EE}. It can be left floating because Pin 3, Pin 5, Pin 9, and Pin 11 provide adequate electrical connection. It can also be soldered to the application board if improved thermal and/or mechanical stability is desired.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CCI} = V_{CCO} = 3.3 V, T_A = 25°C, unless otherwise noted.

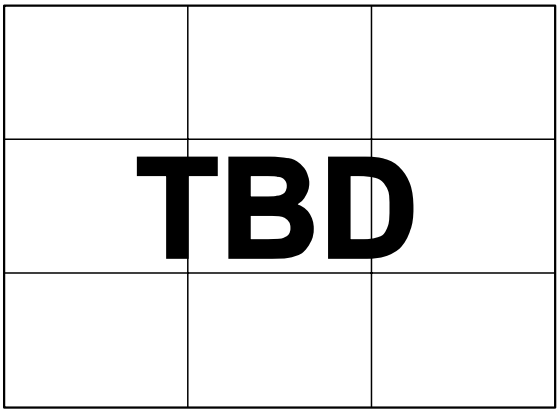

Figure 4. Propagation Delay vs. Input Overdrive

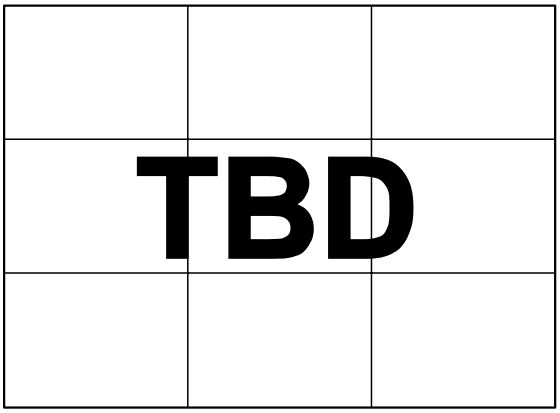

Figure 7. Rise/Fall Time vs. Temperature

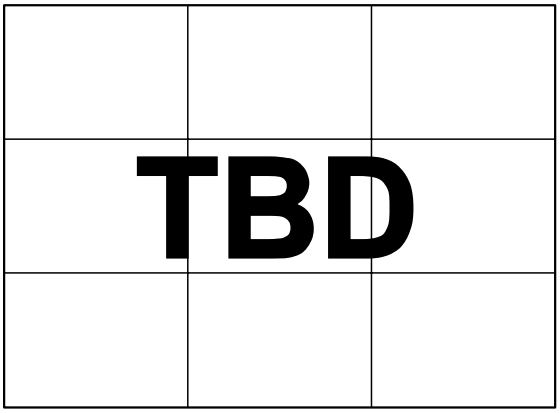

Figure 5. Propagation Delay vs. Input Common Mode

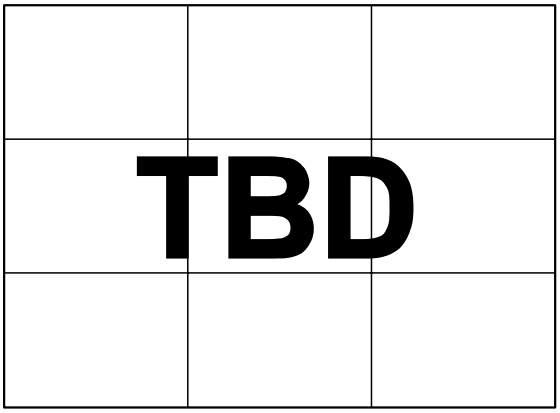

Figure 8. Hysteresis vs. R_{HYS} Control Resistor

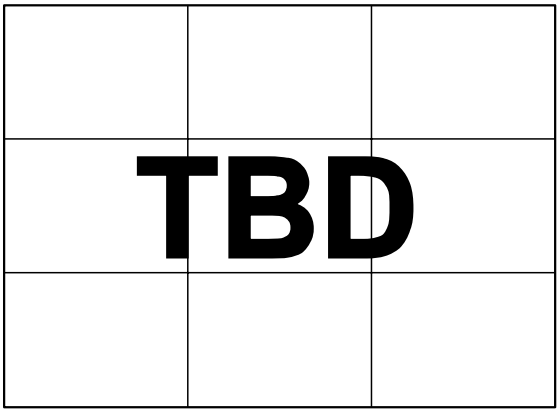

Figure 6. Propagation Delay vs. Temperature

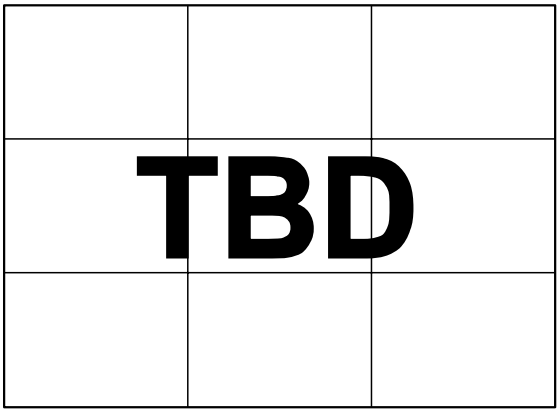

Figure 9. Input Bias Current vs. Input Common Mode

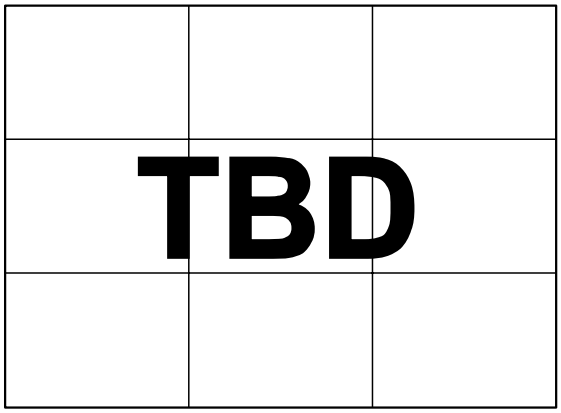

Figure 10. Input Bias Current vs. Temperature

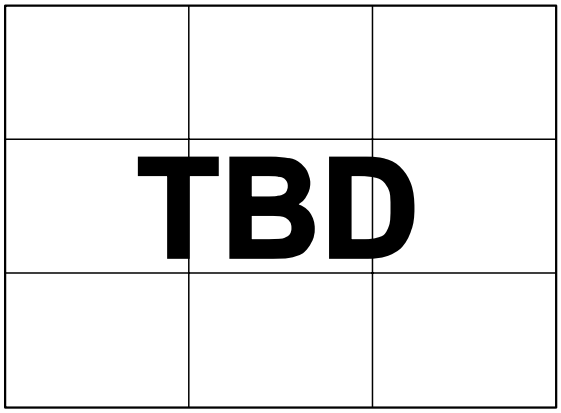

Figure 12 Latch/Hysteresis Control Pin I/V Characteristic.

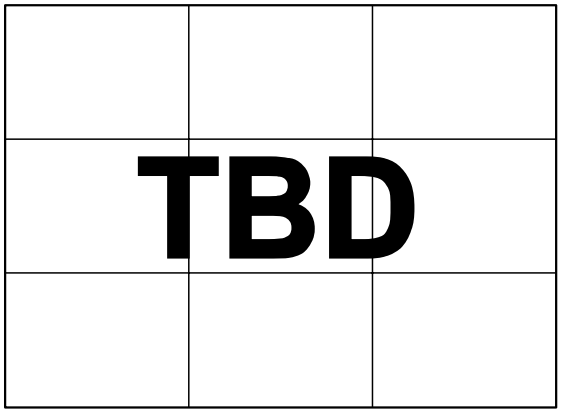

Figure 11. Input Offset Voltage vs. Temperature

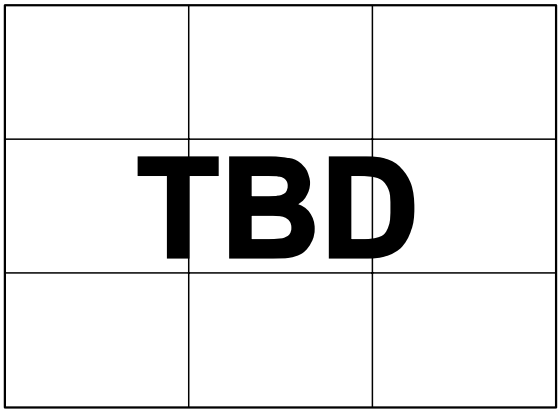

Figure 13 Latch/Hysteresis vs. V_{CC}.

APPLICATION INFORMATION

POWER/GROUND LAYOUT AND BYPASSING

The ADCMP604 and ADCMP605 comparators are very high speed devices. Despite the low noise output stage, it is essential to use proper high speed design techniques to achieve the specified performance. Because comparators are uncompensated amplifiers, feedback in any phase relationship is likely to cause oscillations or undesired hysteresis. Of critical importance is the use of low impedance supply planes, particularly the output supply plane (V_{CCO}) and the ground plane (GND). Individual supply planes are recommended as part of a multilayer board. Providing the lowest inductance return path for switching currents ensures the best possible performance in the target application.

It is also important to adequately bypass the input and output supplies. Multiple high quality 0.01 µF bypass capacitors should be placed as close as possible to each of the V_{CCI} and V_{CCO} supply pins and should be connected to the GND plane with redundant vias. At least one of these should be placed to provide a physically short return path for output currents flowing back from ground to the V_{CC} pin. High frequency bypass capacitors should be carefully selected for minimum inductance and ESR. Parasitic layout inductance should also be strictly controlled to maximize the effectiveness of the bypass at high frequencies.

If the package allows, and the input and output supplies have been connected separately ($V_{CCI} \neq V_{CCO}$), be sure to bypass each of these supplies separately to the GND plane. Do not connect a bypass capacitor between these supplies. It is recommended that the GND plane separate the V_{CCI} and V_{CCO} planes when the circuit board layout is designed to minimize coupling between the two supplies to take advantage of the additional bypass capacitance from each respective supply to the ground plane. This enhances the performance when split input/output supplies are used. If the input and output supplies are connected together for single-supply operation ($V_{CCI} = V_{CCO}$), then coupling between the two supplies is unavoidable; however, careful board placement can help keep output return currents away from the inputs.

LVDS-COMPATIBLE OUTPUT STAGE

Specified propagation delay dispersion performance is only achieved by keeping parasitic capacitive loads at or below the specified minimums. The outputs of the ADCMP604 and ADCMP605 are designed to directly drive any standard LVDS-compatible input.

USING/DISABLING THE LATCH FEATURE

The latch input of the ADCMP605 is designed for maximum versatility. It can safely be left floating or pulled to TTL high for normal comparator operation with no hysteresis, or it can be driven low by any standard TTL/CMOS device as a high speed latch. In addition, the pin can be operated as a hysteresis control pin with a bias voltage of 1.25 V nominal and an input resistance of approximately 7000 Ω. This allows the comparator hysteresis to be easily controlled by either a resistor or an inexpensive CMOS DAC. Driving the pin high or floating the pin disables all hysteresis.

Hysteresis control and latch mode can be used together if an open drain, an open collector, or a three-state driver is connected in parallel to the hysteresis control resistor or to the current source. Due to the programmable hysteresis feature, the logic threshold of the latch pin is approximately 1.1 V regardless of V_{CC}.

OPTIMIZING PERFORMANCE

As with any high speed comparator, proper design and layout techniques are essential for obtaining the specified performance. Stray capacitance, inductance, inductive power and ground impedances, or other layout issues can severely limit performance and often cause oscillation. Large discontinuities along input and output transmission lines can also limit the specified pulse-width dispersion performance. The source impedance should be minimized as much as is practicable. High source impedance, in combination with the parasitic input capacitance of the comparator, will cause an undesirable degradation in bandwidth at the input, thus degrading the overall response. Thermal noise from large resistances can easily cause extra jitter with slowly slewing input signals. Higher impedances encourage undesired coupling.

COMPARATOR PROPAGATION DELAY DISPERSION

The ADCMP604 and ADCMP605 comparator is designed to reduce propagation delay dispersion over a wide input overdrive range of 5 mV TBD V. Propagation delay dispersion is the variation in propagation delay that results from a change in the degree of overdrive or slew rate (how far or how fast the input signal is driven past the switching threshold).

Propagation delay dispersion is a specification that becomes important in high speed, time-critical applications, such as data communication, automatic test and measurement, and instrumentation. It is also important in event-driven applications, such as pulse spectroscopy, nuclear instrumentation, and medical imaging. Dispersion is defined as the variation in propagation delay as the input overdrive conditions are changed (see Figure 14 and Figure 15).

ADCMP604 and ADCMP605 dispersion is typically <TBD ps as the overdrive varies from 10 mV to 500 mV, and the input slew rate varies from 2 V/ns to 10 V/ns. This specification applies to both positive and negative signals because the ADCMP604 and ADCMP605 have very closely matched delays for both positive-going and negative-going inputs, and very low output skews.

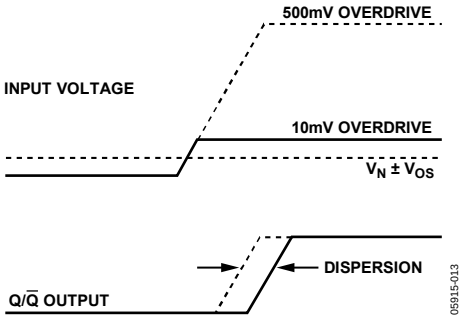

Figure 14. Propagation Delay—Overdrive Dispersion

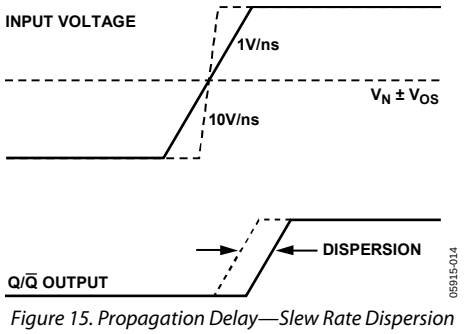

Figure 15. Propagation Delay—Slew Rate Dispersion

COMPARATOR HYSTERESIS

The addition of hysteresis to a comparator is often desirable in a noisy environment, or when the differential input amplitudes are relatively small or slow moving. The transfer function for a comparator with hysteresis is shown in Figure 16. As the input voltage approaches the threshold (0.0 V, in this example) from below the threshold region in a positive direction, the comparator switches from a low to a high when the input crosses $+V_H/2$. The new switching threshold becomes $-V_H/2$. The comparator remains in the high state until the threshold $-V_H/2$ is crossed from below the threshold region in a negative direction. In this manner, noise or feedback output signals centered on 0.0 V input cannot cause the comparator to switch states unless it exceeds the region bounded by $\pm V_H/2$.

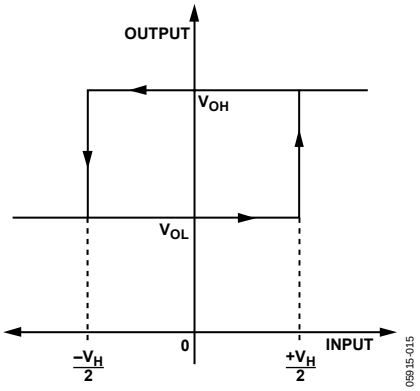

Figure 16. Comparator Hysteresis Transfer Function

The customary technique for introducing hysteresis into a comparator uses positive feedback from the output back to the input. One limitation of this approach is that the amount of hysteresis varies with the output logic levels, resulting in hysteresis that is not symmetric about the threshold. The external feedback network can also introduce significant parasitics that reduce high speed performance, and can even induce oscillation in some cases.

The ADCMP605 comparator offers a programmable hysteresis feature that significantly improves accuracy and stability. Connecting an external pull-down resistor or a current source from the LE/HYS pin to GND, varies the amount of hysteresis in a predictable and stable manner. Leaving the LE/HYS pin disconnected or driving it high removes the hysteresis. The maximum hysteresis that can be applied using this pin is approximately 160 mV. Figure 17 illustrates the amount of hysteresis applied as a function of external resistor value. Figure TBD illustrates hysteresis as a function of current.

The hysteresis control pin appears as a 1.25 V bias voltage seen through a series resistance of 7k ± 20% throughout the hysteresis control range. The advantages of applying hysteresis in this manner are improved accuracy, stability, reduced component count, and maximum versatility. An external bypass capacitor is not recommended on the HYS pin because it would likely degrade the jitter performance of the device and impair the latch function. As described in Using/Disabling the Latch Feature, hysteresis control need not compromise the latch function.

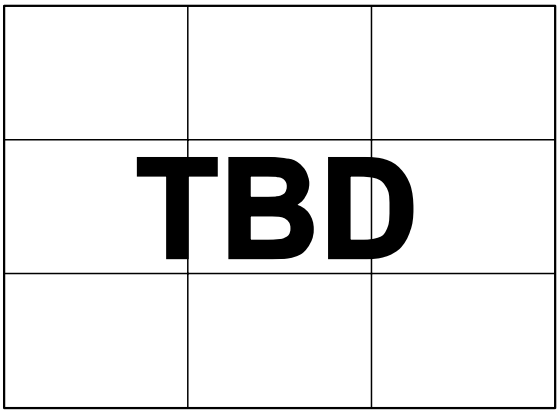

Figure 17. Hysteresis vs. R_{HYS} Control Resistor

CROSSOVER BIAS POINT

Rail-to-rail inputs of this type, in both op amps and comparators have a dual front-end design. Certain devices are active near the V_{CC} rail and others are active near the V_{EE} rail. At some predetermined point in the common-mode range, a crossover occurs. At this point, normally $V_{CC}/2$, the direction of the bias current reverses and there are changes in measured offset voltages and currents.

The ADCMP604/ADCMP605 slightly elaborate on this scheme. With V_{CC} less than 4 V, this crossover is at the expected $V_{CC}/2$, but with V_{CC} greater than 4 V, the crossover point instead follows V_{CC} 1:1, bringing it to approximately 3 V with V_{CC} at 5 V. This means that the comparator input characteristics will more closely resemble the inputs of non rail-to-rail ground sensing comparators, such as the AD8611.

MINIMUM INPUT SLEW RATE REQUIREMENT

(Remove if device is stable.)

As with most high speed comparators, without hysteresis a minimum slew rate requirement must be met to ensure that the device does not oscillate as the input signal crosses the threshold. This oscillation is due in part to the high input bandwidth of the comparator in combination with feedback parasitics inherent in the package and PC board. A minimum slew rate of TBD. V/µs ensures clean output transitions from the ADCMP604/ADCMP605 comparators unless hysteresis is programmed. In many applications, chattering is not harmful.

TYPICAL APPLICATION CIRCUITS

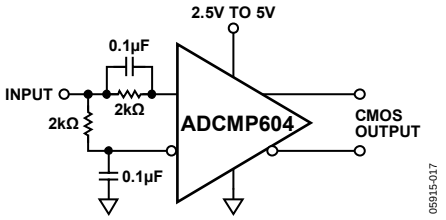

Figure 18. Self-Biased 50% Slicer

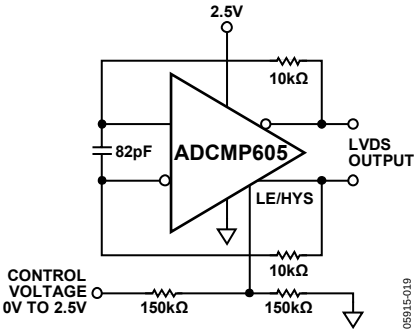

Figure 21. Voltage Controlled Oscillator

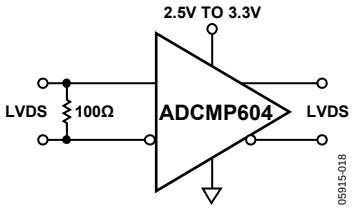

Figure 19. LVDS Repeater

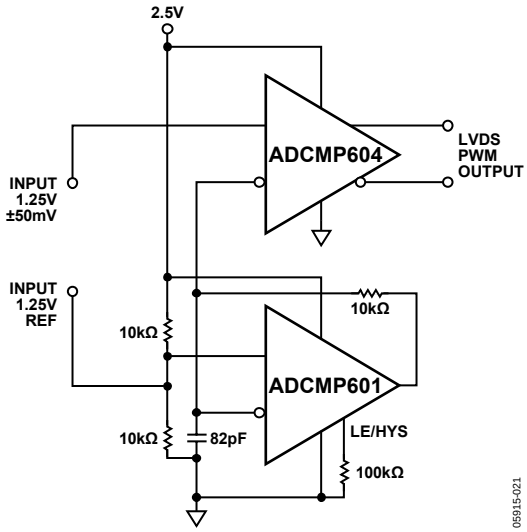

Figure 22. Oscillator and Pulse Width Modulator

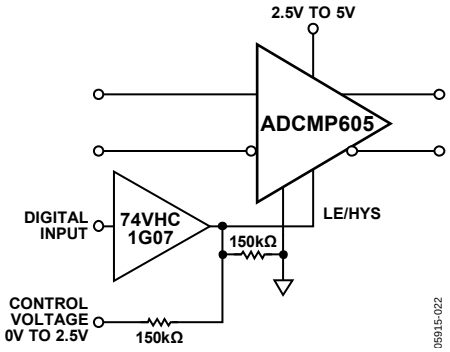

Figure 20. Hysteresis Adjustment with Latch

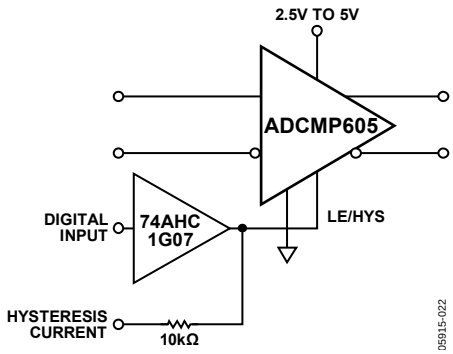

Figure 23. Hysteresis Adjustment with Latch

TIMING INFORMATION

Figure 24 illustrates the ADCMP604/ADCMP605 latch timing relationships. Table 6 provides definitions of the terms found in the figure.

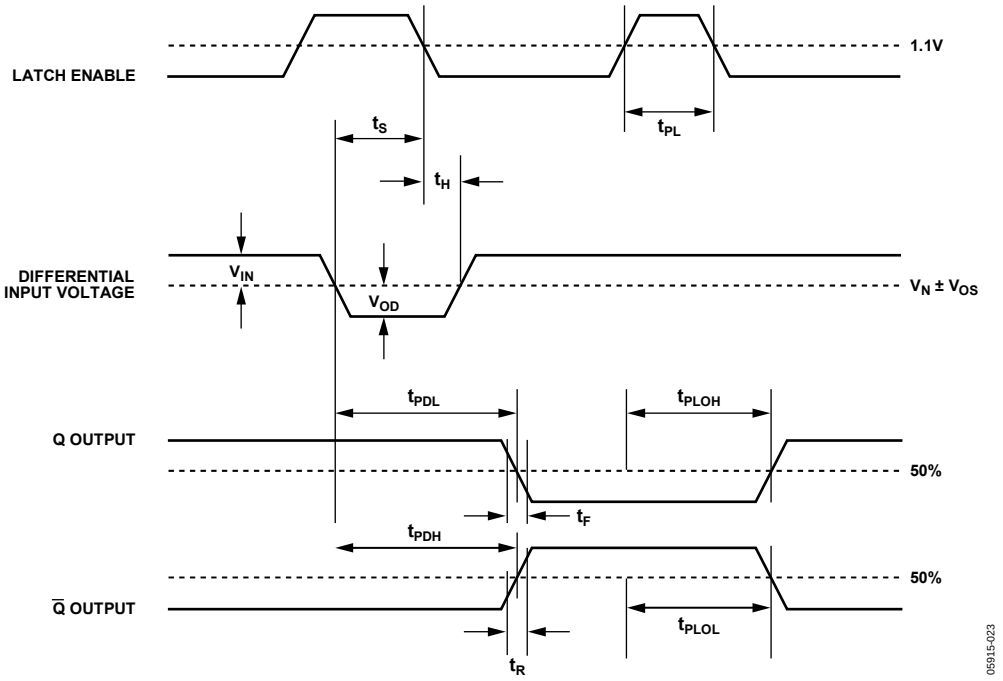

Figure 24. System Timing Diagram

Table 6. Timing Descriptions

Symbol	Timing	Description
t_{PDH}	Input to output high delay	Propagation delay measured from the time the input signal crosses the reference (± the input offset voltage) to the 50% point of an output low-to-high transition.
t_{PDL}	Input to output low delay	Propagation delay measured from the time the input signal crosses the reference (± the input offset voltage) to the 50% point of an output high-to-low transition.
t_{PLOH}	Latch enable to output high delay	Propagation delay measured from the 50% point of the latch enable signal low-to-high transition to the 50% point of an output low-to-high transition.
t_{PLOL}	Latch enable to output low delay	Propagation delay measured from the 50% point of the latch enable signal low-to-high transition to the 50% point of an output high-to-low transition.
t_H	Minimum hold time	Minimum time after the negative transition of the latch enable signal that the input signal must remain unchanged to be acquired and held at the outputs.
t_{PL}	Minimum latch enable pulse width	Minimum time that the latch enable signal must be high to acquire an input signal change.
t_S	Minimum setup time	Minimum time before the negative transition of the latch enable signal occurs that an input signal change must be present to be acquired and held at the outputs.
t_R	Output rise time	Amount of time required to transition from a low to a high output as measured at the 20% and 80% points.
t_F	Output fall time	Amount of time required to transition from a high to a low output as measured at the 20% and 80% points.
V_{OD}	Voltage overdrive	Difference between the input voltages V_A and V_B.

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