ANALOG DEVICES

Dual, 12-/14-/16-Bit, 1.0 GSPS D/A Converter

AD9776/AD9778/AD9779

FEATURES

- **DAC output sample rate: 1 GSPS**
- **1.8 V/3.3 V single supply operation**
- **Low power: 1.0 W @ 1 GSPS, 600 mW @ 500 MSPS, full operating conditions**
- **SFDR = 78 dBc to f_{OUT} = 100 MHz**
- **Single carrier WCDMA ACLR = 79 dBc @ 80 MHz IF**
- **CMOS data input interface with adjustable setup and hold**
- **Analog output: adjustable 8.7 mA to 31.7 mA, RL = 25 Ω to 50 Ω**
- **Novel 2×, 4×, and 8× interpolator/coarse complex modulator allows carrier placement anywhere in DAC bandwidth**
- **Auxiliary DACs allow control of external VGA and offset control**
- **Multiple chip synchronization interface**
- **High performance, low noise PLL clock multiplier**
- **Digital inverse sinc filter**
- **100-lead, exposed paddle TQFP package**

APPLICATIONS

- **Wireless infrastructure**
- **Digital high or low IF synthesis**
- **Internal digital upconversion capability**
- **Transmit diversity**
- **Wideband communications systems point-to-point wireless, LMDS**
- **Multicarrier WCDMA**
- **Multicarrier GSM**

GENERAL DESCRIPTION

The AD9776/AD9778/AD9779 are dual, 12-/14-/16-bit, high dynamic range DACs that provide a sample rate of 1 GSPS, thus permitting multicarrier generation up to its Nyquist frequency. They include features optimized for direct conversion transmit applications, including complex digital modulation, and gain and offset compensation. The DAC outputs are optimized to interface seamlessly with analog quadrature modulators such as the AD8349. A serial peripheral interface (SPI) provides for programming/readback of many internal parameters. The output current can be programmed over a range of 10 mA to 30 mA. The devices are manufactured on an advanced 0.18 μm CMOS process and operate from 1.8 V and 3.3 V supplies for a total power consumption of 1.0 W. They are enclosed in 100-lead TQFP packages.

PRODUCT HIGHLIGHTS

1. Ultralow noise and intermodulation distortion (IMD) enable high quality synthesis of wideband signals from baseband to high intermediate frequencies.
2. A proprietary DAC output switching technique enhances dynamic performance.
3. The current outputs can be easily configured for various single-ended or differential circuit topologies.

Rev. 0

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REVISION HISTORY

7/05—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

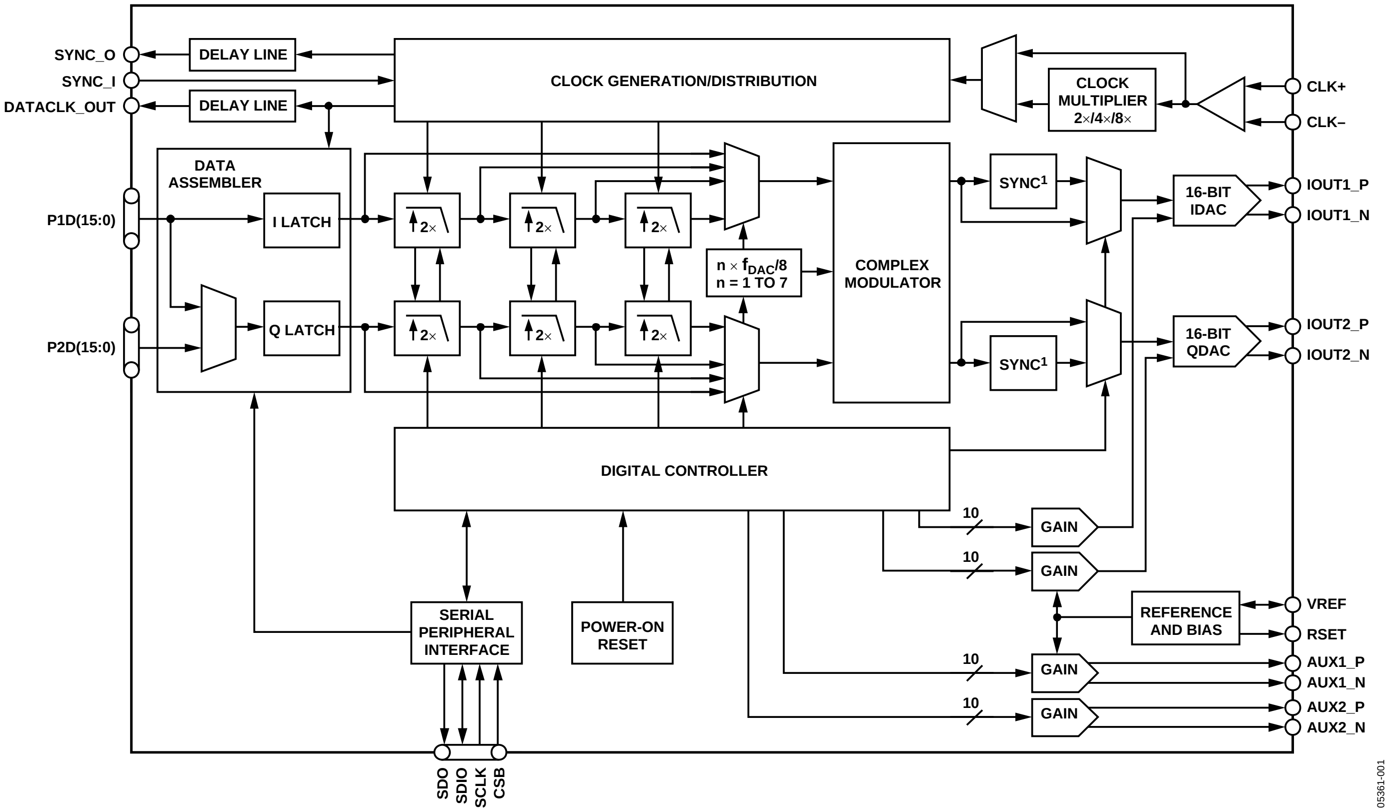
SYNC_O
SYNC_I
DATACLK_OUT
DELAY LINE
DELAY LINE
CLOCK GENERATION/DISTRIBUTION
CLOCK MULTIPLIER 2×/4×/8×
CLK+
CLK–
DATA ASSEMBLER
P1D(15:0)
P2D(15:0)
I LATCH
Q LATCH
2×
2×
2×
2×
2×
2×
n × f_{DAC}/8
n = 1 TO 7
COMPLEX MODULATOR
SYNC^1
SYNC^1
16-BIT IDAC
16-BIT QDAC
IOUT1_P
IOUT1_N
IOUT2_P
IOUT2_N
DIGITAL CONTROLLER
10
GAIN
10
GAIN
REFERENCE AND BIAS
VREF
RSET
10
GAIN
10
GAIN
AUX1_P
AUX1_N
AUX2_P
AUX2_N
SERIAL PERIPHERAL INTERFACE
POWER-ON RESET
SDO
SDIO
SCLK
CSB
05361-001

Figure 1.

SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 =1.8 V, I_{OUTFS} = 20 mA, maximum sample rate, unless otherwise noted.

Table 1. AD9776, AD9778, and AD9779 DC Specifications

	AD9776			AD9778			AD9779			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION		12			14			16		Bits
ACCURACY										
Differential Nonlinearity (DNL)		±0.1			±0.65			±2.1		LSB
Integral Nonlinearity (INL)		±0.6			±1			±3.7		LSB
MAIN DAC OUTPUTS										
Offset Error	−0.001	0	+0.001	−0.001	0	+0.001	−0.001	0	+0.001	% FSR
Gain Error (with Internal Reference)		±2			±2			±2		% FSR
Full-Scale Output Current[1]	8.66	20.2	31.66	8.66	20.2	31.66	8.66	20.2	31.66	mA
Output Compliance Range	−1.0		+1.0	−1.0		+1.0	−1.0		+1.0	V
Output Resistance		10			10			10		MΩ
Gain DAC Monotonicity Guaranteed										
MAIN DAC TEMPERATURE DRIFT										
Offset		0.04			0.04			0.04		ppm/°C
Gain		100			100			100		ppm/°C
Reference Voltage		30			30			30		ppm/°C
AUX DAC OUTPUTS										
Resolution		10			10			10		Bits
Full-Scale Output Current[1]	−1.998		+1.998	−1.998		+1.998	−1.998		+1.998	mA
Output Compliance Range (Source)	0		1.6	0		1.6	0		1.6	V
Output Compliance Range (Sink)	0.8		1.6	0.8		1.6	0.8		1.6	V
Output Resistance		1			1			1		MΩ
Aux DAC Monotonicity Guaranteed										
REFERENCE										
Internal Reference Voltage		1.2			1.2			1.2		V
Output Resistance		5			5			5		kΩ
ANALOG SUPPLY VOLTAGES										
AVDD33	3.13	3.3	3.47	3.13	3.3	3.47	3.13	3.3	3.47	V
CVDD18	1.70	1.8	1.90	1.70	1.8	1.90	1.70	1.8	1.90	V
DIGITAL SUPPLY VOLTAGES										
DVDD33	3.13	3.3	3.47	3.13	3.3	3.47	3.13	3.3	3.47	V
DVDD18	1.70	1.8	1.90	1.70	1.8	1.90	1.70	1.8	1.90	V
POWER CONSUMPTION										
1× Mode, f_{DAC} = 100 MSPS, IF = 1 MHz		250	300		250	300		250	300	mW
2× Mode, f_{DAC} = 320 MSPS, IF = 16 MHz, PLL Off		498			498			498		mW
2× Mode, f_{DAC} = 320 MSPS, IF = 16 MHz, PLL On		588			588			588		mW
4× Mode, f_{DAC}/4 Mod, f_{DAC} = 500 MSPS, IF = 137.5 MHz, Q DAC Off		572			572			572		mW

	AD9776			AD9778			AD9779			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
8× Mode, f_{DAC}/4 Mod, f_{DAC} = 1 GSPS, IF = 262.5 MHz		980			980			980		mW
Power-Down Mode		2	3.7		2	3.7		2	3.7	mW
Power Supply Rejection Ratio—AVDD33	−0.3		+0.3	−0.3		+0.3	−0.3		+0.3	% FSR/V
OPERATING RANGE	−40	+25	+85	−40	+25	+85	−40	+25	+85	°C

[1] Based on a 10 kΩ external resistor.

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{OUTFS} = 20 mA, maximum sample rate, unless otherwise noted. LVDS driver and receiver are compliant to the IEEE-1596 reduced range link, unless otherwise noted.

Table 2. AD9776, AD9778, and AD9779 Digital Specifications

Parameter	Min	Typ	Max	Unit
LVDS RECEIVER INPUTS (SYNC_I+, SYNC_I−), SYNC_I+ = V_{IA}, SYNC_I− = V_{IB}				
Input Voltage Range, V_{IA} or V_{IB}	825		1575	mV
Input Differential Threshold, V_{IDTH}	−100		+100	mV
Input Differential Hysteresis, $V_{IDTHH} - V_{IDTHL}$		20		mV
Receiver Differential Input Impedance, R_{IN}[1]	80		120	Ω
LVDS Input Rate			125	MSPS
Set-Up Time, Sync_I to DAC Clock	−0.2			ns
Hold Time, Sync_I to DAC Clock	1			ns
LVDS DRIVER OUTPUTS (SYNC_O+, SYNC_O−), SYNC_O+ = V_{OA}, SYNC_O− = V_{OB}, 100 Ω Termination				
Output Voltage High, V_{OA} or V_{OB}	825		1575	mV
Output Voltage Low, V_{OA} or V_{OB}	1025			mV
Output Differential Voltage, $\|V_{OD}\|$	150	200	250	mV
Output Offset Voltage, V_{OS}	1150		1250	mV
Output Impedance, Single-Ended, R_O	80	100	120	Ω
Maximum Clock Rate	1			GHz
DAC CLOCK INPUT (CLK+, CLK−)				
Peak-to-Peak Voltage at CLK+ and CLK−[2]	400	800	1600	mV
Common-Mode Voltage	300	400	500	mV
Maximum Clock Rate[3]		1		GSPS
SERIAL PERIPHERAL INTERFACE				
Maximum Clock Rate (SCLK)			40	MHz
Minimum Pulse Width High			12.5	ns
Minimum Pulse Width Low			12.5	ns
INPUT DATA				
Set-Up Time, Input Data To DATACLK (All Modes)	3.0			ns
Hold Time, Input Data To DATACLK (All Modes)	−0.78			ns

[1] Guaranteed at 25°C. Can drift above 120 Ω at temperatures above 25°C.
[2] When using the PLL, a minimum 1 V swing is recommended.
[3] Typical maximum clock rate when DVDD18 = CVDD18 = 1.9 V.

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{OUTFS} = 20 mA, maximum sample rate, unless otherwise noted.

Table 3. AD9776, AD9778, and AD9779 AC Specifications

	AD9776			AD9778			AD9779			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SPURIOUS FREE DYNAMIC RANGE (SFDR)										
f_{DAC} = 100 MSPS, f_{OUT} = 20 MHz		82			82			82		dBc
f_{DAC} = 200 MSPS, f_{OUT} = 50 MHz		81			81			82		dBc
f_{DAC} = 400 MSPS, f_{OUT} = 70 MHz		80			80			80		dBc
f_{DAC} = 800 MSPS, f_{OUT} = 70 MHz		85			85			87		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)										
f_{DAC} = 200 MSPS, f_{OUT} = 50 MHz		87			87			91		dBc
f_{DAC} = 400 MSPS, f_{OUT} = 60 MHz		80			85			85		dBc
f_{DAC} = 400 MSPS, f_{OUT} = 80 MHz		75			81			81		dBc
f_{DAC} = 800 MSPS, f_{OUT} = 100 MHz		75			80			81		dBc
NOISE SPECTRAL DENSITY (NSD) Eight-Tone, 500 kHz Tone Spacing										
f_{DAC} = 200 MSPS, f_{OUT} = 80 MHz		−152			−155			−158		dBm/Hz
f_{DAC} = 400 MSPS, f_{OUT} = 80 MHz		−155			−159			−160		dBm/Hz
f_{DAC} = 800 MSPS, f_{OUT} = 80 MHz		−157.5			−160			−161		dBm/Hz
WCDMA ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE CARRIER										
f_{DAC} = 491.52 MSPS, f_{OUT} = 100 MHz		76			78			79		dBc
f_{DAC} = 491.52 MSPS, f_{OUT} = 200 MHz		69			73			74		dBc
WCDMA SECOND ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE CARRIER										
f_{DAC} = 491.52 MSPS, f_{OUT} = 100 MHz		77.5			80			81		dBc
f_{DAC} = 491.52 MSPS, f_{OUT} = 200 MHz		76			78			78		dBc

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	With Respect to	Rating
AVDD33	AGND DGND CGND	−0.3 V to +3.6 V
DVDD33, DVDD18, CVDD18	AGND DGND CGND	−0.3 V to +1.98 V
AGND	DGND CGND	−0.3 V to +0.3 V
DGND	AGND CGND	−0.3 V to +0.3 V
CGND	AGND DGND	−0.3 V to +0.3 V
I120, VREF, IPTAT	AGND	−0.3 V to AVDD33 + 0.3 V
I_{OUT1-P}, I_{OUT1-N}, I_{OUT2-P}, I_{OUT2-N}, Aux_{1-P}, Aux_{1-N}, Aux_{2-P}, Aux_{2-N}	AGND	−1.0 V to AVDD33 + 0.3 V
P1D15 to P1D0, P2D15 to P2D0	DGND	−0.3 V to DVDD33 + 0.3 V
DATACLK, TXENABLE	DGND	−0.3 V to DVDD33 + 0.3 V
CLK+, CLK−, RESET, IRQ, PLL_LOCK, SYNC_O+, SYNC_O−, SYNC_I+, SYNC_I−	CGND	−0.3 V to CVDD18 + 0.3 V
RESET, IRQ, PLL_LOCK, SYNC_O+, SYNC_O−, SYNC_I+, SYNC_I−, CSB, SCLK, SDIO, SDO	DGND	−0.3 V to DVDD33 + 0.3 V
Junction Temperature		+125°C
Storage Temperature		−65°C to +150°C

Thermal Resistance

100-lead, thermally enhanced TQFP Package $\theta_{JA} = 27.4°C/W$ (with no airflow movement).

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

WARNING!

ESD SENSITIVE DEVICE

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

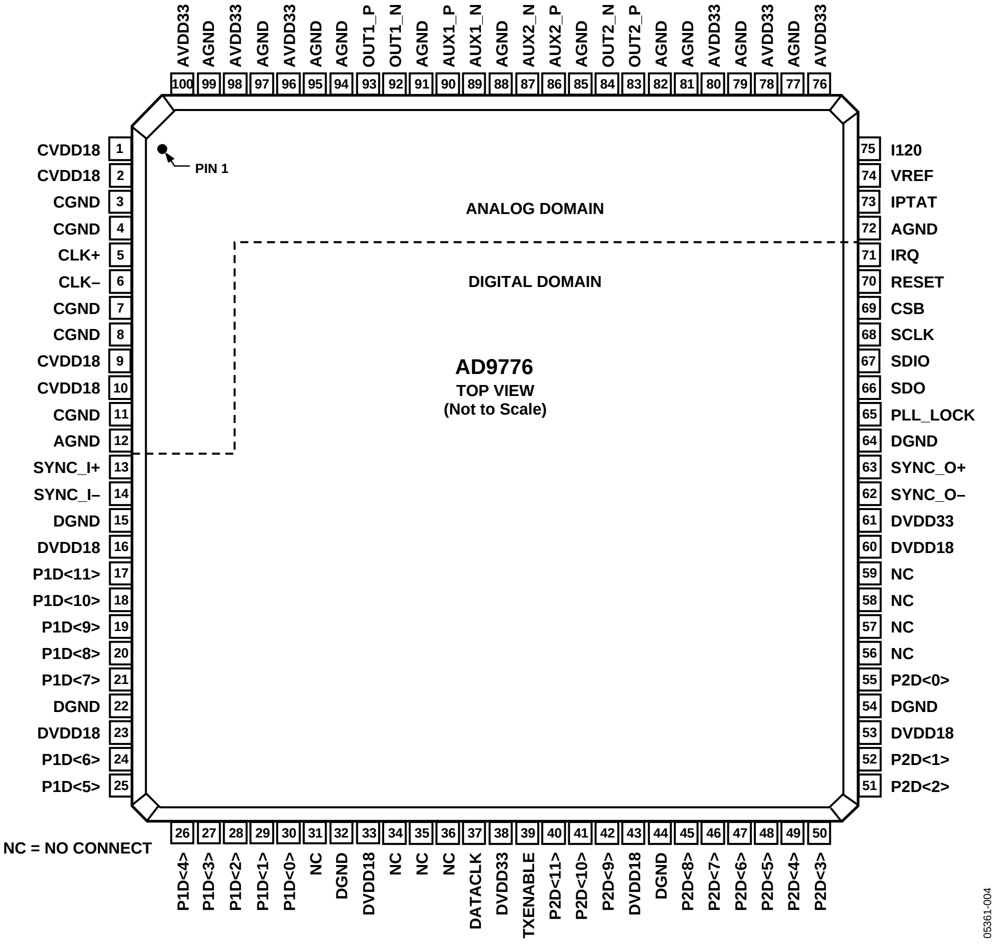
100 AVDD33
99 AGND
98 AVDD33
97 AGND
96 AVDD33
95 AGND
94 AGND
93 OUT1_P
92 OUT1_N
91 AGND
90 AUX1_P
89 AUX1_N
88 AGND
87 AUX2_N
86 AUX2_P
85 AGND
84 OUT2_N
83 OUT2_P
82 AGND
81 AGND
80 AVDD33
79 AGND
78 AVDD33
77 AGND
76 AVDD33
CVDD18 1
CVDD18 2
CGND 3
CGND 4
CLK+ 5
CLK– 6
CGND 7
CGND 8
CVDD18 9
CVDD18 10
CGND 11
AGND 12
SYNC_I+ 13
SYNC_I– 14
DGND 15
DVDD18 16
P1D<11> 17
P1D<10> 18
P1D<9> 19
P1D<8> 20
P1D<7> 21
DGND 22
DVDD18 23
P1D<6> 24
P1D<5> 25
PIN 1
ANALOG DOMAIN
DIGITAL DOMAIN
AD9776
TOP VIEW
(Not to Scale)
75 I120
74 VREF
73 IPTAT
72 AGND
71 IRQ
70 RESET
69 CSB
68 SCLK
67 SDIO
66 SDO
65 PLL_LOCK
64 DGND
63 SYNC_O+
62 SYNC_O–
61 DVDD33
60 DVDD18
59 NC
58 NC
57 NC
56 NC
55 P2D<0>
54 DGND
53 DVDD18
52 P2D<1>
51 P2D<2>
NC = NO CONNECT
26 P1D<4>
27 P1D<3>
28 P1D<2>
29 P1D<1>
30 P1D<0>
31 NC
32 DGND
33 DVDD18
34 NC
35 NC
36 NC
37 DATACLK
38 DVDD33
39 TXENABLE
40 P2D<11>
41 P2D<10>
42 P2D<9>
43 DVDD18
44 DGND
45 P2D<8>
46 P2D<7>
47 P2D<6>
48 P2D<5>
49 P2D<4>
50 P2D<3>
05361-004

Figure 2. AD9776 Pin Configuration

Table 5. AD 9776 Pin Function Description

Pin No.	Mnemonic	Description
1	CVDD18	1.8 V Clock Supply
2	CVDD18	1.8 V Clock Supply
3	CGND	Clock Common
4	CGND	Clock Common
5	CLK+[1]	Differential Clock Input
6	CLK–[1]	Differential Clock Input
7	CGND	Clock Common
8	CGND	Clock Common
9	CVDD18	1.8 V Clock Supply
10	CVDD18	1.8 V Clock Supply
11	CGND	Clock Common
12	AGND	Analog Common
13	SYNC_I+	Differential Synchronization Input
14	SYNC_I–	Differential Synchronization Input
15	DGND	Digital Common
16	DVDD18	1.8 V Digital Supply
17	P1D <11>	Port 1, Data Input D11 (MSB)
18	P1D <10>	Port 1, Data Input D10
19	P1D <9>	Port 1, Data Input D9
20	P1D <8>	Port 1, Data Input D8
21	P1D <7>	Port 1, Data Input D7
22	DGND	Digital Common
23	DVDD18	1.8 V Digital Supply
24	P1D <6>	Port 1, Data Input D6
25	P1D <5>	Port 1, Data Input D5
26	P1D <4>	Port 1, Data Input D4
27	P1D <3>	Port 1, Data Input D3
28	P1D <2>	Port 1, Data Input D2
29	P1D <1>	Port 1, Data Input D1
30	P1D <0>	Port 1, Data Input D0
31	NC	No Connect
32	DGND	Digital Common
33	DVDD18	1.8 V Digital Supply
34	NC	No Connect
35	NC	No Connect
36	NC	No Connect

Pin No.	Mnemonic	Description
37	DATACLK	Data Clock Output
38	DVDD33	3.3 V Digital Supply
39	TXENABLE	Transmit Enable
40	P2D <11>	Port 2, Data Input D11 (MSB)
41	P2D <10>	Port 2, Data Input D10
42	P2D <9>	Port 2, Data Input D9
43	DVDD18	1.8 V Digital Supply
44	DGND	Digital Common
45	P2D <8>	Port 2, Data Input D8
46	P2D <7>	Port 2, Data Input D7
47	P2D <6>	Port 2, Data Input D6
48	P2D <5>	Port 2, Data Input D5
49	P2D <4>	Port 2, Data Input D4
50	P2D <3>	Port 2, Data Input D3
51	P2D <2>	Port 2, Data Input D2
52	P2D <1>	Port 2, Data Input D1
53	DVDD18	1.8 V Digital Supply
54	DGND	Digital Common
55	P2D <0>	Port 2, Data Input D0
56	NC	No Connect
57	NC	No Connect
58	NC	No Connect
59	NC	No Connect
60	DVDD18	1.8 V Digital Supply
61	DVDD33	3.3 V Digital Supply
62	SYNC_O–	Differential Synchronization Output
63	SYNC_O+	Differential Synchronization Output
64	DGND	Digital Common
65	PLL_LOCK	PLL Lock Indicator
66	SDO	SPI Port Data Output
67	SDIO	SPI Port Data Input/Output
68	SCLK	SPI Port Clock
69	CSB	SPI Port Chip Select Bar
70	RESET	Reset, Active High
71	IRQ	Interrupt Request
72	AGND	Analog Common
73	IPTAT	Reference Current
74	VREF	Voltage Reference Output
75	I120	120 µA Reference Current
76	AVDD33	3.3 V Analog Supply
77	AGND	Analog Common
78	AVDD33	3.3 V Analog Supply
79	AGND	Analog Common
80	AVDD33	3.3 V Analog Supply
81	AGND	Analog Common
82	AGND	Analog Common
83	OUT2_P	Differential DAC Current Output, Channel 2
84	OUT2_N	Differential DAC Current Output, Channel 2
85	AGND	Analog Common
86	AUX2_P	Auxiliary DAC Voltage Output, Channel 2
87	AUX2_N	Auxiliary DAC Voltage Output, Channel 2
88	AGND	Analog Common
89	AUX1_N	Auxiliary DAC Voltage Output, Channel 1
90	AUX1_P	Auxiliary DAC Voltage Output, Channel 1
91	AGND	Analog Common
92	OUT1_N	Differential DAC Current Output, Channel 1
93	OUT1_P	Differential DAC Current Output, Channel 1
94	AGND	Analog Common
95	AGND	Analog Common
96	AVDD33	3.3 V Analog Supply
97	AGND	Analog Common
98	AVDD33	3.3 V Analog Supply
99	AGND	Analog Common
100	AVDD33	3.3 V Analog Supply

[1] The combined differential clock input at the CLK+ and CLK– pins are referred to as DACCLK.

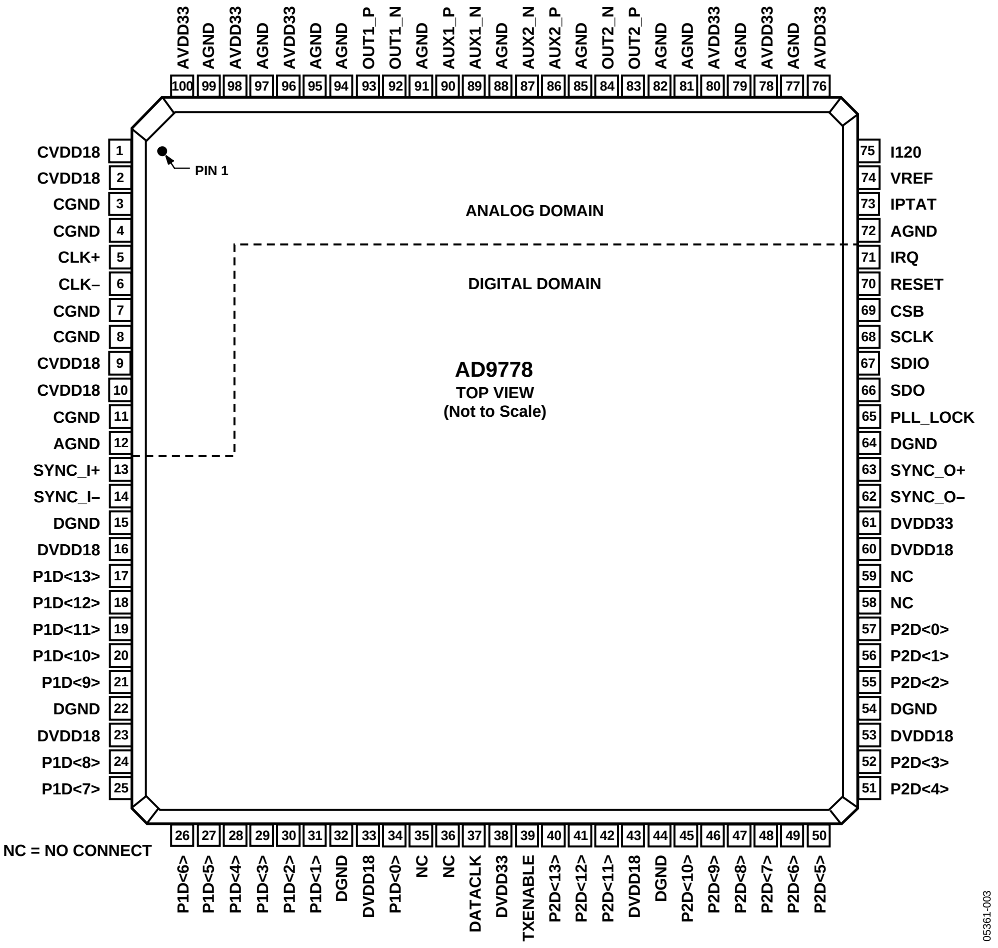
AVDD33 100
AGND 99
AVDD33 98
AGND 97
AVDD33 96
AGND 95
AGND 94
OUT1_P 93
OUT1_N 92
AGND 91
AUX1_P 90
AUX1_N 89
AGND 88
AUX2_N 87
AUX2_P 86
AGND 85
OUT2_N 84
OUT2_P 83
AGND 82
AGND 81
AVDD33 80
AGND 79
AVDD33 78
AGND 77
AVDD33 76
CVDD18 1
CVDD18 2
CGND 3
CGND 4
CLK+ 5
CLK– 6
CGND 7
CGND 8
CVDD18 9
CVDD18 10
CGND 11
AGND 12
SYNC_I+ 13
SYNC_I– 14
DGND 15
DVDD18 16
P1D<13> 17
P1D<12> 18
P1D<11> 19
P1D<10> 20
P1D<9> 21
DGND 22
DVDD18 23
P1D<8> 24
P1D<7> 25
PIN 1
ANALOG DOMAIN
DIGITAL DOMAIN
AD9778
TOP VIEW
(Not to Scale)
75 I120
74 VREF
73 IPTAT
72 AGND
71 IRQ
70 RESET
69 CSB
68 SCLK
67 SDIO
66 SDO
65 PLL_LOCK
64 DGND
63 SYNC_O+
62 SYNC_O–
61 DVDD33
60 DVDD18
59 NC
58 NC
57 P2D<0>
56 P2D<1>
55 P2D<2>
54 DGND
53 DVDD18
52 P2D<3>
51 P2D<4>
NC = NO CONNECT
26 P1D<6>
27 P1D<5>
28 P1D<4>
29 P1D<3>
30 P1D<2>
31 P1D<1>
32 DGND
33 DVDD18
34 P1D<0>
35 NC
36 NC
37 DATACLK
38 DVDD33
39 TXENABLE
40 P2D<13>
41 P2D<12>
42 P2D<11>
43 DVDD18
44 DGND
45 P2D<10>
46 P2D<9>
47 P2D<8>
48 P2D<7>
49 P2D<6>
50 P2D<5>
05361-003

Figure 3. AD9778 Pin Configuration

Table 6. AD 9778 Pin Function Description

Pin No.	Mnemonic	Description
1	CVDD18	1.8 V Clock Supply
2	CVDD18	1.8 V Clock Supply
3	CGND	Clock Common
4	CGND	Clock Common
5	CLK+[1]	Differential Clock Input
6	CLK–[1]	Differential Clock Input
7	CGND	Clock Common
8	CGND	Clock Common
9	CVDD18	1.8 V Clock Supply
10	CVDD18	1.8 V Clock Supply
11	CGND	Clock Common
12	AGND	Analog Common
13	SYNC_I+	Differential Synchronization Input
14	SYNC_I–	Differential Synchronization Input
15	DGND	Digital Common
16	DVDD18	1.8 V Digital Supply
17	P1D <13>	Port 1, Data Input D13 (MSB)
18	P1D <12>	Port 1, Data Input D12
19	P1D <11>	Port 1, Data Input D11
20	P1D <10>	Port 1, Data Input D10
21	P1D <9>	Port 1, Data Input D9
22	DGND	Digital Common
23	DVDD18	1.8 V Digital Supply
24	P1D <8>	Port 1, Data Input D8
25	P1D <7>	Port 1, Data Input D7
26	P1D <6>	Port 1, Data Input D6
27	P1D <5>	Port 1, Data Input D5
28	P1D <4>	Port 1, Data Input D4
29	P1D <3>	Port 1, Data Input D3
30	P1D <2>	Port 1, Data Input D2
31	P1D <1>	Port 1, Data Input D1
32	DGND	Digital Common
33	DVDD18	1.8 V Digital Supply
34	P1D <0>	Port 1, Data Input D0
35	NC	No Connect
36	NC	No Connect
37	DATACLK	Data Clock Output
38	DVDD33	3.3 V Digital Supply
39	TXENABLE	Transmit Enable
40	P2D <13>	Port 2, Data Input D13 (MSB)

Pin No.	Mnemonic	Description
41	P2D <12>	Port 2, Data Input D12
42	P2D <11>	Port 2, Data Input D11
43	DVDD18	1.8 V Digital Supply
44	DGND	Digital Common
45	P2D <10>	Port 2, Data Input D10
46	P2D <9>	Port 2, Data Input D9
47	P2D <8>	Port 2, Data Input D8
48	P2D <7>	Port 2, Data Input D7
49	P2D <6>	Port 2, Data Input D6
50	P2D <5>	Port 2, Data Input D5
51	P2D <4>	Port 2, Data Input D4
52	P2D <3>	Port 2, Data Input D3
53	DVDD18	1.8 V Digital Supply
54	DGND	Digital Common
55	P2D <2>	Port 2, Data Input D2
56	P2D <1>	Port 2, Data Input D1
57	P2D <0>	Port 2, Data Input D0
58	NC	No Connect
59	NC	No Connect
60	DVDD18	1.8 V Digital Supply
61	DVDD33	3.3 V Digital Supply
62	SYNC_O–	Differential Synchronization Output
63	SYNC_O+	Differential Synchronization Output
64	DGND	Digital Common
65	PLL_LOCK	PLL Lock Indicator
66	SDO	SPI Port Data Output
67	SDIO	SPI Port Data Input/Output
68	SCLK	SPI Port Clock
69	CSB	SPI Port Chip Select Bar
70	RESET	Reset, Active High
71	IRQ	Interrupt Request
72	AGND	Analog Common
73	IPTAT	Reference Current
74	VREF	Voltage Reference Output
75	I120	120 µA Reference Current
76	AVDD33	3.3 V Analog Supply
77	AGND	Analog Common
78	AVDD33	3.3 V Analog Supply
79	AGND	Analog Common
80	AVDD33	3.3 V Analog Supply
81	AGND	Analog Common
82	AGND	Analog Common
83	OUT2_P	Differential DAC Current Output, Channel 2
84	OUT2_N	Differential DAC Current Output, Channel 2
85	AGND	Analog Common
86	AUX2_P	Auxiliary DAC Voltage Output, Channel 2
87	AUX2_N	Auxiliary DAC Voltage Output, Channel 2
88	AGND	Analog Common
89	AUX1_N	Auxiliary DAC Voltage Output, Channel 1
90	AUX1_P	Auxiliary DAC Voltage Output, Channel 1
91	AGND	Analog Common
92	OUT1_N	Differential DAC Current Output, Channel 1
93	OUT1_P	Differential DAC Current Output, Channel 1
94	AGND	Analog Common
95	AGND	Analog Common
96	AVDD33	3.3 V Analog Supply
97	AGND	Analog Common
98	AVDD33	3.3 V Analog Supply
99	AGND	Analog Common
100	AVDD33	3.3 V Analog Supply

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[1] The combined differential clock input at the CLK+ and CLK– pins are referred to as DACCLK.

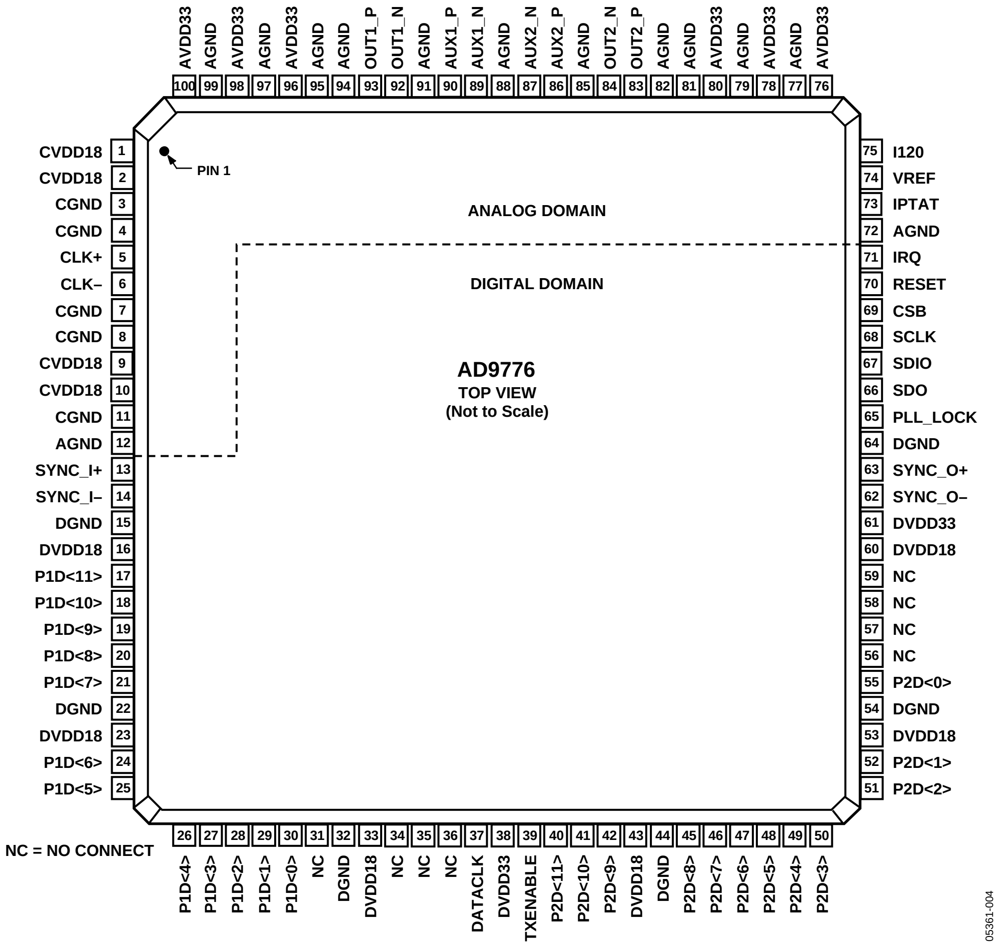
AVDD33 100
AGND 99
AVDD33 98
AGND 97
AVDD33 96
AGND 95
AGND 94
OUT1_P 93
OUT1_N 92
AGND 91
AUX1_P 90
AUX1_N 89
AGND 88
AUX2_N 87
AUX2_P 86
AGND 85
OUT2_N 84
OUT2_P 83
AGND 82
AGND 81
AVDD33 80
AGND 79
AVDD33 78
AGND 77
AVDD33 76
CVDD18 1
CVDD18 2
CGND 3
CGND 4
CLK+ 5
CLK– 6
CGND 7
CGND 8
CVDD18 9
CVDD18 10
CGND 11
AGND 12
SYNC_I+ 13
SYNC_I– 14
DGND 15
DVDD18 16
P1D<11> 17
P1D<10> 18
P1D<9> 19
P1D<8> 20
P1D<7> 21
DGND 22
DVDD18 23
P1D<6> 24
P1D<5> 25
PIN 1
ANALOG DOMAIN
DIGITAL DOMAIN
AD9776
TOP VIEW
(Not to Scale)
75 I120
74 VREF
73 IPTAT
72 AGND
71 IRQ
70 RESET
69 CSB
68 SCLK
67 SDIO
66 SDO
65 PLL_LOCK
64 DGND
63 SYNC_O+
62 SYNC_O–
61 DVDD33
60 DVDD18
59 NC
58 NC
57 NC
56 NC
55 P2D<0>
54 DGND
53 DVDD18
52 P2D<1>
51 P2D<2>
NC = NO CONNECT
26 P1D<4>
27 P1D<3>
28 P1D<2>
29 P1D<1>
30 P1D<0>
31 NC
32 DGND
33 DVDD18
34 NC
35 NC
36 NC
37 DATACLK
38 DVDD33
39 TXENABLE
40 P2D<11>
41 P2D<10>
42 P2D<9>
43 DVDD18
44 DGND
45 P2D<8>
46 P2D<7>
47 P2D<6>
48 P2D<5>
49 P2D<4>
50 P2D<3>
05361-004

Figure 4. AD9779 Pin Configuration

Table 7. AD9779 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CVDD18	1.8 V Clock Supply
2	CVDD18	1.8 V Clock Supply
3	CGND	Clock Common
4	CGND	Clock Common
5	CLK+[1]	Differential Clock Input
6	CLK–[1]	Differential Clock Input
7	CGND	Clock Common
8	CGND	Clock Common
9	CVDD18	1.8 V Clock Supply
10	CVDD18	1.8 V Clock Supply
11	CGND	Clock Common
12	AGND	Analog Common
13	SYNC_I+	Differential Synchronization Input
14	SYNC_I–	Differential Synchronization Input
15	DGND	Digital Common
16	DVDD18	1.8 V Digital Supply
17	P1D <15>	Port 1, Data Input D15 (MSB)
18	P1D <14>	Port 1, Data Input D14
19	P1D <13>	Port 1, Data Input D13
20	P1D <12>	Port 1, Data Input D12
21	P1D <11>	Port 1, Data Input D11
22	DGND	Digital Common
23	DVDD18	1.8 V Digital Supply
24	P1D <10>	Port 1, Data Input D10
25	P1D <9>	Port 1, Data Input D9
26	P1D <8>	Port 1, Data Input D8
27	P1D <7>	Port 1, Data Input D7
28	P1D <6>	Port 1, Data Input D6
29	P1D <5>	Port 1, Data Input D5
30	P1D <4>	Port 1, Data Input D4
31	P1D <3>	Port 1, Data Input D3
32	DGND	Digital Common
33	DVDD18	1.8 V Digital Supply
34	P1D <2>	Port 1, Data Input D2
35	P1D <1>	Port 1, Data Input D1
36	P1D <0>	Port 1, Data Input D0 (LSB)
37	DATACLK	Data Clock Output
38	DVDD33	3.3 V Digital Supply

Pin No.	Mnemonic	Description
39	TXENABLE	Transmit Enable
40	P2D <15>	Port 2, Data Input D15 (MSB)
41	P2D <14>	Port 2, Data Input D14
42	P2D <13>	Port 2, Data Input D13
43	DVDD18	1.8 V Digital Supply
44	DGND	Digital Common
45	P2D <12>	Port 2, Data Input D12
46	P2D <11>	Port 2, Data Input D11
47	P2D <10>	Port 2, Data Input D10
48	P2D <9>	Port 2, Data Input D9
49	P2D <8>	Port 2, Data Input D8
50	P2D <7>	Port 2, Data Input D7
51	P2D <6>	Port 2, Data Input D6
52	P2D <5>	Port 2, Data Input D5
53	DVDD18	1.8 V Digital Supply
54	DGND	Digital Common
55	P2D <4>	Port 2, Data Input D4
56	P2D <3>	Port 2, Data Input D3
57	P2D <2>	Port 2, Data Input D2
58	P2D <1>	Port 2, Data Input D1
59	P2D <0>	Port 2, Data Input D0 (LSB)
60	DVDD18	1.8 V Digital Supply
61	DVDD33	3.3 V Digital Supply
62	SYNC_O–	Differential Synchronization Output
63	SYNC_O+	Differential Synchronization Output
64	DGND	Digital Common
65	PLL_LOCK	PLL Lock Indicator
66	SPI_SDO	SPI Port Data Output
67	SPI_SDIO	SPI Port Data Input/Output
68	SCLK	SPI Port Clock
69	SPI_CSB	SPI Port Chip Select Bar
70	RESET	Reset, Active High
71	IRQ	Interrupt Request
72	AGND	Analog Common
73	IPTAT	Reference Current
74	VREF	Voltage Reference Output
75	I120	120 μA Reference Current
76	AVDD33	3.3 V Analog Supply
77	AGND	Analog Common
78	AVDD33	3.3 V Analog Supply
79	AGND	Analog Common
80	AVDD33	3.3 V Analog Supply
81	AGND	Analog Common
82	AGND	Analog Common
83	OUT2_P	Differential DAC Current Output, Channel 2
84	OUT2_N	Differential DAC Current Output, Channel 2
85	AGND	Analog Common
86	AUX2_P	Auxiliary DAC Voltage Output, Channel 2
87	AUX2_N	Auxiliary DAC Voltage Output, Channel 2
88	AGND	Analog Common
89	AUX1_N	Auxiliary DAC Voltage Output, Channel 1
90	AUX1_P	Auxiliary DAC Voltage Output, Channel 1
91	AGND	Analog Common
92	OUT1_N	Differential DAC Current Output, Channel 1
93	OUT1_P	Differential DAC Current Output, Channel 1
94	AGND	Analog Common
95	AGND	Analog Common
96	AVDD33	3.3 V Analog Supply
97	AGND	Analog Common
98	AVDD33	3.3 V Analog Supply
99	AGND	Analog Common
100	AVDD33	3.3 V Analog Supply

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[1] The combined differential clock input at the CLK+ and CLK– pins are referred to as DACCLK.

TYPICAL PERFORMANCE CHARACTERISTICS

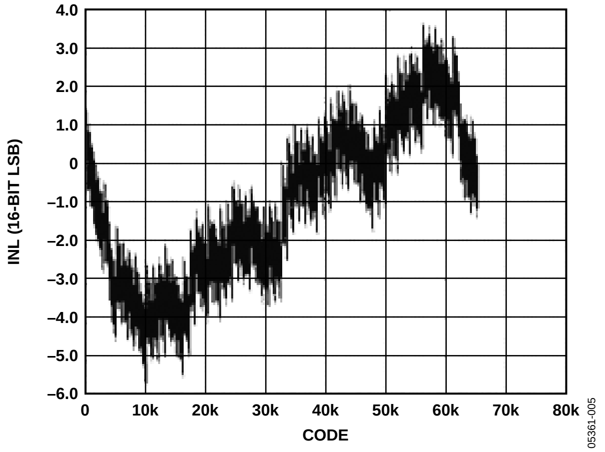


Figure 5. AD9779 Typical INL

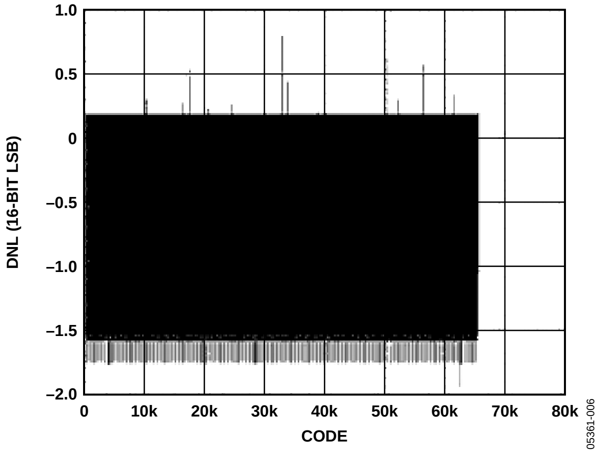


Figure 6. AD9779 Typical DNL

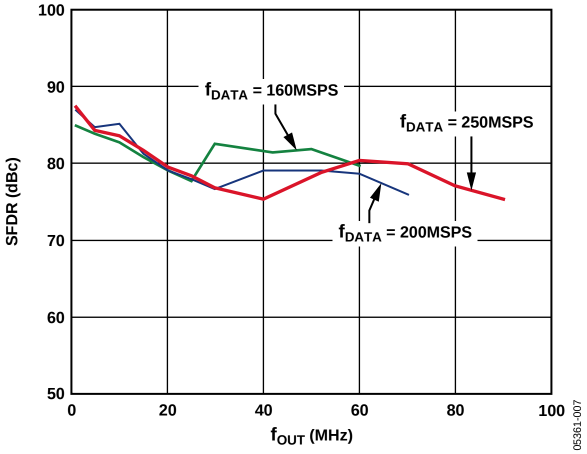


Figure 7. AD9779 In-Band SFDR vs. f_{OUT}, 1x Interpolation

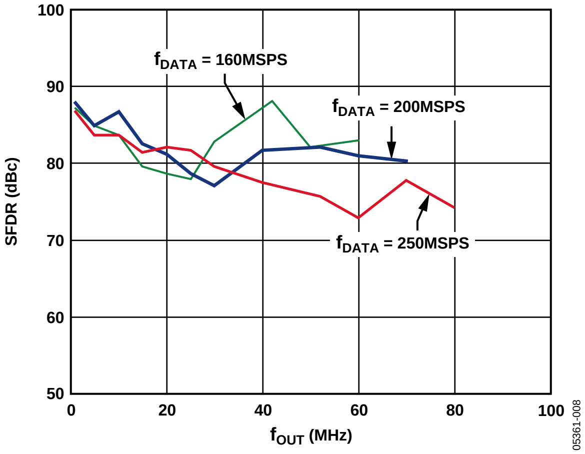


Figure 8. AD9779 In-Band SFDR vs. f_{OUT}, 2× Interpolation

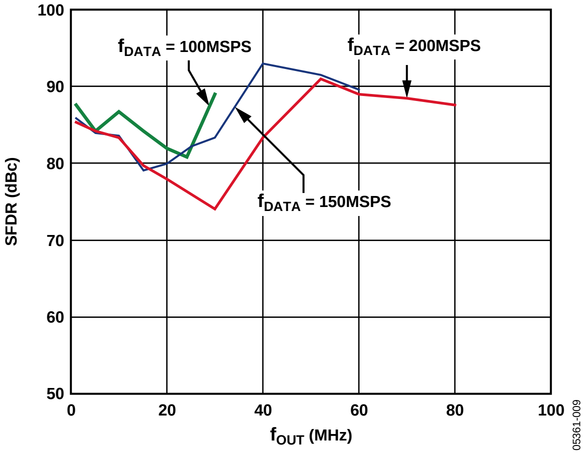


Figure 9. AD9779 In-Band SFDR vs. f_{OUT}, 4× Interpolation

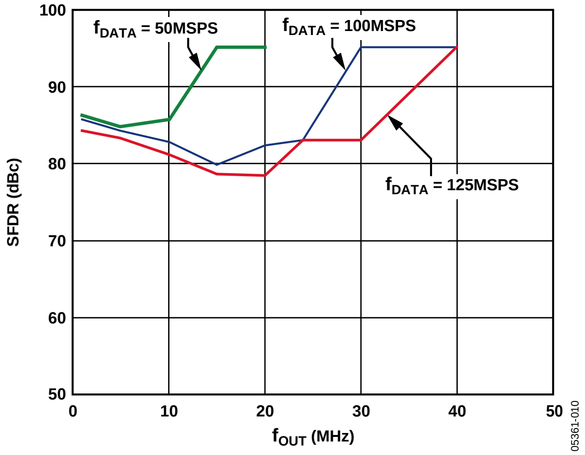


Figure 10. AD9779 In-Band SFDR vs. f_{OUT}, 8× Interpolation

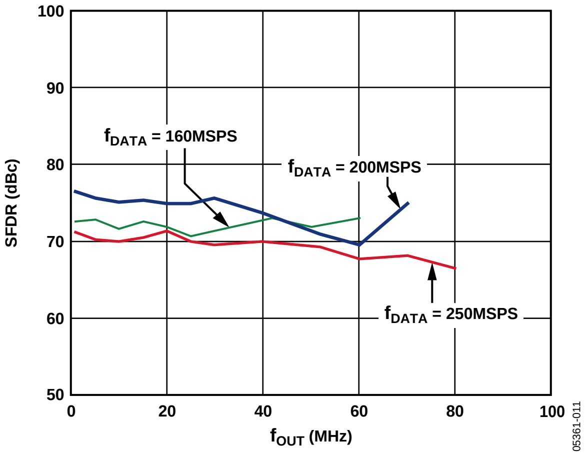


Figure 11. AD9779 Out-of-Band SFDR vs. f_{OUT}, 2× Interpolation

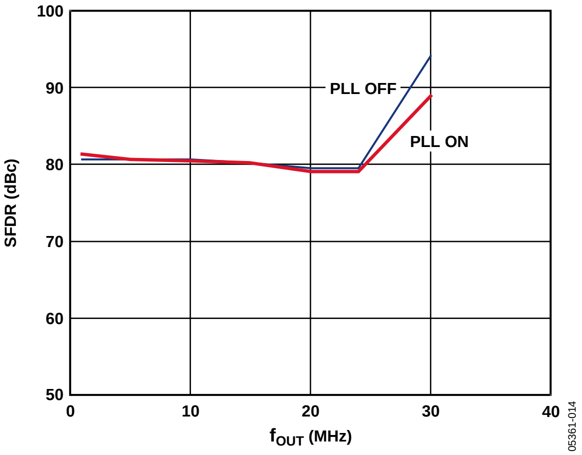


Figure 14. AD9779 In-Band SFDR, 4× Interpolation, f_{DATA} = 100 MSPS, PLL On/Off

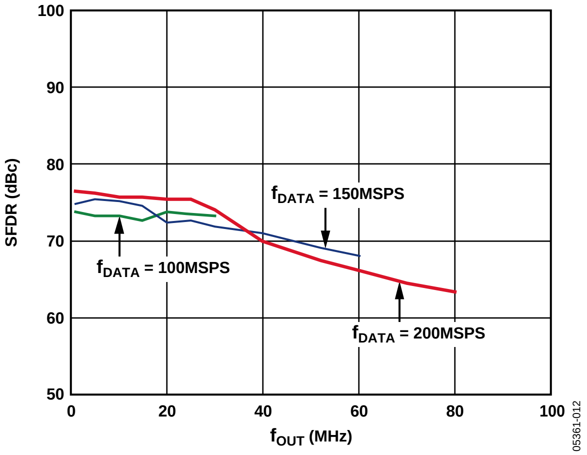


Figure 12. AD9779 Out-of-Band SFDR vs. f_{OUT}, 4× Interpolation

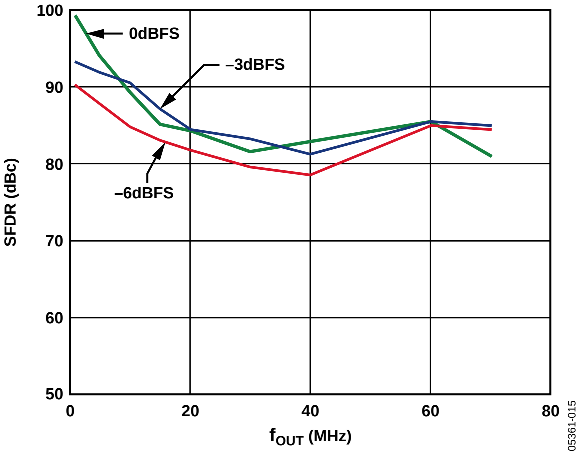


Figure 15. AD9779 In-Band SFDR vs. Digital Full-Scale Input

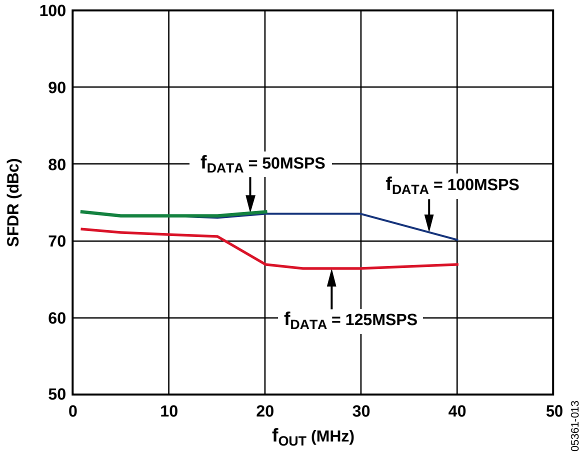


Figure 13. AD9779 Out-of-Band SFDR vs. f_{OUT}, 8× Interpolation

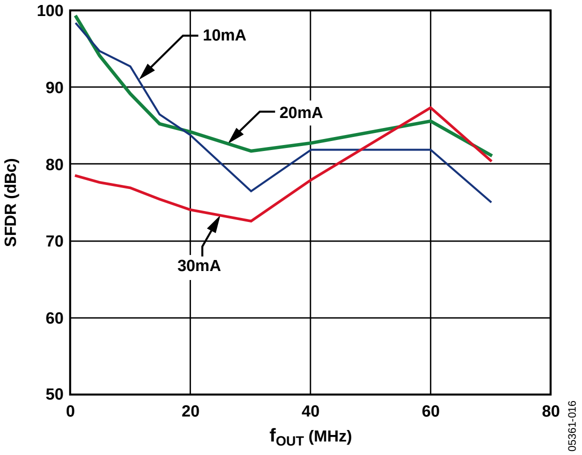


Figure 16. AD9779 In-Band SFDR vs. Output Full-Scale Current

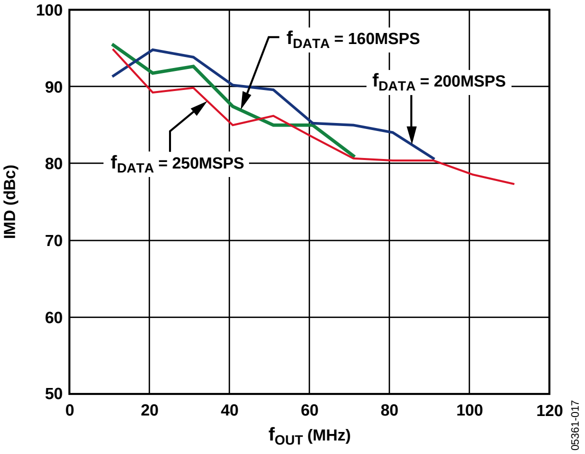


Figure 17. AD9779 Third Order IMD vs. f_{OUT}, 1× Interpolation

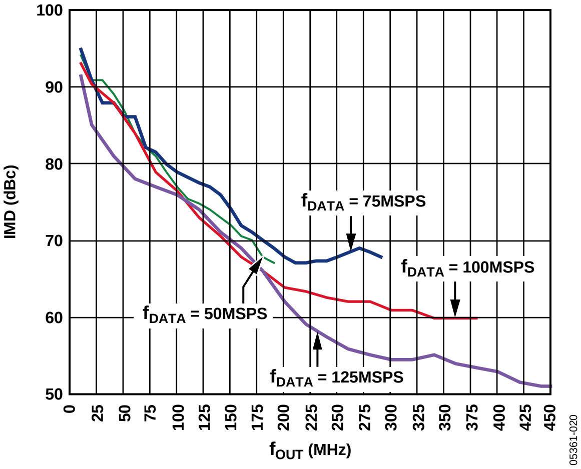


Figure 20. AD9779 Third Order IMD vs. f_{OUT}, 8× Interpolation

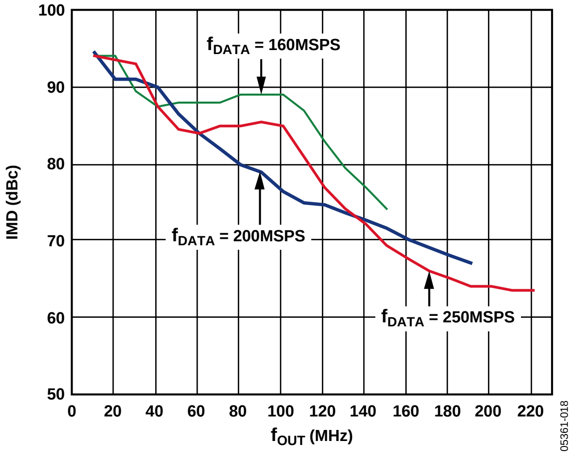


Figure 18. AD9779 Third Order IMD vs. f_{OUT}, 2× Interpolation

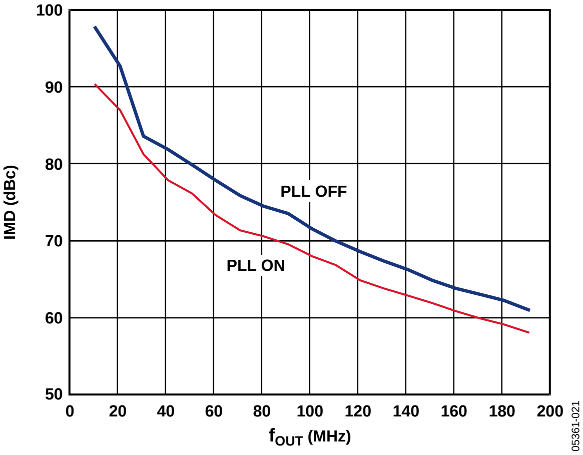


Figure 21. AD9779 Third Order IMD vs. f_{OUT}, 4× Interpolation, f_{DATA} = 100 MSPS, PLL On vs. PLL Off

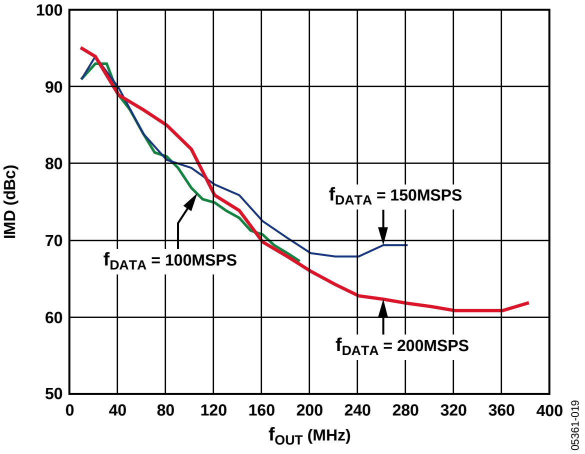


Figure 19. AD9779 Third Order IMD vs. f_{OUT}, 4× Interpolation

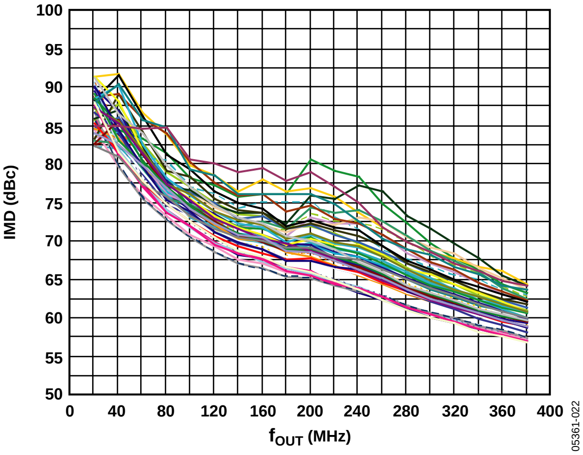


Figure 22. AD9779 Third Order IMD vs. f_{OUT}, over 50 Parts,4× Interpolation, f_{DATA} = 200 MSPS

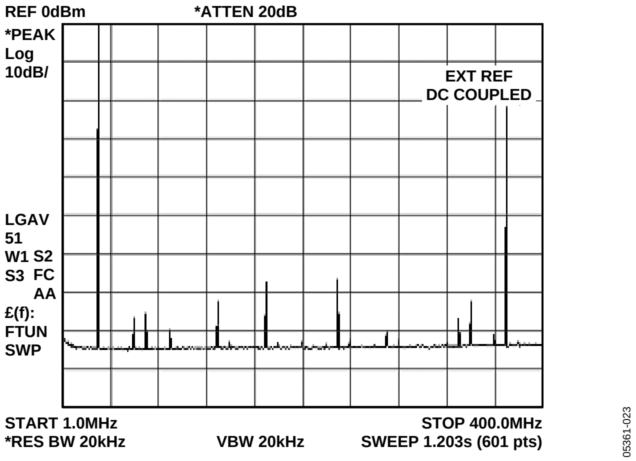


Figure 23. AD9779 Single Tone, 4× Interpolation, f_{DATA} = 100 MSPS, f_{OUT} = 30 MHz

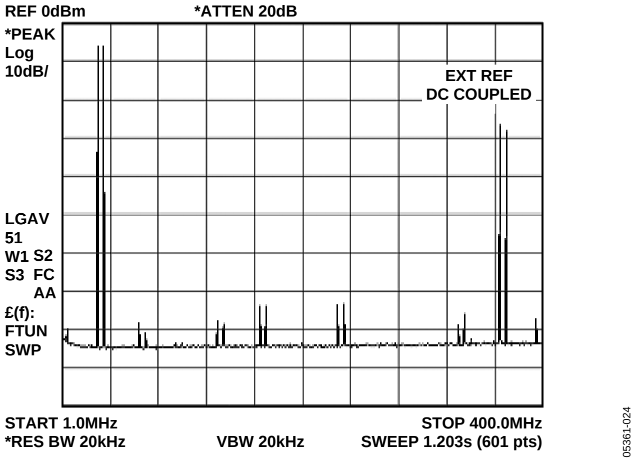


Figure 24. AD9779 Two-Tone Spectrum, 4× Interpolation, f_{DATA} = 100 MSPS, f_{OUT} = 30,35 MHz

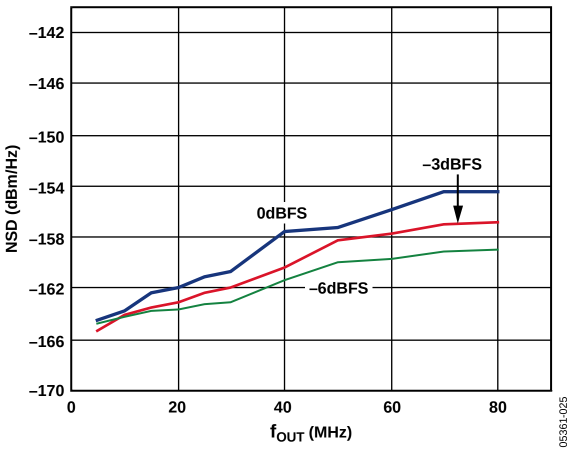


Figure 25. AD9779 Noise Spectral Density vs. Digital Full-Scale of Single-Tone Input, f_{DATA} = 200 MSPS, 2× Interpolation

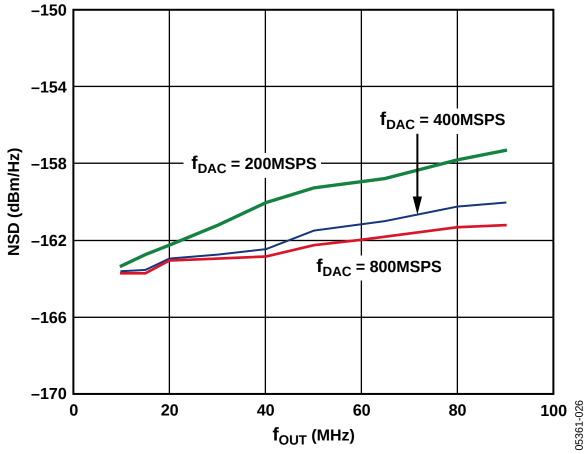


Figure 26. AD9779 Noise Spectral Density vs. f_{DAC}, Eight-Tone Input with 500 kHz Spacing, f_{DATA} = 200 MSPS

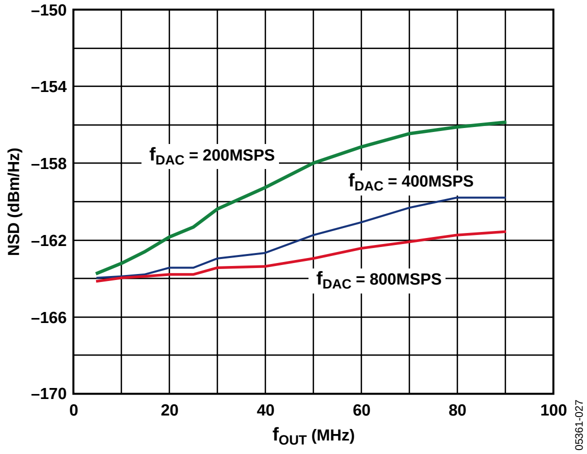


Figure 27. AD9779 Noise Spectral Density vs. f_{DAC}, Single-Tone Input at –6 dBFS

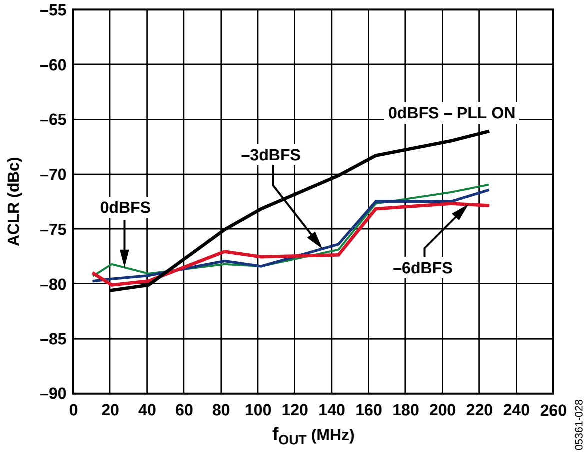
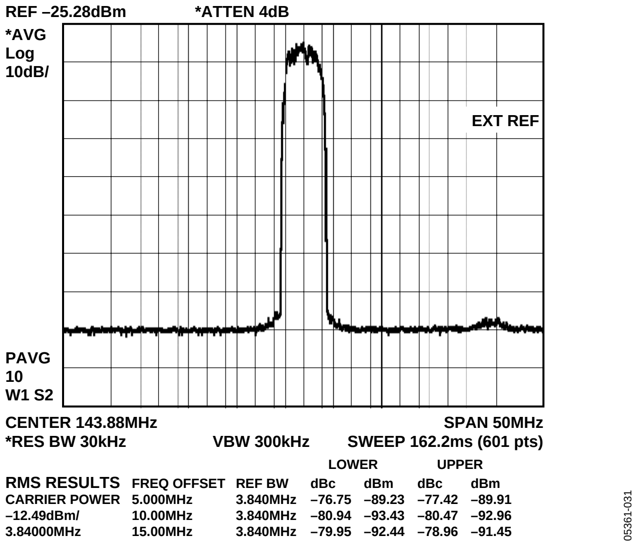


Figure 28. AD9779 ACLR for First Adjacent Band WCDMA, 4× Interpolation, f_{DATA} = 122.88 MSPS, On-Chip Modulation Translates Baseband Signal to IF



RMS RESULTS	FREQ OFFSET	REF BW	LOWER dBc	LOWER dBm	UPPER dBc	UPPER dBm
CARRIER POWER	5.000MHz	3.840MHz	–76.75	–89.23	–77.42	–89.91
–12.49dBm/	10.00MHz	3.840MHz	–80.94	–93.43	–80.47	–92.96
3.84000MHz	15.00MHz	3.840MHz	–79.95	–92.44	–78.96	–91.45

Figure 29. AD9779 WCDMA Signal, 4× Interpolation, f_{DATA} =122.88 MSPS, f_{DAC}/4 Modulation

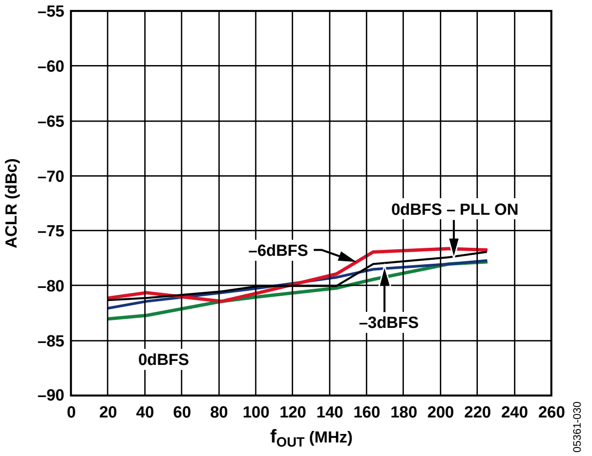


Figure 30. AD9779 ACLR for Third Adjacent Band WCDMA, 4× Interpolation, f_{DATA} = 122.88 MSPS, On-Chip Modulation Translates Baseband Signal to IF

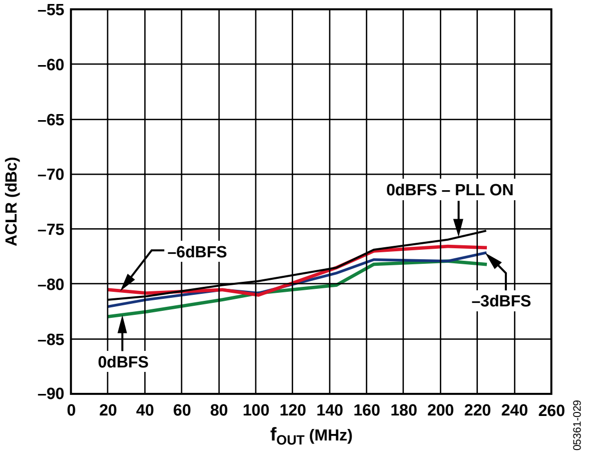
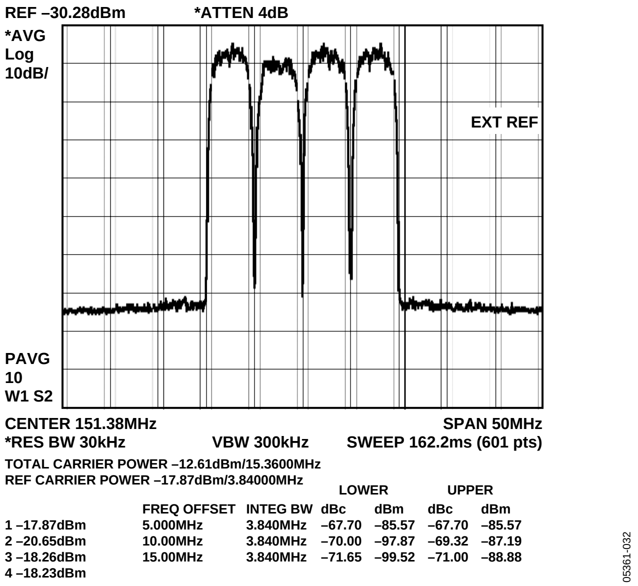


Figure 31. AD9779 ACLR for Second Adjacent Band WCDMA, 4× Interpolation, f_{DATA} = 122.88 MSPS. On-Chip Modulation Translates Baseband Signal to IF



TOTAL CARRIER POWER –12.61dBm/15.3600MHz
REF CARRIER POWER –17.87dBm/3.84000MHz

	FREQ OFFSET	INTEG BW	LOWER dBc	LOWER dBm	UPPER dBc	UPPER dBm
1 –17.87dBm	5.000MHz	3.840MHz	–67.70	–85.57	–67.70	–85.57
2 –20.65dBm	10.00MHz	3.840MHz	–70.00	–97.87	–69.32	–87.19
3 –18.26dBm	15.00MHz	3.840MHz	–71.65	–99.52	–71.00	–88.88
4 –18.23dBm						

Figure 32. AD9779 Multicarrier WCDMA Signal, 4× Interpolation, f_{DAC} =122.88 MSPS, f_{DAC}/4 Modulation

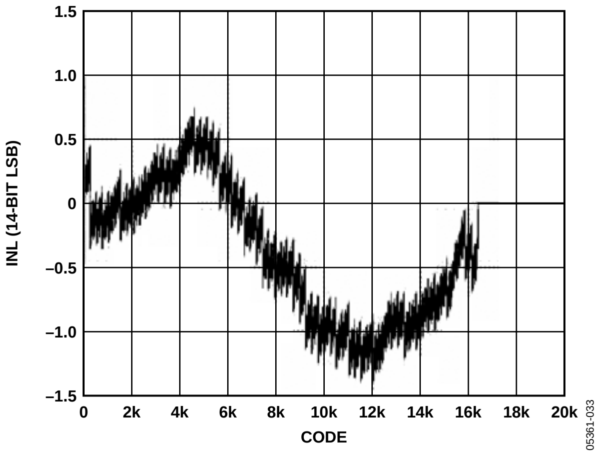


Figure 33. AD778 Typical INL

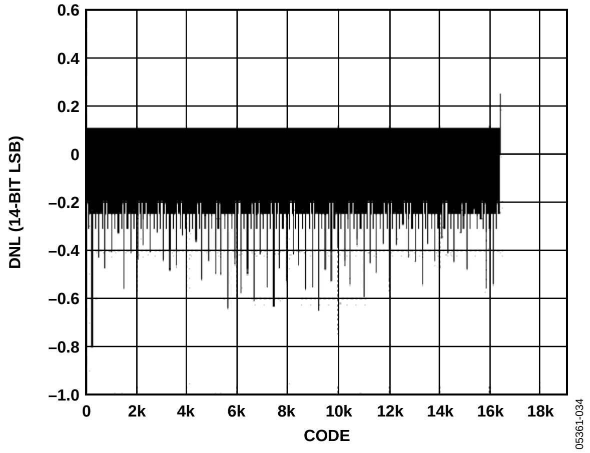


Figure 34. AD9778 Typical DNL

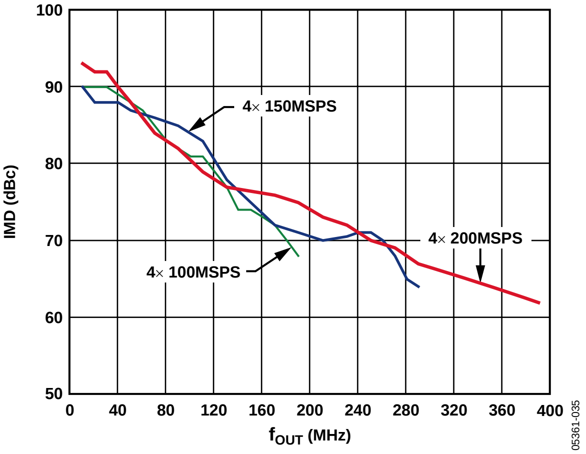


Figure 35. AD9778 IMD, 4× Interpolation

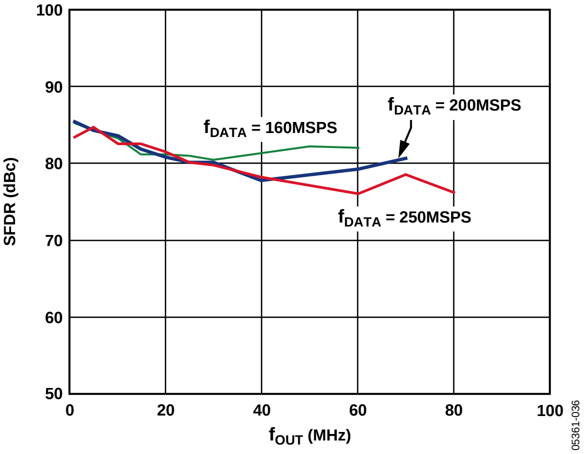


Figure 36. AD9778 In-Band SFDR, 2× Interpolation

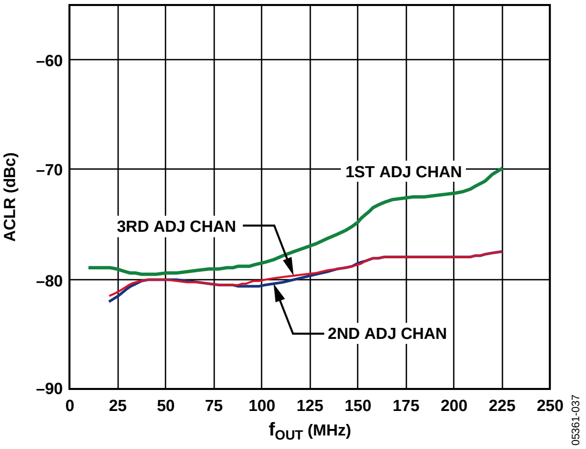
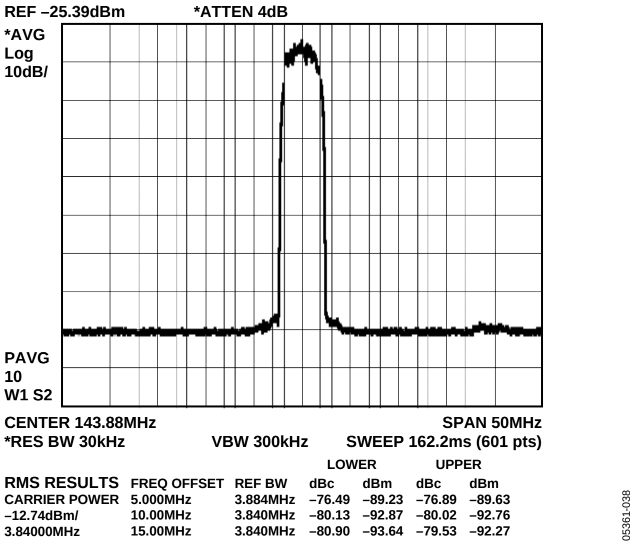


Figure 37. AD9778 ACLR, Single-Carrier WCDMA, 4× Interpolation, f_{DATA} = 122.88 MSPS, Amplitude = –3 dBFS



RMS RESULTS	FREQ OFFSET	REF BW	LOWER dBc	LOWER dBm	UPPER dBc	UPPER dBm
CARRIER POWER	5.000MHz	3.884MHz	−76.49	−89.23	−76.89	−89.63
−12.74dBm/	10.00MHz	3.840MHz	−80.13	−92.87	−80.02	−92.76
3.84000MHz	15.00MHz	3.840MHz	−80.90	−93.64	−79.53	−92.27

Figure 38. AD9778 ACLR, f_{DATA} = 122.88 MSPS, 4× Interpolation, f_{DAC}/4 Modulation

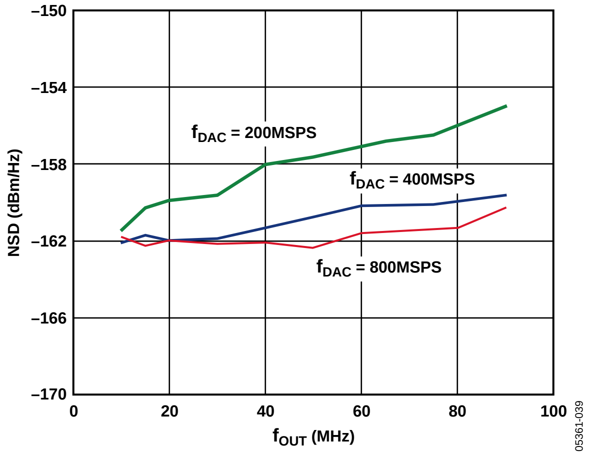


Figure 39. AD9778 Noise Spectral Density vs. f_{DAC} Eight-Tone Input with 500 kHz Spacing, f_{DATA} = 200 MSPS

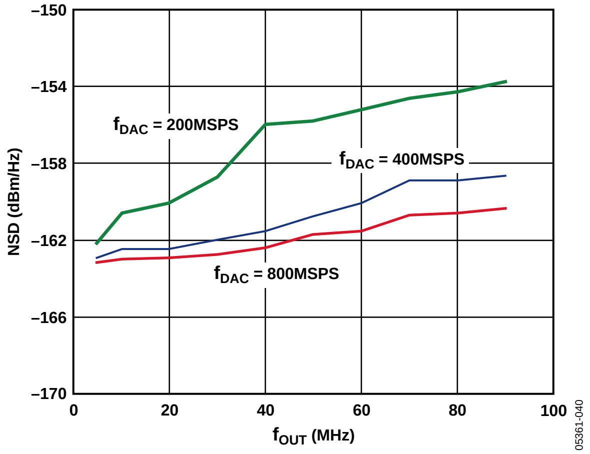


Figure 40. AD9778 Noise Spectral Density vs. f_{DAC} Single-Tone Input at –6 dBFS, f_{DATA} = 200 MSPS

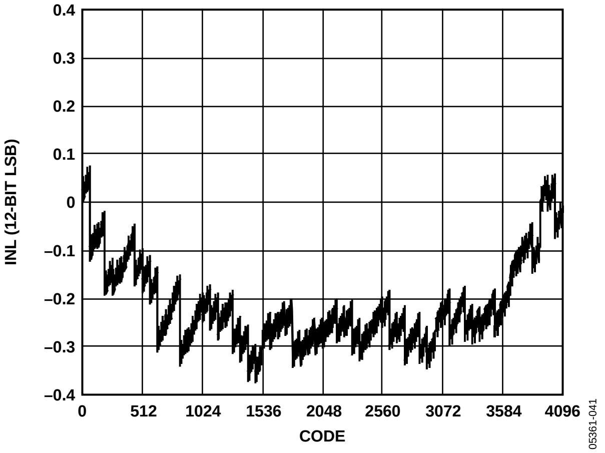


Figure 41. AD9776 Typical INL

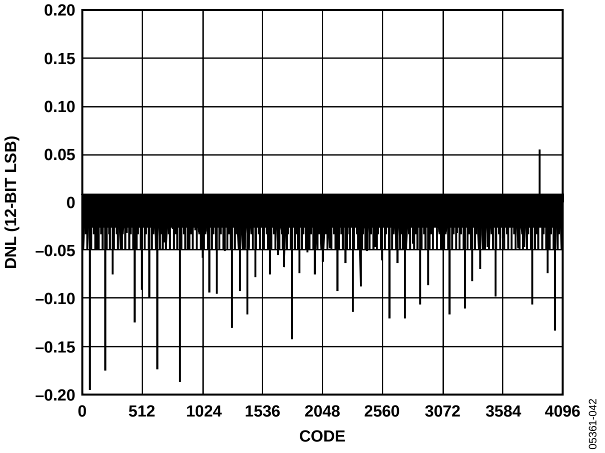


Figure 42. AD9776 Typical DNL

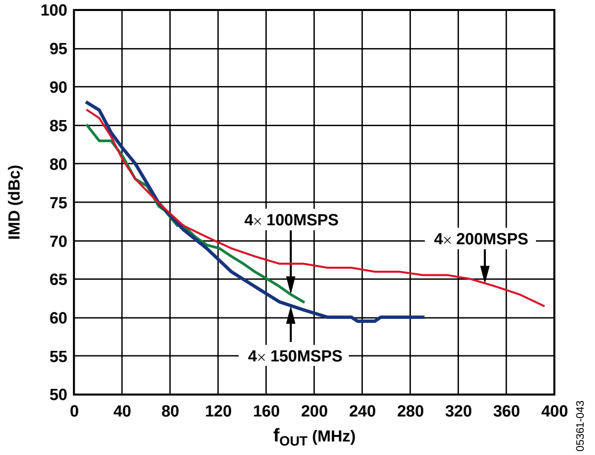


Figure 43. AD9776 IMD, 4× Interpolation

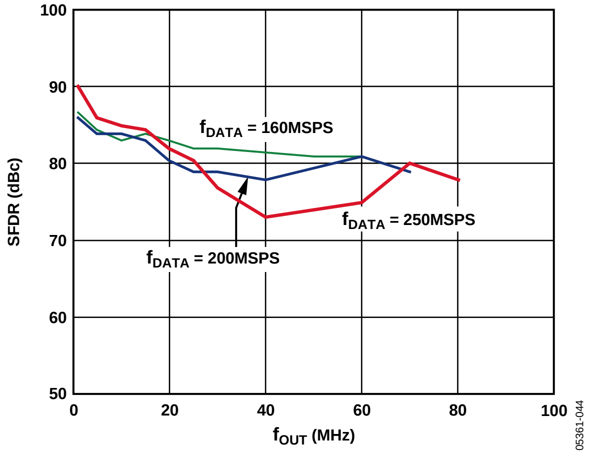


Figure 44. AD9776 In-Band SFDR, 2× Interpolation

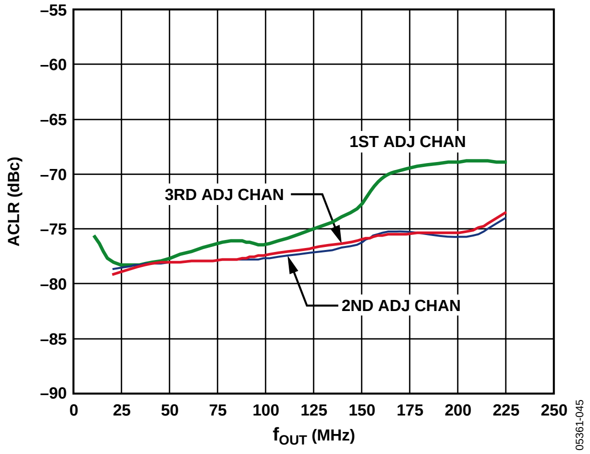
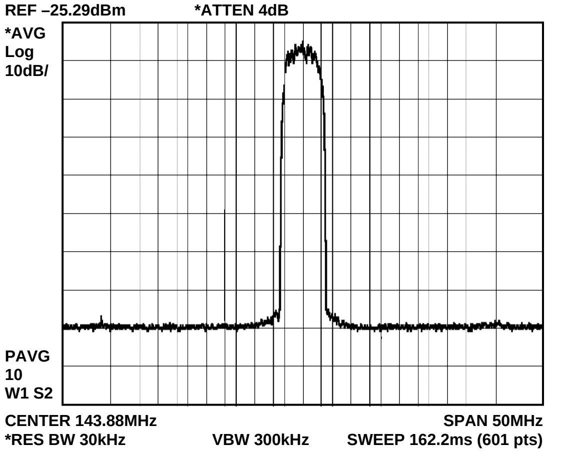


Figure 45. AD9776, Single Carrier WCDMA, 4× Interpolation, f_{DATA} = 122.88 MSPS, Amplitude = –3 dBFS



RMS RESULTS	FREQ OFFSET	REF BW	LOWER dBc	LOWER dBm	UPPER dBc	UPPER dBm
CARRIER POWER	5.000MHz	3.884MHz	–75.00	–87.67	–75.30	–87.97
–12.67dBm/	10.00MHz	3.840MHz	–78.05	–90.73	–77.99	–90.66
3.84000MHz	15.00MHz	3.840MHz	–77.73	–90.41	–77.50	–90.17

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Figure 46. AD9776 ACLR, f_{DATA} = 122.88 MSPS, 4× Interpolation, f_{DAC}/4 Modulation

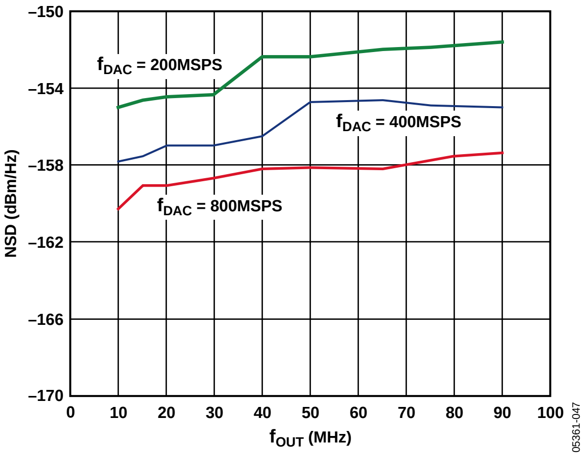

Figure 47. AD9776 Noise Spectral Density vs. f_{DAC}, Eight-Tone Input with 500 kHz Spacing, f_{DATA} = 200 MSPS

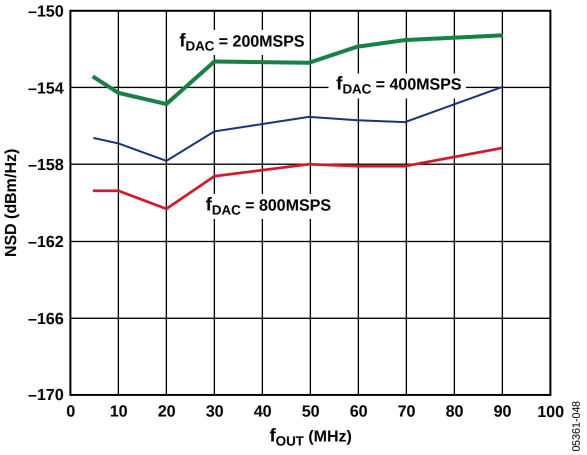

Figure 48. AD9776 Noise Spectral Density vs. f_{DAC}, Single-Tone Input at –6 dBFS, f_{DATA} = 200 MSPS

TERMINOLOGY

Linearity Error (Integral Nonlinearity or INL)
Linearity error is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

Differential Nonlinearity (DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity
A DAC is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
The deviation of the output current from the ideal of zero is called offset error. For I_{OUTA}, 0 mA output is expected when the inputs are all 0s. For I_{OUTB}, 0 mA output is expected when all inputs are set to 1.

Gain Error
The difference between the actual and ideal output span. The actual span is determined by the difference between the output when all inputs are set to 1 and the output when all inputs are set to 0.

Output Compliance Range
The range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits can cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per degree Celsius. For reference drift, the drift is reported in ppm per degree Celsius.

Power Supply Rejection
The maximum change in the full-scale output as the supplies are varied from minimum to maximum specified voltages.

Settling Time
The time required for the output to reach and remain within a specified error band around its final value, measured from the start of the output transition.

In-Band Spurious Free Dynamic Range (SFDR)
The difference, in decibels, between the peak amplitude of the output signal and the peak spurious signal between dc and the frequency equal to half the input data rate.

Out-of-Band Spurious Free Dynamic Range (SFDR)
The difference, in decibels, between the peak amplitude of the output signal and the peak spurious signal within the band that starts at the frequency of the input data rate and ends at the Nyquist frequency of the DAC output sample rate. Normally, energy in this band is rejected by the interpolation filters. This specification therefore defines how well the interpolation filters work and the effect of other parasitic coupling paths to the DAC output.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured fundamental. It is expressed as a percentage or in decibels.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

Interpolation Filter
If the digital inputs to the DAC are sampled at a multiple rate of f_{DATA} (interpolation rate), a digital filter can be constructed that has a sharp transition band near $f_{DATA}/2$. Images that typically appear around f_{DAC} (output data rate) can be greatly suppressed.

Adjacent Channel Leakage Ratio (ACLR)
The ratio in dBc between the measured power within a channel relative to its adjacent channel.

Complex Image Rejection
In a traditional two-part upconversion, two images are created around the second IF frequency. These images have the effect of wasting transmitter power and system bandwidth. By placing the real part of a second complex modulator in series with the first complex modulator, either the upper or lower frequency image near the second IF can be rejected.

THEORY OF OPERATION

The AD9776/AD9778/AD9779 combine many features that make them very attractive DACs for wired and wireless communications systems. The dual digital signal path and dual DAC structure allow an easy interface with common quadrature modulators when designing single sideband transmitters. The speed and performance of the parts allow wider bandwidths and more carriers to be synthesized than in previously available DACs. The digital engine uses a breakthrough filter architecture that combines the interpolation with a digital quadrature modulator. This allows the parts to do digital quadrature frequency upconversion. They also have features that allow simplified synchronization with incoming data and between multiple parts.

The serial port configuration is controlled by Reg. 0x00, Bits <6: 7>. It is important to note that the configuration changes immediately upon writing to the last bit of the byte. For multibyte transfers, writing to this register might occur during the middle of a communication cycle. Care must be taken to compensate for this new configuration for the remaining bytes of the current communication cycle.

The same considerations apply to setting the software reset, RESET (Reg. 0x00, Bit 5) or pulling the RESET pin (Pin 70) high. All registers are set to their default values, except Reg. 0x00 and Reg. 0x04, which remain unchanged.

Use of only single-byte transfers when changing serial port configurations or initiating a software reset is recommended to prevent unexpected device behavior.

As described in this section, all serial port data is transferred to/from the device in synchronization to the SCLK pin. If synchronization is lost, the device has the ability to asynchronously terminate an I/O operation, putting the serial port controller into a known state and thereby regaining synchronization.

SERIAL PERIPHERAL INTERFACE

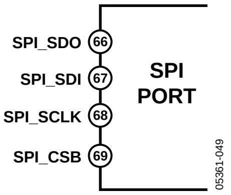

Figure 49. SPI Port

The serial port is a flexible, synchronous serial communications port allowing easy interface to many industry-standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola SPI® and Intel® SSR protocols. The interface allows read/write access to all registers that configure the AD9776/AD9778/AD9779. Single or multiple byte transfers are supported, as well as MSB-first or LSB-first transfer formats. The serial interface ports can be configured as a single pin I/O (SDIO) or two unidirectional pins for input/output (SDIO/SDO).

General Operation of the Serial Interface

There are two phases to a communication cycle with the AD977x. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the device, coincident with the first eight SCLK rising edges. The instruction byte provides the serial port controller with information regarding the data transfer cycle, which is Phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is a read or write, the number of bytes in the data transfer, and the starting register address for the first byte of the data transfer. The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the device.

A logic high on the CSB pin followed by a logic low resets the SPI port timing to the initial state of the instruction cycle. From this state, the next eight rising SCLK edges represent the instruction bits of the current I/O operation, regardless of the state of the internal registers or the other signal levels at the inputs to the SPI port. If the SPI port is in the midst of an instruction cycle or a data transfer cycle, none of the present data is written.

The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the device and the system controller. Phase 2 of the communication cycle is a transfer of 1, 2, 3, or 4 data bytes as determined by the instruction byte. Using one multibyte transfer is preferred. Single-byte data transfers are useful to reduce CPU overhead when register access requires only one byte. Registers change immediately upon writing to the last bit of each transfer byte.

Instruction Byte

The instruction byte contains the information shown in Table 8.

Table 8. SPI Instruction Byte

MSB **LSB**

I7	I6	I5	I4	I3	I2	I1	I0
R/W	N1	N0	A4	A3	A2	A1	A0

R/W, Bit 7 of the instruction byte, determines whether a read or a write data transfer occurs after the instruction byte write. Logic high indicates a read operation. Logic 0 indicates a write operation.

N1 and N0, Bits 6 and 5 of the instruction byte, determine the number of bytes to be transferred during the data transfer cycle. The bit decodes are shown in Table 9.

A4, A3, A2, A1, and A0—Bits 4, 3, 2, 1, and 0, respectively, of the instruction byte—determine which register is accessed during the data transfer portion of the communications cycle. For multibyte transfers, this address is the starting byte address. The remaining register addresses are generated by the device based on the LSB-first bit (Reg. 0x00, Bit 6).

Table 9. Byte Transfer Count

N0	N1	Description
0	0	Transfer one byte
0	1	Transfer two bytes
1	0	Transfer three bytes
1	1	Transfer four bytes

Serial Interface Port Pin Descriptions

Serial Clock (SCLK)

The serial clock pin is used to synchronize data to and from the device and to run the internal state machines. SCLK's maximum frequency is 40 MHz. All data input is registered on the rising edge of SCLK. All data is driven out on the falling edge of SCLK.

Chip Select (CSB)

Active low input starts and gates a communication cycle. It allows more than one device to be used on the same serial communications lines. The SDO and SDIO pins go to a high impedance state when this input is high. Chip select should stay low during the entire communication cycle.

Serial Data I/O (SDIO)

Data is always written into the device on this pin. However, this pin can be used as a bidirectional data line. The configuration of this pin is controlled by Register 0x00, Bit 7. The default is Logic 0, which configures the SDIO pin as unidirectional.

Serial Data Out (SDO)

Data is read from this pin for protocols that use separate lines for transmitting and receiving data. In the case where the device operates in a single bidirectional I/O mode, this pin does not output data and is set to a high impedance state.

MSB/LSB TRANSFERS

The serial port can support both MSB-first and LSB-first data formats. This functionality is controlled by Register Bit LSB first (Reg. 0x00, Bit 6). The default is MSB first (LSB first = 0).

When LSB first = 0 (MSB first) the instruction and data bit must be written from MSB to LSB. Multibyte data transfers in MSB-first format start with an instruction byte that includes the register address of the most significant data byte. Subsequent data bytes should follow from high address to low address. In MSB-first mode, the serial port internal byte address generator decrements for each data byte of the multibyte communication cycle.

When LSB first = 1 (LSB first) the instruction and data bit must be written from LSB to MSB. Multibyte data transfers in LSB-first format start with an instruction byte that includes the register address of the least significant data byte followed by multiple data bytes. The serial port internal byte address generator increments for each byte of the multibyte communication cycle.

The serial port controller data address decrements from the data address written toward 0x00 for multibyte I/O operations if the MSB-first mode is active. The serial port controller address increments from the data address written toward 0x1F for multibyte I/O operations if the LSB-first mode is active.

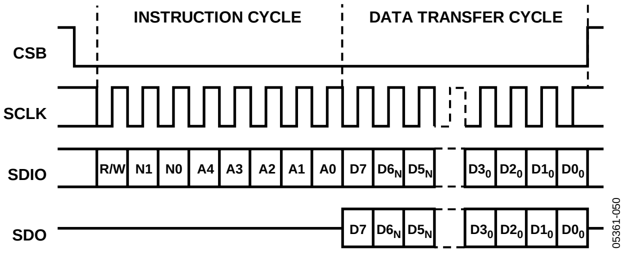
INSTRUCTION CYCLE
DATA TRANSFER CYCLE
CSB
SCLK
SDIO
SDO
R/W N1 N0 A4 A3 A2 A1 A0 D7 D6N D5N
D30 D20 D10 D00
D7 D6N D5N
D30 D20 D10 D00
05361-050

Figure 50. Serial Register Interface Timing MSB First

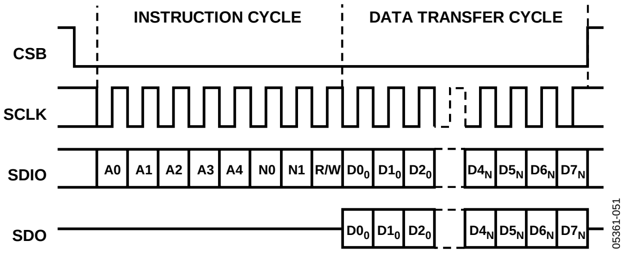
INSTRUCTION CYCLE
DATA TRANSFER CYCLE
CSB
SCLK
SDIO
SDO
A0 A1 A2 A3 A4 N0 N1 R/W D00 D10 D20
D4N D5N D6N D7N
D00 D10 D20
D4N D5N D6N D7N
05361-051

Figure 51. Serial Register Interface Timing LSB First

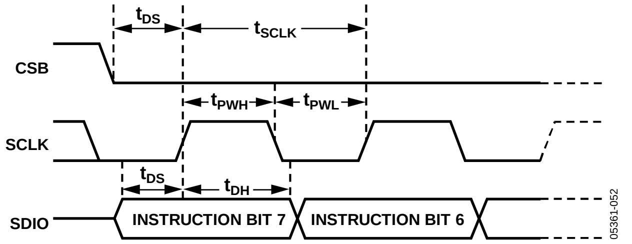
tDS
tSCLK
CSB
tPWH
tPWL
SCLK
tDS
tDH
SDIO
INSTRUCTION BIT 7
INSTRUCTION BIT 6
05361-052

Figure 52. Timing Diagram for SPI Register Write

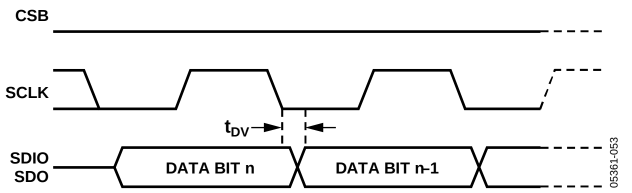
CSB
SCLK
tDV
SDIO
SDO
DATA BIT n
DATA BIT n-1
05361-053

Figure 53. Timing Diagram for SPI Register Read

SPI REGISTER MAP

Table 10.

Register Name	Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Comm	0x00	00	SDIO Bidirectional	LSB/MSB First	Software Reset	Power-Down Mode	Auto Power-Down Enable		PLL Lock Indicator (Read Only)		0x00
Digital Control	0x01	01	Filter Interpolation Factor <1:0>		Filter Modulation Mode <3:0>					Zero Stuffing Enable	0x00
	0x02	02	Data Format	Dual/Interleaved Data Bus Mode	Real Mode	Data Clock Delay Enable	Inverse Sinc Enable	DATACLK Invert	TxEnable Invert	Q First	0x00
Sync Control	0x03	03	Data Clock Delay Mode <1:0>		Data Clock Divide Ratio <1:0>		Reserved				0x00
	0x04	04	Data Clock Delay <3:0>				Output Sync Pulse Divide <2:0>			Sync Out Delay <4>	0x00
	0x05	05	Sync Out Delay <3:0>				Input Sync Pulse Frequency Ratio <2:0>			Sync Input Delay <4>	0x00
	0x06	06	Sync Input Delay <3:0>				Input Sync Pulse Timing Error Tolerance <3:0>				0x00
	0x07	07	Sync Receiver Enable	Sync Driver Enable	Sync Triggering Edge	DAC Clock Offset <4:0>					0x00
PLL Control	0x08	08	PLL Band Select <5:0>						PLL VCO AGC Gain <1:0>		0xCF
	0x09	09	PLL Enable	PLL VCO Divider Ratio <1:0>		PLL Loop Divide Ratio <1:0>		PLL Bias Setting <2:0>			0x37
Misc Control	0x0A	10	PLL Control Voltage Range <2:0> (Read Only)			PLL Loop Bandwidth Adjustment <4:0>					0x38
I DAC Control Register	0x0B	11	I DAC Gain Adjustment<7:0>								0xF9
	0x0C	12	I DAC Sleep	I DAC Power Down					I DAC Gain Adjustment <9:8>		0x01
Aux DAC1 Control Register	0x0D	13	Auxiliary DAC1 Data <7:0>								0x00
	0x0E	14	Auxiliary DAC1 Sign	Auxiliary DAC1 Current Direction	Auxiliary DAC1 Power-Down				Auxiliary DAC1 Data <9:8>		0x00
Q DAC Control Register	0x0F	15	Q DAC Gain Adjustment <7;0>								0xF9
	0x10	16	Q DAC Sleep	Q DAC Power-Down					Q DAC Gain Adjustment <9:8>		0x01
Aux DAC2 Control Register	0x11	17	Auxiliary DAC2 Data <7:0>								0x00
	0x12	18	Auxiliary DAC2 Sign	Auxiliary DAC2 Current Direction	Auxiliary DAC2 Power-Down				Auxiliary DAC2 Data <9:8>		0x00
	0x13 to 0x18	19 to 24	Reserved								
Interrupt Register	0x19	25		Sync Delay IRQ				Sync Delay IRQ Enable		Internal Sync Loopback	0x00
	0x1A to 0x1F	26 to 31	Reserved								

Table 11. SPI Register Description

Register Name	Address Hex	Address Decimal	Name	Function	Default
Comm Register	00	7	SDIO Bidirectional	0: Use SDIO pin as input data only 1: Use SDIO as both input and output data	0
	00	6	LSB/MSB First	0: First bit of serial data is MSB of data byte 1: First bit of serial data is LSB of data byte	0
	00	5	Software Reset	Bit must be written with a 1, then 0 to soft reset SPI register map	0
	00	4	Power-Down Mode	0: All circuitry is active 1: Disable all digital and analog circuitry, only SPI port is active	
	00	3	Auto Power-Down Enable	Controls auto power-down mode, see Power-Down and Sleep Modes section	0
	00	1	PLL Lock (Read Only)	0: PLL is not locked 1: PLL is locked	0
Digital Control Register	01	7:6	Filter Interpolation Factor	00:1× interpolation 01:2× interpolation 10:4× interpolation 11:8× interpolation	00
	01	5:2	Filter Modulation Mode	See Table 19 for filter modes	0000
	01	0	Zero Stuffing	0: Zero stuffing off 1: Zero stuffing on	0
	02	7	Data Format	0: Signed binary 1: Unsigned binary	0
	02	6	Dual/Interleaved Data Bus Mode	0: Both input data ports receive data 1: Data port 1 only receives data	0
	02	5	Real Mode	0: Enable Q path for signal processing 1: Disable Q path data (internal Q channel clocks disabled, I and Q modulators disabled)	0
	02	3	Inverse Sinc Enable	0: Inverse sinc filter disabled 1: Inverse sinc filter enabled	0
	02	2	DATACLK Invert	0: Output DATACLK same phase as internal capture clock 1: Output DATACLK opposite phase as internal capture clock	0
	02	1	TxEnable Invert	Inverts the function of TxEnable Pin 39, see Interleaved Data Mode section	0
	02	0	Q First	0: First byte of data is always I data at beginning of transmit 1: First byte of data is always Q data at beginning of transmit	
Sync Control Register	03	7:6	Data Clock Delay Mode	00: Manual, no error correction	00
	03	5:4	Extra Data Clock Divide Ratio	Data Clock Output Divider (see Table 22 for Divider Ratio)	00
	03	3:0	Reserved		000
	04	7:4	Data Clock Delay	Sets delay of DACCLK in to DATACLK out	0000
	04	3:1	Output Sync Pulse Divide	Sets frequency of Sync_O pulses	000
	04	0	Sync Out Delay	Sync Output Delay, Bit 4	
	05	7:4	Sync Out Delay	Sync Output Delay, Bit <3:0>	0
	05	3:1	Input Sync Pulse Frequency	Input Sync Pulse Frequency Divider, see the Sync Pulse Receiver (Slave Devices) section	000
	05	0	Sync Input Delay	Sync Input Delay, Bit 4	0

Register Name	Address		Name	Function	Default
	Hex	Decimal			
Sync Control Register	06	7:4	Sync Input Delay	See Multi-DAC Synchronization section for details on using these registers to synchronize multiple DACs.	0
	06	3:0	Input Sync Pulse Timing Error Tolerance		0
	07	7	Sync Receiver Enable		0
	07	6	Sync Driver Enable		0
	07	5	Sync Triggering Edge		0
	07	4:0	Sync_I to Input Data Sampling Clock Offset		0
PLL Control	08	7:2	PLL Band Select	VCO frequency range vs. PLL band select value (see Table 17)	110011
	08	1:0	VCO AGC Gain Control	Lower number (low gain) is generally better for performance.	11
	09	7	PLL Enable	0: PLL off, DAC rate clock supplied by outside source 1: PLL on, DAC rate clock synthesized internally from external reference clock via PLL clock multiplier	0
	09	6:5	PLL VCO Divide Ratio	FVCO/f_{DAC} 00 × 1 01 × 2 10 × 4 11 × 8	
	09	4:3	PLL Loop Divide Ratio	f_{DAC}/f_{REF} 00 × 2 01 × 4 10 × 8 11 × 16	
	09	2:0	PLL Bias Setting	Always set to 111	111
Misc Control	0A	7:5	PLL Control Voltage Range	000 to 111, proportional to voltage at PLL loop filter output, readback only	
	0A	4:0	PLL Loop Bandwidth Adjustment	See PLL Loop Filter Bandwidth section for details	
I DAC Control Register	0B	7:0	I DAC Gain Adjustment	(7:0) LSB slice of 10-bit gain setting word for I DAC	11111001
	0C	7	I DAC Sleep	0: I DAC on 1: I DAC off	0
	0C	6	I DAC Power-Down	0: I DAC on 1: I DAC off	0
	0C	1:0	I DAC Gain Adjustment	(9:8) MSB slice of 10-bit gain setting word for I DAC	01
Aux DAC1 Control Register	0D	7:0	Aux DAC1 Gain Adjustment	(7:0) LSB slice of 10-bit gain setting word for Aux DAC1	00000000
	0E	7	Aux DAC1 Sign	0: Positive 1: Negative	
	0E	6	Aux DAC1 Current Direction	0: Source 1: Sink	0
	0E	5	Aux DAC1 Power-Down	0: Aux DAC1 on 1: Aux DAC1 off	0
	0E	1:0	Aux DAC1 Gain Adjustment	(9:8) MSB slice of 10 bit gain setting word for Aux DAC1	00

Register Name	Address		Name	Function	Default
	Hex	Decimal			
Q DAC Control Register	0F	7:0	Q DAC Gain Adjustment	(7:0) LSB slice of 10-bit gain setting word for Q DAC	11111001
	10	7	Q DAC Sleep	0: Q DAC on 1: Q DAC off	0
	10	6	Q DAC Power-Down	0: Q DAC on 1: Q DAC off	0
	10	1:0	Q DAC Gain Adjustment	(9:8) MSB slice of 10-bit gain setting word for Q DAC	
Aux DAC2 Control Register	11	7:0	Aux DAC2 Gain Adjustment	(7:0) LSB slice of 10-bit gain setting word for Aux DAC2	00000000
	12	7	Aux DAC2 Sign	0: Positive 1: Negative	
	12	6	Aux DAC2 Current Direction	0: Source 1: Sink	0
	12	5	Aux DAC2 Power-Down	0: Aux DAC 2 on 1: Aux DAC 2 off	0
	12	1:0	Aux DAC2 Gain Adjustment	(9:8) MSB slice of 10-bit gain setting word for Aux DAC2	00
Interrupt Register	19	7			0
	19	6	Sync Delay IRQ	Readback , must write 0 to clear	0
	19	5			0
	19	3			0
	19	2	Sync Delay IRQ Enable		0
	19	1			0
	19	0	Internal Sync Loopback		0

INTERPOLATION FILTER ARCHITECTURE

The AD9776/AD9778/AD9779 can provide up to 8× interpolation or disable the interpolation filters entirely. It is important to note that the input signal should be backed off by approximately 0.01 dB from full scale to avoid overflowing the interpolation filters. The coefficients of the low-pass filters and the inverse sinc filter are given in Table 12, Table 13, Table 14,and Table 15. Spectral plots for the filter responses are shown in Figure 54, Figure 55, and Figure 56.

Table 12. Halfband Filter 1

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(55)	−4
H(2)	H(54)	0
H(3)	H(53)	13
H(4)	H(52)	0
H(5)	H(51)	−34
H(6)	H(50)	0
H(7)	H(49)	72
H(8)	H(48)	0
H(9)	H(47)	−138
H(10)	H(46)	0
H(11)	H(45)	245
H(12)	H(44)	0
H(13)	H(43)	−408
H(14)	H(42)	0
H(15)	H(41)	650
H(16)	H(40)	0
H(17)	H(39)	−1003
H(18)	H(38)	0
H(19)	H(37)	1521
H(20)	H(36)	0
H(21)	H(35)	−2315
H(22)	H(34)	0
H(23)	H(33)	3671
H(24)	H(32)	0
H(25)	H(31)	−6642
H(26)	H(30)	0
H(27)	H(29)	20755
H(28)		32768

Table 13. Halfband Filter 2

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(23)	−2
H(2)	H(22)	0
H(3)	H(21)	17
H(4)	H(20)	0
H(5)	H(19)	−75
H(6)	H(18)	0
H(7)	H(17)	238
H(8)	H(16)	0
H(9)	H(15)	−660
H(10)	H(14)	0
H(11)	H(13)	2530
H(12)		4096

Table 14. Halfband Filter 3

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(15)	−39
H(2)	H(14)	0
H(3)	H(13)	273
H(4)	H(12)	0
H(5)	H(11)	−1102
H(6)	H(10)	0
H(7)	H(9)	4964
H(8)		8192

Table 15. Inverse Sinc Filter

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(9)	2
H(2)	H(8)	−4
H(3)	H(7)	10
H(4)	H(6)	−35
H(5)		401

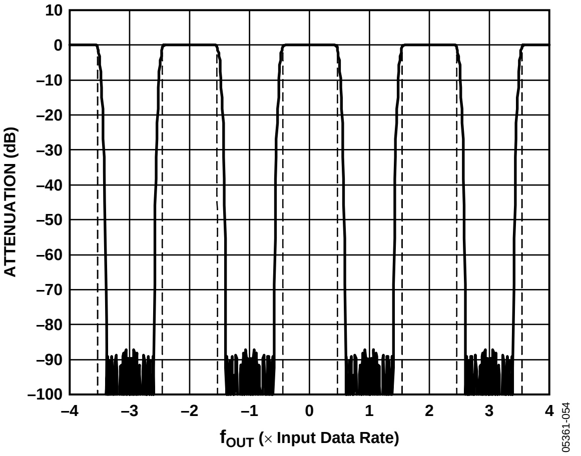

Figure 54. 2× Interpolation, Low-Pass Response to ±4× Input Data Rate (Dotted Lines Indicate 1 dB Roll-Off)

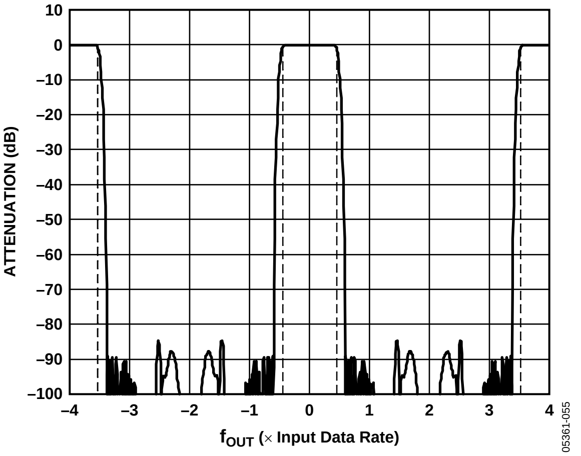

Figure 55. 4× Interpolation, Low-Pass Response to ±4× Input Data Rate (Dotted Lines Indicate 1 dB Roll-Off)

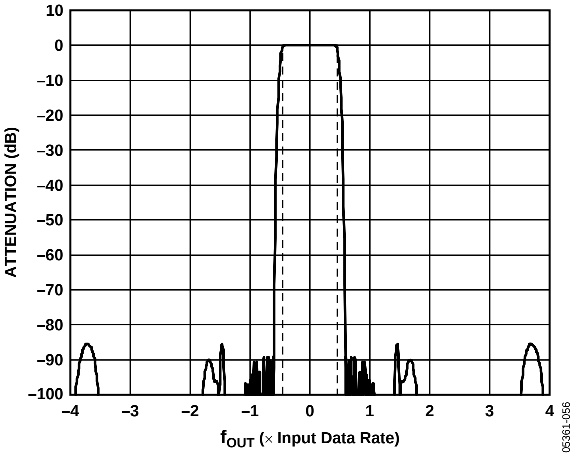

Figure 56. 8× Interpolation, Low-Pass Response to ±4× Input Data Rate (Dotted Lines Indicate 1 dB Roll-Off)

With the interpolation filter and modulator combined, the incoming signal can be placed anywhere within the Nyquist region of the DAC output sample rate. When the input signal is complex, this architecture allows modulation of the input signal to positive or negative Nyquist regions (see Table 16).

The Nyquist regions of up to 4× the input data rate can be seen in Figure 57.

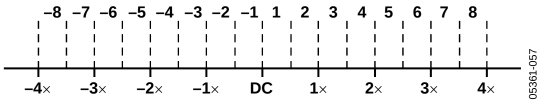

Figure 57. Nyquist Zones

Figure 54, Figure 55, and Figure 56 show the low-pass response of the digital filters with no modulation used. By turning on the modulation feature, the response of the digital filters can be tuned to anywhere within the DAC bandwidth. As an example, Figure 58 to Figure 64 show the nonshifted mode filter responses (refer to Table 16 for shifted/nonshifted mode filter responses).

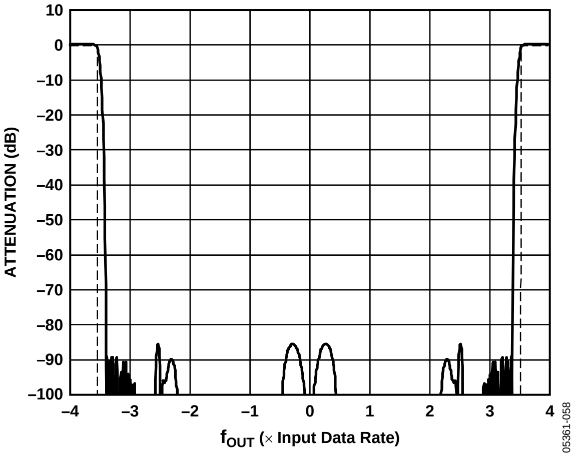

Figure 58. Interpolation/Modulation Combination of $4f_{DAC}/8$ Filter

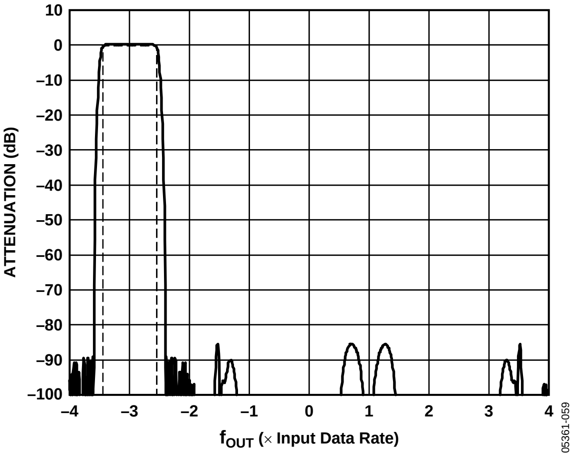

Figure 59. Interpolation/Modulation Combination of $-3f_{DAC}/8$ Filter

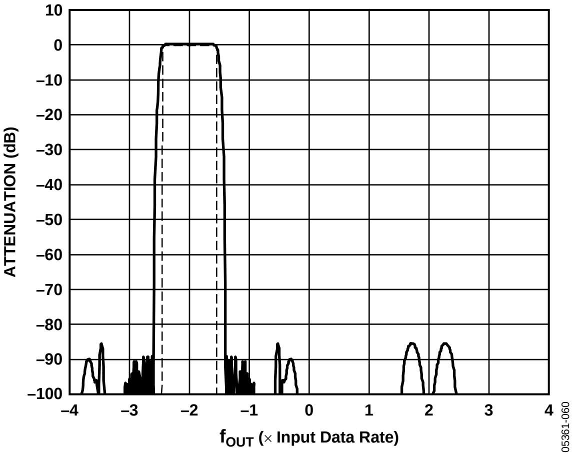

Figure 60. Interpolation/Modulation Combination of $-2f_{DAC}/8$ Filter

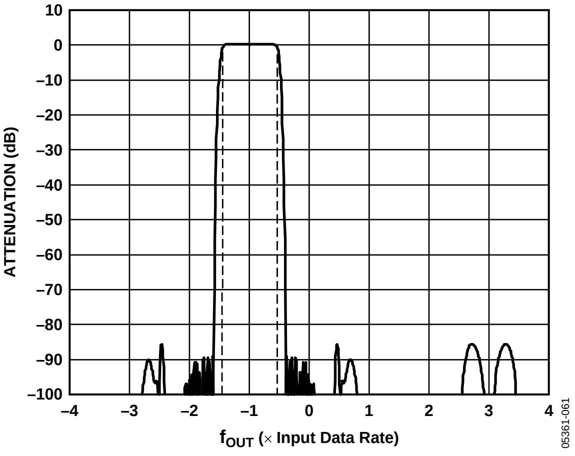

Figure 61. Interpolation/Modulation Combination of $-1f_{DAC}/8$ Filter

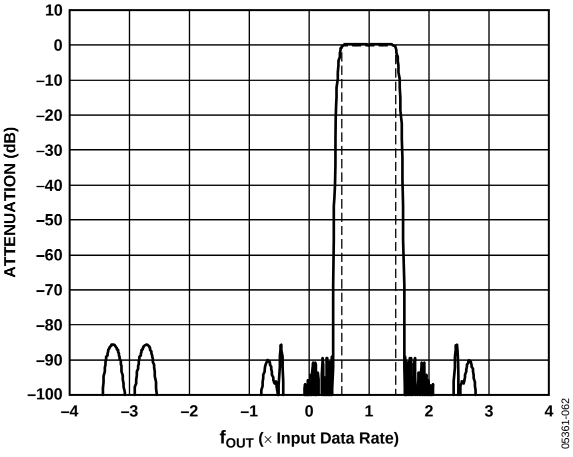

Figure 62. Interpolation/Modulation Combination of $f_{DAC}/8$ Filter

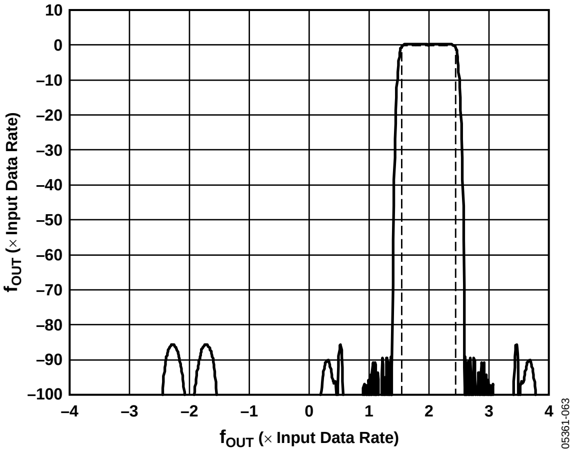

Figure 63. Interpolation/Modulation Combination of $2f_{DAC}/8$ Filter in Odd Mode

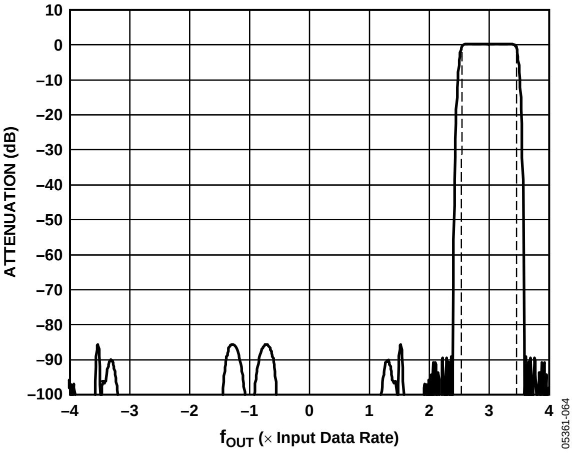

Figure 64. Interpolation/Modulation Combination of $3f_{DAC}/8$ Filter in Odd Mode

Shifted mode filter responses allow the pass band to be centered around ±0.5, ±1.5, ±2.5, and ±3.5 f_{DATA}. Switching to the shifted mode response does not modulate the signal. Instead, the pass band is simply shifted. For example, picture the response shown in Figure 64 and assume the signal in-band is a complex signal over the bandwidth 3.2 f_{DATA} to 3.3 f_{DATA}. If the even mode filter response is then selected, the pass band becomes centered at 3.5 f_{DATA}. However, the signal remains at the same place in the spectrum. The shifted mode capability allows the filter pass band to be placed anywhere in the DAC Nyquist bandwidth.

The AD9776/AD9778/AD9779 are dual DACs with internal complex modulators built into the interpolating filter response. In dual channel mode, the devices expect the real and the imaginary components of a complex signal at Digital Input Port 1 and Digital Input Port 2 (I and Q respectively). The DAC outputs then represent the real and imaginary components of the input signal, modulated by the complex carrier $f_{DAC}/2$, $f_{DAC}/4$, or $f_{DAC}/8$.

With Reg. 2, Bit 6 set, the device accepts interleaved data on Port 1 in the I, Q, I, Q ... sequence. Note that in interleaved mode, the channel data rate at the beginning of the I and the Q data paths are now half the input data rate because of the interleaving. The maximum input data rate is still subject to the maximum specification of the device. This limits the synthesis bandwidth available at the input in interleaved mode.

With Reg. 0x02, Bit 5 (real mode) set, the Q channel and the internal I and Q digital modulation are turned off. The output spectrum at the I DAC then represents the signal at Digital Input Port 1, interpolated by 1×, 2×, 4×, or 8×.

The general recommendation is that if the desired signal is within ±0.4 × f_{DATA}, the odd filter mode should be used. Outside of this, the even filter mode should be used. In any situation, the total bandwidth of the signal should be less than 0.8 × f_{DATA}.

Table 16. Interpolation Filter Modes, (Reg. 0x01, Bits <5:2>)

Interpolation Factor <7:6>	Filter Mode <5:2>	Modulation	Nyquist Zone Pass Band	F_Low[1]	Center[1]	F_High[1]	Comments
8	0x00	DC	1	−0.05	0	+0.05	In 8× interpolation; BW (min) = 0.0375 × f_{DAC} BW (max) = 0.1 × f_{DAC}
8	0x01	DC shifted	2	0.0125	0.0625	0.1125	
8	0x02	F/8	3	0.075	0.125	0.175	
8	0x03	F/8 shifted	4	0.1375	0.1875	0.2375	
8	0x04	F/4	5	0.2	0.25	0.3	
8	0x05	F/4 shifted	6	0.2625	0.3125	0.3625	
8	0x06	3F/8	7	0.325	0.375	0.425	
8	0x07	3F/8 shifted	8	0.3875	0.4375	0.4875	
8	0x08	F/2	−8	−0.55	−0.5	−0.45	
8	0x09	F/2 shifted	−7	−0.4875	−0.4375	−0.3875	
8	0x0A	−3F/8	−6	−0.425	−0.375	−0.343	
8	0x0B	−3F/8 shifted	−5	−0.3625	−0.3125	−0.2625	
8	0x0C	−F/4	−4	−0.3	−0.25	−0.2	
8	0x0D	−F/4 shifted	−3	−0.2375	−0.1875	−0.1375	
8	0x0E	−F/8	−2	−0.175	−0.125	−0.075	
8	0x0F	−F/8 shifted	-1	−0.1125	−0.0625	−0.0125	
4	0x00	DC	1	−0.1	0	+0.1	In 4× interpolation; BW (min) = 0.075 × f_{DAC} BW (max) = 0.2 × f_{DAC}
4	0x01	DC shifted	2	0.025	0.125	0.225	
4	0x02	F/4	3	0.15	0.25	0.35	
4	0x03	F/4 shifted	4	0.275	0.375	0.475	
4	0x04	F/2	−4	−0.6	−0.5	−0.4	
4	0x05	F/2 shifted	−3	−0.475	−0.375	−0.275	
4	0x06	−F/4	−2	−0.35	−0.25	−0.15	
4	0x07	−F/4 shifted	−1	−0.225	−0.125	−0.025	
2	0x00	DC	1	−0.2	0	0.2	In 2× interpolation; BW (min) = 0.15 × f_{DAC} BW (max) = 0.4 × f_{DAC}
2	0x01	DC shifted	2	0.05	0.25	0.45	
2	0x02	F/2	−2	−0.7	−0.5	−0.3	
2	0x03	F/2 shifted	−1	−0.45	−0.25	−0.05	

[1] Frequency normalized to f_{DAC}.

INTERPOLATION FILTER MINIMUM AND MAXIMUM BANDWIDTH SPECIFICATIONS

The AD977x uses a novel interpolation filter architecture that allows DAC IF frequencies to be generated anywhere in the spectrum. Figure 65 shows the traditional choice of DAC IF output bandwidth placement. Note that there are no possible filter modes in which the carrier can be placed near 0.5 × f_{DATA}, 1.5 × f_{DATA}, 2.5 × f_{DATA}, etc.

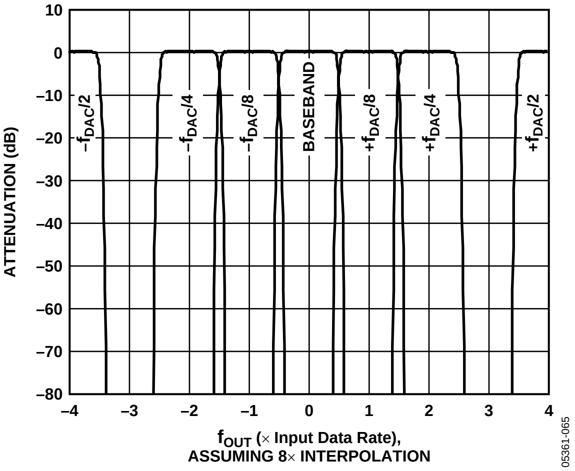

Figure 65. Traditional Bandwidth Options for TxDAC Output IF

The filter architecture not only allows the interpolation filter pass bands to be centered in the middle of the input Nyquist zones (as explained in this section), but also allows the possibility of a 3 × f_{DAC}/8 modulation mode. With all of these filter combinations, a carrier of given bandwidth can be placed anywhere in the spectrum and fall into a possible pass band of the interpolation filters. The possible bandwidths accessible with the filter architecture are shown in Figure 66 and Figure 67. Note that the shifted and nonshifted filter modes are all accessible by programming the filter mode for the particular interpolation rate.

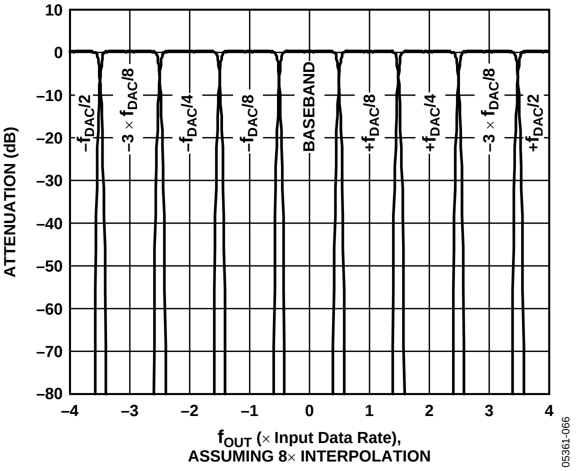

Figure 66. Nonshifted Bandwidths Accessible with the Filter Architecture

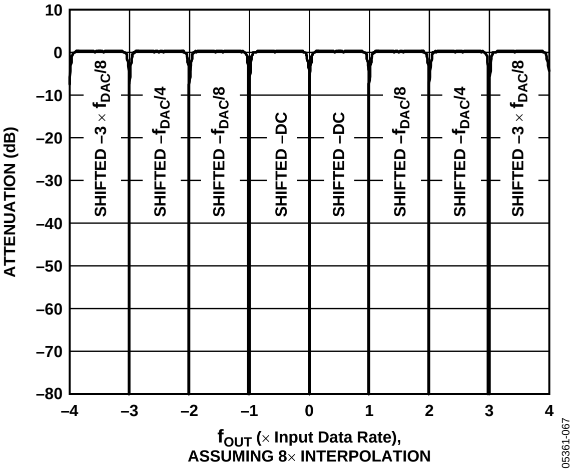

Figure 67. Shifted Bandwidths Accessible with the Filter Architecture

With this filter architecture, a signal placed anywhere in the spectrum is possible. However, the signal bandwidth is limited by the input sample rate of the DAC and the specific placement of the carrier in the spectrum. The bandwidth restriction resulting from the combination of filter response and input sample rate is often referred to as the synthesis bandwidth, since this is the largest bandwidth that the DAC can synthesize.

The maximum bandwidth condition exists if the carrier is placed directly in the center of one of the filter pass bands. In this case, the total 0.1 dB bandwidth of the interpolation filters is equal to 0.8 × f_{DATA}. As Table 16 shows, the synthesis bandwidth as a fraction of DAC output sample rate drops by a factor of 2 for every doubling of interpolation rate. The minimum bandwidth condition exists, for example, if a carrier is placed at 0.25 × f_{DATA}. In this situation, if the nonshifted filter response is enabled, the high end of the filter response cuts off at 0.4 × f_{DATA}, thus limiting the high end of the signal bandwidth. If the shifted filter response is enabled instead, then the low end of the filter response cuts off at 0.1 × f_{DATA}, thus limiting the low end of the signal bandwidth. The minimum bandwidth specification that applies for a carrier at 0.25 × f_{DATA} is therefore 0.3 × f_{DATA}. The minimum bandwidth behavior is repeated over the spectrum for carriers placed at (±n ± 0.25) × f_{DATA}, where n is any integer.

DRIVING THE DACCLK INPUT

The DACCLK input requires a low jitter differential drive signal. It is a PMOS input differential pair powered from the 1.8 V supply, therefore,

it is important to maintain the specified 400 mV input common-mode voltage. Each input pin can safely swing from 200 mV p-p to 1 V p-p about the 400 mV common-mode voltage. While these input levels are not directly LVDS-compatible, DACCLK can be driven by an offset ac-coupled LVDS signal, as shown in Figure 68.

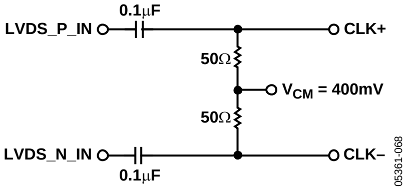
0.1µF
LVDS_P_IN
CLK+
50Ω
V_{CM} = 400mV
50Ω
LVDS_N_IN
CLK–
0.1µF
05361-068

Figure 68. LVDS DACCLK Drive Circuit

If a clean sine clock is available, it can be transformer-coupled to DACCLK, as shown in Figure 68. Use of a CMOS or TTL clock is also acceptable for lower sample rates. It can be routed through a CMOS to LVDS translator, then ac-coupled, as described in this section. Alternatively, it can be transformer-coupled and clamped, as shown in Figure 69.

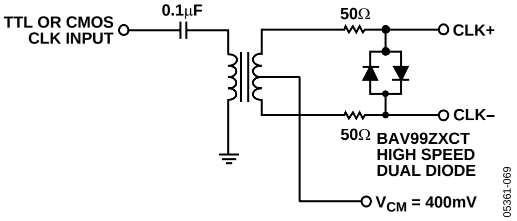
TTL OR CMOS CLK INPUT
0.1µF
50Ω
CLK+
CLK–
50Ω
BAV99ZXCT HIGH SPEED DUAL DIODE
V_{CM} = 400mV
05361-069

Figure 69. TTL or CMOS DACCLK Drive Circuit

A simple bias network for generating VCM is shown in Figure 70. It is important to use CVDD18 and CGND for the clock bias circuit. Any noise or other signal that is coupled onto the clock is multiplied by the DAC digital input signal and can degrade the DAC's performance.

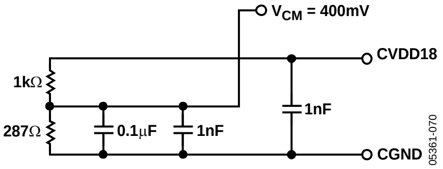
V_{CM} = 400mV
CVDD18
1kΩ
1nF
287Ω
0.1µF
1nF
CGND
05361-070

Figure 70. DACCLK VCM Generator Circuit

Internal PLL Clock Multiplier/Clock Distribution

The internal clock structure on the devices allows the user to drive the differential clock inputs with a clock at 1× or an integer multiple of the input data rate or at the DAC output sample rate. An internal PLL provides input clock multiplication and provides all the internal clocks required for the interpolation filters and data synchronization.

The internal clock architecture is shown in Figure 71. The reference clock is the differential clock at Pins 5 and 6. This clock input can be run differentially or singled-ended by driving Pin 5 with a clock signal and biasing Pin 6 to the midswing point of the signal at Pin 5. The clock architecture can be run in the following configurations:

1. PLL Enabled (Reg. 0x09, Bit 7 = 1). The PLL enable switch shown in Figure 71 is connected to the junction of the N1 dividers (PLL VCO divide ratio) and N2 dividers (PLL loop divide ratio). Divider N3 determines the interpolation rate of the DAC, and the ratio N3/N2 determines the ratio of reference clock/input data rate. The VCO runs optimally over the range of 1.0 GHz to 2.0 GHz, so that N1 keeps the speed of the VCO within this range, although the DAC sample rate can be lower. The loop filter components are entirely internal and no external compensation is necessary.
2. PLL Disabled (Reg. 0x09, Bit 7 = 0). The PLL enable switch shown in Figure 71 is connected to the reference clock input. The differential reference clock input is the same as the DAC output sample rate. N3 determines the interpolation rate.

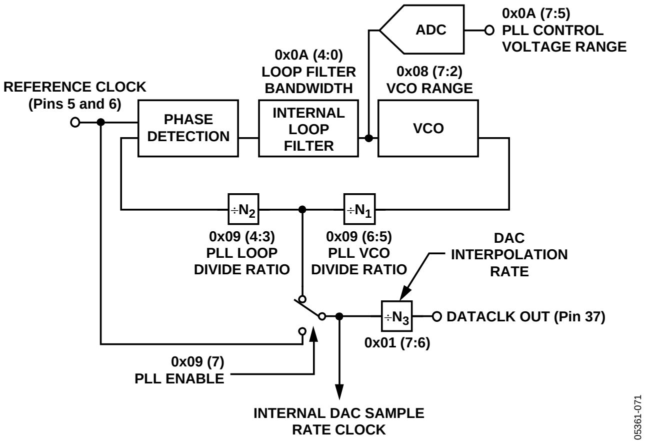
ADC
0x0A (7:5) PLL CONTROL VOLTAGE RANGE
0x0A (4:0) LOOP FILTER BANDWIDTH
0x08 (7:2) VCO RANGE
REFERENCE CLOCK (Pins 5 and 6)
PHASE DETECTION
INTERNAL LOOP FILTER
VCO
÷N2
÷N1
0x09 (4:3) PLL LOOP DIVIDE RATIO
0x09 (6:5) PLL VCO DIVIDE RATIO
DAC INTERPOLATION RATE
÷N3
DATACLK OUT (Pin 37)
0x01 (7:6)
0x09 (7) PLL ENABLE
INTERNAL DAC SAMPLE RATE CLOCK
05361-071

Figure 71. Internal Clock Architecture

Table 17. VCO Frequency Range vs. PLL Band Select Value

Typical PLL Lock Ranges				
	VCO Frequency Range in MHz			
PLL Band Select	**Typ at 25°C**		**Typ over Temp**	
	f_{LOW}	f_{HIGH}	f_{LOW}	f_{HIGH}
111111 (63)	Auto Mode			
111110 (62)	2056	2170	2105	2138
111101 (61)	2002	2113	2048	2081
111100 (60)	1982	2093	2029	2061
111011 (59)	1964	2075	2010	2043
111010 58)	1947	2057	1992	2026
111001 (57)	1927	2037	1971	2006
111000 (56)	1907	2016	1951	1986
110111 (55)	1894	2003	1936	1972
110110 (54)	1872	1981	1913	1952
110101 (53)	1852	1960	1892	1931
110100 (52)	1841	1948	1881	1920
110011 (51)	1816	1923	1855	1895
110010 (50)	1796	1903	1835	1874
110001 (49)	1789	1895	1828	1867
110000 (48)	1764	1871	1803	1844
101111 (47)	1746	1853	1784	1826
101110 (46)	1738	1842	1776	1815
101101 (45)	1714	1820	1752	1794
101100 (44)	1700	1804	1737	1779

Typical PLL Lock Ranges

PLL Band Select	VCO Frequency Range in MHz			
	Typ at 25°C		Typ over Temp	
	f_{LOW}	f_{HIGH}	f_{LOW}	f_{HIGH}
101011 (43)	1689	1790	1726	1764
101010 (42)	1657	1757	1695	1734
101001 (41)	1641	1738	1679	1714
101000 (40)	1610	1707	1649	1684
100111 (39)	1597	1689	1635	1666
100110 (38)	1568	1661	1607	1639
100101 (37)	1553	1641	1592	1617
100100 (36)	1525	1613	1562	1592
100011 (35)	1511	1595	1548	1572
100010 (34)	1484	1570	1519	1549
100001 (33)	1470	1552	1506	1528
100000 (32)	1441	1525	1474	1504
011111 (31)	1429	1509	1463	1487
011110 (30)	1403	1485	1433	1464
011101 (29)	1390	1469	1422	1447
011100 (28)	1362	1443	1391	1423
011011 (27)	1352	1429	1380	1407
011010 (26)	1325	1405	1352	1385
011001 (25)	1314	1390	1340	1369
011000 (24)	1290	1368	1315	1350
010111 (23)	1276	1351	1302	1332
010110 (22)	1253	1331	1277	1313
010101 (21)	1239	1313	1264	1295
010100 (20)	1183	1255	1205	1240
010011 (19)	1204	1275	1227	1259
010010 (18)	1151	1221	1172	1207
010001 (17)	1171	1240	1193	1224
010000 (16)	1148	1218	1170	1204
001111 (15)	1137	1204	1159	1189
001110 (14)	1116	1184	1137	1170
001101 (13)	1106	1171	1127	1157
001100 (12)	1086	1152	1106	1138
001011 (11)	1075	1138	1095	1124
001010 (10)	1055	1119	1075	1106
001001 (9)	1045	1107	1065	1093
001000 (8)	1027	1090	1047	1076
000111 (7)	1016	1076	1034	1062
000110 (6)	998	1059	1016	1046
000101 (5)	987	1046	1005	1032
000100 (4)	960	1017	977	1004
000011 (3)	933	989	949	976
000010 (2)	908	962	923	950
000001 (1)	883	936	898	925
000000 (0)	859	911	873	899

VCO Frequency Ranges

Because the PLL band covers greater than a 2× frequency range, there can be two options for the PLL band select: one at the low end of the range and one at the high end of the range. Under these conditions, the VCO phase noise is optimal when the user selects the band select value corresponding to the high end of the frequency range. Figure 72 shows how the VCO bandwidth and the optimal VCO frequency varies with the band select value.

PLL Loop Filter Bandwidth

The loop filter bandwidth of the PLL is programmed via SPI Reg. 0x0A, Bits <4:0>. Changing these values switches capacitors on the internal loop filter. No external loop filter components are required. This loop filter has a pole at 0 (P1), and then a zero- (Z1) pole (P2) combination. Z1 and P2 occur within a decade of each other. The location of the zero pole is determined by Bit <4:0>. For a setting of 00000, the zero pole occurs near 10 MHz. By setting Bits <4:0> to 11111, the Z1/P2 combination can be lowered to approximately 1 MHz. The relationship between Bits <4:0> and the position of the zero pole between 1 MHz and 10 MHz is linear. The internal components are not low tolerance, however, and can drift by as much as ±30%.

For optimal performance, the bandwidth adjustment (Reg. 0x0A, Bits <4:0>) should be set to 11111 for all operating modes with PLL enabled. The PLL bias settings (Reg. 0x09, Bits <2:0>) should be set to 111. The PLL control voltage (Reg. 0x0A, Bits <7:5>) is read back and is proportional to the dc voltage at the internal loop filter output. With the PLL bias settings given in this section, the readback from the PLL control voltage should typically be 010 or possibly 001 or 011. Anything outside of this range indicates that the PLL is not operating correctly.

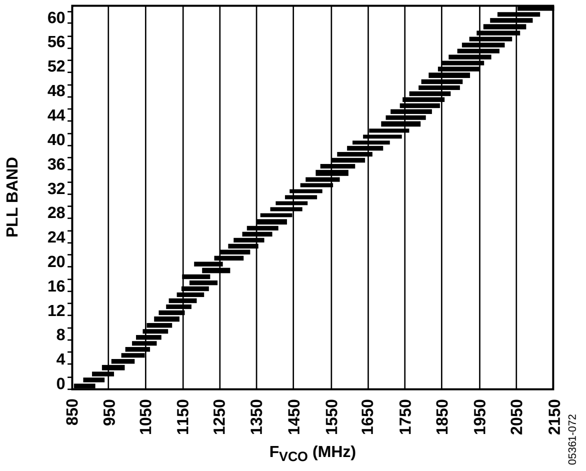

Figure 72. Typical PLL Band Select vs. Frequency at 25°C

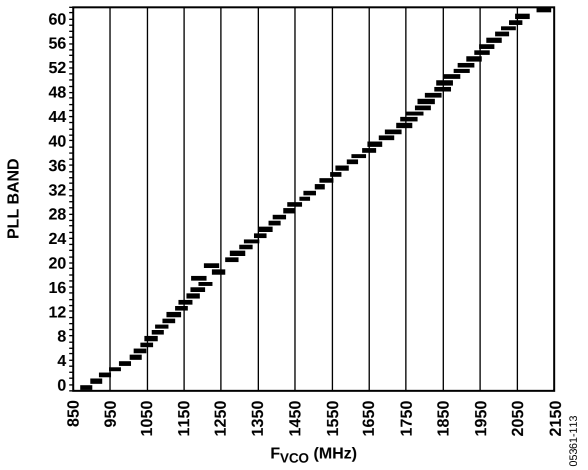

Figure 73. Typical PLL Band Select vs. Frequency over Temperature

The AD977x has an autosearch feature that can be used to determine the optimal settings for the PLL. To enable the autosearch mode, set Reg. 0x08, Bits <7:2> to 11111b, and read back the value from Reg. 0x08, Bits <7:2>. Autosearch mode is intended to find the optimal PLL settings only, after which the same settings should be applied in manual mode. It is not recommended that the PLL be set to autosearch mode during regular operation.

FULL-SCALE CURRENT GENERATION

Internal Reference

Full-scale current on the I DAC and Q DAC can be set from 8.66 mA to 31.66 mA. Initially, the 1.2 V band gap reference is used to set up a current in an external resistor connected to I120 (Pin 75). A simplified block diagram of the reference circuitry is shown in Figure 74. The recommended value for the external resistor is 10 kΩ, which sets up an $I_{REFERENCE}$ in the resistor of 120 µA, which in turn provides a DAC output full-scale current of 20 mA. Because the gain error is a linear function of this resistor, a high precision resistor improves gain matching to the internal matching specification of the devices. Internal current mirrors provide a current-gain scaling, where I DAC or Q DAC gain is a 10-bit word in the SPI port register (Reg. 0x0A, 0x0B, 0x0E, and 0x0F). The default value for the DAC gain registers gives an I_{FS} of approximately 20 mA, where I_{FS} is equal to

$$\frac{1.2\,V}{R}\times\left(\frac{27}{12}+\left(\frac{6}{1024}\times DAC\ gain\right)\right)\times 32$$

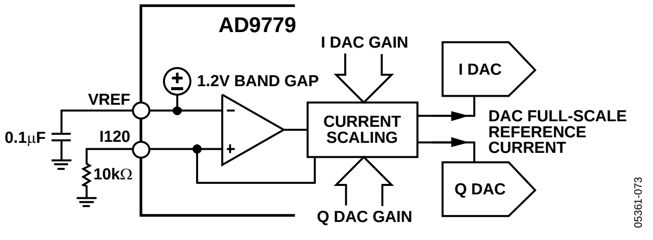

Figure 74. Reference Circuitry

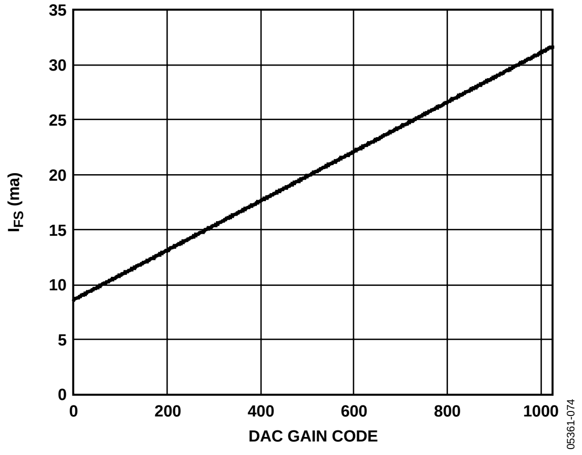

Figure 75. I_{FS} vs. DAC Gain Code

Auxiliary DACS

Two auxiliary DACs are provided on the AD977x. The full-scale output current on these DACs is derived from the 1.2 V band gap reference and external resistor. The gain scale from the reference amplifier current $I_{REFERENCE}$ to the auxiliary DAC reference current is 16.67 with the auxiliary DAC gain set to full scale (10-bit values, SPI Reg. 0x0C, 0x0D, 0x10, and 0x11), this gives a full-scale current of approximately 2 mA for auxiliary DAC1 and auxiliary DAC2. The auxiliary DAC outputs are not differential. Only one side of the auxiliary DAC (P or N) is active at one time. The inactive side goes into a high impedance state (>100 kΩ). In addition, the P or N outputs can act as current sources or sinks. The control of the P and N side for both auxiliary DACs is via Reg. 0x0E and 0x10, Bits <7:6>. When sourcing current, the output compliance voltage is 0 V to 1.6 V; when sinking current, the output compliance voltage is 0.8 V to 1.6 V.

The auxiliary DACs can be used for local oscillator (LO) cancellation when the DAC output is followed by a quadrature modulator. A typical DAC-to-quadrature modulator interface is shown in Figure 76. Often, the input common-mode voltage for the modulator is much higher than the output compliance range of the DAC, so that ac coupling is necessary. If the required common-mode input voltage on the quadrature modulator matches that of the DAC, then the ac coupling capacitors can be removed. The input referred dc offset voltage of the quadrature modulator (and the DAC output offset voltage mismatch) can result in LO feedthrough on the modulator output, thus degrading system performance. If the configuration of Figure 76 is used, the auxiliary DACs can be used to compensate for this dc offset, thus reducing LO feedthrough. A low-pass or band-pass filter is recommended when spurious signals from the DAC (distortion and DAC images) at the quadrature modulator inputs can affect the system performance. This filter should be placed at the quadrature modulator inputs.

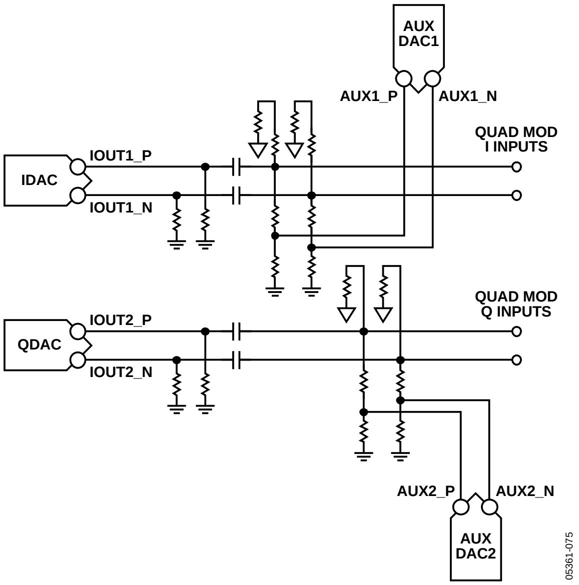
AUX
DAC1
AUX1_P
AUX1_N
QUAD MOD
I INPUTS
IOUT1_P
IDAC
IOUT1_N
QUAD MOD
Q INPUTS
IOUT2_P
QDAC
IOUT2_N
AUX2_P
AUX2_N
AUX
DAC2
05361-075

Figure 76. Typical Use of Auxiliary DACs

POWER DISSIPATION

Figure 77 to Figure 85 show the power dissipation of the 1.8 V and 3.3 V digital and clock supplies in single DAC and dual DAC modes. In addition to this, the power dissipation/current of the 3.3 V supply (mode and speed independent) in single DAC mode is 102 mW/31 mA. In dual DAC mode, this is 182 mW/51 mA.

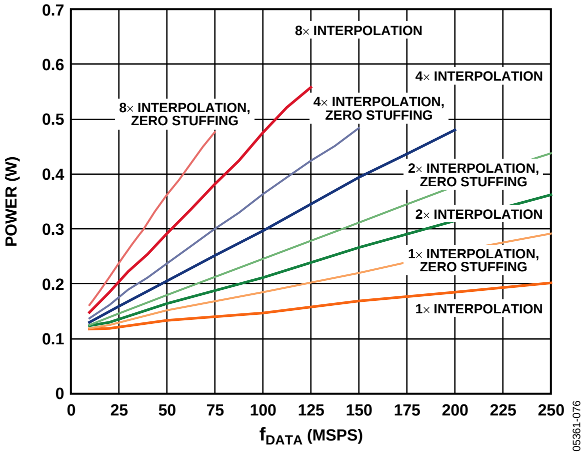

Figure 77. Power Dissipation, I Data Only, Single DAC Mode

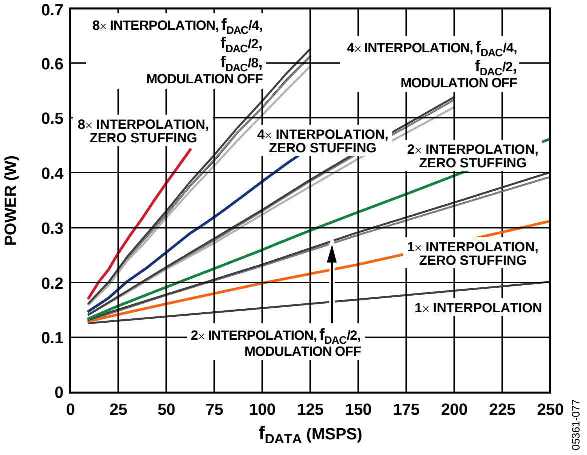

Figure 78. Power Dissipation, Dual DAC Mode

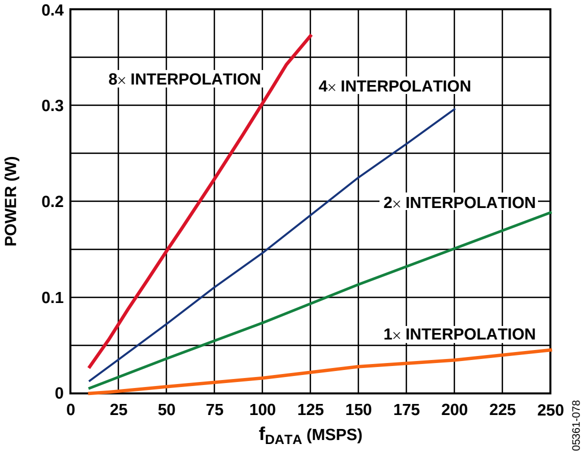

Figure 79. Power Dissipation, Digital 1.8 V Supply, I Data Only, Real Mode, Does Not Include Zero Stuffing

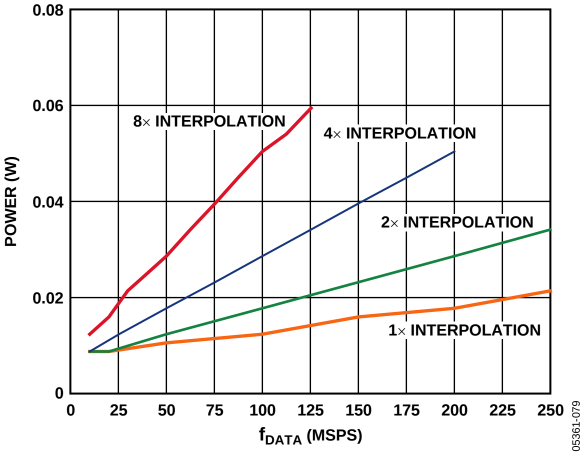

Figure 80. Power Dissipation, Clock 1.8 V Supply, I Data Only, Real Mode, Includes Modulation Modes, Does Not Include Zero Stuffing

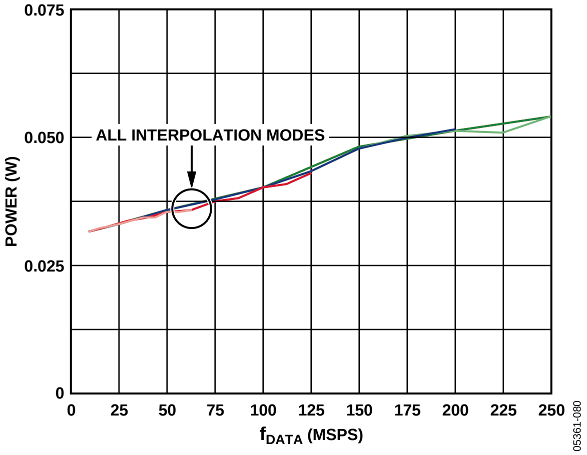

Figure 81. Digital 3.3 V Supply, I Data Only, Real Mode, Includes Modulation Modes and Zero Stuffing

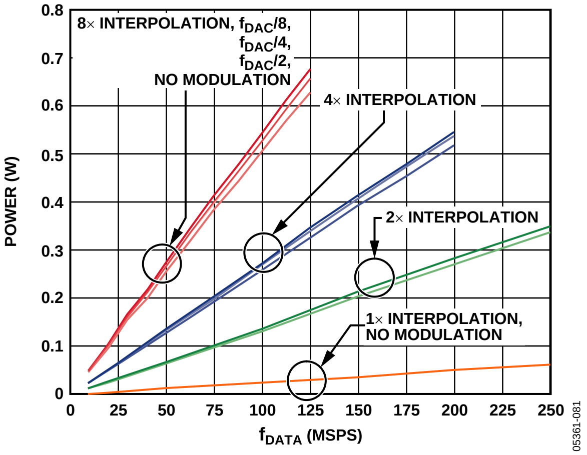

Figure 82. Power Dissipation, Digital 1.8 V Supply, I and Q Data, Dual DAC Mode, Does Not Include Zero Stuffing

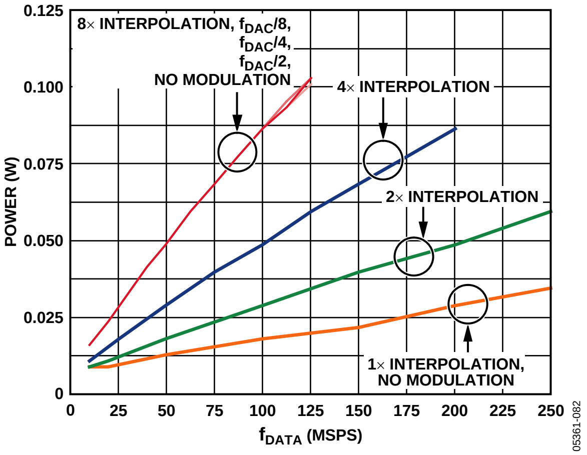

Figure 83. Power Dissipation, Clock 1.8 V Supply, I and Q Data, Dual DAC Mode, Does Not Include Zero Stuffing

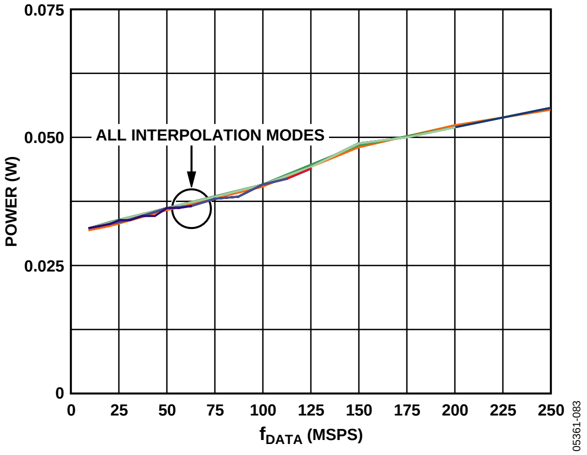

Figure 84. Digital 3.3 V Supply, I and Q Data, Dual DAC Mode

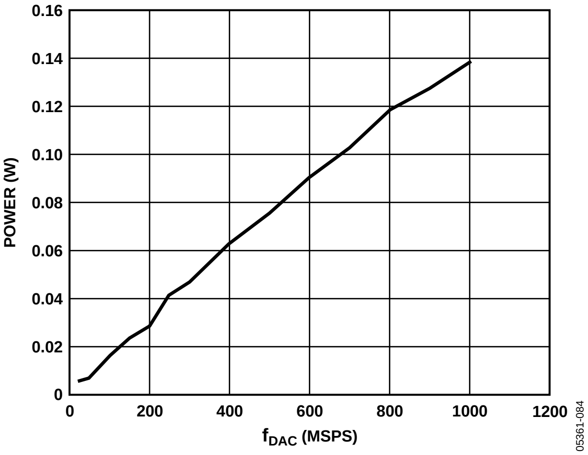

Figure 85. Power Dissipation of Inverse Sinc Filter

POWER-DOWN AND SLEEP MODES

The AD977x has a variety of power-down modes, so that the digital engine, main TxDACs, or auxiliary DACs can be powered down individually or together. Via the SPI port, the main TxDACs can be placed in sleep or power-down mode. In sleep mode, the TxDAC output is turned off, thus reducing power dissipation. The reference remains powered on, however, so that recovery from sleep mode is very fast. With the power-down mode bit set (Reg. 0x00, Bit 4), all analog and digital circuitry, including the reference, is powered down. The SPI port remains active in this mode. This mode offers more substantial power savings than sleep mode, but the turn on time is much longer. The auxiliary DACs also have the capability to be programmed into sleep mode via the SPI port.

The auto power-down enable bit (Reg. 0x00, Bit 3) controls the power-down function for the digital section of the devices. The auto power-down function works in conjunction with the TXENABLE pin (Pin 39) according to the following:

TXENABLE (Pin 39) =

0: autopower-down enable =
  0: Flush data path with 0s
  1: Flush data for multiple DACCLK cycles; then automatically place the digital engine in power-down state. DACs, reference, and SPI port are not affected.

or TXENABLE (Pin 39) =

1: Normal operation

If the TxEnable invert bit (Reg. 0x02, Bit 1) is set, the function of this TXENABLE pin is inverted.

INTERLEAVED DATA MODE

The TxEnable bit is dual function. In dual port mode, it is simply used to power down the digital section of the devices. In interleaved mode, the IQ data stream is synchronized to TxEnable. Therefore, to achieve IQ synchronization, TxEnable should be held low until an I data word is present at the inputs to Data Port 1. If a DATACLK rising edge occurs while TxEnable is at a high logic level, IQ data becomes synchronized to the DATACLK output. TxEnable can remain high and the input IQ data remains synchronized. To be backwards-compatible with previous DACs from ADI, such as the AD9777 and AD9786, the user can also toggle TxEnable once during each data input cycle, thus continually updating the synchronization. If TxEnable is brought low and held low for multiple DACCLK cycles, then the devices flush the data in the interpolation filters, and shut down the digital engine after the filters are flushed. The amount of DACCLK cycles it takes to go into this power-down mode is then a function of the length of the equivalent 2×, 4×, or 8× interpolation filter. The timing of TxEnable, I/Q select, filter flush, and digital power-down are shown in Figure 86.

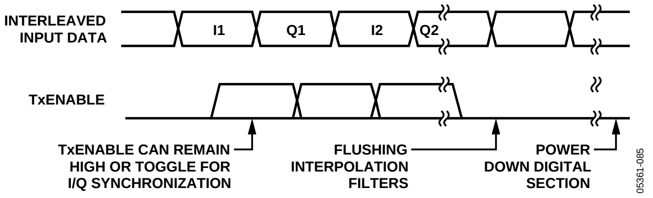
INTERLEAVED INPUT DATA
I1
Q1
I2
Q2
TxENABLE
TxENABLE CAN REMAIN HIGH OR TOGGLE FOR I/Q SYNCHRONIZATION
FLUSHING INTERPOLATION FILTERS
POWER DOWN DIGITAL SECTION
05361-085

Figure 86. TxEnable Function

The TxEnable function can be inverted by changing the status of Reg. 0x02, Bit 1. The other bit that controls IQ ordering is the Q-first bit (Reg. 0x02, Bit 0). With the Q-first bit reset to the default of 0, the IQ pairing that is latched is the I1Q1, I2Q2, etc. With IQ first set to 1, the first I data is discarded and the pairing is I2Q1, I3Q2, etc. Note that with IQ-first set, the I data is still routed to the internal I channel, the Q data is routed to the internal Q channel, and only the pairing changes.

TIMING INFORMATION

Figure 87 to Figure 89 show some of the various timing possibilities when the PLL is enabled. The combination of the settings of N2 and N3 means that the reference clock frequency can be a multiple of the actual input data rate. Figure 87 to Figure 89 show, respectively, what the timing looks like when N2/N3 = 1 and 2.

In interleaved mode, set-up and hold times of DATACLK out to data in are the same as those shown in Figure 87 to Figure 89. It is recommended that any toggling of TxEnable occurs concurrently with the digital data input updating. In this way, timing margins between DATACLK, TxEnable, and digital input data are optimized.

Figure 89 shows the timing specifications when PLL is disabled. The reference clock is at the DAC output sample rate. In the example shown in Figure 89, if PLL is disabled, the interpolation is 4×. The set-up and hold time for the input data are with respect to the rising edge of DATACLK out. Note that if Reg. 0x02, Bit 2 is set, DATACLK out is inverted so the latching clock edge becomes DATACLK out falling edge.

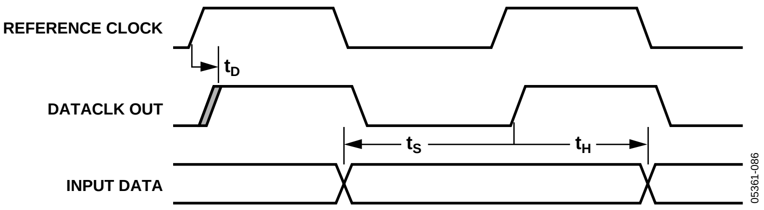

Figure 87. Timing Specifications, PLL Enabled, Reference Clock = 1× Input Sample Rate[1]

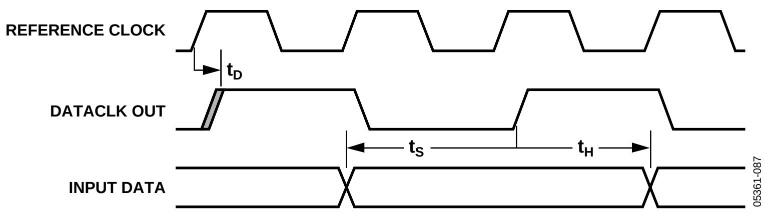
REFERENCE CLOCK
t_D
DATACLK OUT
t_S
t_H
INPUT DATA
05361-087

Figure 88. Timing Specifications, PLL Enabled, Reference Clock = 2× Input Sample Rate[1]

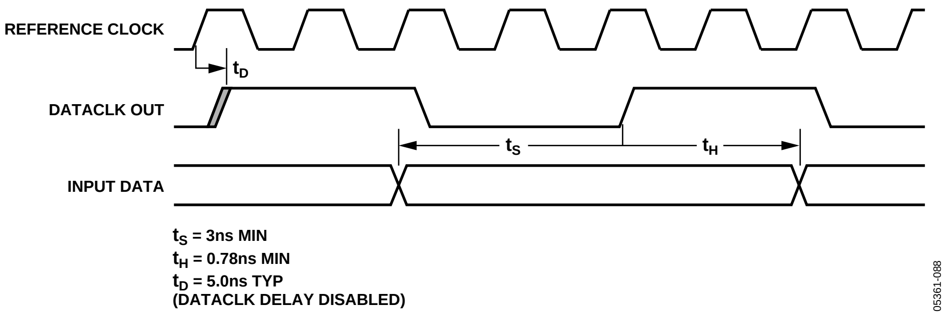
REFERENCE CLOCK
t_D
DATACLK OUT
t_S
t_H
INPUT DATA
t_S = 3ns MIN
t_H = 0.78ns MIN
t_D = 5.0ns TYP
(DATACLK DELAY DISABLED)
05361-088

Figure 89. Timing Specifications, PLL Disabled, 4× Interpolation

Using Data Delay to Meet Timing Requirements

To meet strict timing requirements at input data rates of up to 250 MSPS, the AD977x has a fine timing feature. Fine timing adjustments can be made by programming values into the data clock delay register (Reg. 0x04, Bit <7:4>). This register can be used to add delay between the DACCLK in and the DATACLK out. Figure 90 shows the default delay present when DATACLK delay is disabled. The disable function bit is found in Reg. 0x02, Bit 4. Figure 91 shows the delay present when DATACLK delay is enabled and set to 0000. Figure 92 indicates the delay when DATACLK delay is enabled and set to 1111. Note that the set-up and hold times specified for data to DATACLK are defined for DATACLK delay disabled.

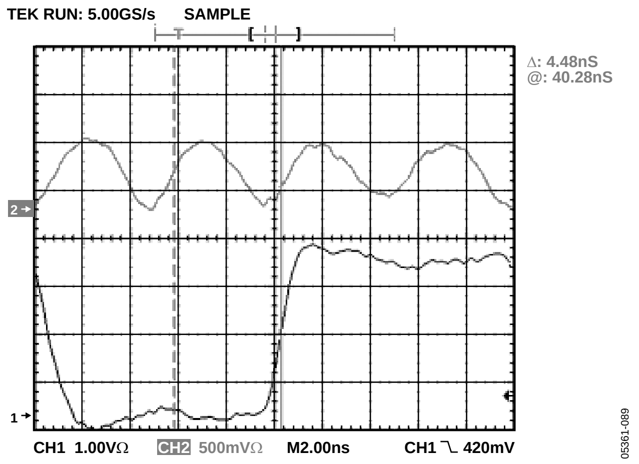

Figure 90. Delay from DACCLK to DATACLK with DATACLK Delay Disabled

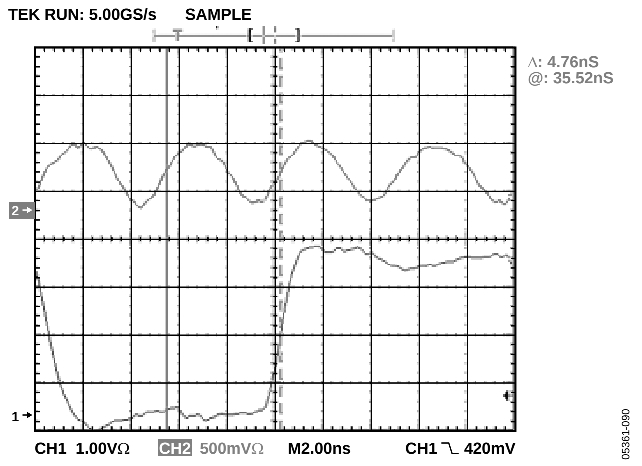

Figure 91. Delay from DACCLK to DATACLK Out with DATACLK Delay = 0000

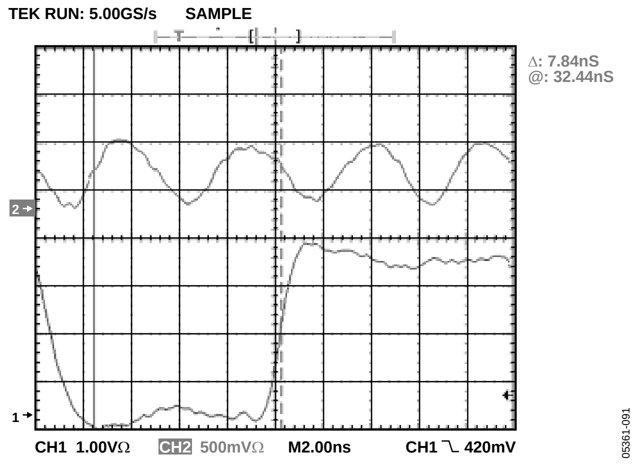

Figure 92. Delay from DACCLK to DATACLK Out with DATACLK Delay = 1111

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[1] For an in-depth description of how TxDAC timing specifications are specified, please read Analog Devices, application note AN748, “Set-up and Hold Measurements in High Speed CMOS Input DACs.”

The difference between the minimum delay shown in Figure 91 and the maximum delay shown in Figure 92 is the range programmable via the DATACLK delay register. The delay (in absolute time) when programming DATACLK delay between 0000 and 1111 is a linear extrapolation between these two figures. The typical delays per increment over temperature are shown in Table 18.

Table 18. Data Delay Line Typical Delays Over Temperature

Delays	–40°C	+25°C	+85°C	Unit
Delay Between Disabled and Enabled	370	416	432	ps
Average Delay per Increment	171	183	197	ps

The frequency of DATACLK out depends on several programmable settings. Interpolation, zero stuffing, and interleaved/dual port mode all have an effect on the DACCLK frequency. The divisor function between DACCLK and DATACLK is equal to the values shown in Table 19.

Table 19.

Interpolation	Zero Stuffing	Input Mode	Divisor
1	Disabled	Dual port	1
2	Disabled	Dual port	2
4	Disabled	Dual port	4
8	Disabled	Dual port	8
1	Disabled	Interleaved	invalid
2	Disabled	Interleaved	1
4	Disabled	Interleaved	2
8	Disabled	Interleaved	4
1	Enabled	Dual port	2
2	Enabled	Dual port	4
4	Enabled	Dual port	8
8	Enabled	Dual port	16
1	Enabled	Interleaved	1
2	Enabled	Interleaved	2
4	Enabled	Interleaved	4
8	Enabled	Interleaved	8

In addition to this divisor function, DATACLK can be divided by up to an additional factor of 4, according to the state of the DATACLK divide register (Reg. 0x03, Bit <5:4>) (see Table 20).

Table 20.

Reg. 0x03, Bit <5:4>	Divider Ratio
00	1
01	2
10	4
11	1

The maximum divisor resulting from the combination of the values in Table 19, and the DATACLK divide register is 32.

Manual Input Timing Correction

Correction of input timing can be achieved manually. The correction function is controlled by Reg. 0x03, Bits <7:6>. The function is programmed as shown in Table 21.

Table 21.

Reg. 0x03, Bits <7:6>	Function
00	Error check disabled
01	Reserved
10	Reserved
11	Reserved

Necessary corrections can be made by adjusting DATACLK delay and the DATACLK invert bit (Reg. 2, Bit 2). When doing initial timing verification, the user should set input data timing error tolerance (Reg. 0x03, Bit <3:0>) to 1111. DATACLK delay can then be swept to find the range over which the timing is valid. The final value for data delay should be the value that corresponds to the middle of the valid timing range. If a valid timing range is not found during this sweep, the user should invert the DATACLK invert bit and repeat the process. If a valid timing window is still not found, then the input data timing error tolerance should be decremented by 1, and the procedure should be repeated.

Multi-DAC Synchronization

Sync Pulse Generation (Master Devices)

In applications where multiple devices are used and need to be synchronized, the AD977x provides a flexible synchronization engine. There are two options for multi-DAC synchronization. In the first situation, one device can be used as a master and the rest of the devices can be used as slaves. The second option is that all devices operate as slaves. Both operations have the same timing restrict-ions and there are no performance tradeoffs for either mode. The following text describes the master mode. The differential input clock drives the master device and the master in turn generates SYNC_O+ and SYNC_O–. These two signals use LVDS levels to generate a differential synchronization signal, which in turn is used to synchronize all the slave devices. SYNC_O+ and SYNC_O– must loop back to the sync inputs (SYNC_I+ and SYNC_I–) of the master for multiple device synchronization. The master mode is enabled by writing the sync driver enable bit (Reg. 0x07, Bit 6) to a Logic 1. The SYNC_O signal speed can be an integer divisor of the DACCLK speed, according to Reg. 0x04, Bits <3:1>. Enabling a device in slave mode is accomplished by writing the sync receiver enable bit (Reg. 0x07, Bit 7) to a Logic 1. The timing of the DAC input clock and the sync output signals on the master device are shown in Figure 93.

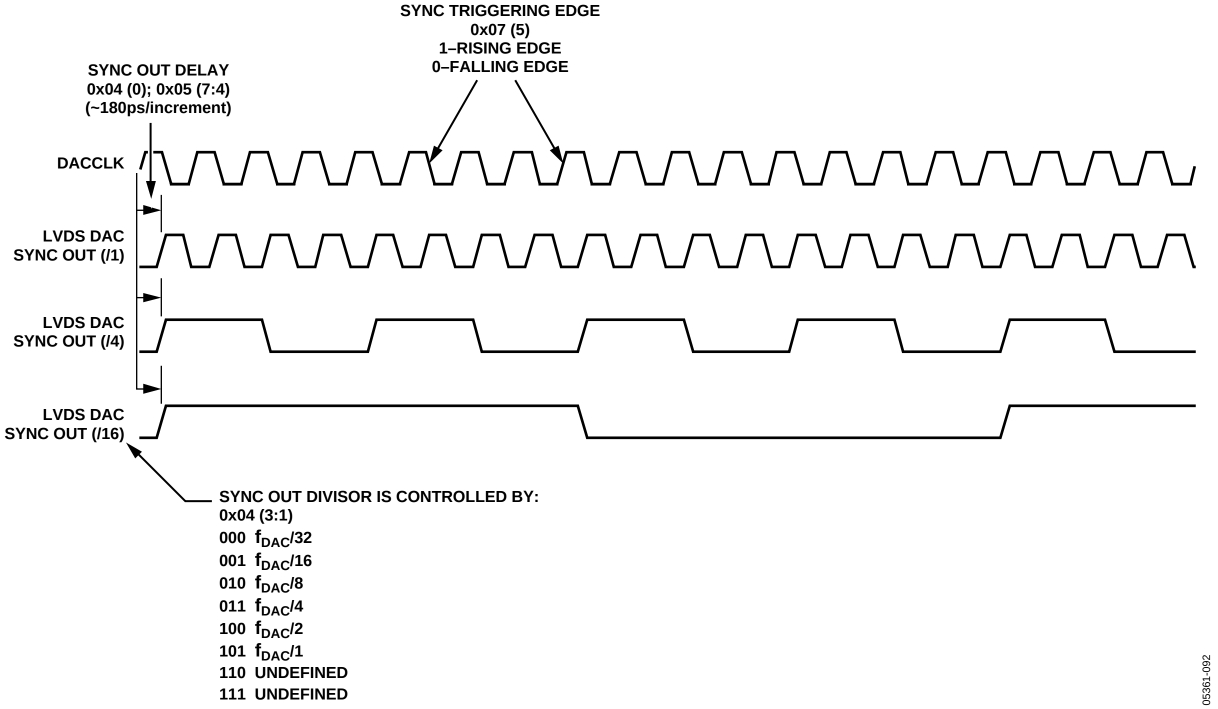

SYNC TRIGGERING EDGE
0x07 (5)
1–RISING EDGE
0–FALLING EDGE
SYNC OUT DELAY
0x04 (0); 0x05 (7:4)
(~180ps/increment)
DACCLK
LVDS DAC SYNC OUT (/1)
LVDS DAC SYNC OUT (/4)
LVDS DAC SYNC OUT (/16)
SYNC OUT DIVISOR IS CONTROLLED BY:
0x04 (3:1)
000 $f_{DAC}/32$
001 $f_{DAC}/16$
010 $f_{DAC}/8$
011 $f_{DAC}/4$
100 $f_{DAC}/2$
101 $f_{DAC}/1$
110 UNDEFINED
111 UNDEFINED
05361-092

Figure 93. DACCLK/Sync Output Timing

The sync output pulse must then be distributed from the master to all the slave devices. This might require that the user implement circuitry outside of the device that splits the LVDS signal. The splitter delivers the SYNC_O signal from the master to the multiple slave device SYNC_I pins. A block diagram of this implementation is shown in Figure 94. The equalization from the CLK source and SYNC_O to the DACCLK and sync inputs of the multiple AD977x devices is critical. For the multichip synchronization to operate correctly at maximum specified DAC sample rates, the DACCLK inputs must be phase aligned to ±100 ps. The SYNC_I inputs must also be phase aligned to ±100 ps. At lower DAC sample rates, this timing alignment can be relaxed.

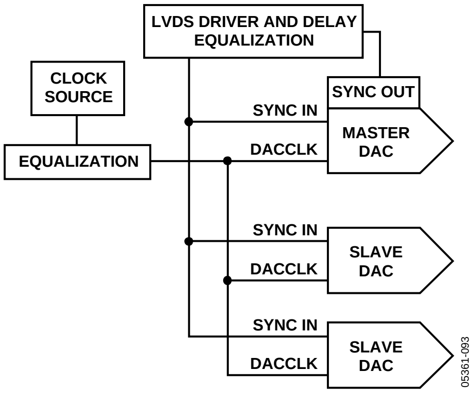

LVDS DRIVER AND DELAY EQUALIZATION
CLOCK SOURCE
EQUALIZATION
SYNC OUT
SYNC IN
DACCLK
MASTER DAC
SYNC IN
DACCLK
SLAVE DAC
SYNC IN
DACCLK
SLAVE DAC
05361-093

Figure 94. Implementation of Sync Signal Distribution in Master/Slave Mode

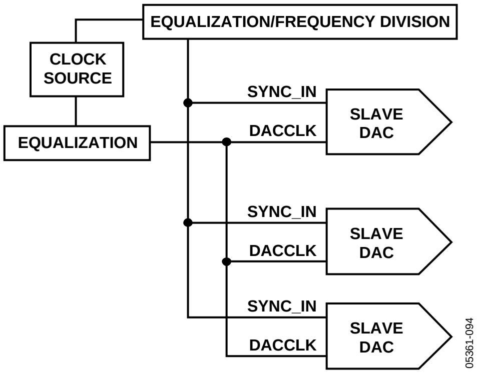

EQUALIZATION/FREQUENCY DIVISION
CLOCK SOURCE
EQUALIZATION
SYNC_IN
DACCLK
SLAVE DAC
SYNC_IN
DACCLK
SLAVE DAC
SYNC_IN
DACCLK
SLAVE DAC
05361-094

Figure 95. Implementation of Sync Signal Distribution in Slave Mode

Sync Pulse Receiver (Slave Devices)

The following description of SYNC_I on the slave devices also applies to the SYNC_I on the master device. The timing for SYNC_I on the master must match that of the slave devices. The SYNC_I pulses, referred to in Figure 94 and shown in more detail in Figure 96 are not restricted by their duty cycle. The only restriction is that each sync pulse remains high for at least one DACCLK cycle. However, the slave DAC receiving the sync pulse must know the speed of the input sync pulse.

The ratio of DACCLK to the SYNC_I speed is determined by the values of the input sync pulse frequency (Reg. 0x05, Bits <3:1>), as shown in Table 22.

Table 22.

Reg. 0x05, Bits <3:1>	Divider Ratio
000	DACCLK/32 (default)
001	DACCLK/16
010	DACCLK/8
011	DACCLK/4
100	DACCLK/2
101	Undefined
110	Undefined
111	Undefined

Internal Synchronization in Slave Devices

The internal timing functions in the slave device are shown in Figure 96. The duty cycle of the SYNC_I signal is not restricted to 50%. The minimum restriction on duty cycle for SYNC_I is that it stays high for at least one full DACCLK cycle. Figure 96 shows two possible SYNC_I signals: one with a 50% duty cycle and another one with a minimum duty cycle. More details on SYNC_I timing restriction are given in the SYNC_I Timing Restrictions section.

DACCLK samples SYNC_I and generates the internal sync signal (SYNC_I_int). The period of SYNC_I_int is always DACCLK/32. If the rate of SYNC_I is greater than DACCLK/32, the extra pulses are stripped off. Figure 96 shows that the SYNC_I period = DACCLK/16, so that every other SYNC_I pulse is stripped. DACCLK_SMP is an internal signal, equal in frequency to the DACCLK/interpolation rate. DACCLK_SMP is synthesized by DACCLK, but synchronized by SYNC_I. Note that there is also a programmable delay (sync input delay) between SYNC_I_int and DACCLK_SMP. This programmable delay adds even more flexibility to the timing interface. Figure 96 shows that the interpolation is set to 8× (DACCLK_SMP rate is 1/8 that of DACCLK).

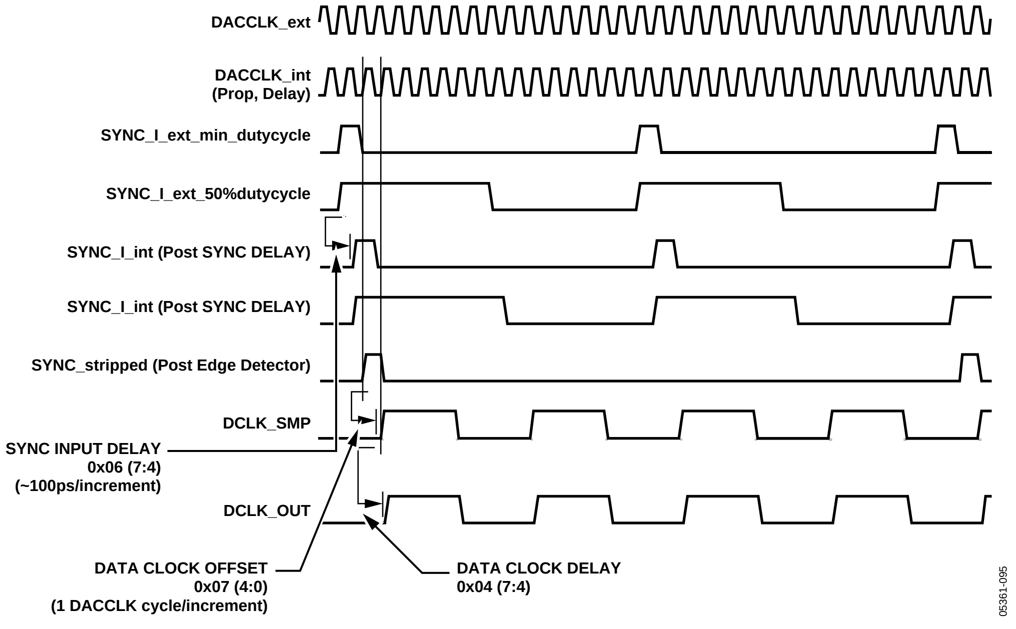

DACCLK_ext
DACCLK_int
(Prop, Delay)
SYNC_I_ext_min_dutycycle
SYNC_I_ext_50%dutycycle
SYNC_I_int (Post SYNC DELAY)
SYNC_I_int (Post SYNC DELAY)
SYNC_stripped (Post Edge Detector)
DCLK_SMP
SYNC INPUT DELAY
0x06 (7:4)
(~100ps/increment)
DCLK_OUT
DATA CLOCK OFFSET
0x07 (4:0)
(1 DACCLK cycle/increment)
DATA CLOCK DELAY
0x04 (7:4)
05361-095

Figure 96. Internal and External Timing for Master or Slave Device

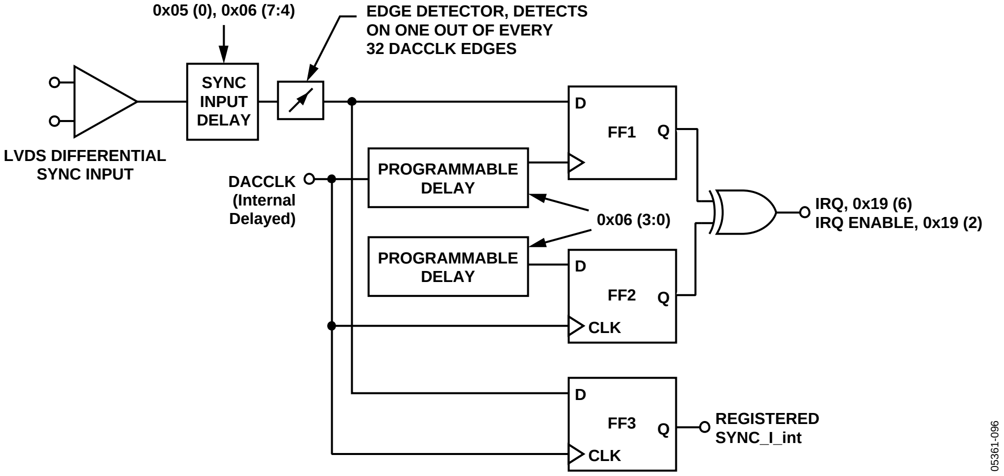

0x05 (0), 0x06 (7:4)
EDGE DETECTOR, DETECTS ON ONE OUT OF EVERY 32 DACCLK EDGES
SYNC INPUT DELAY
LVDS DIFFERENTIAL SYNC INPUT
DACCLK (Internal Delayed)
PROGRAMMABLE DELAY
PROGRAMMABLE DELAY
0x06 (3:0)
D
FF1
Q
D
FF2
Q
CLK
D
FF3
Q
CLK
IRQ, 0x19 (6)
IRQ ENABLE, 0x19 (2)
REGISTERED SYNC_I_int
05361-096

Figure 97. Simplified Internal Synchronization Logic

SYNC_I Timing Restrictions

The AD977x can register timing errors for the SYNC_I signals. The block diagram for this synchronization logic is shown in Figure 94, which is very similar to the data input synchronization circuit shown in Figure 95. The difference is that the circuit shown in Figure 95 uses the DACCLK to properly register SYNC_I. The delay is programmable by Reg. 0x06, Bits <3:0>. IRQ is registered in Reg. 0x19, Bit 6.

EVALUATION BOARD OPERATION

The AD977x evaluation board is designed to optimize the DAC performance and the speed of the digital interface while remaining user friendly. To operate the board, the user needs a power source, a clock source, and a digital data source. The user also needs a spectrum analyzer or an oscilloscope to look at the DAC output. The diagram in Figure 98 illustrates the test setup. A sine or square wave clock works well as a clock source. The dc offset on the clock is not a problem, since the clock is ac-coupled on the evaluation board before the DACCLK inputs. All necessary connections to the evaluation board are shown in more detail in Figure 99.

The evaluation board comes with software that allows the user to program the SPI port. Via the SPI port, the devices can be programmed into any of its various operating modes. When first operating the evaluation board, it is useful to start with a simple configuration, that is, a configuration in which the SPI port settings are as close as possible to the default settings. The default software window is shown in Figure 100. The arrows indicate which settings need to be changed for an easy first time evaluation. Note that this implies that the PLL is not being used and that the clock being used is at the speed of the DAC output sample rate. For a more detailed description of how to use the PLL, see the PLL Loop Filter Bandwidth section.

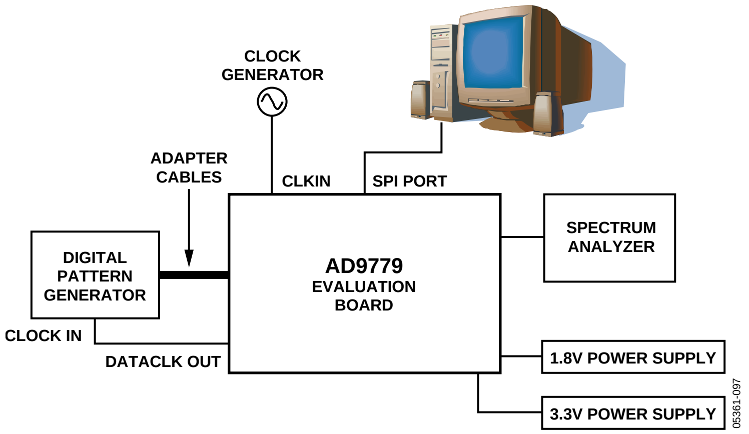

CLOCK GENERATOR
ADAPTER CABLES
CLKIN
SPI PORT
DIGITAL PATTERN GENERATOR
AD9779 EVALUATION BOARD
SPECTRUM ANALYZER
CLOCK IN
DATACLK OUT
1.8V POWER SUPPLY
3.3V POWER SUPPLY
05361-097

Figure 98. Typical Test Setup

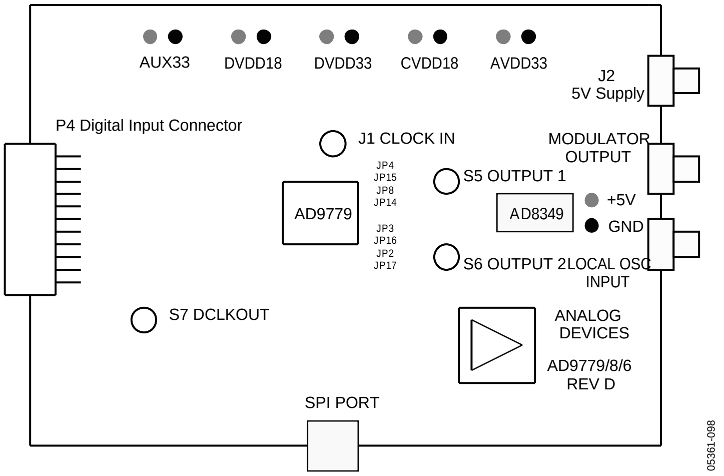
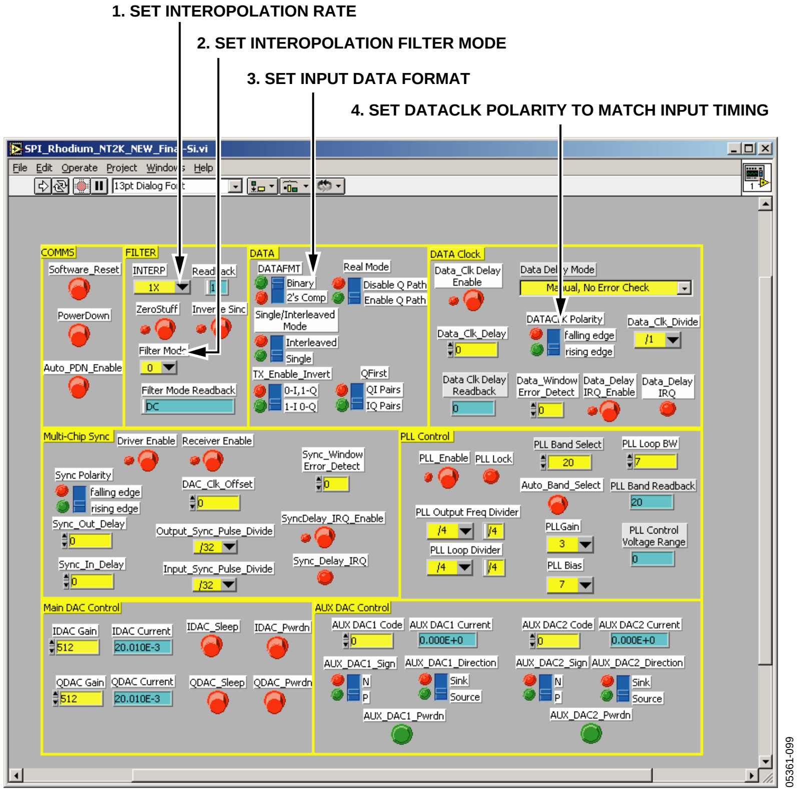

AUX33
DVDD18
DVDD33
CVDD18
AVDD33
J2
5V Supply
P4 Digital Input Connector
J1 CLOCK IN
MODULATOR OUTPUT
JP4
JP15
JP8
JP14
S5 OUTPUT 1
AD9779
AD8349
+5V
GND
JP3
JP16
JP2
JP17
S6 OUTPUT 2
LOCAL OSC INPUT
S7 DCLKOUT
ANALOG DEVICES
AD9779/8/6
REV D
SPI PORT
05361-098

Figure 99. AD977x Evaluation Board Showing all Connections



1. SET INTEROPOLATION RATE

2. SET INTEROPOLATION FILTER MODE

3. SET INPUT DATA FORMAT

4. SET DATACLK POLARITY TO MATCH INPUT TIMING

SPI_Rhodium_NT2K_NEW_Fina -Si.vi

INTERP: 1X

Readback: 1

Filter Mode: 0

Filter Mode Readback: DC

Data Delay Mode: Manual, No Error Check

Data_Clk_Delay: 0

Data_Clk_Divide: /1

Data Clk Delay Readback: 0

Data_Window Error_Detect: 0

Sync_Window Error_Detect: 0

DAC_Clk_Offset: 0

Sync_Out_Delay: 0

Sync_In_Delay: 0

Output_Sync_Pulse_Divide: /32

Input_Sync_Pulse_Divide: /32

PLL Band Select: 20

PLL Loop BW: 7

PLL Band Readback: 20

PLL Output Freq Divider: /4 /4

PLL Loop Divider: /4 /4

PLLGain: 3

PLL Bias: 7

PLL Control Voltage Range: 0

IDAC Gain: 512

IDAC Current: 20.010E-3

QDAC Gain: 512

QDAC Current: 20.010E-3

AUX DAC1 Code: 0

AUX DAC1 Current: 0.000E+0

AUX DAC2 Code: 0

AUX DAC2 Current: 0.000E+0

File
Edit
Operate
Project
Windows
Help
13pt Dialog Font
COMMS
Software_Reset
PowerDown
Auto_PDN_Enable
FILTER
ZeroStuff
Inverse Sinc
DATA
DATAFMT
Binary
2's Comp
Real Mode
Disable Q Path
Enable Q Path
Single/Interleaved Mode
Interleaved
Single
TX_Enable_Invert
0-I,1-Q
1-I 0-Q
QFirst
QI Pairs
IQ Pairs
DATA Clock
Data_Clk Delay Enable
DATACLK Polarity
falling edge
rising edge
Data_Delay IRQ_Enable
Data_Delay IRQ
Multi-Chip Sync
Driver Enable
Receiver Enable
Sync Polarity
falling edge
rising edge
SyncDelay_IRQ_Enable
Sync_Delay_IRQ
PLL Control
PLL_Enable
PLL Lock
Auto_Band_Select
Main DAC Control
IDAC_Sleep
IDAC_Pwrdn
QDAC_Sleep
QDAC_Pwrdn
AUX DAC Control
AUX_DAC1_Sign
N
P
AUX_DAC1_Direction
Sink
Source
AUX_DAC1_Pwrdn
AUX_DAC2_Sign
N
P
AUX_DAC2_Direction
Sink
Source
AUX_DAC2_Pwrdn
05361-099

Figure 100. SPI Port Software Window

The default settings for the evaluation board allow the user to view the differential outputs through a transformer that converts the DAC output signal to a single-ended signal. On the evaluation board, these transformers are designated T1A, T2A, T3A, and T4A. There are also four common-mode transformers on the board that are designated T1B, T2B, T3B, and T4B. The recommended operating setup is to place the transformer and common-mode transformer in series. A pair of transformers and common-mode transformers are installed on each DAC output, so that the pairs can be set up in either order. As an example, for the frequency range of dc to 30 MHz, it is recommended that the transformer is placed right after the DAC. Above DAC output frequencies of 30 MHz, it is recommended that the common-mode transformer is placed right after the DAC outputs, followed by the transformer.

MODIFYING THE EVALUATION BOARD TO USE THE AD8349 ON-BOARD QUADRATURE MODULATOR

The evaluation board contains an Analog Devices AD8349 quadrature modulator. The AD977x and AD8349 provide an easy-to-interface DAC/modulator combination that can be easily evaluated on the evaluation board. To route the DAC output signal to the quadrature modulator, the following jumper settings must be made:

Unsoldered: JP14, JP15, JP16, JP17
Soldered: JP2, JP3, JP4, JP8

The DAC output area of the evaluation board is shown in Figure 101. The jumpers that need to be changed to use the AD8349 are circled. Also circled are the 5 V and GND connections for the AD8349.

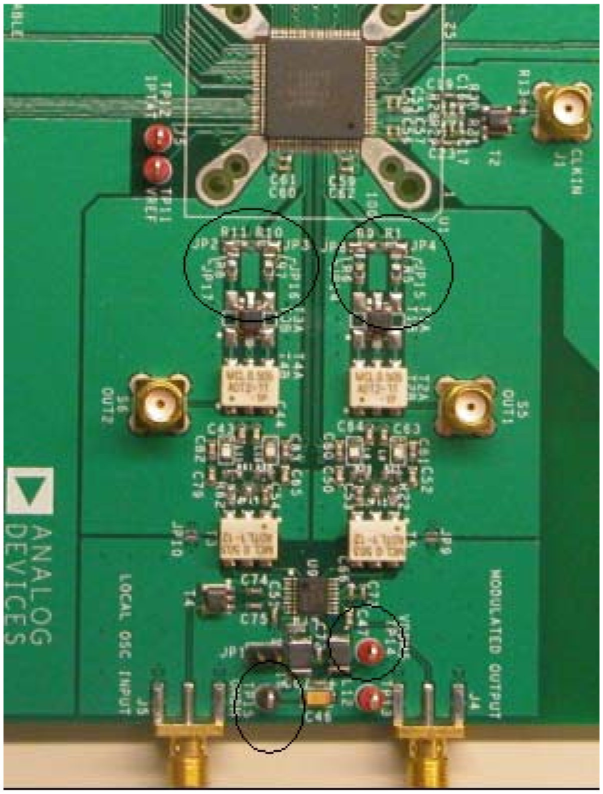

JP2
R11
R10
JP3
JP4
R9
R1
JP17
JP16
JP15
CLKIN
J1
OUT2
J6
OUT1
J5
ANALOG
DEVICES
LOCAL OSC INPUT
MODULATED OUTPUT
JP10
JP9
JP1
C74
C75
C46
J4
05361-100

Figure 101. Photo of Evaluation Board, DAC Output Area

EVALUATION BOARD SCHEMATICS

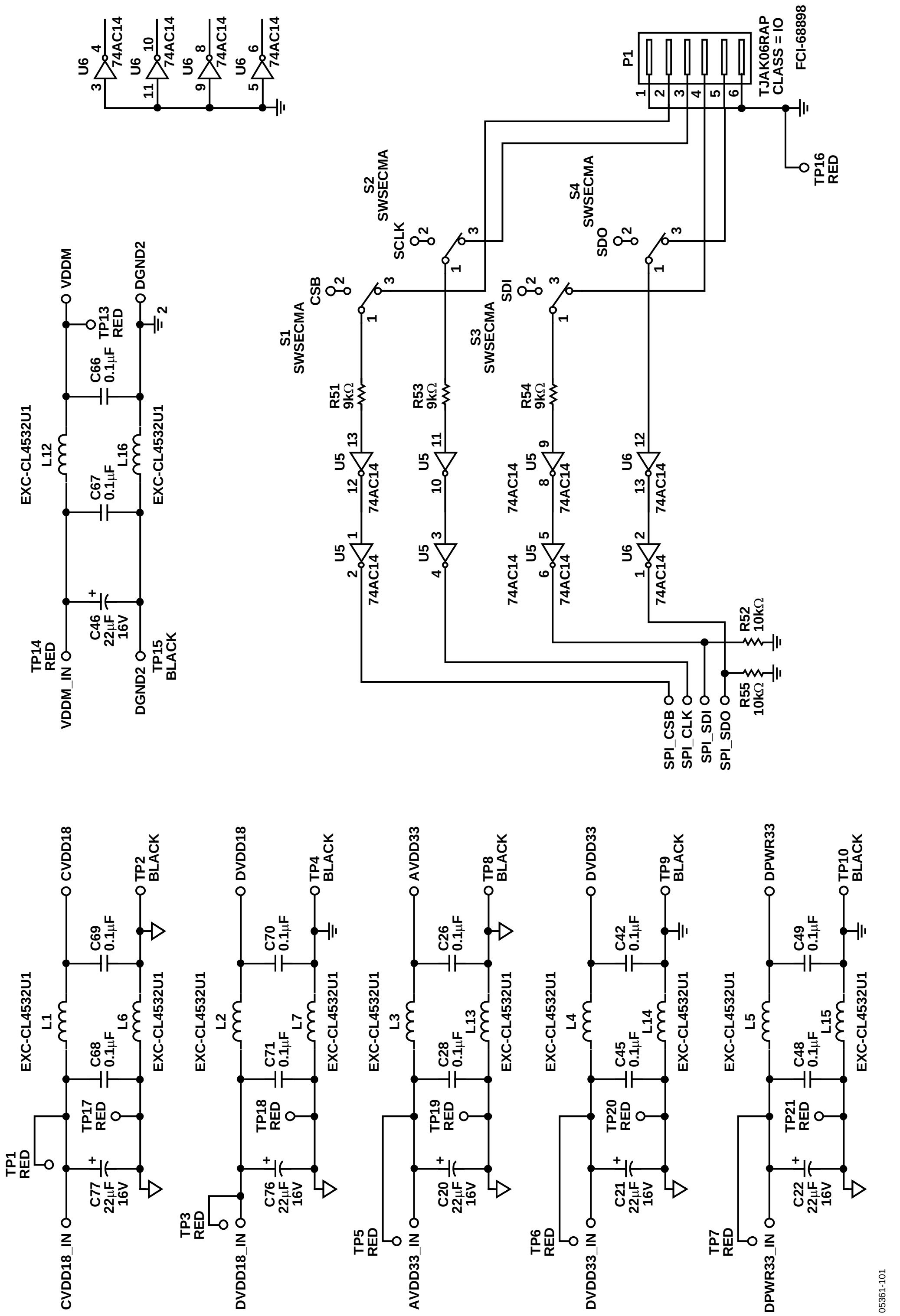

U6
74AC14
VDDM
DGND2
TP13
RED
C66
0.1µF
C67
0.1µF
C46
22µF
16V
L12
L16
EXC-CL4532U1
TP14
RED
TP15
BLACK
VDDM_IN
P1
TJAK06RAP
CLASS = IO
FCI-68898
TP16
RED
S1
S2
S3
S4
SWSECMA
CSB
SCLK
SDI
SDO
R51
R53
R54
9kΩ
R52
R55
10kΩ
U5
74AC14
SPI_CSB
SPI_CLK
SPI_SDI
SPI_SDO
CVDD18
DVDD18
AVDD33
DVDD33
DPWR33
CVDD18_IN
DVDD18_IN
AVDD33_IN
DVDD33_IN
DPWR33_IN
TP1
TP3
TP5
TP6
TP7
TP17
TP18
TP19
TP20
TP21
RED
TP2
TP4
TP8
TP9
TP10
BLACK
L1
L2
L3
L4
L5
L6
L7
L13
L14
L15
C69
C70
C26
C42
C49
C68
C71
C28
C45
C48
0.1µF
C77
C76
C20
C21
C22
22µF
16V
05361-101

Figure 102. Evaluation Board, Rev. D, Power Supply Decoupling and SPI Interface

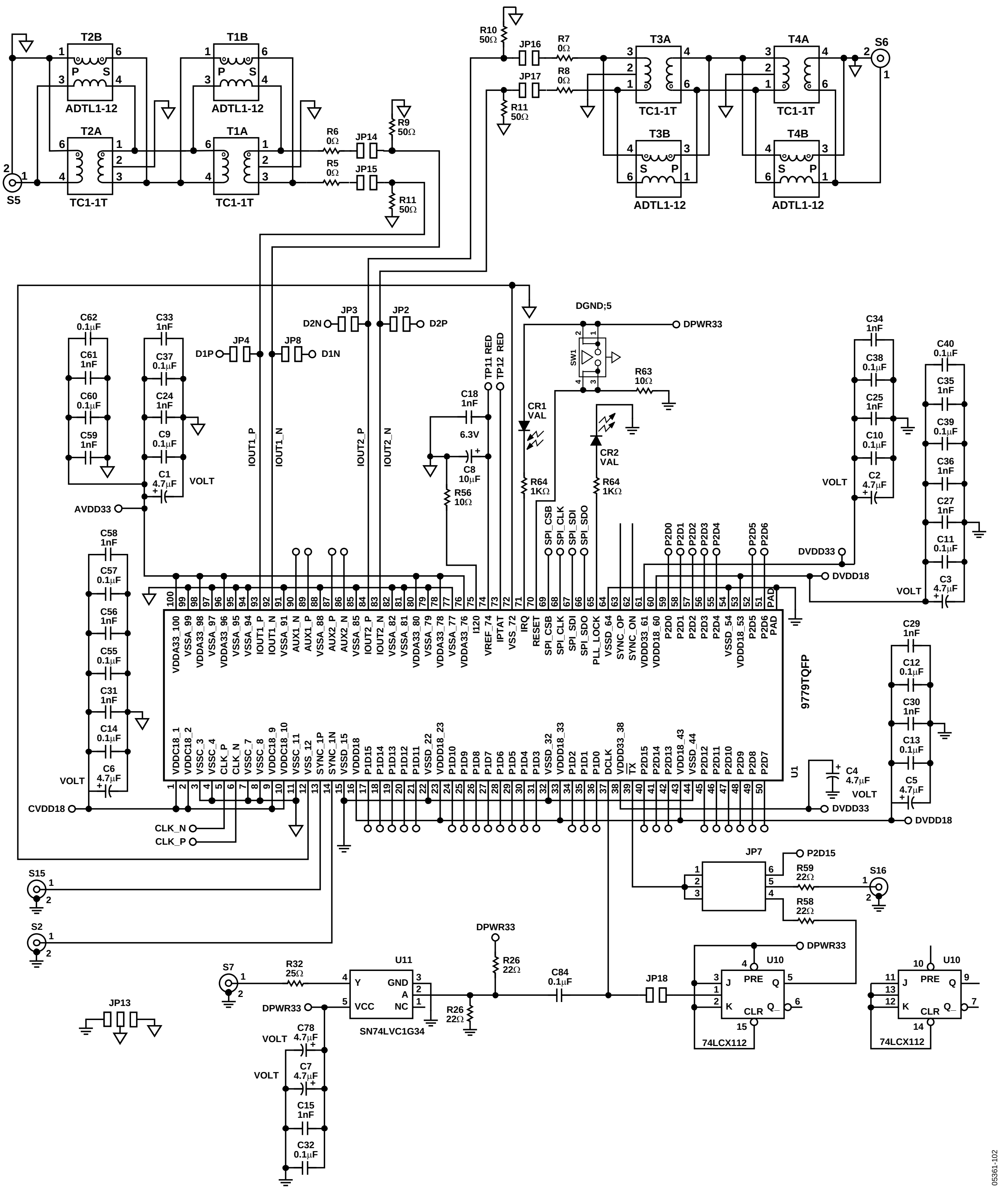

T2B
ADTL1-12
T2A
TC1-1T
T1B
ADTL1-12
T1A
TC1-1T
P
S
S5
R6
0Ω
R5
0Ω
JP14
JP15
R9
50Ω
R11
50Ω
R10
50Ω
JP16
JP17
R7
0Ω
R8
0Ω
R11
50Ω
T3A
TC1-1T
T3B
ADTL1-12
T4A
TC1-1T
T4B
ADTL1-12
S6
C62
0.1µF
C61
1nF
C60
0.1µF
C59
1nF
C33
1nF
C37
0.1µF
C24
1nF
C9
0.1µF
C1
4.7µF
VOLT
AVDD33
D1P
JP4
JP8
D1N
D2N
JP3
JP2
D2P
IOUT1_P
IOUT1_N
IOUT2_P
IOUT2_N
TP11 RED
TP12 RED
C18
1nF
6.3V
C8
10µF
R56
10Ω
DGND;5
DPWR33
SW1
R63
10Ω
CR1
VAL
CR2
VAL
R64
1KΩ
R64
1KΩ
SPI_CSB
SPI_CLK
SPI_SDI
SPI_SDO
P2D0
P2D1
P2D2
P2D3
P2D4
P2D5
P2D6
C34
1nF
C38
0.1µF
C25
1nF
C10
0.1µF
C2
4.7µF
VOLT
DVDD33
DVDD18
C40
0.1µF
C35
1nF
C39
0.1µF
C36
1nF
C27
1nF
C11
0.1µF
C3
4.7µF
VOLT
C58
1nF
C57
0.1µF
C56
1nF
C55
0.1µF
C31
1nF
C14
0.1µF
C6
4.7µF
VOLT
CVDD18
VDDA33_100
VSSA_99
VDDA33_98
VSSA_97
VDDA33_96
VSSA_95
VSSA_94
IOUT1_P
IOUT1_N
VSSA_91
AUX1_N
AUX1_P
VSSA_88
AUX2_P
AUX2_N
VSSA_85
IOUT2_P
IOUT2_N
VSSA_82
VSSA_81
VDDA33_80
VSSA_79
VDDA33_78
VSSA_77
VDDA33_76
I120
VREF_74
IPTAT
VSS_72
IRQ
RESET
SPI_CSB
SPI_CLK
SPI_SDI
SPI_SDO
PLL_LOCK
VSSD_64
SYNC_OP
SYNC_ON
VDDD33_61
VDDD18_60
P2D0
P2D1
P2D2
P2D3
P2D4
VSSD_54
VDDD18_53
P2D5
P2D6
PAD
9779TQFP
U1
VDDC18_1
VDDC18_2
VSSC_3
VSSC_4
CLK_P
CLK_N
VSSC_7
VSSC_8
VDDC18_9
VDDC18_10
VSSC_11
VSS_12
SYNC_1P
SYNC_1N
VSSD_15
VDDD18
P1D15
P1D14
P1D13
P1D12
P1D11
VSSD_22
VDDD18_23
P1D10
P1D9
P1D8
P1D7
P1D6
P1D5
P1D4
P1D3
VSSD_32
VDDD18_33
P1D2
P1D1
P1D0
DCLK
VDDD33_38
TX
P2D15
P2D14
P2D13
VDDD18_43
VSSD_44
P2D12
P2D11
P2D10
P2D9
P2D8
P2D7
C29
1nF
C12
0.1µF
C30
1nF
C13
0.1µF
C5
4.7µF
VOLT
C4
4.7µF
VOLT
DVDD33
DVDD18
CLK_N
CLK_P
S15
S2
JP7
P2D15
R59
22Ω
S16
R58
22Ω
DPWR33
S7
R32
25Ω
U11
Y
GND
A
VCC
NC
SN74LVC1G34
DPWR33
R26
22Ω
C84
0.1µF
R26
22Ω
JP18
DPWR33
U10
J
PRE
Q
K
CLR
Q_
74LCX112
U10
J
PRE
Q
K
CLR
Q_
74LCX112
JP13
C78
4.7µF
VOLT
C7
4.7µF
VOLT
C15
1nF
C32
0.1µF
05361-102

Figure 103. Evaluation Board, Rev. D, Circuitry Local to Devices

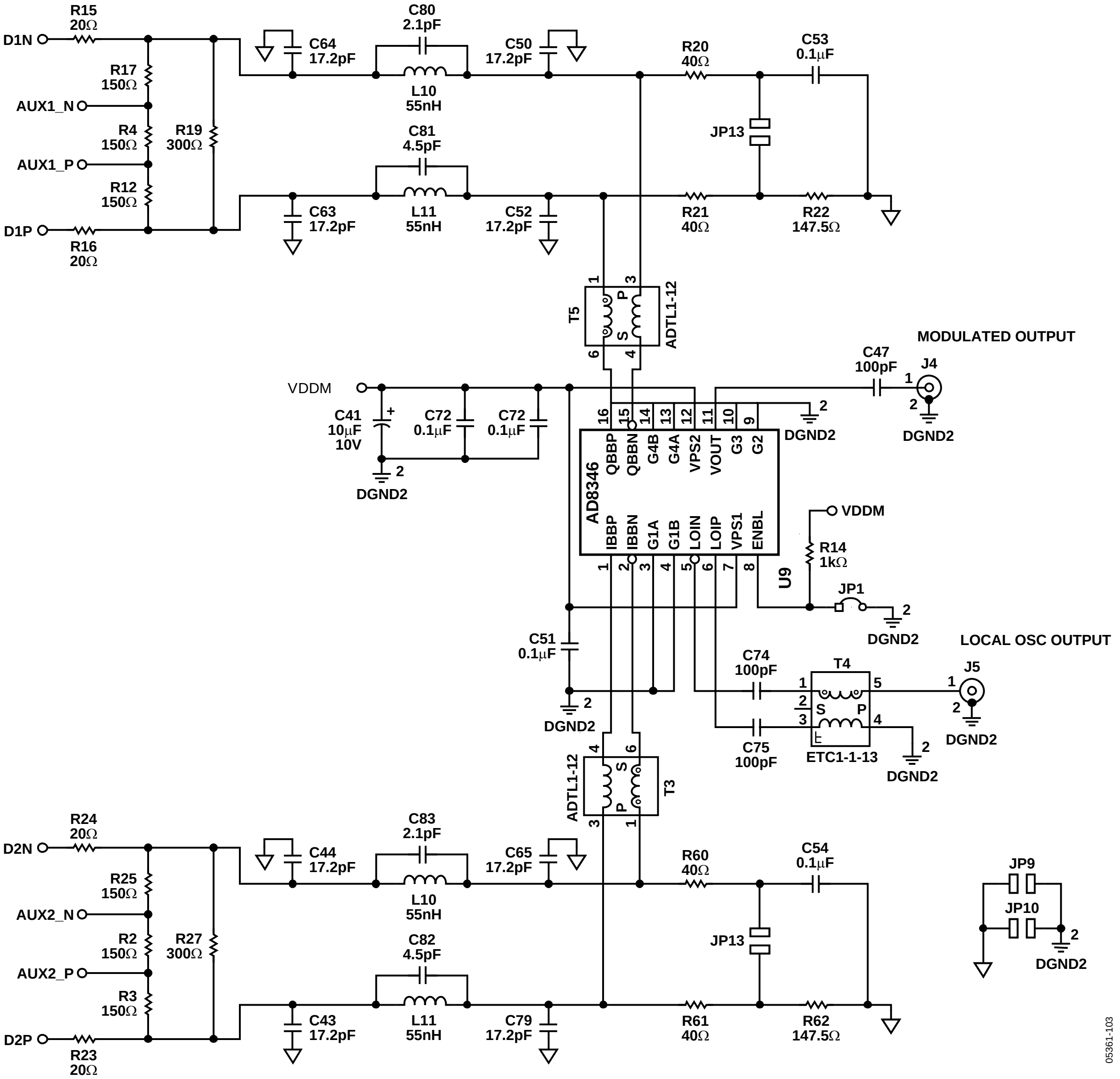

R15
20Ω
D1N
C80
2.1pF
C64
17.2pF
C50
17.2pF
R20
40Ω
C53
0.1µF
R17
150Ω
L10
55nH
AUX1_N
JP13
R4
150Ω
R19
300Ω
C81
4.5pF
AUX1_P
R12
150Ω
L11
55nH
C63
17.2pF
C52
17.2pF
R21
40Ω
R22
147.5Ω
D1P
R16
20Ω
T5
S
P
ADTL1-12
1
3
6
4
MODULATED OUTPUT
C47
100pF
J4
VDDM
C41
10µF
10V
C72
0.1µF
C72
0.1µF
DGND2
16
15
14
13
12
11
10
9
QBBP
QBBN
G4B
G4A
VPS2
VOUT
G3
G2
AD8346
IBBP
IBBN
G1A
G1B
LOIN
LOIP
VPS1
ENBL
1
2
3
4
5
6
7
8
U9
VDDM
R14
1kΩ
JP1
DGND2
LOCAL OSC OUTPUT
C51
0.1µF
C74
100pF
T4
J5
S
P
ETC1-1-13
C75
100pF
DGND2
ADTL1-12
T3
R24
20Ω
D2N
C83
2.1pF
C44
17.2pF
C65
17.2pF
R60
40Ω
C54
0.1µF
JP9
R25
150Ω
L10
55nH
JP10
AUX2_N
R2
150Ω
R27
300Ω
JP13
DGND2
AUX2_P
C82
4.5pF
R3
150Ω
C43
17.2pF
L11
55nH
C79
17.2pF
R61
40Ω
R62
147.5Ω
D2P
R23
20Ω
05361-103

Figure 104. Evaluation Board, Rev. D, AD8349 Quadrature Modulator

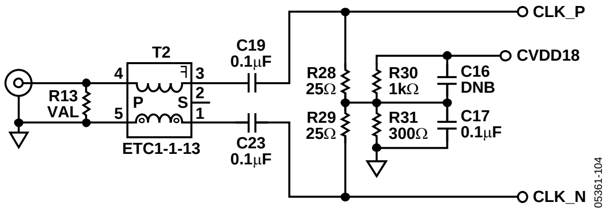

CLK_P
T2
C19
0.1µF
CVDD18
R28
25Ω
R30
1kΩ
C16
DNB
R13
VAL
P
S
R29
25Ω
R31
300Ω
C17
0.1µF
4
5
3
2
1
ETC1-1-13
C23
0.1µF
CLK_N
05361-104

Figure 105. Evaluation Board, Rev. D, DAC Clock Interface

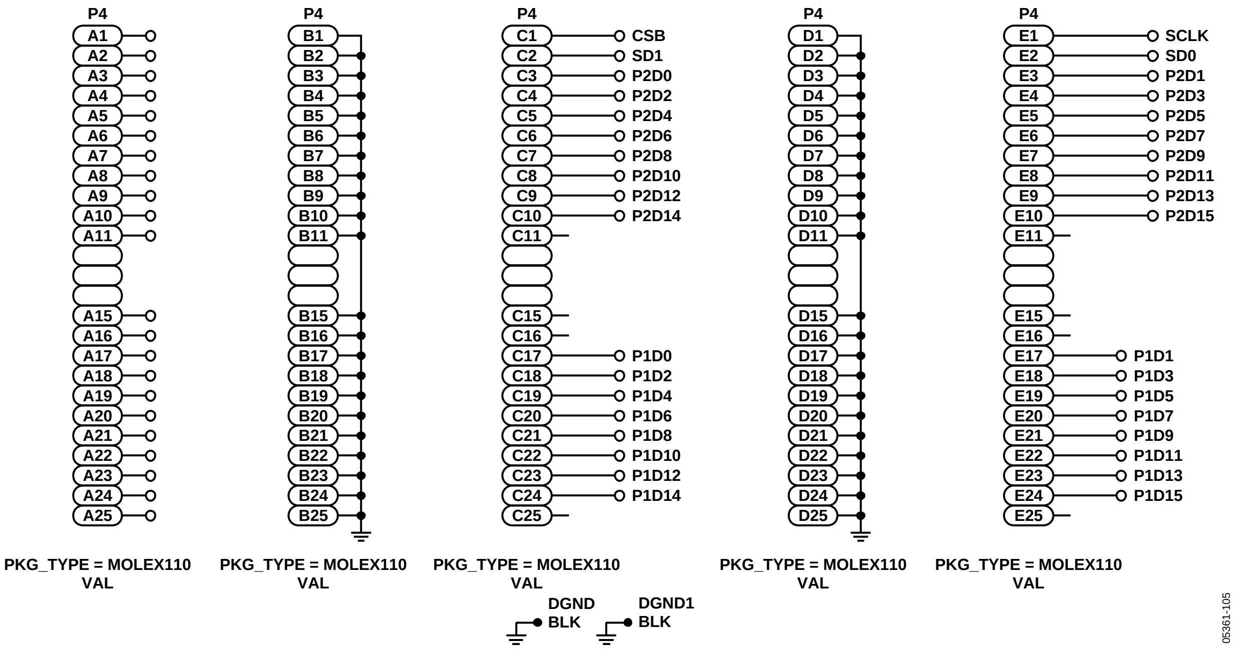

P4
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A15
A16
A17
A18
A19
A20
A21
A22
A23
A24
A25
PKG_TYPE = MOLEX110
VAL
P4
B1
B2
B3
B4
B5
B6
B7
B8
B9
B10
B11
B15
B16
B17
B18
B19
B20
B21
B22
B23
B24
B25
PKG_TYPE = MOLEX110
VAL
P4
C1
CSB
C2
SD1
C3
P2D0
C4
P2D2
C5
P2D4
C6
P2D6
C7
P2D8
C8
P2D10
C9
P2D12
C10
P2D14
C11
C15
C16
C17
P1D0
C18
P1D2
C19
P1D4
C20
P1D6
C21
P1D8
C22
P1D10
C23
P1D12
C24
P1D14
C25
PKG_TYPE = MOLEX110
VAL
DGND
BLK
DGND1
BLK
P4
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D15
D16
D17
D18
D19
D20
D21
D22
D23
D24
D25
PKG_TYPE = MOLEX110
VAL
P4
E1
SCLK
E2
SD0
E3
P2D1
E4
P2D3
E5
P2D5
E6
P2D7
E7
P2D9
E8
P2D11
E9
P2D13
E10
P2D15
E11
E15
E16
E17
P1D1
E18
P1D3
E19
P1D5
E20
P1D7
E21
P1D9
E22
P1D11
E23
P1D13
E24
P1D15
E25
PKG_TYPE = MOLEX110
VAL
05361-105

Figure 106. Evaluation Board, Rev. D, Digital Input Buffers

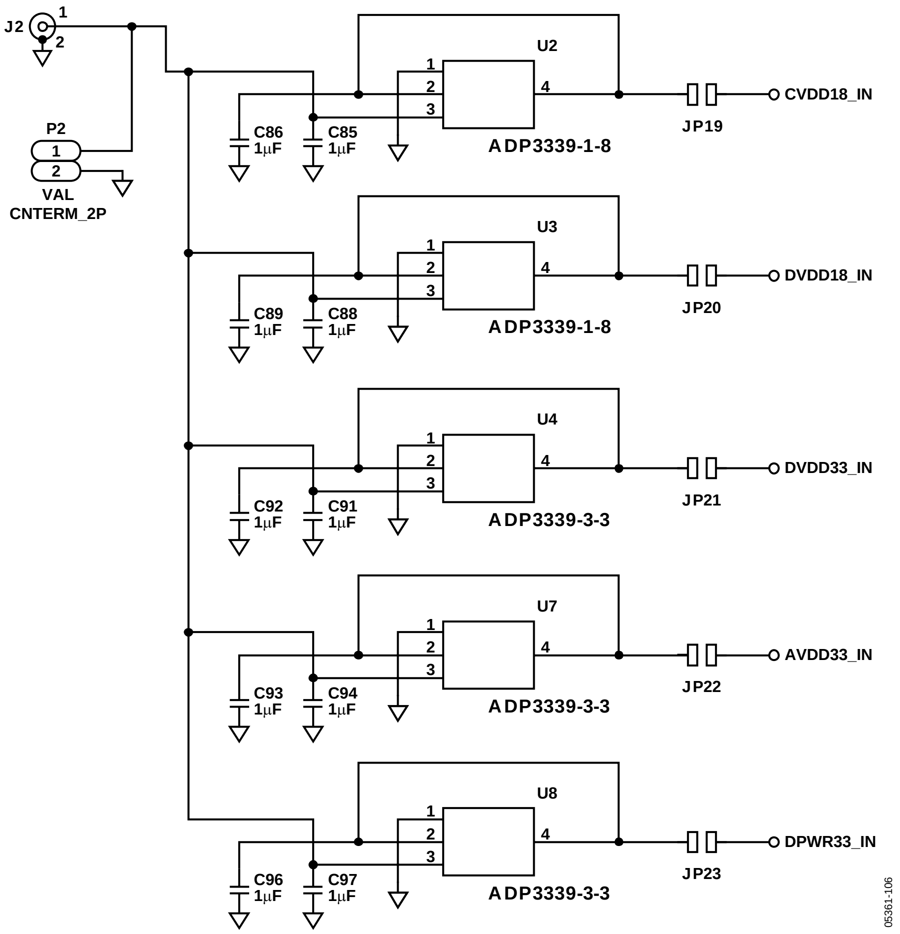

J2
1
2
P2
1
2
VAL
CNTERM_2P
U2
1
2
3
4
C86
1µF
C85
1µF
ADP3339-1-8
JP19
CVDD18_IN
U3
1
2
3
4
C89
1µF
C88
1µF
ADP3339-1-8
JP20
DVDD18_IN
U4
1
2
3
4
C92
1µF
C91
1µF
ADP3339-3-3
JP21
DVDD33_IN
U7
1
2
3
4
C93
1µF
C94
1µF
ADP3339-3-3
JP22
AVDD33_IN
U8
1
2
3
4
C96
1µF
C97
1µF
ADP3339-3-3
JP23
DPWR33_IN
05361-106

Figure 107. Evaluation Board, On-Board Voltage Regulators

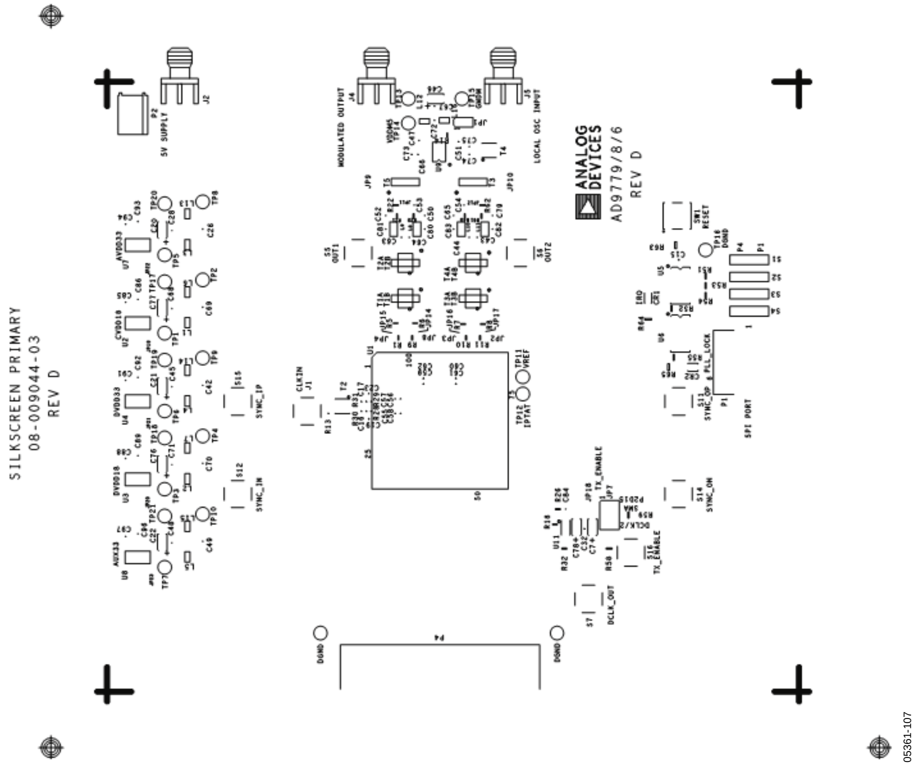

SILKSCREEN PRIMARY
08-009044-03
REV D
ANALOG DEVICES
AD9779/8/6
REV D
5V SUPPLY
MODULATED OUTPUT
LOCAL OSC INPUT
SPI PORT
05361-107

Figure 108. Evaluation Board, Rev. D, Top Silk Screen

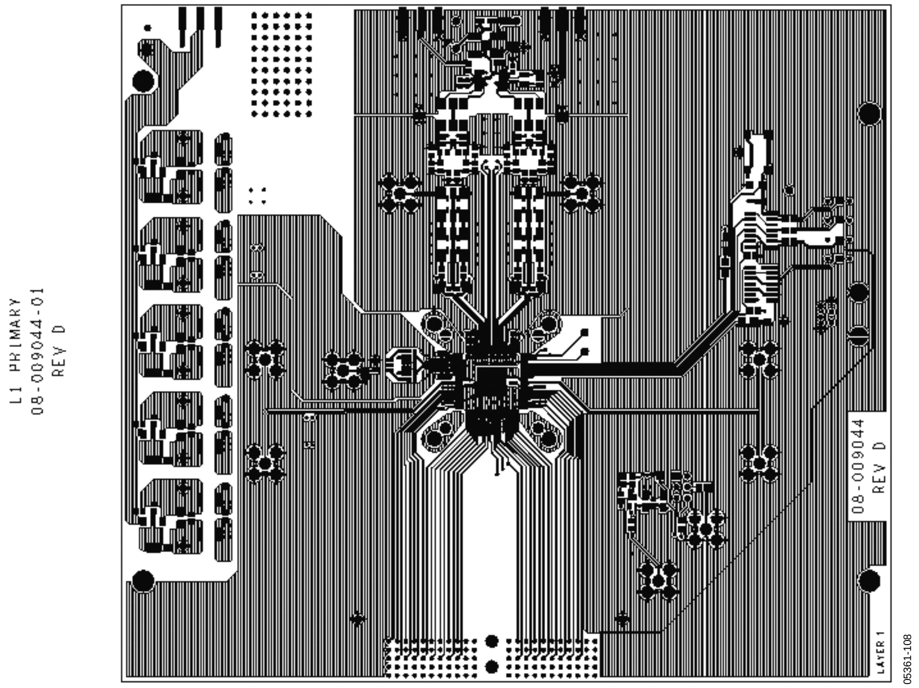

L1 PRIMARY
08-009044-01
REV D
08-009044
REV D
LAYER 1
05361-108

Figure 109. Evaluation Board, Rev. D, Top Layer

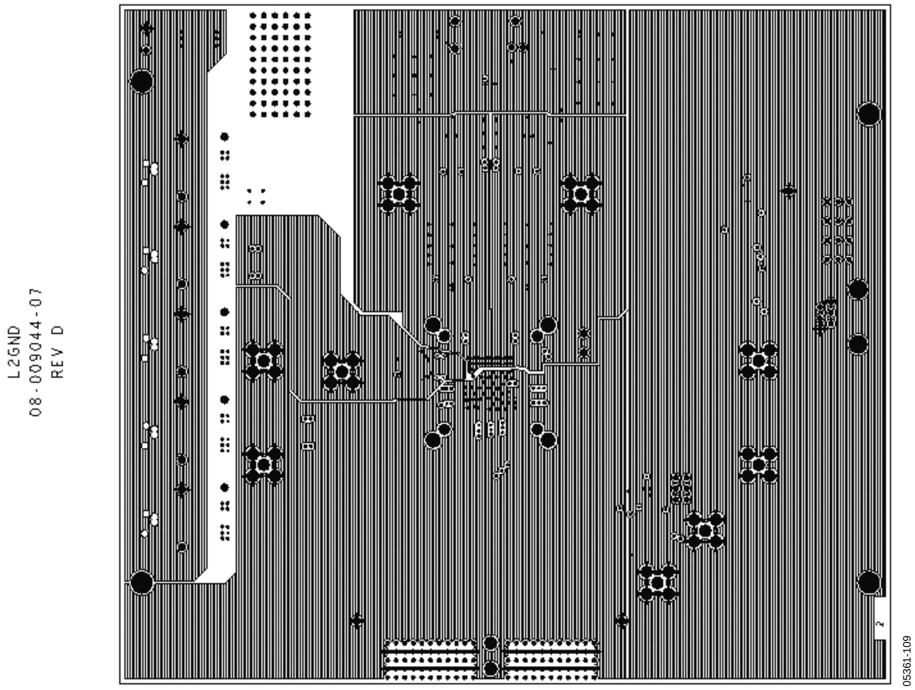

L2GND
08-009044-07
REV D
2
05361-109

Figure 110. Evaluation Board, Rev. D, Layer 2

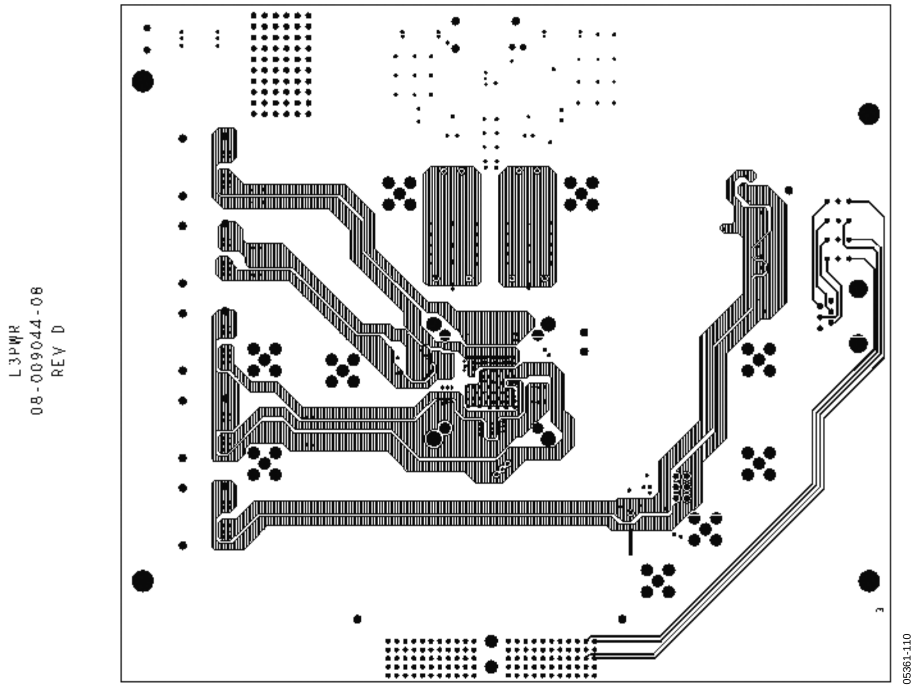

L3PWR
08-009044-08
REV D
3
05361-110

Figure 111. Evaluation Board, Rev. D, Layer 3

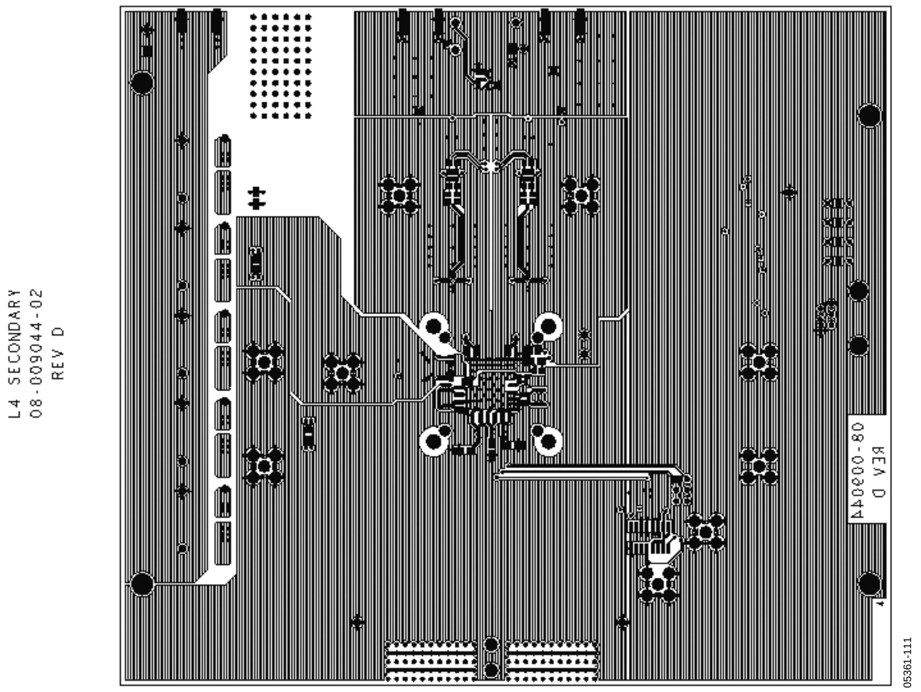

L4 SECONDARY
08-009044-02
REV D
08-009044
REV D
05361-111

Figure 112. Evaluation Board, Rev. D, Bottom Layer

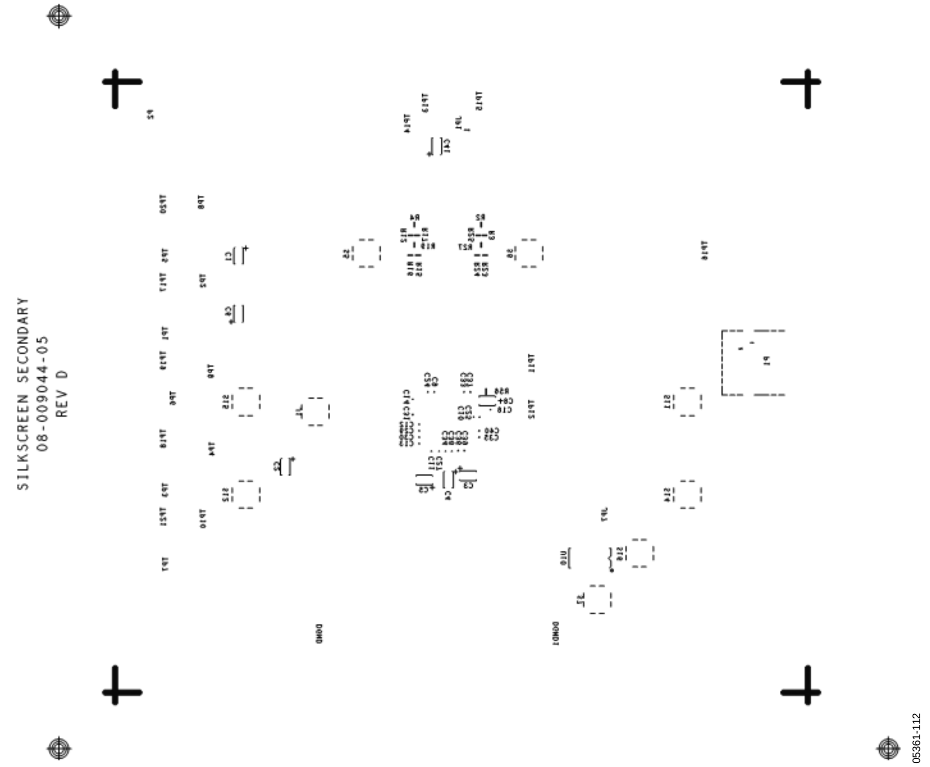
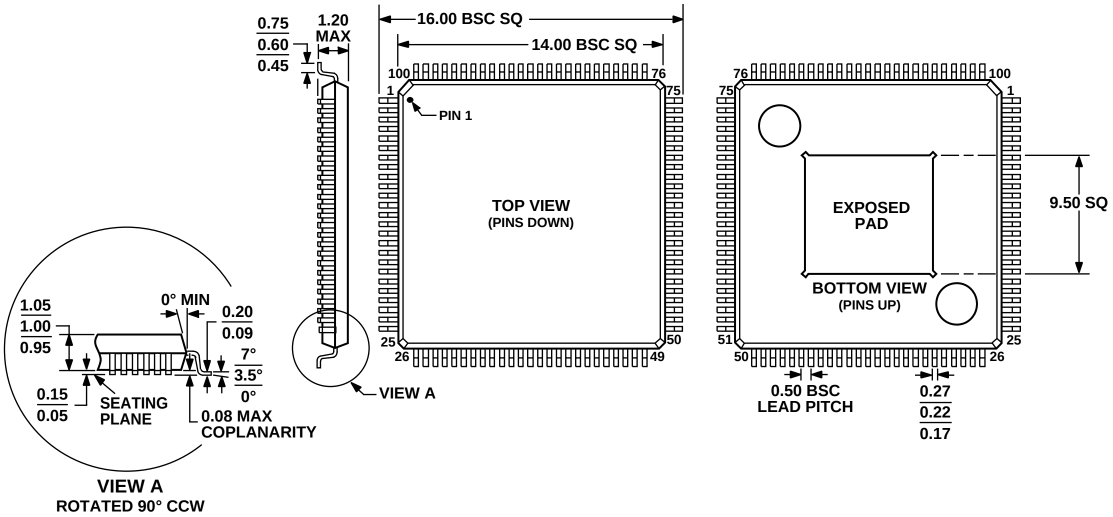

SILKSCREEN SECONDARY
08-009044-05
REV D
05361-112

Figure 113. Evaluation Board, Rev. D, Bottom Silkscreen

OUTLINE DIMENSIONS


0.75
0.60
0.45
1.20
MAX
16.00 BSC SQ
14.00 BSC SQ
100
76
1
75
PIN 1
TOP VIEW
(PINS DOWN)
25
50
26
49
76
100
75
1
EXPOSED
PAD
9.50 SQ
BOTTOM VIEW
(PINS UP)
51
25
50
26
0.50 BSC
LEAD PITCH
0.27
0.22
0.17
VIEW A
1.05
1.00
0.95
0° MIN
0.20
0.09
7°
3.5°
0°
0.15
0.05
SEATING
PLANE
0.08 MAX
COPLANARITY
VIEW A
ROTATED 90° CCW

COMPLIANT TO JEDEC STANDARDS MS-026-AED-HD

Figure 114. 100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]
(SV-100-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9776BSVZ[1]	−40°C to +85°C	100-lead TQFP_EP	SV-100-3
AD9776BSVZRL[1]	−40°C to +85°C	100-lead TQFP_EP	SV-100-3
AD9778BSVZ[1]	−40°C to +85°C	100-lead TQFP_EP	SV-100-3
AD9778BSVZRL[1]	−40°C to +85°C	100-lead TQFP_EP	SV-100-3
AD9779BSVZ[1]	−40°C to +85°C	100-lead TQFP_EP	SV-100-3
AD9779BSVZRL[1]	−40°C to +85°C	100-lead TQFP_EP	SV-100-3
AD9776-EB		Evaluation Board	
AD9778-EB		Evaluation Board	
AD9779-EB		Evaluation Board	

[1] Z = Pb-free part.

NOTES

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