# 2.7 V to 5.5 V, 250 µA, Rail-to-Rail Output, Dual 16-Bit *nano*DAC®

# AD5663

## FEATURES

**Low power, dual 16-bit *nano*DAC**
**Relative accuracy: ±12 LSBs maximum**
**Guaranteed monotonic by design**
**10-lead MSOP and 3 mm × 3 mm LFCSP_WD**
**2.7 V to 5.5 V power supply**
**Per channel power-down**
**Power-on reset to zero scale or midscale**
**Hardware $\overline{\text{LDAC}}$ and $\overline{\text{CLR}}$ functions**
**Serial interface; up to 50 MHz**

## APPLICATIONS

**Process control**
**Data acquisition systems**
**Portable battery-powered instruments**
**Digital gain and offset adjustment**
**Programmable voltage and current sources**
**Programmable attenuators**

## GENERAL DESCRIPTION

The AD5663, a member of the *nano*DAC family, is a low power, dual, 16-bit buffered voltage-out DAC that operates from a single 2.7 V to 5.5 V supply and is guaranteed monotonic by design.

The AD5663 requires an external reference voltage to set the output range of the DAC. The part incorporates a power-on reset circuit that ensures the DAC output powers up to 0 V or midscale (AD5663-1) and remains there until a valid write takes place. The part contains a power-down feature that reduces the current consumption of the device to 480 nA at 5 V and provides software-selectable output loads while in power-down mode.

The low power consumption of this part in normal operation makes it ideally suited to portable, battery-operated equipment. The power consumption is 1.25 mW at 5 V, going down to 2.4 µW in power-down mode.

The on-chip precision output amplifier of the AD5663 allows rail-to-rail output swing to be achieved.

The AD5663 uses a versatile, 3-wire serial interface that operates at clock rates up to 50 MHz and is compatible with standard SPI®, QSPI™, MICROWIRE™, and DSP interface standards.

## FUNCTIONAL BLOCK DIAGRAM

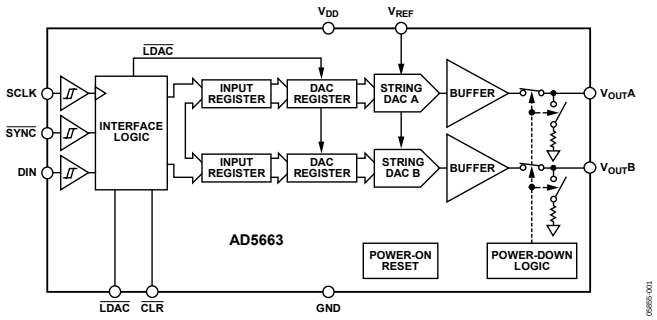


*Figure 1.*

**Table 1. Related Devices**

| Part No. | Description |
|---|---|
| AD5623R/AD5643R/AD5663R | 2.7 V to 5.5 V, dual 12-/14-/16-bit DACs with internal reference |

## PRODUCT HIGHLIGHTS

1. Dual 16-bit DAC; relative accuracy of ±12 LSBs maximum.
2. Available in 10-lead MSOP and 10-lead, 3 mm × 3 mm LFCSP_WD packages.
3. Low power; typically consumes 0.6 mW at 3 V and 1.25 mW at 5 V.
4. 7 µs maximum settling time.

**Rev. 0**


**One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.**
**Tel: 781.329.4700** **www.analog.com**
**Fax: 781.461.3113** 

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## REVISION HISTORY

**4/06—Revision 0: Initial Version**

# SPECIFICATIONS

$V_{DD}$ = 2.7 V to 5.5 V; $R_L$ = 2 kΩ to GND; $C_L$ = 200 pF to GND; $V_{REF} = V_{DD}$; all specifications $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 2.**

| | A Grade[1] | | | B Grade[1] | | | | |
|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** | **Conditions/Comments** |
| STATIC PERFORMANCE[2] | | | | | | | | |
| AD5663 | | | | | | | | |
| Resolution | 16 | | | 16 | | | Bits | |
| Relative Accuracy | | ±8 | ±16 | | ±6 | ±12 | LSB | |
| Differential Nonlinearity | | | ±1 | | | ±1 | LSB | Guaranteed monotonic by design |
| Zero-Scale Error | | +2 | +10 | | +2 | +10 | mV | All 0s loaded to DAC register |
| Offset Error | | ±1 | ±10 | | ±1 | ±10 | mV | |
| Full-Scale Error | | −0.15 | ±1 | | −0.15 | ±1 | % of FSR | All 1s loaded to DAC register |
| Gain Error | | | ±1.5 | | | ±1.5 | % of FSR | |
| Zero-Scale Error Drift[3] | | ±2 | | | ±2 | | µV/°C | |
| Gain Temperature Coefficient | | ±2.5 | | | ±2.5 | | ppm | Of FSR/°C |
| DC Power Supply Rejection Ratio | | −100 | | | −100 | | dB | DAC code = midscale, $V_{DD}$ ± 10% |
| DC Crosstalk | | 10 | | | 10 | | µV | Due to full-scale output change<br>$R_L$ = 2 kΩ to GND or $V_{DD}$ |
| | | 10 | | | 10 | | µV/mA | Due to load current change |
| | | 5 | | | 5 | | µV | Due to powering down (per channel) |
| OUTPUT CHARACTERISTICS[2] | | | | | | | | |
| Output Voltage Range | 0 | | $V_{DD}$ | 0 | | $V_{DD}$ | V | |
| Capacitive Load Stability | | 2 | | | 2 | | nF | $R_L = \infty$ |
| | | 10 | | | 10 | | nF | $R_L$ = 2 kΩ |
| DC Output Impedance | | 0.5 | | | 0.5 | | Ω | |
| Short-Circuit Current | | 30 | | | 30 | | mA | $V_{DD}$ = 5 V |
| Power-Up Time | | 4 | | | 4 | | µs | Coming out of power-down mode;<br>$V_{DD}$ = 5 V |
| REFERENCE INPUTS | | | | | | | | |
| Reference Current | | 170 | 200 | | 170 | 200 | µA | $V_{REF} = V_{DD}$ = 5.5 V, 3.6 V |
| Reference Input Range | 0.75 | | $V_{DD}$ | 0.75 | | $V_{DD}$ | V | |
| Reference Input Impedance | | 26 | | | 26 | | kΩ | |
| LOGIC INPUTS[3] | | | | | | | | |
| Input Current | | | ±2 | | | ±2 | µA | All digital inputs |
| $V_{INL}$, Input Low Voltage | | | 0.8 | | | 0.8 | V | $V_{DD}$ = 5 V, 3 V |
| $V_{INH}$, Input High Voltage | 2 | | | 2 | | | V | $V_{DD}$ = 5 V, 3 V |
| Pin Capacitance | | 3 | | | 3 | | pF | DIN, SCLK, and $\overline{SYNC}$ |
| | | 19 | | | 19 | | pF | $\overline{LDAC}$ and $\overline{CLR}$ |
| POWER REQUIREMENTS | | | | | | | | |
| $V_{DD}$ | 2.7 | | 5.5 | 2.7 | | 5.5 | V | |
| $I_{DD}$ (Normal Mode)[4] | | | | | | | | $V_{IH} = V_{DD}$ and $V_{IL}$ = GND |
| $V_{DD}$ = 4.5 V to 5.5 V | | 250 | 450 | | 250 | 450 | µA | |
| $V_{DD}$ = 2.7 V to 3.6 V | | 200 | 425 | | 200 | 425 | µA | |
| $I_{DD}$ (All Power-Down Modes)[5] | | | | | | | | $V_{IH} = V_{DD}$, $V_{IL}$ = GND |
| $V_{DD}$ = 4.5 V to 5.5 V | | 0.48 | 1 | | 0.48 | 1 | µA | |
| $V_{DD}$ = 2.7 V to 3.6 V | | 0.2 | 1 | | 0.2 | 1 | µA | |

[1] Temperature range: A grade and B grade are both equal to −40°C to +105°C.
[2] Linearity calculated using a reduced code range: AD5663 (Code 512 to Code 65024). Output unloaded.
[3] Guaranteed by design and characterization, not production tested.
[4] Interface inactive. All DACs active. DAC outputs unloaded.
[5] Both DACs powered down.

## AC CHARACTERISTICS

$V_{DD}$ = 2.7 V to 5.5 V; $R_L$ = 2 kΩ to GND; $C_L$ = 200 pF to GND; $V_{REF}$ = $V_{DD}$; all specifications $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.[1]

**Table 3.**

| Parameter[2] | Min | Typ | Max | Unit | Conditions/Comments |
|---|---|---|---|---|---|
| Output Voltage Settling Time | | 4 | 7 | µs | 1/4 to 3/4 scale settling to ±2 LSB |
| Slew Rate | | 1.8 | | V/µs | |
| Digital-to-Analog Glitch Impulse | | 10 | | nV-s | 1 LSB change around major carry |
| Digital Feedthrough | | 0.1 | | nV-s | |
| Reference Feedthrough | | −90 | | dBs | $V_{REF}$ = 2 V ± 0.1 V p-p, frequency 10 Hz to 20 MHz |
| Digital Crosstalk | | 0.1 | | nV-s | |
| Analog Crosstalk | | 1 | | nV-s | |
| DAC-to-DAC Crosstalk | | 1 | | nV-s | |
| Multiplying Bandwidth | | 340 | | kHz | $V_{REF}$ = 2 V ± 0.1 V p-p |
| Total Harmonic Distortion | | −80 | | dB | $V_{REF}$ = 2 V ± 0.1 V p-p; frequency = 10 kHz |
| Output Noise Spectral Density | | 120 | | nV/√Hz | DAC code = midscale, 1 kHz |
| | | 100 | | nV/√Hz | DAC code = midscale, 10 kHz |
| Output Noise | | 15 | | µV p-p | 0.1 Hz to 10 Hz |

[1] Guaranteed by design and characterization, not production tested.
[2] See the Terminology section.

## TIMING CHARACTERISTICS

All input signals are specified with $t_R = t_F = 1$ ns/V (10% to 90% of $V_{DD}$) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. $V_{DD}$ = 2.7 V to 5.5 V; all specifications $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.[1]

**Table 4.**

| Parameter | Limit at $T_{MIN}$, $T_{MAX}$ $V_{DD}$ = 2.7 V to 5.5 V | Unit | Conditions/Comments |
|---|---|---|---|
| $t_1$[2] | 20 | ns min | SCLK cycle time |
| $t_2$ | 9 | ns min | SCLK high time |
| $t_3$ | 9 | ns min | SCLK low time |
| $t_4$ | 13 | ns min | $\overline{SYNC}$ to SCLK falling edge setup time |
| $t_5$ | 5 | ns min | Data setup time |
| $t_6$ | 5 | ns min | Data hold time |
| $t_7$ | 0 | ns min | SCLK falling edge to $\overline{SYNC}$ rising edge |
| $t_8$ | 15 | ns min | Minimum $\overline{SYNC}$ high time |
| $t_9$ | 13 | ns min | $\overline{SYNC}$ rising edge to SCLK fall ignore |
| $t_{10}$ | 0 | ns min | SCLK falling edge to $\overline{SYNC}$ fall ignore |
| $t_{11}$ | 10 | ns min | $\overline{LDAC}$ pulse width low |
| $t_{12}$ | 15 | ns min | SCLK falling edge to $\overline{LDAC}$ rising edge |
| $t_{13}$ | 5 | ns min | $\overline{CLR}$ pulse width low |
| $t_{14}$ | 0 | ns min | SCLK falling edge to $\overline{LDAC}$ falling edge |
| $t_{15}$ | 300 | ns max | $\overline{CLR}$ pulse activation time |

[1] Guaranteed by design and characterization; not production tested.
[2] Maximum SCLK frequency is 50 MHz at $V_{DD}$ = 2.7 V to 5.5 V.

## TIMING DIAGRAM

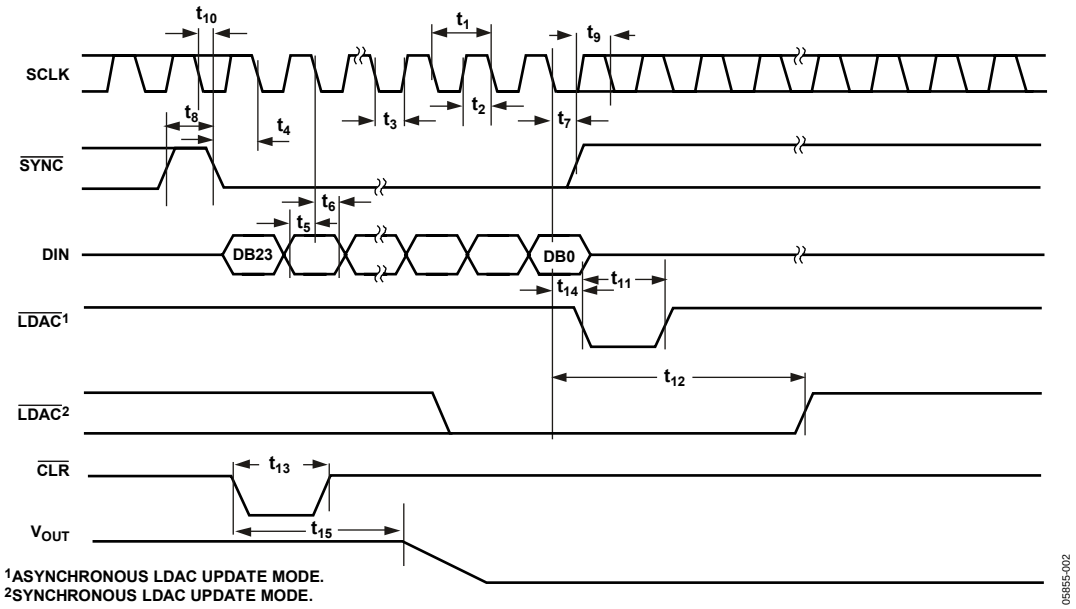



*Figure 2. Serial Write Operation*

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted.

**Table 5.**

| Parameter | Rating |
|---|---|
| $V_{DD}$ to GND | −0.3 V to +7 V |
| $V_{OUT}$ to GND | −0.3 V to $V_{DD}$ + 0.3 V |
| $V_{REF}$ to GND | −0.3 V to $V_{DD}$ + 0.3 V |
| Digital Input Voltage to GND | −0.3 V to $V_{DD}$ + 0.3 V |
| Operating Temperature Range | |
| Industrial | −40°C to +105°C |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature ($T_J$ max) | 150°C |
| Power Dissipation | ($T_J$ max − $T_A$)/$\theta_{JA}$ |
| LFCSP_WD Package (4-Layer Board) | |
| $\theta_{JA}$ Thermal Impedance | 61°C/W |
| MSOP Package (4-Layer Board) | |
| $\theta_{JA}$ Thermal Impedance | 142°C/W |
| $\theta_{JC}$ Thermal Impedance | 43.7°C/W |
| Reflow Soldering Peak Temperature | |
| Pb-Free | 260(+0/−5)°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTION

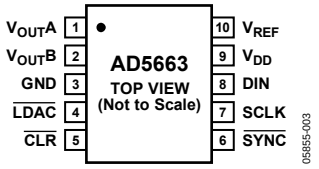



*Figure 3. Pin Configuration*

**Table 6. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | $V_{OUT}A$ | Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation. |
| 2 | $V_{OUT}B$ | Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation. |
| 3 | GND | Ground Reference Point for All Circuitry on the Part. |
| 4 | $\overline{LDAC}$ | Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data. This allows simultaneous update of all DAC outputs. Alternatively, this pin can be tied permanently low. |
| 5 | $\overline{CLR}$ | Asynchronous Clear Input. The $\overline{CLR}$ input is falling edge sensitive. While $\overline{CLR}$ is low, all $\overline{LDAC}$ pulses are ignored. When $\overline{CLR}$ is activated, zero scale is loaded to all input and DAC registers. This clears the output to 0 V. The part exits clear code mode on the 24th falling edge of the next write to the part. If $\overline{CLR}$ is activated during a write sequence, the write is aborted. |
| 6 | $\overline{SYNC}$ | Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, it powers on the SCLK and DIN buffers and enables the input shift register. Data is transferred in on the falling edges of the next 24 clocks. If $\overline{SYNC}$ is taken high before the 24th falling edge, the rising edge of $\overline{SYNC}$ acts as an interrupt, and the write sequence is ignored by the device. |
| 7 | SCLK | Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates up to 50 MHz. |
| 8 | DIN | Serial Data Input. This device has a 24-bit shift register. Data is clocked into the register on the falling edge of the serial clock input. |
| 9 | $V_{DD}$ | Power Supply Input. These parts can be operated from 2.7 V to 5.5 V, and the supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND. |
| 10 | $V_{REF}$ | Reference Voltage Input. |

# TYPICAL PERFORMANCE CHARACTERISTICS

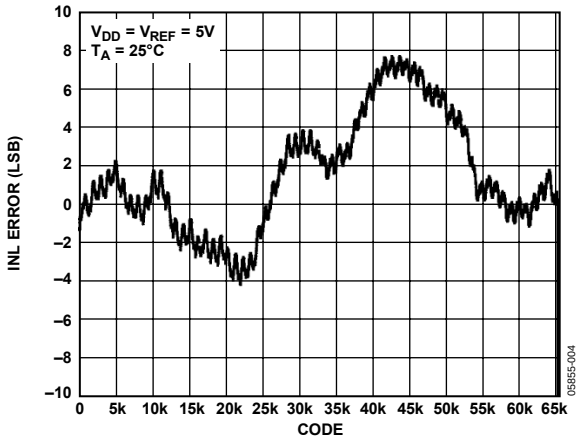



Figure 4. INL

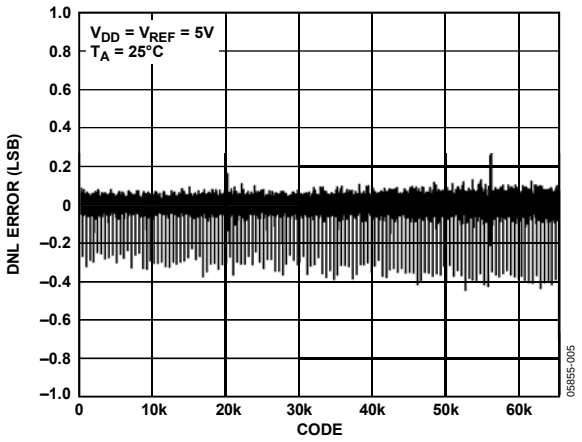



Figure 5. DNL

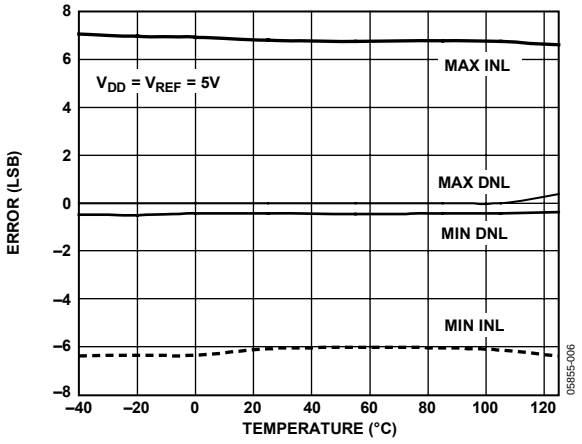



Figure 6. INL Error and DNL Error vs. Temperature

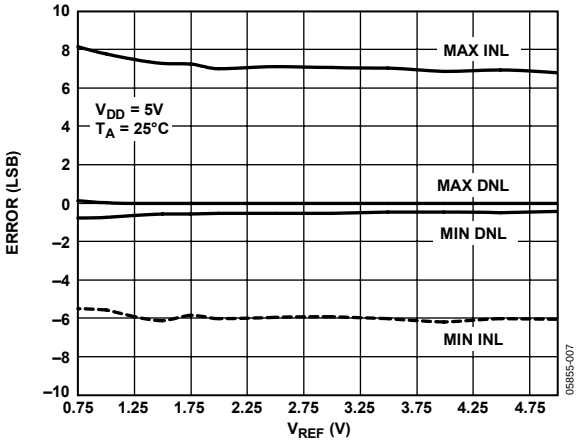



Figure 7. INL and DNL Error vs. $V_{REF}$

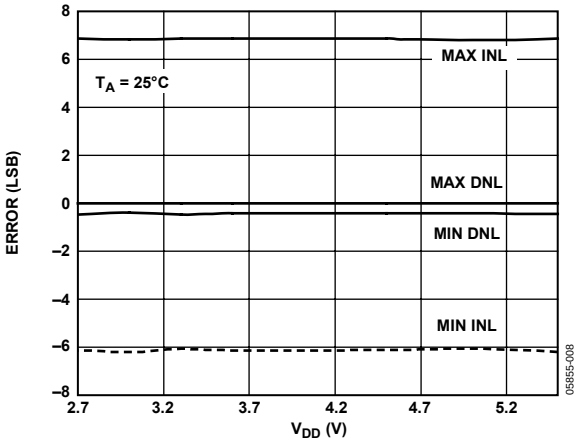



Figure 8. INL and DNL Error vs. Supply

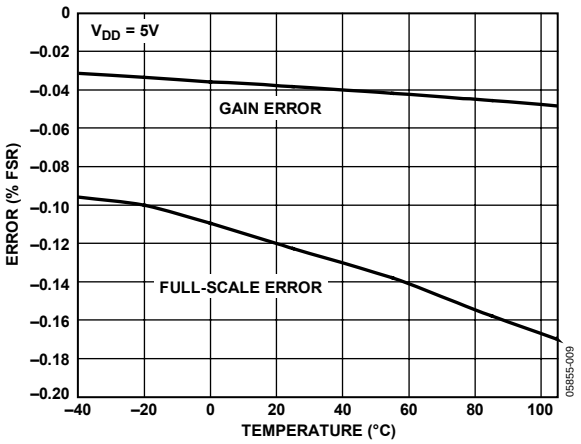



Figure 9. Gain Error and Full-Scale Error vs. Temperature

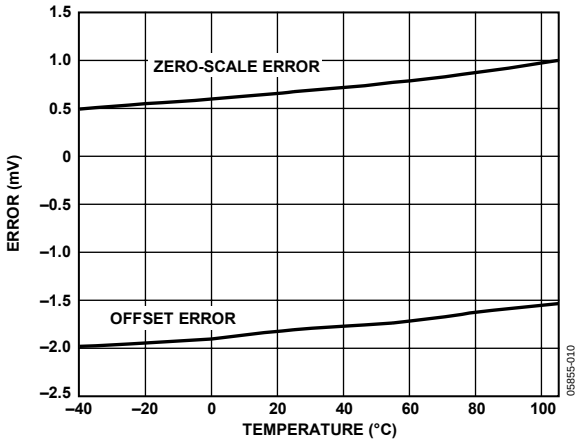



Figure 10. Zero-Scale and Offset Error vs. Temperature

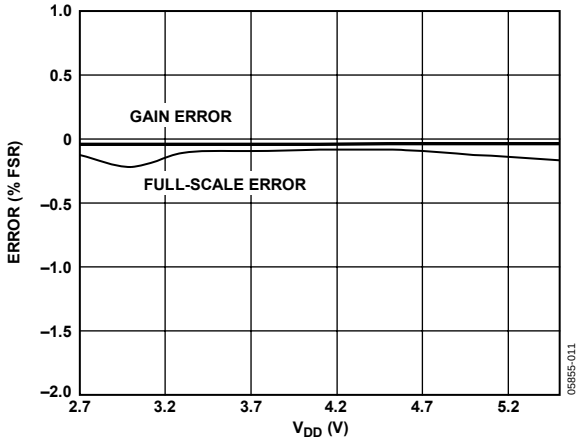



Figure 11. Gain Error and Full-Scale Error vs. Supply

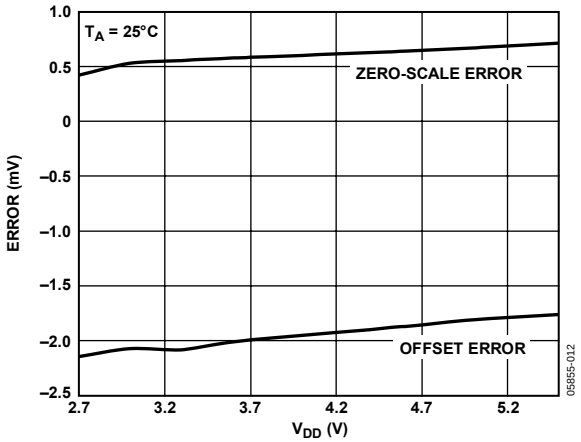



Figure 12. Zero-Scale and Offset Error vs. Supply

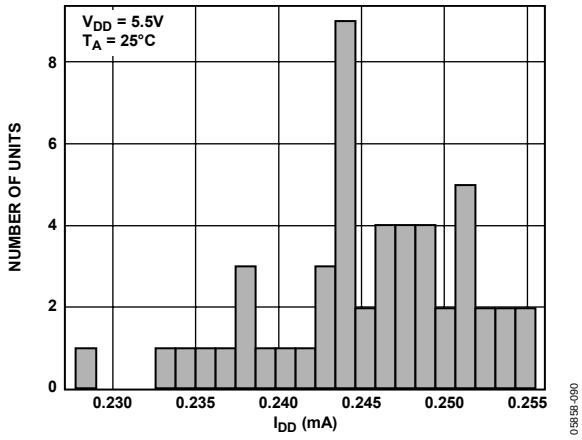



Figure 13. $I_{DD}$ Histogram with $V_{DD}$ = 5.5 V

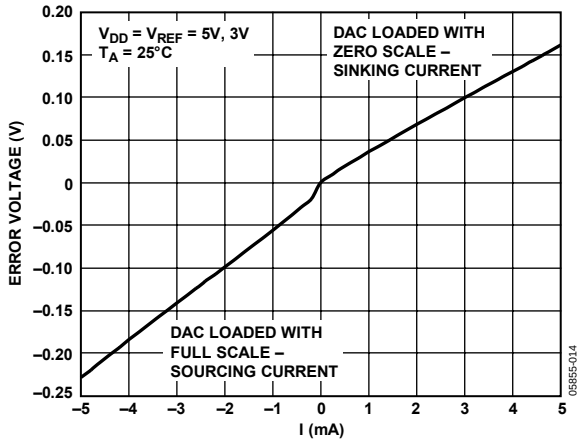



Figure 14. Headroom at Rails vs. Source and Sink Current

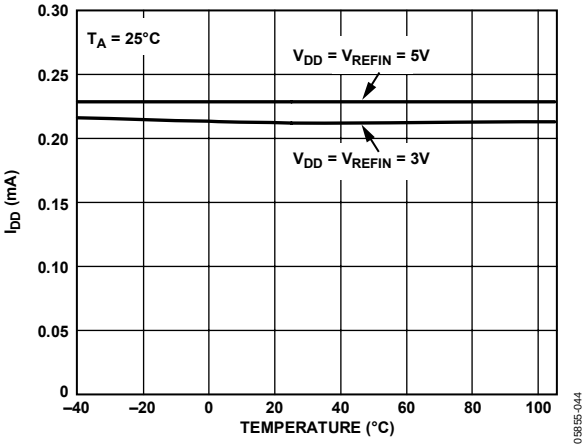



Figure 15. Supply Current vs. Temperature

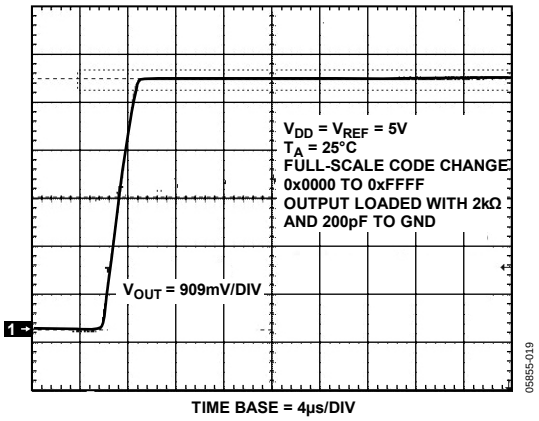



Figure 16. Full-Scale Settling Time, 5 V

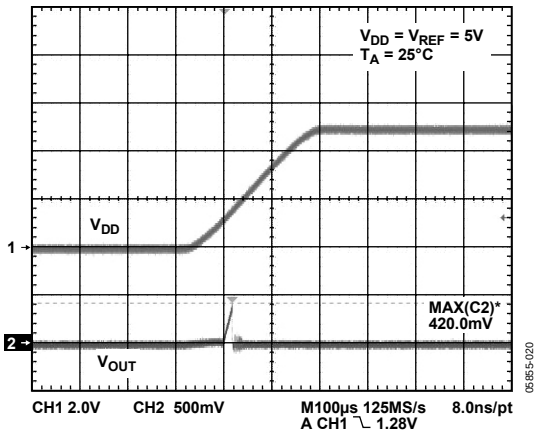



Figure 17. Power-On Reset to 0 V

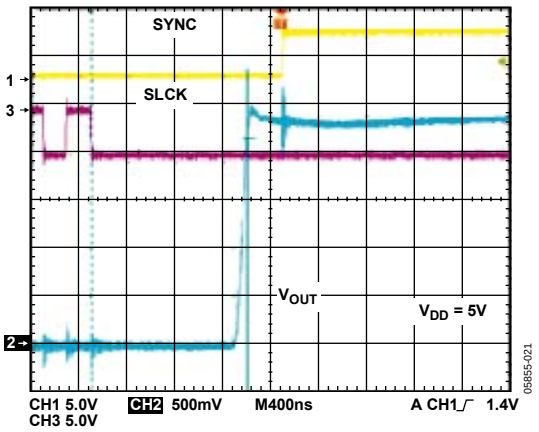



Figure 18. Exiting Power-Down to Midscale

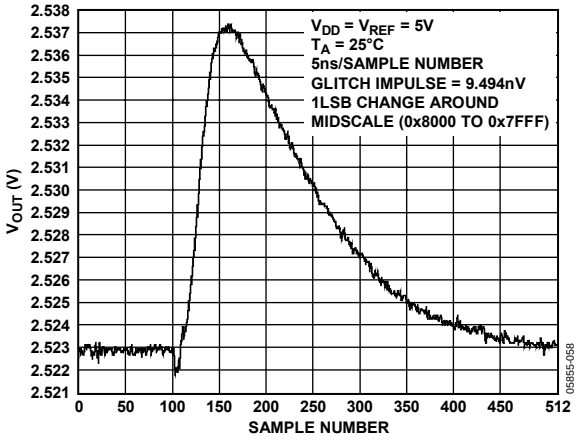



Figure 19. Digital-to-Analog Glitch Impulse (Negative)

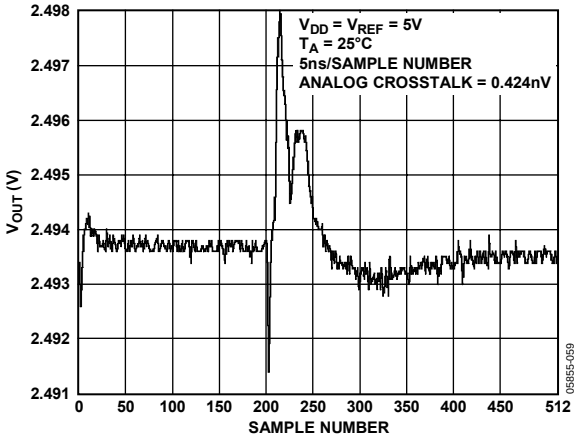



Figure 20. Analog Crosstalk

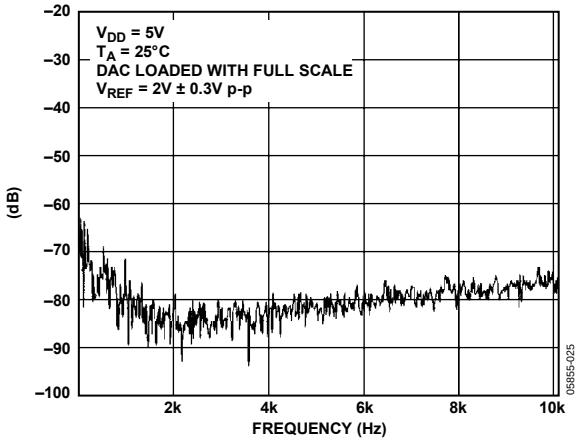



Figure 21. Total Harmonic Distortion

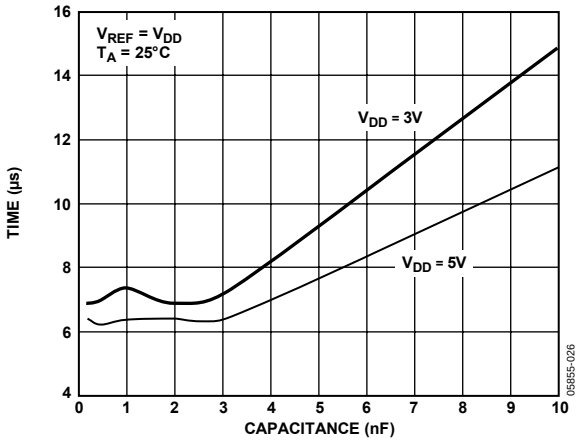



Figure 22. Settling Time vs. Capacitive Load

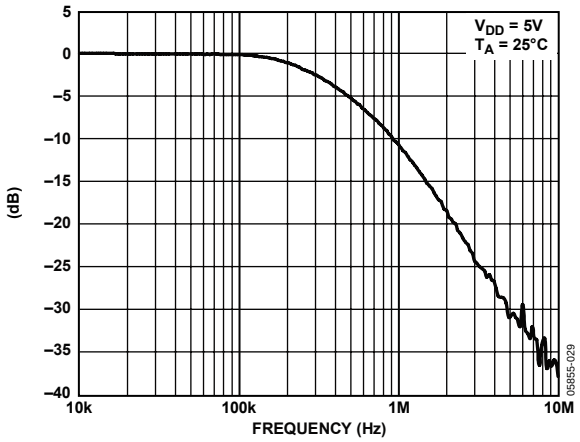



Figure 25. Multiplying Bandwidth

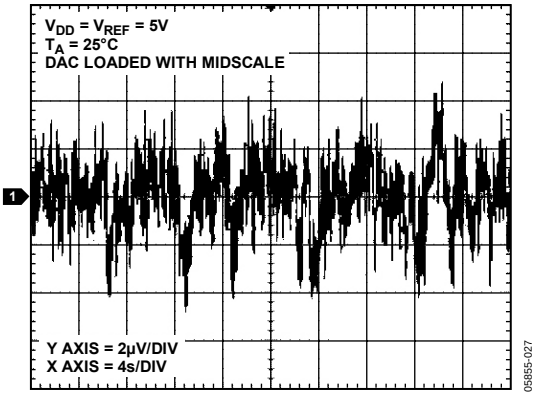



Figure 23. 0.1 Hz to 10 Hz Output Noise Plot

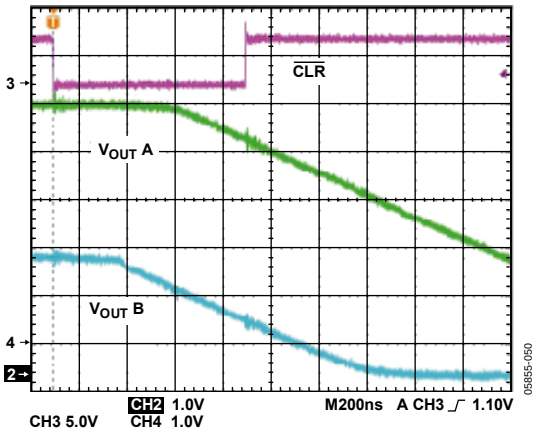



Figure 26. $\overline{CLR}$ Pulse Activation Time

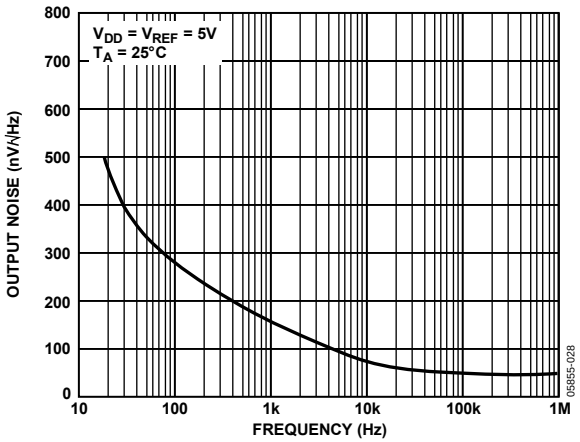



Figure 24. Noise Spectral Density

# TERMINOLOGY

**Relative Accuracy or Integral Nonlinearity (INL)**
For the DAC, relative accuracy or integral nonlinearity is a measurement of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot is shown in Figure 4.

**Differential Nonlinearity (DNL)**
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL vs. code plot is shown in Figure 5.

**Zero-Scale Error**
Zero-scale error is a measurement of the output error when zero code (0x0000) is loaded to the DAC register. Ideally, the output should be 0 V. The zero-scale error is always positive in the AD5663 because the output of the DAC cannot go below 0 V. It is due to a combination of the offset errors in the DAC and the output amplifier. Zero-scale error is expressed in mV. A plot of zero-scale error vs. temperature is shown in Figure 10.

**Full-Scale Error**
Full-scale error is a measurement of the output error when full-scale code (0xFFFF) is loaded to the DAC register. Ideally, the output should be $V_{DD}$ − 1 LSB. Full-scale error is expressed in percent of full-scale range. A plot of full-scale error vs. temperature is shown in Figure 9.

**Gain Error**
Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from ideal expressed as a percent of the full-scale range.

**Zero-Scale Error Drift**
Zero-scale error drift is a measurement of the change in zero-scale error with a change in temperature. It is expressed in µV/°C.

**Gain Temperature Coefficient**
Gain temperature coefficient is a measurement of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

**Offset Error**
Offset error is a measure of the difference between $V_{OUT}$ (actual) and $V_{OUT}$ (ideal) expressed in mV in the linear region of the transfer function. Offset error is measured on the AD5663 with Code 512 loaded in the DAC register. It can be negative or positive.

**DC Power Supply Rejection Ratio (PSRR)**
PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in $V_{OUT}$ to a change in $V_{DD}$ for full-scale output of the DAC. It is measured in dB. $V_{REF}$ is held at 2 V, and $V_{DD}$ is varied by ±10%.

**Output Voltage Settling Time**
Output voltage settling time is the amount of time it takes for the output of a DAC to settle to a specified level for a 1/4 to 3/4 full-scale input change and is measured from the 24th falling edge of SCLK.

**Digital-to-Analog Glitch Impulse**
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-s, and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000). See Figure 19.

**Digital Feedthrough**
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but it is measured when the DAC output is not updated. It is specified in nV-s and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

**Total Harmonic Distortion (THD)**
Total harmonic distortion is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measurement of the harmonics present on the DAC output. It is measured in dB.

**Noise Spectral Density**
Noise spectral density is a measurement of the internally generated random noise. Random noise is characterized as a spectral density (voltage per √Hz). It is measured by loading the DAC to midscale and measuring noise at the output. It is measured in nV/√Hz. **Figure 24** shows a plot of noise spectral density.

**DC Crosstalk**
DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC (or soft power-down and power-up) while monitoring another DAC kept at midscale. It is expressed in µV.

DC crosstalk due to load current change is a measure of the impact that a change in load current on one DAC has to another DAC kept at midscale. It is expressed in µV/mA.

**Digital Crosstalk**
Digital crosstalk is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nV-s.

**Analog Crosstalk**
Analog crosstalk is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s and vice versa) while keeping $\overline{\text{LDAC}}$ high. Then pulse $\overline{\text{LDAC}}$ low and monitor the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nV-s.

**DAC-to-DAC Crosstalk**
DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of another DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s and vice versa) with $\overline{\text{LDAC}}$ low and monitoring the output of another DAC. The energy of the glitch is expressed in nV-s.

**Multiplying Bandwidth**
The amplifiers within the DAC have a finite bandwidth. The multiplying bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

# THEORY OF OPERATION

## D/A SECTION

The AD5663 DAC is fabricated on a CMOS process. The architecture consists of a string DAC followed by an output buffer amplifier. Figure 27 shows a block diagram of the DAC architecture.

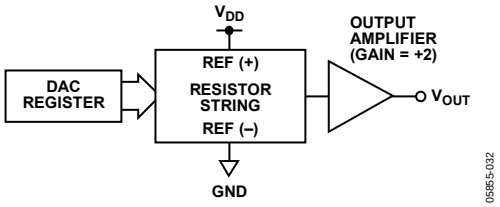



*Figure 27. DAC Architecture*

Because the input coding to the DAC is straight binary, the ideal output voltage is given by

$$V_{OUT} = V_{REF} \times \left( \frac{D}{65{,}536} \right)$$

where *D* is the decimal equivalent of the binary code that is loaded to the DAC register. It can range from 0 to 65,535.

## RESISTOR STRING

The resistor string section is shown in Figure 28. It is a string of resistors, each of Value R. The code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

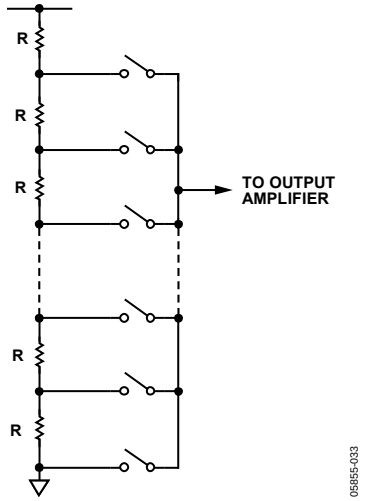



*Figure 28. Resistor String*

## OUTPUT AMPLIFIER

The output buffer amplifier can generate rail-to-rail voltages on its output, which gives an output range of 0 V to $V_{DD}$. It can drive a load of 2 kΩ in parallel with 1000 pF to GND.

The source and sink capabilities of the output amplifier can be seen in Figure 14. The slew rate is 1.8 V/μs with a 1/4 to 3/4 full-scale settling time of 10 μs.

## SERIAL INTERFACE

The AD5663 has a 3-wire serial interface ($\overline{\text{SYNC}}$, SCLK, and DIN) that is compatible with SPI, QSPI, and MICROWIRE interface standards, as well as with most DSPs. See Figure 2 for a timing diagram of a typical write sequence.

The write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. Data from the DIN line is clocked into the 24-bit shift register on the falling edge of SCLK. The serial clock frequency can be as high as 50 MHz, making the AD5663 compatible with high speed DSPs. On the 24th falling clock edge, the last data bit is clocked in and the programmed function is executed; that is, there is a change in DAC register contents and/or a change in the mode of operation. At this stage, the $\overline{\text{SYNC}}$ line can be kept low or be brought high. In either case, it must be brought high for a minimum of 15 ns before the next write sequence so that a falling edge of $\overline{\text{SYNC}}$ can initiate the next write sequence. Because the $\overline{\text{SYNC}}$ buffer draws more current when $V_{IN}$ = 2.0 V than it does when $V_{IN}$ = 0.10 V, $\overline{\text{SYNC}}$ should be idled low between write sequences for even lower power operation. As mentioned previously, however, it must be brought high again just before the next write sequence.

## INPUT SHIFT REGISTER

The input shift register is 24 bits wide (see Figure 29). The first two bits are don't cares. The next three are the Command Bit C2 to Command Bit C0 (see Table 7), followed by the 3-bit DAC Address A2 to DAC Address A0 (see Table 8), and, finally, the 16-bit data-word. These are transferred to the DAC register on the 24th falling edge of SCLK.

**Table 7. Command Definition**

| C2 | C1 | C0 | Command |
|---|---|---|---|
| 0 | 0 | 0 | Write to input register *n* |
| 0 | 0 | 1 | Update DAC register *n* |
| 0 | 1 | 0 | Write to input register *n*, update all (software $\overline{\text{LDAC}}$) |
| 0 | 1 | 1 | Write to and update DAC channel *n* |
| 1 | 0 | 0 | Power down DAC (power up) |
| 1 | 0 | 1 | Reset |
| 1 | 1 | 0 | $\overline{\text{LDAC}}$ register setup |
| 1 | 1 | 1 | Reserved |

**Table 8. Address Command**

| A2 | A1 | A0 | ADDRESS (*n*) |
|---|---|---|---|
| 0 | 0 | 0 | DAC A |
| 0 | 0 | 1 | DAC B |
| 0 | 1 | 0 | Reserved |
| 0 | 1 | 1 | Reserved |
| 1 | 1 | 1 | All DACs |

## $\overline{\text{SYNC}}$ INTERRUPT

In a normal write sequence, the $\overline{\text{SYNC}}$ line is kept low for at least 24 falling edges of SCLK, and the DAC is updated on the 24th falling edge. However, if $\overline{\text{SYNC}}$ is brought high before the 24th falling edge, this acts as an interrupt to the write sequence. The shift register is reset and the write sequence is seen as invalid. Neither an update of the DAC register contents nor a change in the operating mode occurs (see Figure 30).

## POWER-ON RESET

The AD5663 family contains a power-on reset circuit that controls the output voltage during power-up. The AD5663 DAC outputs power up to 0 V, the AD5663-1 powers up to midscale, and the output remains there until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up. Any events on $\overline{\text{LDAC}}$ or $\overline{\text{CLR}}$ during power-on reset are ignored.

## SOFTWARE RESET

The AD5663 contains a software reset function. Command 101 is reserved for the software reset function (see Table 7). The software reset command contains two reset modes that are software-programmable by setting Bit DB0 in the control register.

Table 9 shows how the state of the bit corresponds to the mode of operation of the device. Table 10 shows the contents of the input shift register during the software reset mode of operation.

**Table 9. Software Reset Modes for the AD5663**

| DB0 | Registers Reset to 0 |
|---|---|
| 0 | DAC register<br>Input register |
| 1 (Power-On Reset) | DAC register<br>Input register<br>$\overline{\text{LDAC}}$ register<br>Power-down register |

**Table 10. 24-Bit Input Shift Register Contents for Software Reset Command**

| MSB | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| DB23 to DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 to DB1 | DB0 |
| x | 1 | 0 | 1 | x | x | x | x | 1/0 |
| Don't care | Command bits (C2 to C0) | | | Address bits (A2 to A0) | | | Don't care | Determines software reset mode |

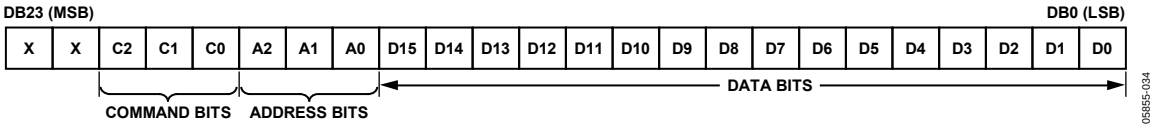



*Figure 29. Input Register Contents*

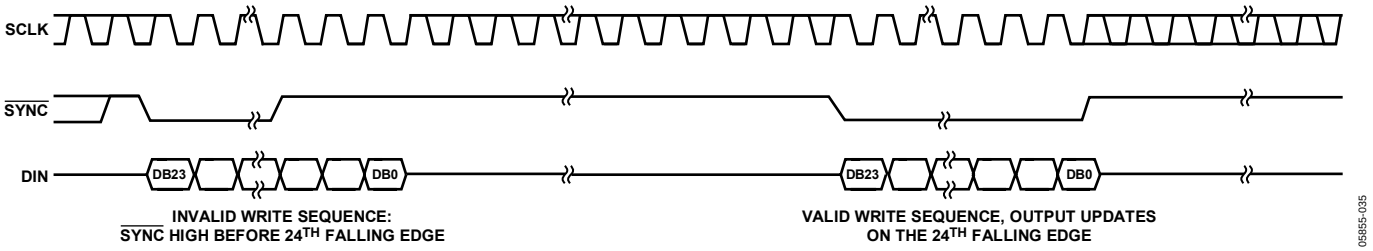



*Figure 30. $\overline{\text{SYNC}}$ Interrupt Facility*

## POWER-DOWN MODES

The AD5663 contains four separate modes of operation. Command 100 is reserved for the power-down function (see Table 7). These modes are software-programmable by setting Bit DB5 and Bit DB4 in the control register. Table 11 shows how the state of the bits corresponds to the mode of operation of the device. Any or all DACs (DAC B and DAC A) can be powered down to the selected mode by setting the corresponding two bits (Bit DB1 and Bit DB0) to 1. By executing the same Command 100, any combination of DACs can be powered up by setting Bit DB5 and Bit DB4 to normal operation mode. Again, to select which combination of DAC channels to power up, set the corresponding two bits (Bit DB1 and Bit DB0) to 1. See Table 12 for contents of the input shift register during power-down/power-up operation.

The DAC output powers up to the value in the input register while $\overline{\text{LDAC}}$ is low. If $\overline{\text{LDAC}}$ is high, the DAC output powers up to the value held in the DAC register before power-down.

When both bits are set to 0, the part works normally with its normal power consumption of 500 μA at 5 V. However, for the three power-down modes, the supply current falls to 480 nA at 5 V (100 nA at 3 V). Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the part is known while the part is in power-down mode. The outputs can either be connected internally to GND through a 1 kΩ or 100 kΩ register or left open-circuited (three-state) (see Figure 31).

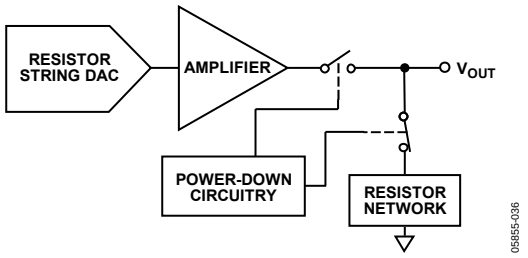



*Figure 31. Output Stage During Power-Down*

The bias generator, the output amplifier, the resistor string, and other associated linear circuitry are shut down when power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down.

The time required to exit power-down is typically 4 μs for $V_{DD}$ = 5 V and for $V_{DD}$ = 3 V (see Figure 18).

**Table 11. Power-Down Modes of Operation for the AD5663**

| DB5 | DB4 | Operating Mode |
|---|---|---|
| 0 | 0 | Normal operation |
| | | **Power-Down Modes** |
| 0 | 1 | 1 kΩ to GND |
| 1 | 0 | 100 kΩ to GND |
| 1 | 1 | Three-state |

## $\overline{\text{LDAC}}$ FUNCTION

The AD5663 DAC has double-buffered interfaces consisting of two banks of registers: input registers and DAC registers. The input registers are connected directly to the input shift register and the digital code is transferred to the relevant input register on completion of a valid write sequence. The DAC registers contain the digital code used by the resistor strings.

Access to the DAC registers is controlled by the $\overline{\text{LDAC}}$ pin. When the $\overline{\text{LDAC}}$ pin is high, the DAC registers are latched and the input registers can change state without affecting the contents of the DAC registers. When $\overline{\text{LDAC}}$ is brought low, however, the DAC registers become transparent and the contents of the input registers are transferred to them. The double-buffered interface is useful if the user requires simultaneous updating of all DAC outputs. The user can write to one of the input registers individually and then, by bringing $\overline{\text{LDAC}}$ low when writing to the other DAC input register, all outputs update simultaneously.

These parts each contain an extra feature whereby a DAC register is not updated unless its input register has been updated since the last time $\overline{\text{LDAC}}$ was brought low. Normally, when $\overline{\text{LDAC}}$ is brought low, the DAC registers are filled with the contents of the input registers. In the case of the AD5663, the DAC register updates only if the input register has changed since the last time the DAC register was updated, thereby removing unnecessary digital crosstalk.

The outputs of all DACs can be updated simultaneously using the hardware $\overline{\text{LDAC}}$ pin.

**Table 12. 24-Bit Input Shift Register Contents of Power-Up/Power-Down Function**

| MSB | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **DB23 to DB22** | **DB21** | **DB20** | **DB19** | **DB18** | **DB17** | **DB16** | **DB15 to DB6** | **DB5** | **DB4** | **DB3** | **DB2** | **DB1** | **DB0** |
| x | 1 | 0 | 0 | x | x | x | x | PD1 | PD0 | x | x | DAC B | DAC A |
| Don't care | Command bits (C2 to C0) | | | Address bits (A2 to A0); don't care | | | Don't care | Power-down mode | | Don't care | | Power down/Power up channel selection; set bit to 1 to select channel | |

**Synchronous $\overline{\text{LDAC}}$:** The DAC registers are updated after new data is read in on the falling edge of the 24th SCLK pulse. $\overline{\text{LDAC}}$ can be permanently low or pulsed, as shown in Figure 2.

**Asynchronous $\overline{\text{LDAC}}$:** The outputs are not updated at the same time that the input registers are written to. When $\overline{\text{LDAC}}$ goes low, the DAC registers are updated with the contents of the input register.

The $\overline{\text{LDAC}}$ register gives the user full flexibility and control over the hardware $\overline{\text{LDAC}}$ pin. This register allows the user to select which combination of channels to simultaneously update when the hardware $\overline{\text{LDAC}}$ pin is executed. Setting the $\overline{\text{LDAC}}$ bit register to 0 for a DAC channel means that the update of this channel is controlled by the $\overline{\text{LDAC}}$ pin. If this bit is set to 1, this channel synchronously updates; that is, the DAC register is updated after new data is read in, regardless of the state of the $\overline{\text{LDAC}}$ pin. It effectively sees the $\overline{\text{LDAC}}$ pin as being pulled low. See Table 13 for the $\overline{\text{LDAC}}$ register mode of operation.

This flexibility is useful in applications where the user wants to simultaneously update select channels while the rest of the channels are synchronously updating

Writing to the DAC using Command 110 loads the 2-bit $\overline{\text{LDAC}}$ register [DB1:DB0]. The default for each channel is 0; that is, the $\overline{\text{LDAC}}$ pin works normally. Setting the bits to 1 means the DAC register is updated regardless of the state of the $\overline{\text{LDAC}}$ pin. See Table 14 for contents of the input shift register during the $\overline{\text{LDAC}}$ register setup command.

**Table 13. $\overline{\text{LDAC}}$ Register Mode of Operation**

| **$\overline{\text{LDAC}}$ Bits (DB1 to DB0)** | **$\overline{\text{LDAC}}$ Pin** | **$\overline{\text{LDAC}}$ Operation** |
|---|---|---|
| 0 | 1/0 | Determined by $\overline{\text{LDAC}}$ pin |
| 1 | x = don't care | The DAC registers are updated after new data is read in on the falling edge of the 24th SCLK pulse |

**Table 14. 24-Bit Input Shift Register Contents for $\overline{\text{LDAC}}$ Register Setup Command**

| **MSB** | | | | | | | | | **LSB** |
|---|---|---|---|---|---|---|---|---|---|
| **DB23 to DB22** | **DB21** | **DB20** | **DB19** | **DB18** | **DB17** | **DB16** | **DB15 to DB2** | **DB1** | **DB0** |
| x | 1 | 1 | 0 | x | x | x | x | DAC B | DAC A |
| Don't care | Command bits (C2 to C0) | | | Address bits (A3 to A0); Don't care | | | Don't care | Set DAC to 0 or 1 for required mode of operation | |

## MICROPROCESSOR INTERFACING

### *AD5663 to Blackfin® ADSP BF53x Interface*

Figure 32 shows a serial interface between the AD5663 and the Blackfin ADSP-BF53x microprocessor. The ADSP-BF53x processor family incorporates two dual-channel synchronous serial ports, SPORT1 and SPORT0, for serial and multiprocessor communications. Using SPORT0 to connect to the AD5663, the setup for the interface is as follows:

- DT0PRI drives the DIN pin of the AD5663.
- TSCLK0 drives the SCLK of the part.
- The $\overline{\text{SYNC}}$ pin is driven from TFS0.

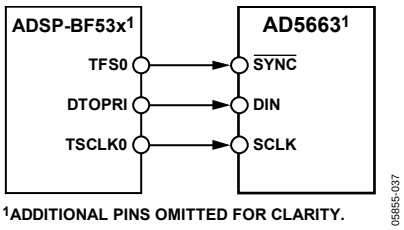



*Figure 32. AD5663 to Blackfin ADSP-BF53x Interface*

### *AD5663 to 68HC11/68L11 Interface*

Figure 33 shows a serial interface between the AD5663 and the 68HC11/68L11 microcontroller. SCK of the 68HC11/68L11 drives the SCLK of the AD5663, and the MOSI output drives the serial data line of the DAC.

The $\overline{\text{SYNC}}$ signal is derived from a port line (PC7). The setup conditions for correct operation of this interface are as follows:

- The 68HC11/68L11 is configured with its CPOL bit as 0.
- The 68HC11/68L11 is configured with its CPHA bit as 1.

When data is being transmitted to the DAC, the $\overline{\text{SYNC}}$ line is taken low (PC7). When the 68HC11/68L11 is configured as previously described, data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11/68L11 is transmitted in 10-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. To load data to the AD5663, PC7 is left low after the first eight bits are transferred, and a second serial write operation is performed to the DAC. PC7 is taken high at the end of this procedure.

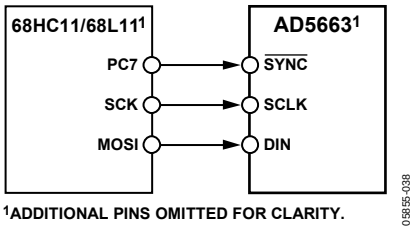



*Figure 33. AD5663 to 68HC11/68L11 Interface*

### *AD5663 to 80C51/80L51 Interface*

Figure 34 shows a serial interface between the AD5663 and the 80C51/80L51 microcontroller. The setup for the interface is as follows:

- TxD of the 80C51/80L51 drives SCLK of the AD5663.
- RxD drives the serial data line of the part.

The $\overline{\text{SYNC}}$ signal is again derived from a bit-programmable pin on the port. In this case, Port Line P3.3 is used. When data is to be transmitted to the AD5663, P3.3 is taken low. The 80C51/80L51 transmits data in 10-bit bytes only; thus only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left low after the first eight bits are transmitted, and a second write cycle is initiated to transmit the second byte of data. P3.3 is taken high following the completion of this cycle. The 80C51/80L51 outputs the serial data in a format that has the LSB first. The AD5663 must receive data with the MSB first. The 80C51/80L51 transmit routine should take this into account.

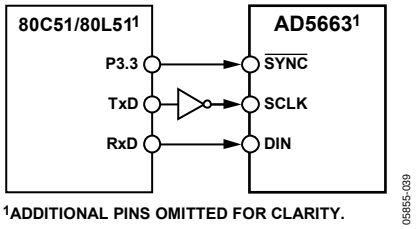



*Figure 34. AD5663 to 80C51/80L51 Interface*

### *AD5663 to MICROWIRE Interface*

Figure 35 shows an interface between the AD5663 and any MICROWIRE-compatible device. Serial data is shifted out on the falling edge of the serial clock and is clocked into the AD5663 on the rising edge of the SK.

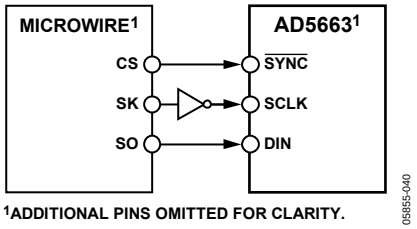



*Figure 35. AD5663 to MICROWIRE Interface*

# APPLICATIONS

## CHOOSING A REFERENCE FOR THE AD5663

To achieve the optimum performance from the AD5663, thought should be given to the choice of a precision voltage reference. The AD5663 has only one reference input, $V_{REF}$. The voltage on the reference input is used to supply the positive input to the DAC. Therefore, any error in the reference is reflected in the DAC.

When choosing a voltage reference for high accuracy applications, the sources of error are initial accuracy, ppm drift, long-term drift, and output voltage noise. Initial accuracy on the output voltage of the DAC leads to a full-scale error in the DAC. To minimize these errors, a reference with high initial accuracy is preferred. Also, choosing a reference with an output trim adjustment, such as the ADR423, allows a system designer to trim system errors out by setting a reference voltage to a voltage other than the nominal. The trim adjustment can also be used at temperature to trim out any error.

Long-term drift is a measurement of how much the reference drifts over time. A reference with a tight long-term drift specification ensures that the overall solution remains relatively stable during its entire lifetime.

The temperature coefficient of a reference's output voltage affects INL, DNL, and TUE. A reference with a tight temperature coefficient specification should be chosen to reduce temperature dependence of the DAC output voltage in ambient conditions.

In high accuracy applications, which have a relatively low noise budget, reference output voltage noise needs to be considered. It is important to choose a reference with as low an output noise voltage as practical for the system noise resolution required. Precision voltage references, such as the ADR425, produce low output noise in the 0.1 Hz to 10 Hz range. Examples of recommended precision references for use as supplies to the AD5663 are shown in the Table 15.

## USING A REFERENCE AS A POWER SUPPLY FOR THE AD5663

Because the supply current required by the AD5663 is extremely low, an alternative option is to use a voltage reference to supply the required voltage to the part (see Figure 36). This is especially useful if the power supply is quite noisy, or if the system supply voltages are at some value other than 5 V or 3 V (for example, 15 V). The voltage reference outputs a steady supply voltage for the AD5663; see Table 15 for a suitable reference. If the low dropout REF195 is used, it must supply 250 µA of current to the AD5663, with no load on the output of the DAC. When the DAC output is loaded, the REF195 also needs to supply the current to the load. The total current required (with a 5 kΩ load on the DAC output) is

$$250\ \mu A + (5\ V/5\ k\Omega) = 1.25\ mA$$

The load regulation of the REF195 is typically 2 ppm/mA, which results in a 2.5 ppm (12.5 µV) error for the 1.25 mA current drawn from it. This corresponds to a 0.164 LSB error.

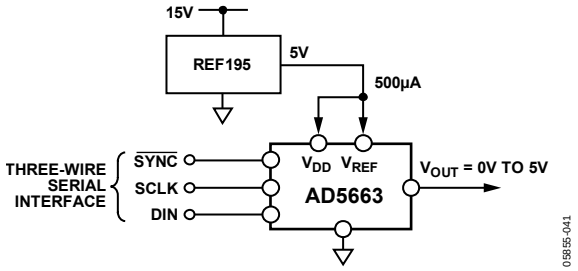



*Figure 36. REF195 as Power Supply to the AD5663*

**Table 15. Partial List of Precision References for Use with the AD5663**

| Part No. | Initial Accuracy (mV Max) | Temperature Drift (ppm°C Max) | 0.1 Hz to 10 Hz Noise (µV p-p Typ) | $V_{OUT}$ (V) |
|---|---|---|---|---|
| ADR425 | ±2 | 3 | 3.4 | 5 |
| ADR395 | ±6 | 25 | 5 | 5 |
| REF195 | ±2 | 5 | 50 | 5 |
| AD780 | ±2 | 3 | 4 | 2.5/3 |
| ADR423 | ±2 | 3 | 3.4 | 3 |

## BIPOLAR OPERATION USING THE AD5663

The AD5663 has been designed for single-supply operation, but a bipolar output range is also possible using the circuit in Figure 37. The circuit gives an output voltage range of ±5 V. Rail-to-rail operation at the amplifier output is achievable using an AD820 or an OP295 as the output amplifier.

The output voltage for any input code can be calculated as

$$V_O = \left[ V_{DD} \times \left( \frac{D}{65{,}536} \right) \times \left( \frac{R1 + R2}{R1} \right) - V_{DD} \times \left( \frac{R2}{R1} \right) \right]$$

where $D$ represents the input code in decimal (0 to 65,535).

With $V_{DD}$ = 5 V, $R1 = R2$ = 10 kΩ

$$V_O = \left( \frac{10 \times D}{65{,}536} \right) - 5 \text{ V}$$

This is an output voltage range of ±5 V, with 0x0000 corresponding to a −5 V output, and 0xFFFF corresponding to a +5 V output.

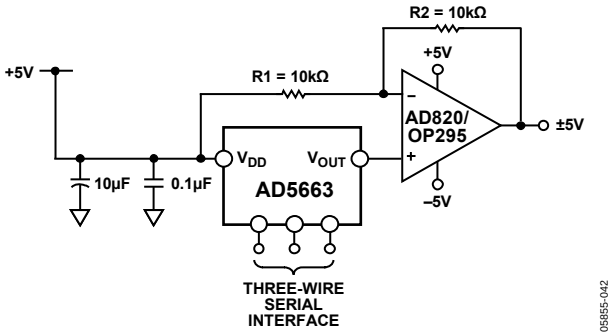



*Figure 37. Bipolar Operation with the AD5663*

## USING THE AD5663 WITH A GALVANICALLY ISOLATED INTERFACE

In process control applications in industrial environments, it is often necessary to use a galvanically isolated interface to protect and isolate the controlling circuitry from any hazardous common-mode voltages that can occur in the area where the DAC is functioning. *i*Coupler® provides isolation in excess of 2.5 kV. The AD5663 use a 3-wire serial logic interface, so the ADuM1300 three-channel digital isolator provides the required isolation (see Figure 38). The power supply to the part also needs to be isolated, which is done by using a transformer. On the DAC side of the transformer, a 5 V regulator provides the 5 V supply required for the AD5663.

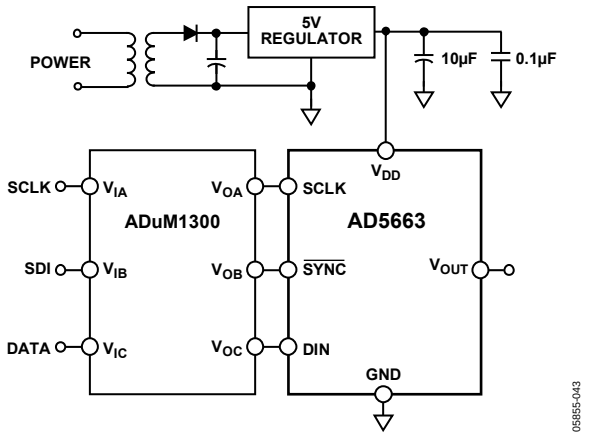



*Figure 38. AD5663 with a Galvanically Isolated Interface*

## POWER SUPPLY BYPASSING AND GROUNDING

When accuracy is important in a circuit, it is helpful to carefully consider the power supply and ground return layout on the board. The printed circuit board containing the AD5663 should have separate analog and digital sections, each having its own area of the board. If the AD5663 is in a system where other devices require an AGND-to-DGND connection, the connection should be made at one point only. This ground point should be as close as possible to the AD5663.

The power supply to the AD5663 should be bypassed with 10 µF and 0.1 µF capacitors. The capacitors should be located as close as possible to the device, with the 0.1 µF capacitor ideally right up against the device. The 10 µF capacitors are of the tantalum bead type. It is important that the 0.1 µF capacitor have low effective series resistance (ESR) and effective series inductance (ESI) as in, for example, common ceramic types of capacitors. This 0.1 µF capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching.

The power supply line itself should have as large a trace as possible to provide a low impedance path and to reduce glitch effects on the supply line. Clocks and other fast switching digital signals should be shielded from other parts of the board by digital ground. Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects through the board. The best board layout technique is the microstrip technique, where the component side of the board is dedicated to the ground plane only, and the signal traces are placed on the solder side. However, this is not always possible with a 2-layer board.

# OUTLINE DIMENSIONS

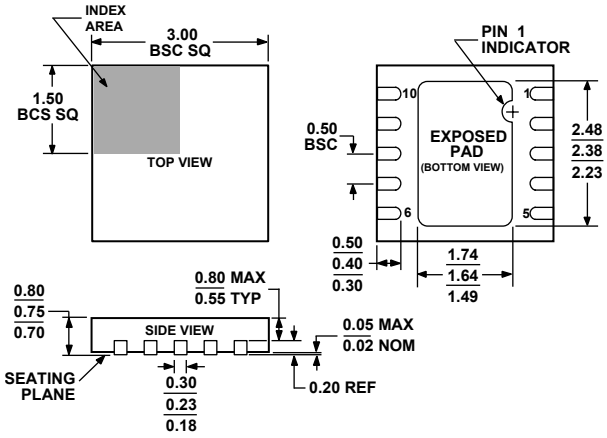
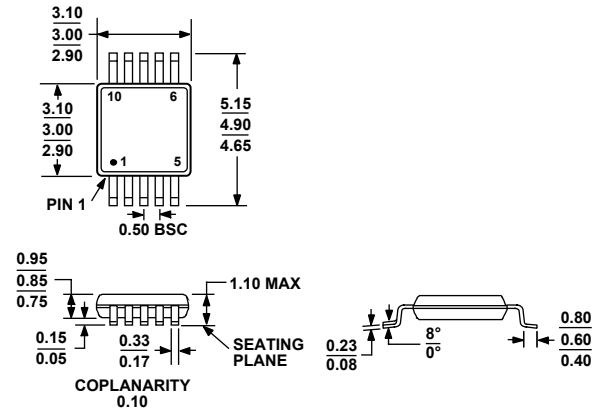



*Figure 39. 10-Lead Lead Frame Chip Scale Package [LFCSP_WD]*
*3 mm x 3 mm Body, Very Very Thin, Dual Lead*
*(CP-10-9)*
*Dimensions shown in millimeters*




**COMPLIANT TO JEDEC STANDARDS MO-187-BA**

*Figure 40. 10-Lead Mini Small Outline Package [MSOP]*
*(RM-10)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model | Temperature Range | Power-On Reset Code | Accuracy | Package Description | Package Option | Branding |
|---|---|---|---|---|---|---|
| AD5663ARMZ[1] | −40°C to +105°C | Zero | ±16 LSB INL | 10-lead MSOP | RM-10 | D80 |
| AD5663ARMZ-REEL7[1] | −40°C to +105°C | Zero | ±16 LSB INL | 10-lead MSOP | RM-10 | D80 |
| AD5663BRMZ[1] | −40°C to +105°C | Zero | ±12 LSB INL | 10-lead MSOP | RM-10 | D8C |
| AD5663BRMZ-REEL7[1] | −40°C to +105°C | Zero | ±12 LSB INL | 10-lead MSOP | RM-10 | D8C |
| AD5663BRMZ-1[1] | −40°C to +105°C | Midscale | ±12 LSB INL | 10-lead MSOP | RM-10 | D7J |
| AD5663BRMZ-1REEL7[1] | −40°C to +105°C | Midscale | ±12 LSB INL | 10-lead MSOP | RM-10 | D7J |
| AD5663BCPZ-250RL7[1] | −40°C to +105°C | Zero | ±12 LSB INL | 10-lead LFCSP_WD | CP-10-9 | D8C |
| AD5663BCPZ-REEL7[1] | −40°C to +105°C | Zero | ±12 LSB INL | 10-lead LFCSP_WD | CP-10-9 | D8C |

[1] Z = Pb-free part.

## NOTES

## NOTES

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D05855-0-4/06(0)