High Efficiency Dual Power Supply Controller

ADP3026

FEATURES

Wide input voltage range: 5.5 V to 25 V
High conversion efficiency > 96%
Integrated current sense—no external resistor required
Low shutdown current: 19 µA (typical)
Voltage mode PWM with input feed-forward for fast line transient response
Dual synchronous buck controllers
Built-in gate drive boost circuit for driving external N-channel MOSFETs
2 fixed output voltages: 3.3 V and 5 V
PWM frequency: 200 kHz
Extensive circuit protection functions

APPLICATIONS

Portable instruments
General-purpose dc-to-dc converters

GENERAL DESCRIPTION

The ADP3026 is a highly efficient dual synchronous buck switching regulator controller optimized for converting a battery or adapter input into multiple supply voltages. The ADP3026 provides accurate and reliable short-circuit protection using an internal current sense circuit, which reduces cost and increases overall efficiency. Other protection features include programmable soft start, UVLO, and integrated output undervoltage/overvoltage protection.

The ADP3026 is specified over the 0°C to 70°C commercial temperature range and is available in a 28-lead TSSOP package.

FUNCTIONAL BLOCK DIAGRAM

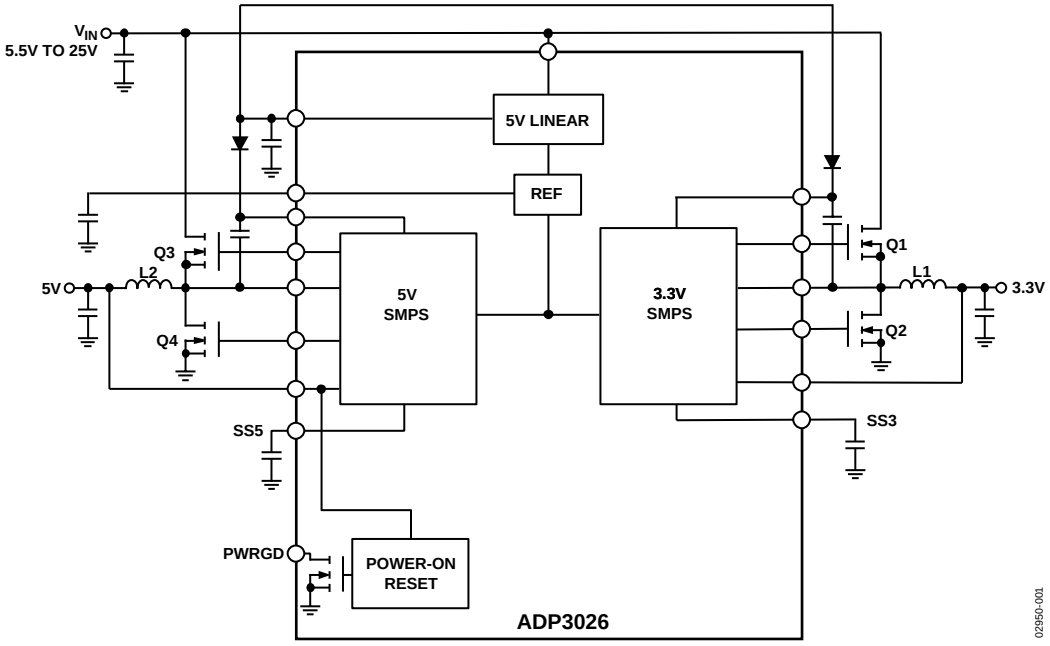

Figure 1.

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REVISION HISTORY

10/04—Revision 0: Initial Version

SPECIFICATIONS

@ T_A = 0°C to 70°C, V_{IN} = 12 V, SS5 = SS3 = INTVCC, INTVCC Load = 0 mA, REF Load = 0 mA, $\overline{SD}$ = 5 V, unless otherwise noted. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INTERNAL 5 V REGULATOR	INTVCC					
Input Voltage Range			5.5		25	V
5 V Voltage		T_A = 25°C	4.95	5.02	5.15	V
Line Regulation		5.5 V ≤ V_{IN} ≤ 25 V		1.0		mV/V
Total Variation		Line, temperature	4.8		5.2	V
Undervoltage Lockout		INTVCC falling	4.05	4.25	4.5	V
Threshold Voltage						
Undervoltage Lockout				270		mV
Hysteresis						
REFERENCE						
Output Voltage[1]	REF	5.5 V ≤ V_{IN} ≤ 25 V	784	800	816	V
SUPPLY CURRENT	I_Q					
Shutdown Current		$\overline{SD}$ = 0 V		19	50	µA
Standby Current		SS3 = SS5 = 0 V		120	200	µA
		$\overline{SD}$ = 5 V				
Quiescent Current		No loads		1.3	1.9	mA
		SS3 = SS5 = 5 V				
		FB5 = 5.05 V, FB3 = 3.33 V				
OSCILLATOR						
Frequency	f_{OSC}	5.5 V ≤ V_{IN} ≤ 25 V	165	200	235	kHz
POWER GOOD	PWRGD					
Output Voltage in Regulation		10 kΩ pull-up to 5 V	4.8			V
Output Voltage out of Regulation		10 kΩ pull-up to 5 V			0.4	V
		FB5 < 90% of nominal output value				
PWRGD Trip Threshold		FB5 rising	−6	−3.7	−1.5	%
PWRGD Hysteresis		FB5 falling		4		%
CPOR Pull-Up Current		CPOR = 1.2 V	−3	−1	−0.3	µA
ERROR AMPLIFIER						
DC Gain[2]				47		dB
Gain-Bandwidth Product	GBW			10		MHz
MAIN SMPS CONTROLLERS						
Fixed 5 V Output Voltage	FB5	5.5 V ≤ V_{IN} ≤25 V	4.90	5.0	5.10	V
Fixed 3.3 V Output Voltage	FB3	5.5 V ≤ V_{IN} ≤25 V	3.234	3.3	3.366	V
Current Limit Threshold						
CLSET5 = CLSET3 = Floating		5.5 V ≤ V_{IN} ≤ 25 V, T_A = 25°C	54	72	90	mV
CLSET5 = CLSET3 = 0 V		5.5 V ≤ V_{IN} ≤ 25 V, T_A = 25°C	240	300	360	mV
Soft-Start Current		SS3 = SS5 = 3 V	0.7	2.1	3.8	µA
Soft-Start Turn-On Threshold	SS5, SS3		0.4	0.6	0.8	V
Transition Time (DRVL)						
Rise	t_R(DRVL)	C_{LOAD} = 3000 pF, 10% to 90%		40	70	ns
Fall	t_F(DRVL)	C_{LOAD} = 3000 pF, 90% to 10%		45	70	ns
Transition Time (DRVH)						
Rise	t_R(DRVH)	C_{LOAD} = 3000 pF, 10% to 90%		50	100	ns
Fall	t_F(DRVH)	C_{LOAD} = 3000 pF, 90% to 10%		50	100	ns
Logic Input Low Voltage		$\overline{SD}$			0.6	V
Logic Input High Voltage		$\overline{SD}$	2.9			V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
FAULT PROTECTION						
Output Overvoltage Trip Threshold		With respect to nominal output	115	120	125	%
Output Undervoltage Lockout Threshold		With respect to nominal output	70	80	90	%

[1] The reference's line regulation error is insignificant. The reference cannot be used for external load.
[2] Guaranteed by design, not tested in production.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V_{IN} to AGND	−0.3 V to +27 V
AGND to PGND	±0.3 V
INTVCC	AGND − 0.3 V to +6 V
BST5, BST3 to PGND	−0.3 V to +32 V
BST5 to SW5	−0.3 V to +6 V
BST3 to SW3	−0.3 V to +6 V
CS5, CS3	AGND − 0.3 V to VIN
SW3, SW5 to PGND	−2 V to VIN + 0.3 V
$\overline{SD}$	AGND − 0.3 V to +27 V
DRVL5/3 to PGND	−0.3 V to INTVCC + 0.3 V
DRVH5/3 to SW5/3	−0.3 V to INTVCC + 0.3 V
All Other Inputs and Outputs	AGND − 0.3 V to INTVCC + 0.3 V
θ_{JA}	98°C/W
Operating Ambient Temperature Range	0°C to 70°C
Junction Temperature Range	0°C to 150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering 10 s)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified, all other voltages are referenced to GND.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

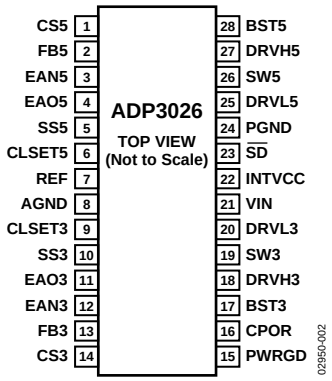

Figure 2. 28-Lead TSSOP Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	CS5	Current Sense Input for the Top N-Channel MOSFET of the 5 V Buck Converter. Connect to the drain of the top N-channel MOSFET.
2	FB5	Feedback Input for the 5 V Buck Converter. Connect to the output sense point in fixed output mode.
3	EAN5	Inverting Input of the Error Amplifier of the 5 V Buck Converter. Use for external loop compensation.
4	EAO5	Error Amplifier Output for the 5 V Buck Converter.
5	SS5	Soft Start for the 5 V Buck Converter. Also used as an on/off pin.
6	CLSET5	Current Limit Setting. A resistor can be connected from AGND to CLSET5. A minimum current limit is obtained by leaving it unconnected. A maximum current limit is obtained by connecting it to AGND.
7	REF	800 mV Band Gap Reference. Bypass it with a capacitor (22 nF typical) to AGND. REF cannot be used directly with an external load.
8	AGND	Analog Signal Ground.
9	CLSET3	Current Limit Setting. A resistor can be connected from AGND to CLSET3. A minimum current limit is obtained by leaving it unconnected. A max current limit is obtained by connecting it to AGND.
10	SS3	Soft Start for the 3.3 V Buck Converter. Also used as an on/off pin.
11	EAO3	Error Amplifier Output for the 3.3 V Buck Converter.
12	EAN3	Error Amplifier Inverting Input of the 3.3 V Buck Converter. Use for external loop compensation.
13	FB3	Feedback Input for the 3.3 V Buck Converter. Connect to output sense point.
14	CS3	Current Sense Input for the Top N-Channel MOSFET of the 3.3 V Buck Converter. It should be connected to the drain of the N-channel MOSFET.
15	PWRGD	Power Good Output. PWRGD goes low with no delay whenever the 5 V output drops 7% below its nominal value. When the 5 V output is within −3% of its nominal value, PWRGD will be released after a time delay determined by the timing capacitor on the CPOR pin.
16	CPOR	Connect a capacitor between CPOR and AGND to set the delay time for the PWRGD pin. A 1 µA pull-up current is used to charge the capacitor. A manual reset ($\overline{MR}$) function can also be implemented by grounding this pin.
17	BST3	Boost Capacitor Connection for High-Side Gate Driver of the 3.3 V Buck Converter.
18	DRVH3	High-Side Gate Driver for the 3.3 V Buck Converter.
19	SW3	Switching Node (Inductor) Connection of the 3.3 V Buck Converter.
20	DRVL3	Low-Side Gate Driver of the 3.3 V Buck Converter.
21	VIN	Main Supply Input (5.5 V to 25 V).
22	INTVCC	Linear Regulator Bypass for the internal 5 V LDO. Bypass this pin with a 4.7 µF capacitor to AGND.
23	$\overline{SD}$	Shutdown Control Input, Active Low. If $\overline{SD}$ = 0 V, the chip is in shutdown with very low quiescent current. For automatic startup, connect $\overline{SD}$ to VIN directly.
24	PGND	Power Ground.
25	DRVL5	Low-Side Driver for the 5 V Buck Converter.
26	SW5	Switching Node (Inductor) Connection for the 5 V Buck Converter.
27	DRVH5	High-Side Gate Driver for the 5 V Buck Converter.
28	BST5	Boost Capacitor Connection for the High-Side Gate Driver of the 5 V Buck Converter.

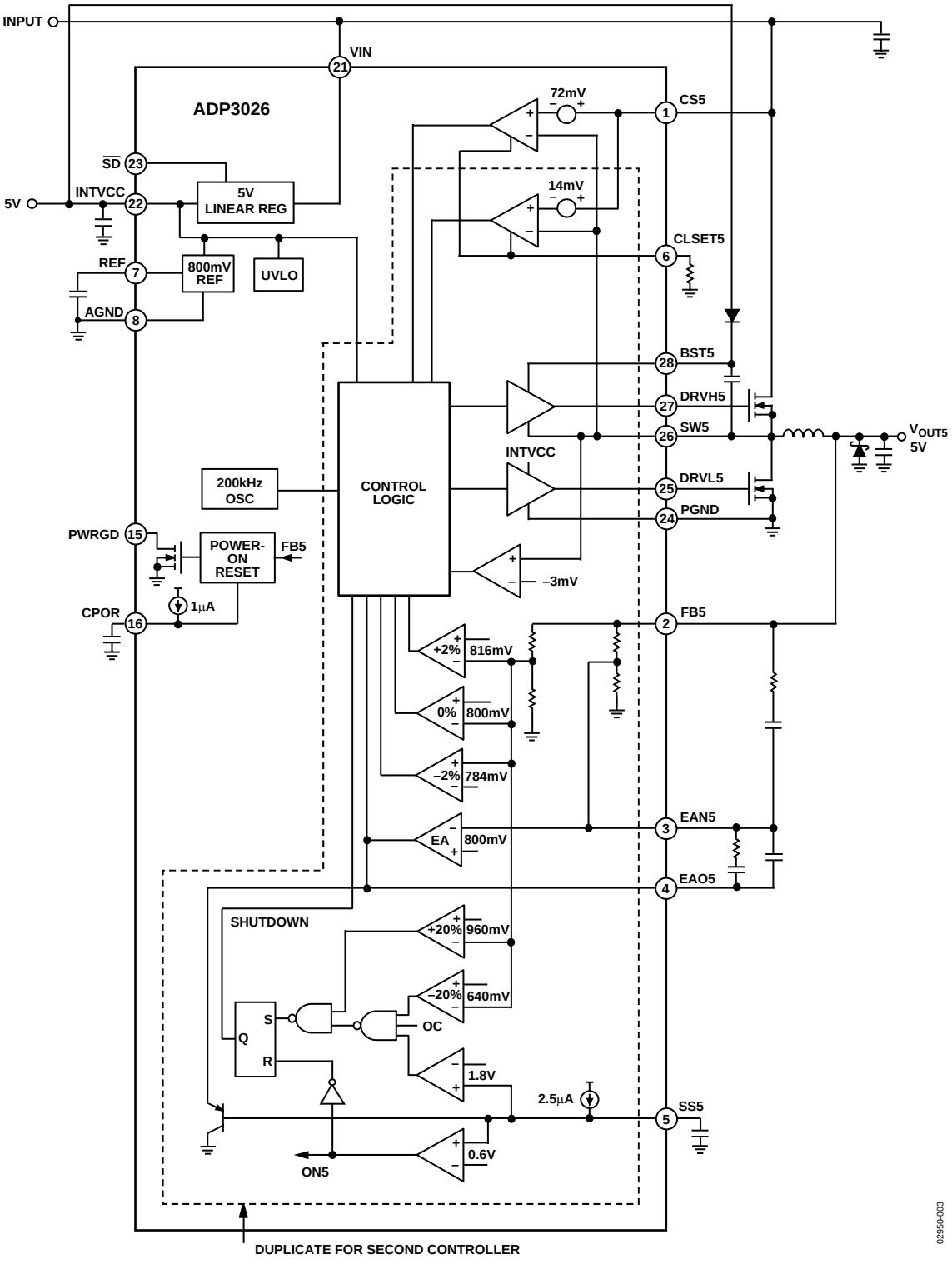

Figure 3. Detailed Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

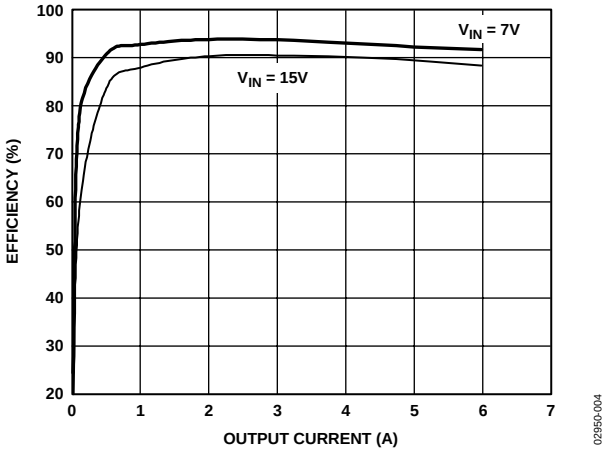

Figure 4. Efficiency vs. 5 V Output Current

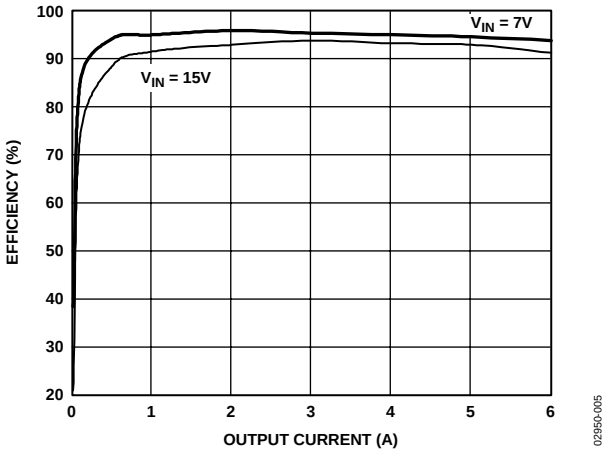

Figure 5. Efficiency vs. 3.3 V Output Current

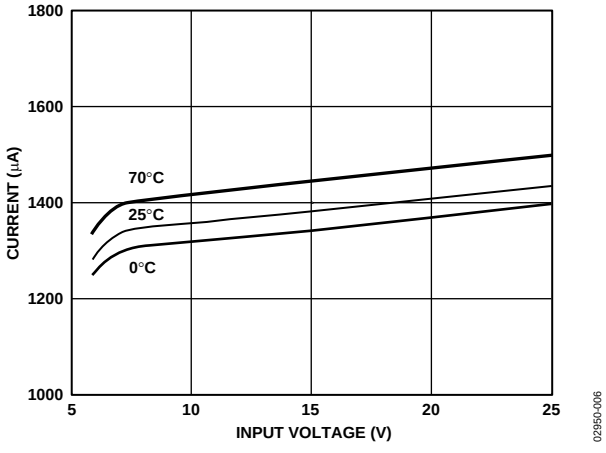

Figure 6. Input Standby Current vs. Input Voltage

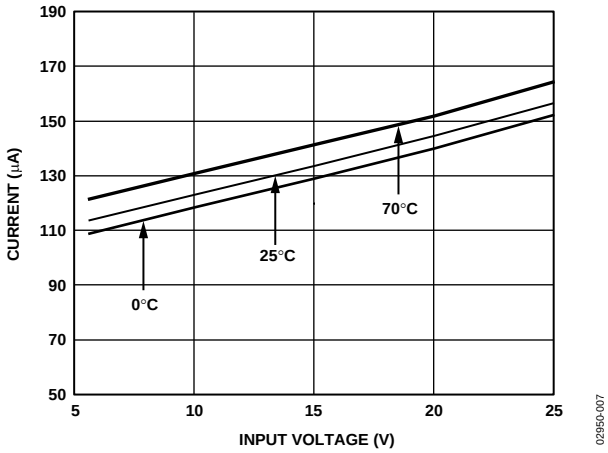

Figure 7. Input Shutdown Current vs. Input Voltage

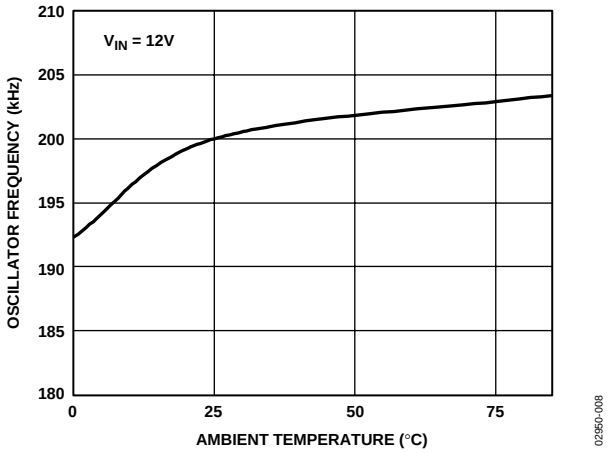

Figure 8. Oscillator Frequency vs. Temperature

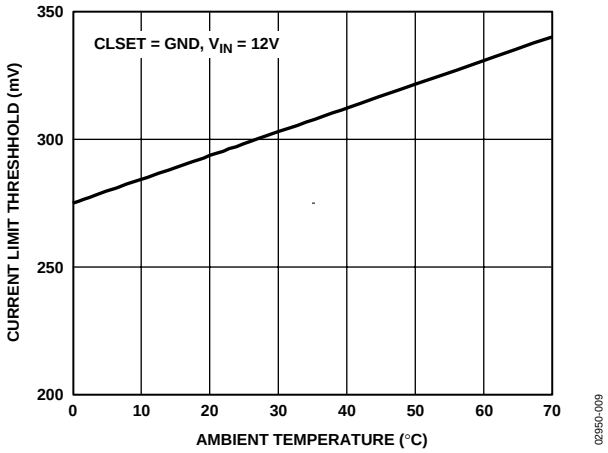

Figure 9. Current Limit Threshold vs. Temperature

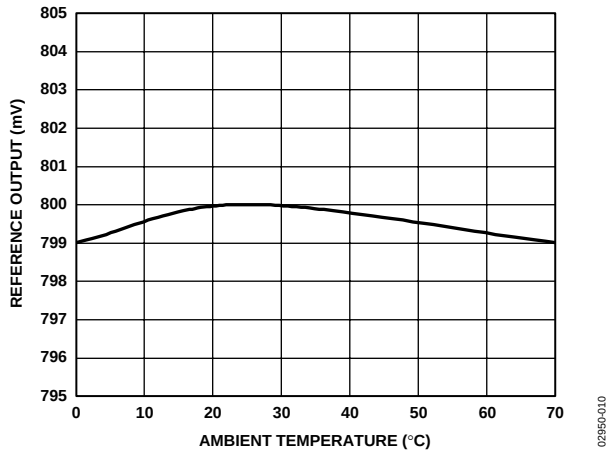

Figure 10. Reference Output vs. Temperature

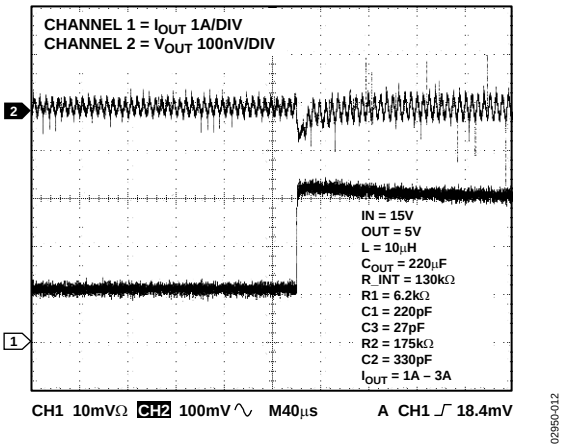

Figure 13. Load Transient Response - 1A to 3A

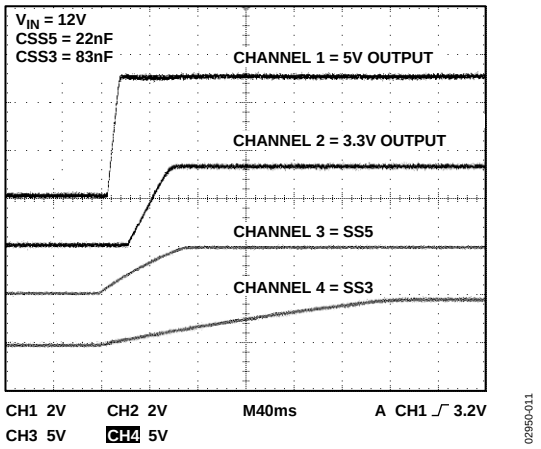

Figure 11. Soft Start Sequencing

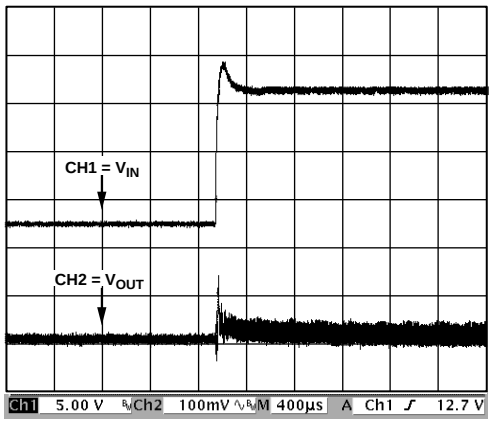

Figure 14. V_{IN} = 7.5 V to 22 V Transient, 5 V Output, CH1—Input Voltage, CH2—Output Voltage

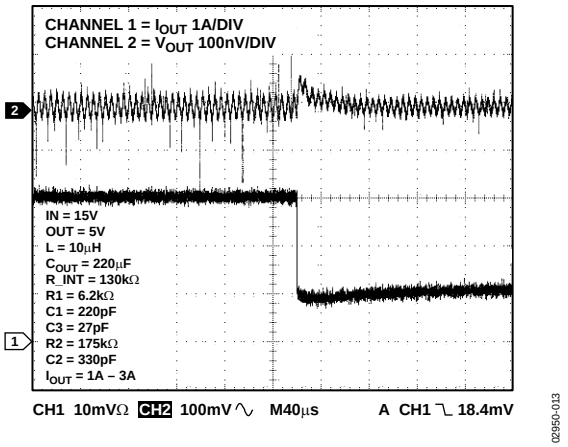

Figure 12. Load Transient Response - 3A to 1A

THEORY OF OPERATION

The ADP3026 is a step-down power supply controller for battery-powered applications. The ADP3026 contains the control circuit for two synchronous step-down converter. for fixed 3.3 V and 5 V outputs.

CIRCUIT DESCRIPTION

Internal 5 V Supply (INTVCC)

An internal low dropout regulator (LDO) generates a 5 V supply (INTVCC) to power all of the functional blocks within the IC. The total current rating of this LDO is 50 mA. However, this current is used for supplying gate-drive power, and it is recommended that current is not drawn from this pin for other purposes. Bypass INTVCC to AGND with a 4.7 µF capacitor. A UVLO circuit is also included in the regulator. When INTVCC < 4.1 V, the two switching regulators and the linear regulator controller are shut down. The UVLO hysteresis voltage is about 270 mV. The internal LDO has a built-in foldback current limit so that it will be protected if a short circuit is applied to the 5 V output.

Reference (REF)

The ADP3026 contains a precision 800 mV band gap reference. Bypass REF to AGND with a 22 nF ceramic capacitor. The reference is for internal use only; do not draw current from REF.

Boosted High-Side Gate Drive Supply (BST)

The gate drive voltage for the high-side N-channel MOSFET is generated by a flying capacitor boost circuit. The boost capacitor connected between BST and SW is charged from the INTVCC supply. Use only small-signal diodes for the boost circuit.

Synchronous Rectifier (DRVL)

Synchronous rectification is used to improve efficiency, reduce conduction losses, and ensure proper start-up of the boost gate driver circuit. Antishoot-through protection is included to prevent cross conduction during switch transitions. The low-side driver must be turned off before the high-side driver is turned on. For typical N-channel MOSFETs, the dead time is about 50 ns. On the other edge, a dead time of about 50 ns is achieved by an internal delay circuit. The synchronous rectifier is turned off when the current flowing through the low-side MOSFET falls to zero when in discontinuous conduction mode (DCM). In continuous conduction mode (CCM), the current flowing through the low-side MOSFET never reaches zero, so the synchronous rectifier is turned off by the next clock cycle.

Shutdown ($\overline{SD}$)

Holding $\overline{SD}$ low puts the ADP3026 into ultralow current shutdown mode. For automatic startup, tie $\overline{SD}$ to VIN through a resistor.

Soft Start and Power-Up Sequencing (SS)

SS3 and SS5 are soft start pins for the two controllers. A 2.1 µA pull-up current charges an external soft start capacitor. Power-up sequencing is easily done by choosing different capacitance. When SS3/SS5 < 0.6 V, the two switching regulators are turned off. When 0.6 V < SS5/SS3 < 1.8 V, the regulators start working in soft start mode. When SS3/SS5 > 1.8 V, the regulators are in normal operating mode. The minimum soft start time (~20 µs) is set by an internal capacitor. Table 4 shows the ADP3026's operating modes.

Current Limiting (CLSET)

A cycle-by-cycle current limiting scheme is used by monitoring current through the top N-channel MOSFET when it is turned on. By measuring the voltage drop across the high-side MOSFET $V_{DS(ON)}$, the external sense resistor is not required. The current limit value is controlled by CLSET. When CLSET is floating, the maximum $V_{DS(ON)}$ = 72 mV at room temperature; when CLSET = 0 V, the maximum $V_{DS(ON)}$ = 300 mV at room temperature. An external resistor (R_{EXT}) between CLSET and AGND sets a current limit value between 72 mV and 300 mV. The relationship between the external resistance and the maximum $V_{DS(ON)}$ is

$$V_{DS(ON)MAX} = 72\,\text{mV}\,\frac{(110\,\text{k}\Omega + R_{EXT})}{(26\,\text{k}\Omega + R_{EXT})} \quad (1)$$

The temperature coefficient of $R_{DS(ON)}$ of the N-channel MOSFET is canceled by the internal current limit circuitry so that the current limit value is accurate over a wide temperature range.

Table 4. Operating Modes

$\overline{SD}$	SS5	SS3	Description
Low	X	X	All Circuits Turned Off
High	SS5 < 0.6 V	SS3 < 0.6 V	5 V and 3.3 V Off; INTVCC = 5 V, REF = 0.8 V
High	0.6 V < SS5 < 1.8 V	X	5 V in Soft Start
High	1.8 V < SS5	X	5 V in Normal Operation
High	X	0.6 V < SS3 < 1.8 V	3.3 V in Soft Start
High	X	1.8 V < SS3	3.3 V in Normal Operation

Output Undervoltage Protection

Each switching controller has an undervoltage protection circuit. When the current flowing through the high-side MOSFET reaches the current limit continuously for eight clock cycles, and the output voltage is below 20% of the nominal output voltage, both controllers are latched off and do not restart until $\overline{SD}$ or SS3/SS5 is toggled, or until V_{IN} is cycled below 4.1 V. This feature is disabled during soft start.

Output Overvoltage and Reverse Voltage Protection

Both converter outputs are continuously monitored for overvoltage. If either output voltage is higher than the nominal output voltage by more than 20%, both converters' high-side gate drivers (DRVH5/3) are latched off; the low-side gate drivers are latched on and neither restart until $\overline{SD}$ or SS5/SS3 is toggled, or until V_{IN} is cycled below 4 V. The low-side gate driver (DRVL) is kept high when the controller is in off-state and the output voltage is less than 93% of the nominal output voltage. Discharging the output capacitors through the main inductor and low-side N-channel MOSFET causes the output voltage to ring. This makes the output momentarily go below GND. To prevent damage to the circuit, use a reverse-biased 1 A Schottky diode in parallel with the output capacitors to clamp the negative surge.

Power Good Output (PWRGD)

The ADP3026 provides a PWRGD signal that is used to indicate to a microprocessor that the ADP3026 output voltages are in regulation. During startup, the PWRGD pin is held low until the 5 V output is within −3% of its preset voltage. Then, after a time delay determined by an external timing capacitor connected from CPOR to GND, PWRGD is actively pulled up to INTVCC by an external pull-up resistor. The delay is calculated by

$$Td = \frac{1.2\ \text{V} \times C_{CPOR}}{1\ \mu\text{A}} \quad (2)$$

CPOR can also be used as a manual reset ($\overline{MR}$) function. When the 5 V output is lower than the preset voltage by more than 7%, PWRGD is immediately pulled low.

APPLICATION INFORMATION

A typical application circuit using the ADP3026 is shown in Figure 15. Although the component values given in Figure 16 are based on a 5 V @ 4 A/3.3 V @ 4 A design, the ADP3026's output drivers are capable of handling output currents anywhere from less than 1 A to more than 10 A. Throughout this section, design examples and component values are given for three different power levels. For simplicity, these levels are referred to as low power, basic, and extended power. Table 5 shows the input/output specifications for these three levels.

Input Voltage Range

The input voltage range of the ADP3026 is 5.5 V to 25 V. The converter design is optimized to deliver the best performance within a 7.5 V to 18 V range, which is the nominal voltage for three to four cell Li-Ion battery stacks. Voltages above 18 V may occur under light loads and when the system is powered from an ac adapter with no battery installed.

Maximum Output Current and MOSFET Selection

The maximum output current for each switching regulator is limited by sensing the voltage drop between the drain and source of the high-side MOSFET when it is turned on. A current sense comparator senses voltage drop between CS5 and SW5 for the 5 V converter, and between CS3 and SW3 for the 3.3 V converter. The sense comparator threshold is 72 mV when the programming pin, CLSET, is floating, and 300 mV when CLSET is connected to ground. Current-limiting is based on sensing the peak current. Peak current varies with input voltage and depends on the inductor value. The higher the inductor ripple current or input voltage, the lower the converter's maximum output current at the set current sense amplifier threshold. The relation between peak inductor and dc output current is given by

$$I_{PEAK} = I_{OUT} + V_{OUT} \times \left(\frac{V_{IN(MAX)} - V_{OUT}}{2 \times f \times L \times V_{IN(MAX)}} \right) \quad (3)$$

At a given current comparator threshold, V_{TH}, and MOSFET $R_{DS(ON)}$, the maximum inductor peak current is

$$I_{PEAK} = \frac{V_{TH}}{R_{DS(ON)}} \quad (4)$$

Rearranging Equation 2 to solve for $I_{OUT(MAX)}$ gives

$$I_{(OUT)MAX} = \frac{V_{TH}}{R_{DS(ON)}} - V_{OUT} \times \left(\frac{V_{IN(MAX)} - V_{OUT}}{2 \times f \times L \times V_{IN(MAX)}} \right) \quad (5)$$

Thus, V_{TH} can be chosen to design the required maximum output current. It is important to remember that this current limit circuit is designed to protect against high current or short-circuit conditions only. This protects the IC and MOSFETs long enough to allow the output undervoltage protection circuitry to latch off the supply.

Table 5. Typical Power Level Examples

	Low Power	Basic	Extended Power
Input Voltage Range	5.5 V to 25 V	5.5 V to 25 V	5.5 V to 25 V
Switching Output 1	3.3 V/2 A	3.3 V/4 A	3.3 V/10 A
Switching Output 2	5 V/2 A	5 V/4 A	5 V/10 A

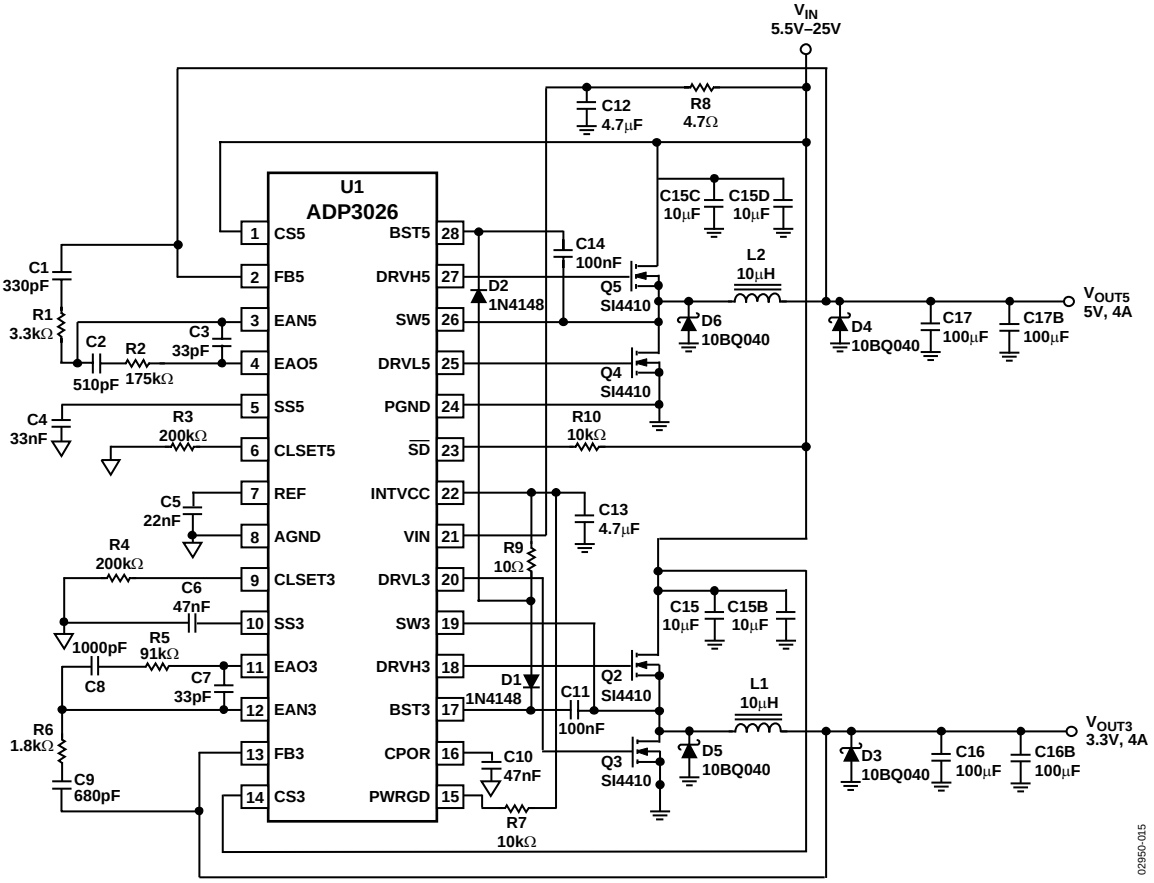

Figure 15. 33 W, Dual-Output DC-DC Converter

Nominal Inductor Value

The inductor guidelines in this data sheet are based on the assumption that the inductor ripple current is 30% of the maximum output dc current at the nominal 12 V input voltage. The inductor ripple current and inductance value are not critical, but this choice is important in analyzing the trade-offs between cost, size, efficiency, and volume. The higher the ripple current, the lower the inductor size and volume. However, this leads to higher ac losses in the windings. Conversely, a higher inductance means lower ripple current and smaller output filter capacitors, but slower transient response.

The inductance should be based on the maximum output current plus 15% (½ of the 30% ripple allowance) at the nominal input voltage

$$L \geq 3 \times (V_{IN(NOM)} - V_{OUT}) \times \frac{V_{OUT}}{V_{IN(NOM)} \times I_{OUT} \times f} \qquad (6)$$

Optimum standard inductor values for the three power levels are shown in Table 6.

Table 6. Standard Inductor Values (200 kHz Frequency)

3.3 V/2A	3.3 V/2A	3.3 V/10A	5 V/2A	5 V/4A	5 V/10A
20 µH	8.2 µH	3.3 µH	22 µH	10 µH	4.7 µH

Inductor Selection

Once the value for the inductor is known, there are two ways to proceed: design the inductor in-house or buy the closest inductor that meets the overall design goals.

Standard Inductors

Buying a standard inductor provides the fastest, easiest solution, and many companies offer suitable power inductor solutions. A list of power inductor manufacturers is given in Table 7.

Table 7. Recommended Inductor Manufacturers

Coilcraft	Coiltronics	Murata Electronics North America Inc.
Phone: 847/639-6400 Fax: 847/639-1469 Web: www.coilcraft.com	Phone: 561/241-7876 Fax: 561/241-9339 Web: www.coiltronics.com	Phone: 770/436-1300 Fax: 770/436-3030 Web: www.murata.com
SMT Power Inductors Series 1608, 3308, 3316, 5022, 5022HC, DO3340 Low Cost Solution	SMT Power Inductors Series UNI-PAC2, UNI-PAC3 and UNI-PAC4 Low Cost Solution	SMT Power Inductors Series LQT2535 Best for Low EMI/RFI
SMT Shielded Power Inductors Series DS5022, DS3316, DT3316 Best for Low EMI/RFI	SMT Power Inductors Series, ECONO-PAC, VERSA-PAC Best for Low Profile or Flexible Design	
Power Inductors and Chokes, Series DC1012, PCV-0, PCV-1, PCV-2, PCH-27, PCH-45 Low Cost	Power Inductors CTX Series Low EMI/RFI Low Cost Toroidal Inductors but Not Miniature	Chip Inductors LQN6C, LQS66C

C_{IN} and C_{OUT} Selection

In continuous conduction mode, the source current of the upper MOSFET is approximately a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients use a low ESR input capacitor sized for the maximum rms current. The maximum rms capacitor current is given by

$$I_{RMS} = \sqrt{V_{OUT} \times (V_{IN} - V_{OUT})} \times \frac{I_{OUT(MAX)}}{V_{IN}} \quad (7)$$

This formula has a maximum at $V_{IN} = 2 \times V_{OUT}$, where $I_{RMS} = I_{OUT(MAX)}/2$. Note that the capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. It is therefore advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be connected in parallel to meet size or height requirements in the design. If electrolytic or tantalum capacitors are used, place an additional 0.1 µF to 1 µF ceramic bypass capacitor in parallel with C_{IN}.

The selection of the output capacitor, C_{OUT}, is driven by the required effective series resistance (ESR) and the desired output ripple. A good guideline is to limit the ripple voltage to 1% of the nominal output voltage. It is assumed that the total ripple is caused by two factors: 25% comes from the C_{OUT} bulk capacitance value, and 75% comes from the capacitor ESR.

The value of C_{OUT} is determined by

$$C_{OUT} = \frac{I_{RIPPLE}}{2 \times f \times V_{RIPPLE}} \quad (8)$$

where $I_{RIPPLE} = 0.3 \times I_{OUT}$ and $V_{RIPPLE} = 0.01 \times V_{OUT}$. The maximum acceptable ESR of C_{OUT} is found using

$$ESR \leq 0.75 \times \frac{V_{RIPPLE}}{I_{RIPPLE}} \quad (9)$$

Manufacturers such as Vishay, AVX, Elna, WIMA, and Sanyo provide good high performance capacitors. Sanyo's OSCON semiconductor dielectric capacitors have lower ESR for a given size, at a somewhat higher price. Choosing sufficient capacitors to meet the ESR requirement for C_{OUT} normally exceeds the amount of capacitance needed to meet the ripple current requirement.

In surface-mount applications, multiple capacitors may have to be paralleled to meet the capacitance, ESR, or rms current handling requirements. Aluminum electrolytic and dry tantalum capacitors are available in surface-mount configurations. In the case of tantalum, it is critical that capacitors are surge tested for use in switching power supplies. Recommendations for output capacitors are shown in Table 8.

Table 8. Recommended Capacitor Manufacturers

Maximum Output Current	2 A	4 A
Input Capacitor	TOKIN Multilayer	TOKIN Multilayer
	Ceramic Cap, 22 µF/25 V	Ceramic Cap, 2 × 22 µF/25 V
	P/N:C55Y5U1E226Z	P/N:C55Y5U1E226Z
	TAIYO YUDEN INC.	TAIYO YUDEN INC.
	Ceramic Caps, Y5V Series 10 µF/25 V	Ceramic Caps, Y5V Series 10 µF/25 V
	P/N: TMK432BJ106KM	P/N: TMK432BJ106KM
Output Capacitor	SANYO POSCAP TPC	SANYO POSCAP TPC
3.3 V Output	Series, 68 µF/10 V	Series, 2 × 68 µF/10 V
Output Capacitor	SANYO POSCAP TPC	SANYO POSCAP TPC
5 V Output	Series, 68 µF/10 V	Series,2 × 68 µF/10 V

Power MOSFET Selection

N-channel power MOSFETs are used for both the main and synchronous switches. The important selection parameters for the power MOSFETs are threshold voltage ($V_{GS(TH)}$) and on resistance ($R_{DS(ON)}$). An internal LDO regulator generates a 5 V supply that is boosted above the input voltage using a bootstrap circuit. This floating 5 V supply is used for the upper (main) MOSFET gate drive. Logic-level threshold MOSFETs must be used for both the main and synchronous switches.

Maximum output current (I_{MAX}) determines the $R_{DS(ON)}$ requirement for the two power MOSFETs. When the ADP3026 is operating in continuous mode, the simplifying assumption can be made that one of the two MOSFETs is always conducting the load current. The duty cycles for the MOSFETs are given by

$$Upper\ MOSFET\ Duty\ Cycle = \frac{V_{OUT}}{V_{IN}} \quad (10)$$

$$Lower\ MOSFET\ Duty\ Cycle = \frac{V_{IN} - V_{OUT}}{V_{IN}} \quad (11)$$

From the duty cycle, the required minimum $R_{DS(ON)}$ for each MOSFET can be derived by the following equations:

Upper MOSFET:

$$R_{DS(ON)}(Upper) = \frac{V_{IN} \times P_D}{V_{OUT} \times I_{MAX^2} \times (1 \times \alpha\Delta T)} \quad (12)$$

Lower MOSFET:

$$R_{DS(ON)}(Lower) = \frac{V_{IN} \times P_D}{(V_{IN} - V_{OUT}) \times I_{MAX^2} \times (1 + \alpha\Delta T)} \quad (13)$$

where P_D is the allowable power dissipation and α is the temperature dependency of $R_{DS(ON)}$. P_D is determined by efficiency and/or thermal requirements (see the Efficiency Enhancement section). (1 + αΔT) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ versus temperature curve, but α = 0.007/°C can be used as an approximation for low voltage MOSFETs.

Maximum MOSFET power dissipation occurs at maximum output current, and is calculated as follows:

Upper MOSFET:

$$P_D(Upper) = \frac{V_{OUT}}{V_{IN}} \times I_{MAX^2} \times R_{DS(ON)} \times (1 + \alpha\Delta T) \quad (14)$$

Lower MOSFET:

$$P_D(Lower) = \frac{V_{IN} - V_{OUT}}{V_{IN}} \times I_{MAX^2} \times R_{DS(ON)} \times (1 + \alpha\Delta T) \quad (15)$$

The Schottky diode, D1 in Figure 15, conducts only during the dead time between conduction of the two power MOSFETs. D1's purpose is to prevent the body diode of the lower N-channel MOSFET from turning on and storing charge during the dead time, which could cost as much as 1% in efficiency. D1 should be selected for a forward voltage of less than 0.5 V when conducting I_{MAX}. Recommended transistors for upper and lower MOSFETs are given in Table 9.

Table 9. Recommended MOSFETs

Maximum Output	2 A	4 A	10 A
Vishay/Siliconix	Si4412DY, 28 mΩ	Si4410DY, 13.5 mΩ	Si4874DY, 7.5 mΩ
International Rectifier	IRF7805, 11 mΩ	IRF7811, 8.9 mΩ	IRFBA3803, 5.5 mΩ
		IRF7805, 11 mΩ	IRF7809, 7.5 mΩ

Soft Start

The soft start time of each switching regulator is programmed by connecting a soft start capacitor to the corresponding soft start pin (SS3 or SS5). The time it takes each regulator to ramp up to its full duty ratio depends proportionally on the values of the soft start capacitors. The charging current is 2.5 µA ±20%. The capacitor value to set a given soft start time, t_{SS}, is given by

$$C_{SS} = 2.5\ \mu A \frac{(t_{SS(ms)})}{1.8\ V}(pF) \quad (16)$$

Efficiency Enhancement

The efficiency of each switching regulator is inversely proportional to the losses during the switching conversion. The main factors to consider when attempting to maximize efficiency are

1. Resistive losses, which include the $R_{DS(ON)}$ of upper and lower MOSFETs, trace resistances, and output equivalent series resistance.

   These losses contribute a major part of the overall power loss in low voltage battery-powered applications. However, trying to reduce these resistive losses by using multiple MOSFETs and thick traces may lead to lower efficiency and higher price. This is due to the trade-off between reduced resistive loss and increased gate drive loss that must be considered when optimizing efficiency.

2. Switching losses due to the limited time of switching transitions.

   This occurs due to the gate drive losses of both upper and lower MOSFETs, and switching node capacitive losses, as well as through hysteresis and eddy current losses in power choke. Input and output capacitor ripple current losses should also be considered as switching losses. These losses are input voltage dependent and can be estimated as follows:

$$P_{SWLOSS} = 2.5 \times V_{IN}^{1.85} \times I_{MAX} \times C_{SN} \times f \quad (17)$$

   where C_{SN} is the overall capacitance of the switching node related to loss.

3. Supply current of the switching controller (independent of the input current redirected to supply the MOSFET's gates).

   This is a very small portion of the overall loss, but it does increase with input voltage.

Transient Response Considerations

Both stability and regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in output load current. When a load step occurs, output voltage shifts by an amount equal to the current step multiplied by the total ESR of the summed output capacitor array. Output overshoot or ringing during the recovery time (in both directions of the current step change) indicates poor regulation stability. The external feedback compensation components shown in Figure 16 provide adequate compensation for most applications.

Feedback Loop Compensation

The ADP3026 uses voltage mode control to stabilize the switching controller outputs. Figure 16 shows the voltage mode control loop for one of the buck switching regulators. The internal reference voltage V_{REF} is applied to the positive input of the internal error amplifier. The other input of the error amplifier is EAN, which is internally connected to the feedback sensing pin FB via an internal resistor. The error amplifier creates the closed-loop voltage level for the pulse-width modulator that drives the external power MOSFETs. The output LC filter smoothes the pulse-width modulated input voltage to a dc output voltage.

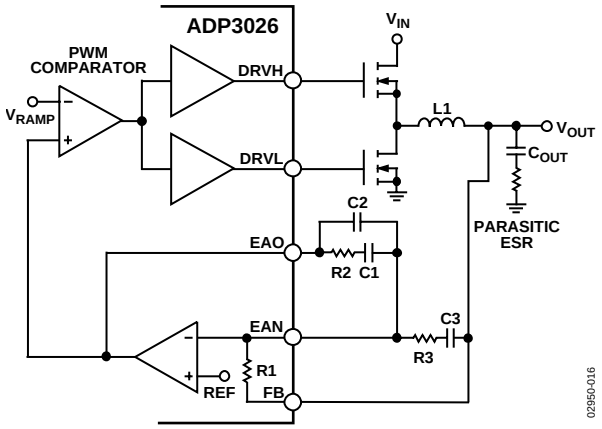

Figure 16. Buck Regulator Voltage Control Loop

The pulse-width modulator transfer function is V_{OUT}/VEA_{OUT}, where VEA_{OUT} is the output voltage of the error amplifier. That function is dominated by the impedance of the output filter with its double-pole resonance frequency (f_{LC}), a single zero at the output capacitor (f_{ESR}), and the dc gain of the modulator, and is equal to the input voltage divided by the peak ramp height (V_{RAMP}), which is equal to 1.2 V when V_{IN} = 12 V.

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L_F \times C_{OUT}}} \quad (18)$$

$$F_{ESR} = \frac{1}{2\pi \times ESR \times C_{OUT}} \quad (19)$$

The compensation network consists of the internal error amplifier and two external impedance networks, Z_{IN} and Z_{FB}. Once the application and the output filter capacitance and ESR are chosen, the specific component values of the external impedance networks, Z_{IN} and Z_{FB}, can be determined. There are two design criteria for achieving stable switching regulator behavior within the line and load range. One is the maximum bandwidth of the loop, which affects fast transient response, if needed; the other is the minimum accepted by the design phase margin.

The phase margin is the difference between the closed-loop phase and 180°. Recommended phase margin is 45° to 60° for most applications.

The equations for calculating the compensation poles and zeros are

$$f_{P1} \frac{1}{2\pi \times R2 \times \frac{C1 \times C2}{C1 + C2}} \quad (20)$$

$$f_{P2} = \frac{1}{2\pi \times R3 \times C3} \quad (21)$$

$$f_{Z1} = \frac{1}{2\pi \times R2 \times C1} \quad (22)$$

$$f_{Z2} = \frac{1}{2\pi \times (R1 + R3) \times C3} \quad (23)$$

The value of the internal resistor *R1* is 89 kΩ for the 3.3 V switching regulator, and 150 kΩ for the 5 V switching regulator.

Compensation Loop Design and Test Method

1. Choose the gain (R2/R1) for the desired bandwidth.
2. Place f_{Z1} 20% to 30% below f_{LC}.
3. Place f_{Z2} 20% to 30% above f_{LC}.
4. Place f_{P1} at f_{ESR}, and check the output capacitor for worst-case ESR tolerances.
5. Place f_{P2} at 40% to 60% of the oscillator frequency.
6. Estimate phase margins in full frequency range (zero frequency to zero gain crossing frequency).
7. Apply the designed compensation and test the transient response under a moderate step load change (30% to 60%) and various input voltages. Monitor the output voltage via the oscilloscope. The voltage overshoot or undershoot should be within 1% to 3% of the nominal output, without ringing and abnormal oscillation.

LAYOUT CONSIDERATIONS

The following guidelines are recommended for optimal performance of a switching regulator in a portable PC system.

General Recommendations

1. For best results, a 4-layer (minimum) PCB is recommended. This allows the needed versatility for control circuitry interconnections with optimal placement, a signal ground plane, power planes for both power ground and the input power, and wide interconnection traces in the rest of the power delivery current paths. Each square unit of 1 ounce copper trace has a resistance of ~0.53 mΩ at room temperature.
2. Whenever high currents must be routed between PCB layers, use vias liberally to create several parallel current paths so that the resistance and inductance introduced by these current paths is minimized and the via current rating is not exceeded.
3. Minimize overlapping of the power and ground planes as much as possible. It is generally easiest (although not necessary) to have the power and signal ground planes on the same PCB layer. Connect the planes together nearest to the first input capacitor where the input ground current flows from the converter back to the battery.
4. If critical signal lines (including the voltage and current sense lines of the ADP3026) must cross through power circuitry, place a signal ground plane between those signal lines and the traces of the power circuitry. This serves as a shield to minimize noise injection into the signals at the expense of making signal ground a bit noisier.
5. Connect the PGND pin of the ADP3026 first to a ceramic bypass capacitor on the VIN pin, and then into the power ground plane using the shortest possible trace. However, do not route the power ground plane under other signal components, including the ADP3026 itself. If necessary, follow the preceding guideline to use the signal plane as a shield between the power ground plane and the signal circuitry.
6. Connect the AGND pin of the ADP3026 first to the REF capacitor, and then into the signal ground plane. In cases where no signal ground plane can be used, use short interconnections to other signal ground circuitry in the power converter.
7. Connect the output capacitors of the power converter to the signal ground plane even though power current flows in the ground of these capacitors. It is advisable to avoid critical ground connections (e.g., the signal circuitry of the power converter) in the signal ground plane between the input and output capacitors. It is also advisable to keep the planar interconnection path short (i.e., have input and output capacitors close together).
8. Connect the output capacitors as close as possible to the load (or connector) that receives the power. If the load is distributed, also distribute the capacitors, and generally in proportion to where the load tends to be more dynamic.
9. Absolutely avoid crossing any signal lines over the switching power path loop, as described in the Power Circuitry section.

Power Circuitry

10. Route the switching power path on the PCB to encompass the smallest possible area in order to minimize radiated switching noise energy (i.e., EMI). Failure to take proper precautions often results in EMI problems for the entire PC system as well as noise related operational problems in the power converter control circuitry. The switching power path is the loop formed by the current path through the input capacitors, the two FETs, and the power Schottky diode, if used, including all interconnecting PCB traces and planes. The use of short and wide interconnection traces is especially critical in this path for two reasons: it minimizes the inductance in the switching loop, which causes high energy ringing, and it accommodates the high current demand with minimal voltage loss.

11. A power Schottky diode (1 A ~ 2 A dc rating) placed from the lower FET's source (anode) to drain (cathode) helps to minimize switching power dissipation in the upper FET. In the absence of an effective Schottky diode, this dissipation occurs through the following sequence of switching events. The lower FET turns off in advance of the upper FET turning on (necessary to prevent cross-conduction). The circulating current in the power converter, no longer finding a path for current through the channel of the lower FET, draws current through the inherent body-drain diode of the FET. The upper FET turns on, and the reverse recovery characteristic of the lower FET's body-drain diode prevents the drain voltage from being pulled high quickly.

    The upper FET then conducts very large current while it momentarily has a high voltage forced across it, which translates into added power dissipation in the upper FET. The Schottky diode minimizes this problem by carrying a majority of the circulating current when the lower FET is turned off, and by virtue of its essentially nonexistent reverse recovery time.

12. Whenever a power-dissipating component (e.g., a power MOSFET) is soldered to a PCB, liberally use vias, both directly on the mounting pad and immediately surrounding it. Two important reasons for this are improved current rating through the vias (if it is a current path) and improved thermal performance, especially if the vias are extended to the opposite side of the PCB where a plane can more readily transfer the heat to the air.

13. Route the output power path, though not as critical as the switching power path, to encompass a small area. The output power path is formed by the current path through the inductor, the output capacitors, and back to the input capacitors.

14. Extend the power ground plane fully under all the power components except the output capacitors for best EMI containment. These are the input capacitors, the power MOSFETs and Schottky diode, the inductor, and any snubbing elements that might be added to dampen ringing. Avoid extending the power ground under any other circuitry or signal lines, including the voltage and current sense lines.

Signal Circuitry

15. Kelvin connect the CS and SW traces to the upper MOSFET drain and source so that the additional voltage drop due to current flow on the PCB at the current sense comparator connections does not affect the sensed voltage. It is desirable to have the ADP3026 close to the output capacitor bank and not in the output power path, so that any voltage drop between the output capacitors and the AGND pin is minimized, and voltage regulation is not compromised.

OUTLINE DIMENSIONS

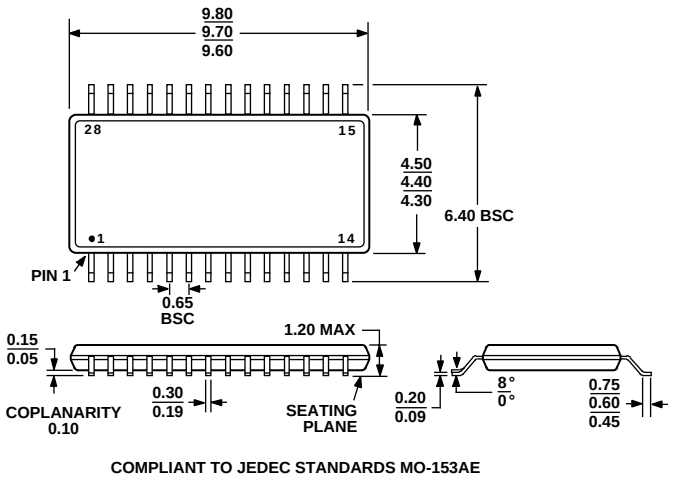

Figure 17. 28-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-28)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADP3026JRUZ-REEL[1]	0°C to 70°C	Thin Shrink Small Outline (TSSOP)	RU-28

[1] Z = Pb-free part.

NOTES

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