Multiformat Progressive Scan/HDTV Encoder with Three 11-Bit DACs, 10-Bit Data Input, and Macrovision

ADV7196A

FEATURES

INPUT FORMATS

- YCrCb in 2 × 10-Bit (4:2:2) or 3 × 10-Bit (4:4:4) Format Compliant to SMPTE-293M (525p), ITU-R.BT1358 (625p), SMPTE274M (1080i), SMPTE296M (720p) and Any Other High Definition Standard Using Async Timing Mode
- RGB in 3 × 10 Bit (4:4:4) Format

OUTPUT FORMATS

- YPrPb Progressive Scan (EIA-770.1, EIA-770.2)
- YPrPb HDTV (EIA-770.3)
- RGB Levels Compliant to RS-170 and RS-343A
- 11-Bit and Sync (DAC A)
- 11-Bit DACs (DAC B, DAC C)

PROGRAMMABLE FEATURES

- Internal Test Pattern Generator with Color Control
- Y/C Delay (±)
- Gamma Correction
- Individual DAC On/Off Control
- 54 MHz Output (2× Oversampling)
- Sharpness Filter with Programmable Gain/Attenuation
- Programmable Adaptive Filter Control
- Undershoot Limiter
- I²C® Filter
- VBI Open Control
- Macrovision Rev. 1.0 (525p)
- CGMS-A (525p)
- 2-Wire Serial MPU Interface
- Single Supply 3.3 V Operation
- 52-MQFP Package

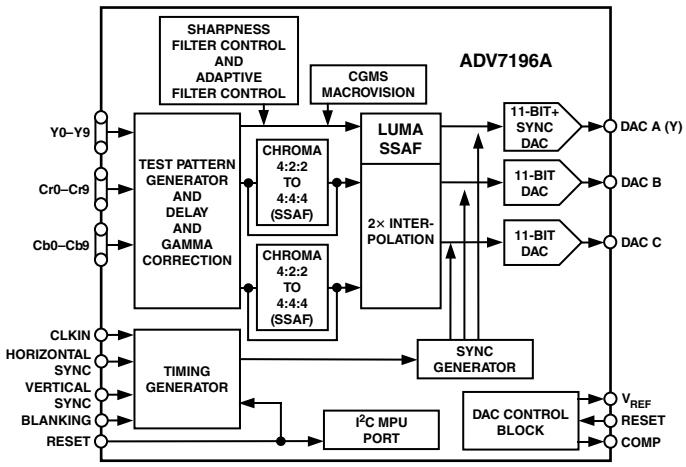
APPLICATIONS

- Progressive Scan/HDTV Display Devices
- DVD Players
- MPEG 2 at 81 MHz
- Progressive Scan/HDTV Projection Systems
- Digital Video Systems
- High Resolution Color Graphics
- Image Processing/Instrumentation
- Digital Radio Modulation/Video Signal Reconstruction

GENERAL DESCRIPTION

The ADV7196A is a triple high-speed, digital-to-analog encoder on a single monolithic chip. It consists of three high-speed video D/A converters with TTL-compatible inputs.

FUNCTIONAL BLOCK DIAGRAM



The ADV7196A has three separate 10-bit-wide input ports which accept data in 4:4:4 10-bit YCrCb or RGB or 4:2:2 10-bit YCrCb. This data is accepted in progressive scan format at 27 MHz or HDTV format at 74.25 MHz or 74.1758 MHz. For any other high-definition standard but SMPTE 293M, ITU-R BT.1358, SMPTE274M or SMPTE296M the Async Timing Mode can be used to input data to the ADV7196A. For all standards, external horizontal, vertical, and blanking signals or EAV/SAV codes control the insertion of appropriate synchronization signals into the digital data stream and therefore the output signals.

The ADV7196A outputs analog YPrPb progressive scan format complying to EIA-770.1, EIA-770.2; YPrPb HDTV complying to EIA-770.3; RGB complying to RS-170/RS-343A.

The ADV7196A requires a single 3.3 V power supply, an optional external 1.235 V reference and a 27 MHz clock in Progressive Scan Mode or a 74.25 MHz (or 74.1758 MHz) clock in HDTV mode.

In Progressive Scan Mode, a sharpness filter with programmable gain allows high-frequency enhancement on the luminance signal. Programmable Adaptive Filter Control, which may be used, allows removal of ringing on the incoming Y data. The ADV7196A supports CGMS-A data control generation and the Macrovision Anticopy algorithm in 525p mode.

The ADV7196A is packaged in a 52-lead MQFP package.

I²C is a registered trademark of Philips Corporation.

REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

TABLE OF CONTENTS

ADV7196A–SPECIFICATIONS

3.3 V SPECIFICATIONS

(V_{AA} = 3.15 V to 3.45 V, V_{REF} = 1.235 V, R_{SET} = 2470 Ω, R_{LOAD} = 300 Ω. All specifications T_{MIN} to T_{MAX} (0°C to 70°C) unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions
STATIC PERFORMANCE					
Resolution (Each DAC)		11		Bits	
Integral Nonlinearity		1.5		LSB	
Differential Nonlinearity		0.9	2.0	LSB	
DIGITAL OUTPUTS					
Output High Voltage, V_{OL}			0.4	V	I_{SINK} = 3.2 mA
Output Low Voltage, V_{OH}	2.4			V	I_{SOURCE} = 400 μA
Three State Leakage Current			10	μA	V_{IN} = 0.4 V
Three State Output Capacitance		4		pF	
DIGITAL AND CONTROL INPUTS					
Input High Voltage, V_{IH}	2			V	
Input Low Voltage, V_{IL}		0.8	0.65	V	
Input Current, I_{IN}		0	1	μA	V_{IN} = 0.0 V or V_{DD}
Input Capacitance, C_{IN}		4		pF	
ANALOG OUTPUTS					
Full-Scale Output Current	3.92	4.25	4.56	mA	DAC A
Output Current Range	3.92	4.25	4.56	mA	DAC A
Full-Scale Output Current	2.54	2.83	3.11	mA	DAC B, C
Output Current Range	2.39	2.66	2.93	mA	DAC B, C
DAC-to-DAC Matching		1.4		%	
Output Compliance Range, V_{OC}	0	1.4		V	
Output Impedance, R_{OUT}		100		kΩ	
Output Capacitance, C_{OUT}		7		pF	
VOLTAGE REFERENCE (External)					
Reference Range, V_{REF}	1.112	1.235	1.359	V	
POWER REQUIREMENTS					
I_{DD}[2]		25	35	mA	1× Interpolation
I_{DD}[2]		51	60	mA	2× Interpolation
I_{DD}[2]		40		mA	HDTV Mode (with f_{CLK} = 74.25 MHz)
I_{AA}[3, 4]		11	15	mA	1× Interpolation, 2× Interpolation, and HDTV Mode
I_{PLL}		6.0	12	mA	1× Interpolation, 2× Interpolation, and HDTV Mode
Power Supply Rejection Ratio		0.01		%/%	

NOTES
[1]Guaranteed by characterization.
[2]I_{DD} or the circuit current is the continuous current required to drive the digital core without I_{PLL}.
[3]I_{AA} is the total current required to supply all DACs including the V_{REF} circuitry.
[4]All DACs on.

Specifications subject to change without notice.

3 V DYNAMIC–SPECIFICATIONS

(V_{AA} = 3.15 V to 3.45 V, V_{REF} = 1.235 V, R_{SET} = 2470 Ω, R_{LOAD} = 300 Ω. All specifications T_{MIN} to T_{MAX} (0°C to 70°C) unless otherwise noted.)

Parameter	Min	Typ	Max	Unit
Luma Bandwidth		13.5		MHz
Chroma Bandwidth		6.75		MHz
Signal-to-Noise Ratio		64		dB Luma Ramp Unweighted
Chroma/Luma Delay Inequality		0		ns

Specifications subject to change without notice.

3.3 V TIMING–SPECIFICATIONS

(V_{AA} = 3.15 V to 3.45 V, V_{REF} = 1.235 V, R_{SET} = 2470 Ω, R_{LOAD} = 300 Ω. All specifications T_{MIN} to T_{MAX} (0°C to 70°C) unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Conditions
MPU PORT[1]					
SCLOCK Frequency	0		400	kHz	
SCLOCK High Pulsewidth, t_1	0.6			µs	
SCLOCK Low Pulsewidth, t_2	1.3			µs	
Hold Time (Start Condition), t_3	0.6			µs	After This Period the 1st Clock Is Generated
Setup Time (Start Condition), t_4	0.6			µs	Relevant for Repeated Start Condition
Data Setup Time, t_5	100			ns	
SDATA, SCLOCK Rise Time, t_6			300	ns	
SDATA, SCLOCK Fall Time, t_7			300	ns	
Setup Time (Stop Condition), t_8	0.6			µs	
Reset Low Time	100			ns	
ANALOG OUTPUTS					
Analog Output Delay[2]		10		ns	
Analog Output Skew		0.5		ns	
CLOCK CONTROL AND PIXEL PORT[3]					
f_{CLK}			27	MHz	Progressive Scan Mode
f_{CLK}			74.25	MHz	HDTV Mode
f_{CLK}			81	MHz	Async Timing Mode and 1× Interpolation
Clock High Time t_9	5.0	1.5		ns	
Clock Low Time t_{10}	5.0	2.0		ns	
Data Setup Time t_{11}	2.0			ns	
Data Hold Time t_{12}	4.5			ns	
Control Setup Time t_{11}	7.0			ns	
Control Hold Time t_{12}	4.0			ns	
Pipeline Delay	16			Clock Cycles	For 4:4:4 Pixel Input Format at 1× Oversampling
Pipeline Delay	29			Clock Cycles	For 4:4:4 or 4:2:2 Pixel Input Format at 2× Oversampling

NOTES
[1]Guaranteed by characterization.
[2]Output delay measured from 50% point of the rising edge of CLOCK to the 50% point of DAC output full-scale transition.
[3]Data: Cb/Cr [9–0], Cr [9–0], Y [9:0]
Control: $\overline{\text{HSYNC}}$/$\overline{\text{SYNC}}$, $\overline{\text{VSYNC}}$/TSYNC, DV

Specifications subject to change without notice.

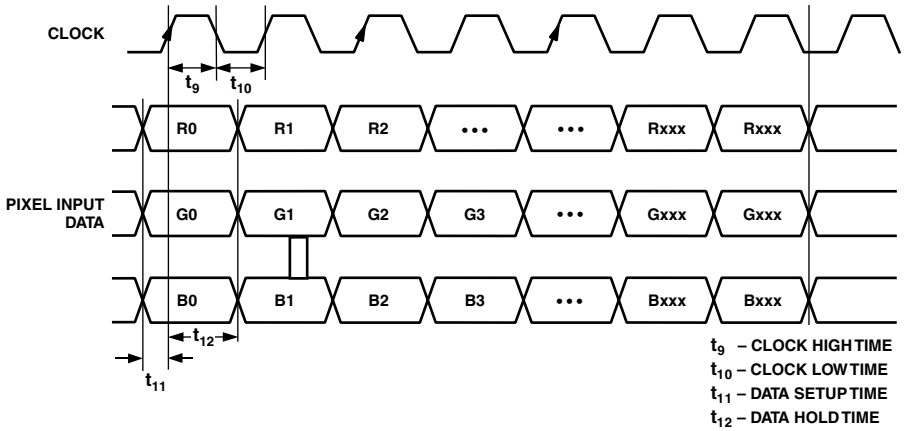


Figure 1. 4:4:4 RGB Input Data Format Timing Diagram

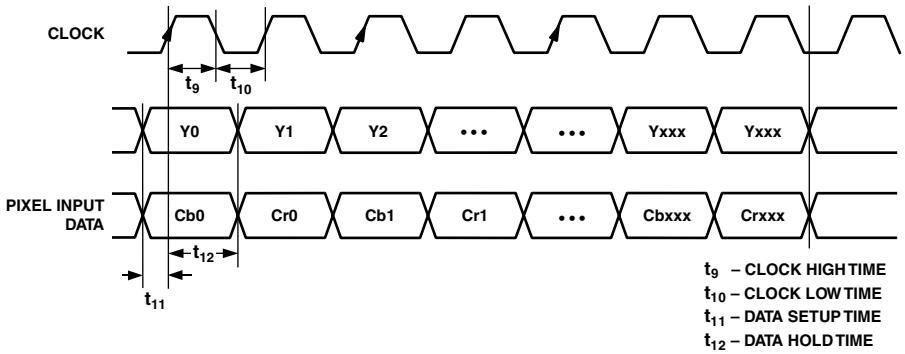


Figure 2. 4:2:2 Input Data Format Timing Diagram

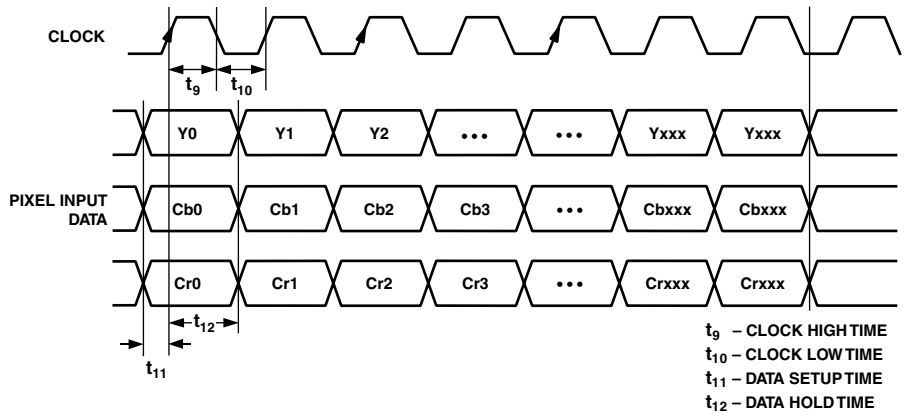


Figure 3. 4:4:4 YCrCb Input Data Format Timing Diagram

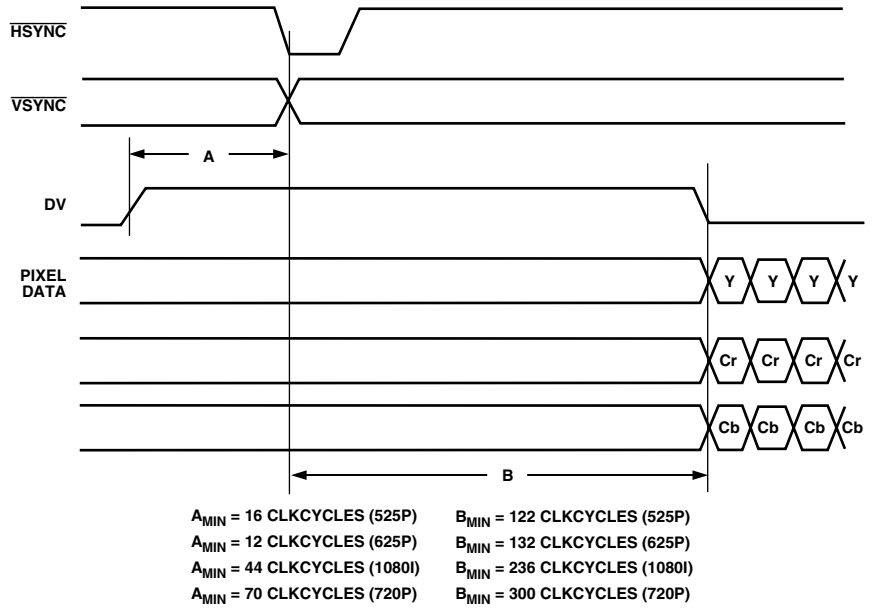


Figure 4. Input Timing Diagram

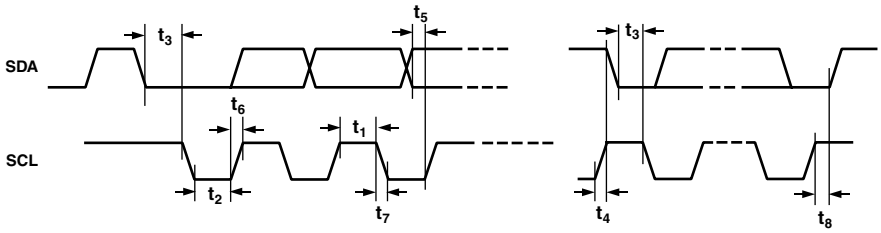


Figure 5. MPU Port Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]

V_{AA} to GND . . . . . 7 V
Voltage on Any Digital Pin . . . . GND – 0.5 V to V_{AA} + 0.5 V
Ambient Operating Temperature (T_A) . . . . . –40°C to +85°C
Storage Temperature (T_S) . . . . . –65°C to +150°C
Infrared Reflow Soldering (20 secs) . . . . . 225°C
Vapor Phase Soldering (1 minute) . . . . . 220°C
I_{OUT} to GND[2] . . . . . 0 V to V_{AA}

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Analog Output Short Circuit to any Power Supply or Common can be of an indefinite duration.

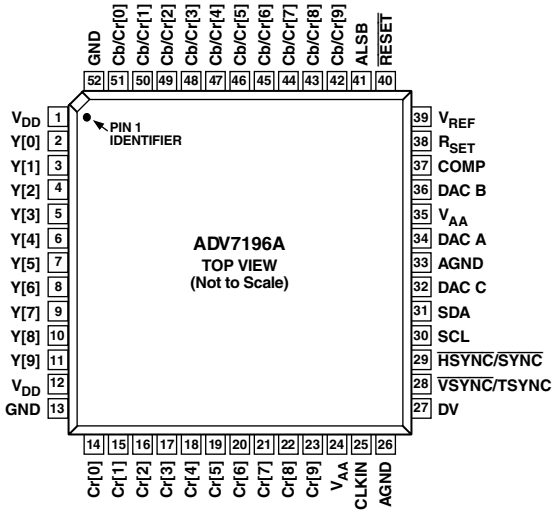
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADV7196AKS	0°C to 70°C	Plastic Quad Flatpack (MQFP)	S-52

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV7196A features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Input/Output	Function
1, 12	V_{DD}	P	Digital Power Supply
2–11	Y0–Y9	I	10-Bit Progressive Scan/HDTV Input Port for Y Data. Input for G data when RGB data is input.
13, 52	GND	G	Digital Ground
14–23	Cr0–Cr9	I	10-Bit Progressive Scan/HDTV Input Port for Color Data in 4:4:4 Input Mode. In 4:2:2 mode this input port is not used. Input port for R data when RGB data is input.
24, 35	V_{AA}	P	Analog Power Supply
25	CLKIN	I	Pixel Clock Input. Requires a 27 MHz reference clock for standard operation in Progressive Scan Mode or a 74.25 MHz (74.1758 MHz) reference clock in HDTV mode.
26, 33	AGND	G	Analog Ground
27	DV	I	Video Blanking Control Signal Input
28	$\overline{\text{VSYNC}}$/ TSYNC	I	$\overline{\text{VSYNC}}$, Vertical Sync Control Signal Input or TSYNC Input Control Signal in Async Timing Mode
29	$\overline{\text{HSYNC}}$/ $\overline{\text{SYNC}}$	I	$\overline{\text{HSYNC}}$, Horizontal Sync Control Signal Input or $\overline{\text{SYNC}}$ Input Control Signal in Async Timing Mode
30	SCL	I	MPU Port Serial Interface Clock Input
31	SDA	I/O	MPU Port Serial Data Input/Output
32	DAC C	O	Color Component Analog Output of Input Data on Cb/Cr9–0 Input Pins
34	DAC A	O	Y Analog Output
36	DAC B	O	Color Component Analog Output of Input Data on Cr9–Cr0 Input Pins
37	COMP	O	Compensation Pin for DACs. Connect 0.1 μF capacitor from COMP pin to V_{AA}.
38	R_{SET}	I	A 2470 Ω resistor (for input ranges 64–940 and 64–960; output standards EIA-770.1–EIA-770.3) must be connected from this pin to ground and is used to control the amplitudes of the DAC outputs. For input ranges 0–1023 (output standards RS-170, RS-343A) the R_{SET} value must be 2820 Ω.
39	V_{REF}	I/O	Optional External Voltage Reference Input for DACs or Voltage Reference Output (1.235 V)
40	$\overline{\text{RESET}}$	I	This input resets the on-chip timing generator and sets the ADV7196A into Default Register setting. Reset is an active low signal.
41	ALSB	I	TTL Address Input. This signal sets up the LSB of the MPU address. When this pin is tied high, the I^2C filter is activated which reduces noise on the I^2C interface. When this pin is tied low, the input bandwidth on the I^2C interface is increased.
42–51	Cb/Cr9–0	I	10-Bit Progressive Scan/HDTV Input Port for Color Data. In 4:2:2 mode the multiplexed CrCb data must be input on these pins. Input port for B data when RGB is input.

FUNCTIONAL DESCRIPTION

Digital Inputs

The digital inputs of the ADV7196A are TTL compatible. 30-bit YCrCb or RGB pixel data in 4:4:4 format or 20-bit YCrCb pixel data in 4:2:2 format is latched into the device on the rising edge of each clock cycle at 74.25 MHz or 74.1758 in HDTV mode. It is also possible to input 3 × 10 bit RGB data in 4:4:4 to the ADV7196A. It is recommended to input data in 4:2:2 mode to make use of the Chroma SSAFs on the ADV7196A. As can be seen in the figure below, this filter has a 0 dB pass band response and prevents signal components being folded back in to the frequency band. In 4:4:4: input mode, the video data is already interpolated by the external input device and the Chroma SSAFs of the ADV7196A are bypassed.

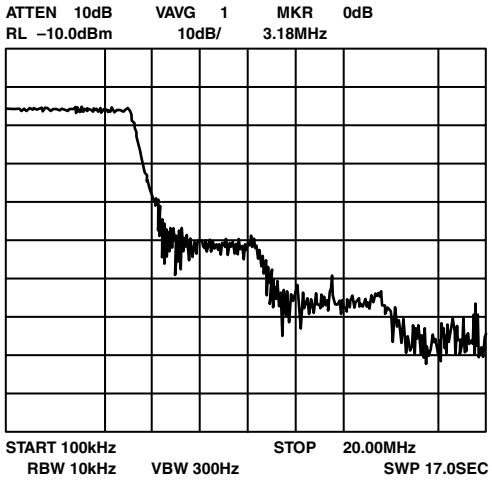


Figure 6. ADV7196A SSAF Response to a 2.5 MHz Chroma Sweep Using 4:2:2 Input Mode

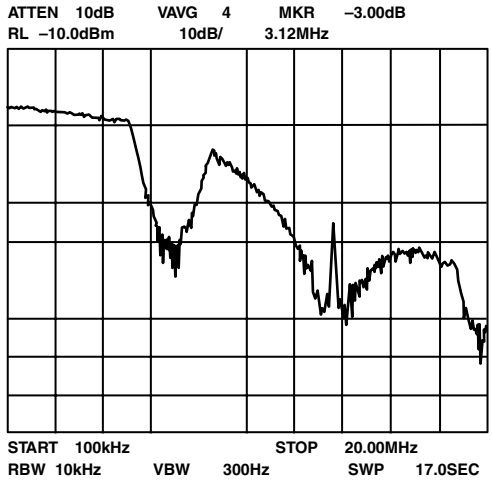


Figure 7. Conventional Filter Response to a 2.5 MHz Chroma Sweep Using 4:4:4 Input Mode

Control Signals

The ADV7196A accepts sync control signals accompanied by valid 4:2:2 or 4:4:4 data. These external horizontal, vertical and blanking pulses (or EAV/SAV codes) control the insertion of appropriate sync information into the output signals.

Analog Outputs

The analog Y signal is output on the 11-Bit + Sync DAC A, the color component analog signals on the 11-Bit DACs B, C conforming to EIA-770.1 or EIA-770.2 standards in PS mode or EIA-770.3 in HDTV mode. R_{SET} has a value of 2470 Ω (EIA-770.1, EIA-770.2, EIA-770.3), R_{LOAD} has a value of 300 Ω. For RGB outputs conforming to RS-170/RS-343A output standards R_{SET} must have a value of 2820 Ω.

I^2C Filters

A selectable internal I^2C filter allows significant noise reduction on the I^2C interface. In setting ALSB high, the input bandwidth on the I^2C lines is reduced and pulses of less than 50 ns are not passed to the I^2C controller. Setting ALSB low allows greater input bandwidth on the I^2C lines.

Undershoot Limiter

A limiter can be applied to the Y data before it is applied to the DACs. Available limit values are –1.5 IRE, –6 IRE, –11 IRE below blanking. This functionality is available in Progressive Scan mode only.

Internal Test Pattern Generator

The ADV7196A can generate a cross-hatch pattern (white lines against a black background). Additionally, the ADV7196A can output a uniform color pattern. The color of the lines or uniform field/frame can be programmed by the user.

Y/CrCb Delay

The Y output and the color component outputs can be delayed wrt the falling edge of the horizontal sync signal by up to four clock cycles.

Gamma Correction

Gamma correction may be performed on the luma data. The user has the choice to use either of two different gamma curves, A or B. At any one time one of these curves is operational if gamma correction is enabled. Gamma correction allows the mapping of the luma data to a user-defined function.

54 MHz Operation

In Progressive Scan mode, it is possible to operate the three output DACs at 54 MHz or 27 MHz. The ADV7196A is supplied with a 27 MHz clock synced with the incoming data. If required, a second stage interpolation filter interpolates the data to 54 MHz before it is applied to the three output DACs. The second stage interpolation filter is controlled by MR36. After applying a Reset it is recommended to toggle this bit. Before toggling this bit, 3Ehex must be written to address 09hex.

PROGRAMMABLE SHARPNESS FILTER

Sharpness Filter Mode is applicable to the Y data only in Progressive Scan mode. The desired frequency response can be chosen by the user in programming the correct value via the I^2C. The variation of frequency responses can be seen in the figures on the following pages.

PROGRAMMABLE ADAPTIVE FILTER CONTROL

If the Adaptive Filter Mode is enabled (Progressive Scan mode only), it is possible to compensate for large edge transitions on the incoming Y data. Sensitivity and attenuation are all programmable over the I^2C. For further information refer to Sharpness Filter Control and Adaptive Filter Control section.

Input/Output Configuration
Table I shows possible input/output configurations when using the ADV7196A.

Table I.

Input Format	Output
YCrCb Progressive Scan	
4:2:2	2×
4:4:4	1× or 2×
YCrCb HDTV	
4:2:2	1×
4:4:4	1×
RGB Progressive Scan	
4:4:4	2×
RGB HDTV	
4:4:4	1×
Async Timing Mode	
All Inputs	1×

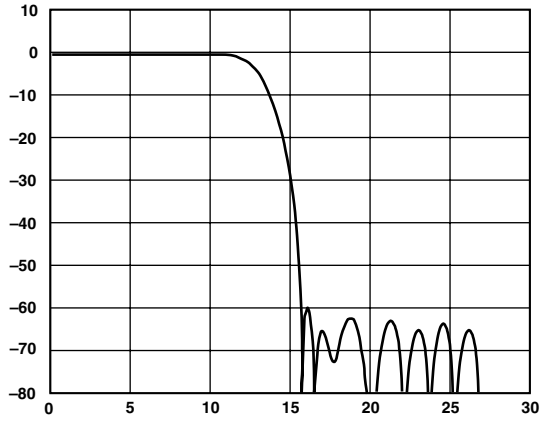


Figure 8. 2× Interpolation Filter – Y-Channel

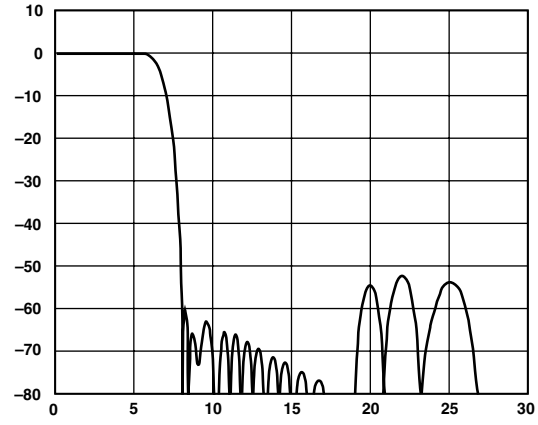


Figure 9. Interpolation Filter – CrCb Channels for 4:2:2 Input Data

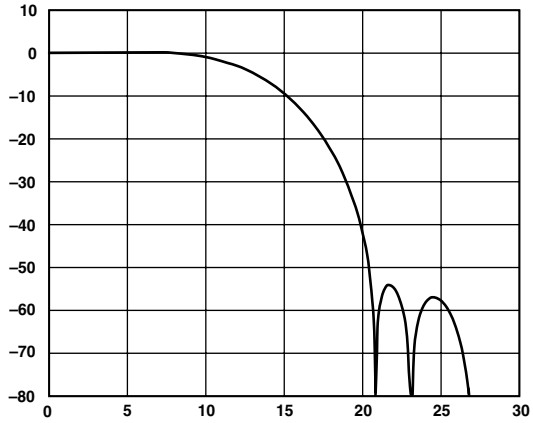


Figure 10. Interpolation Filter – CrCb Channels for 4:4:4 Input Data

MPU PORT DESCRIPTION
The ADV7196A support a 2-wire serial (I^2C-compatible) microprocessor bus driving multiple peripherals. Two inputs, Serial Data (SDA) and Serial Clock (SCL), carry information between any device connected to the bus. Each slave device is recognized by a unique address. The ADV7196A has four possible slave addresses for both read and write operations. These are unique addresses for each device and illustrated in Figure 11. The LSB sets either a read or write operation. Logic Level "1" corresponds to a read operation while Logic Level "0" corresponds to a write operation. A1 is set by setting the ALSB pin of the ADV7196A to Logic Level "0" or Logic Level "1." When ALSB is set to "0," there is greater input bandwidth on the I^2C lines, which allows high-speed data transfers on this bus. When ALSB is set to "1," there is reduced input bandwidth on the I^2C lines, which means that pulses of less than 50 ns will not pass into the I^2C internal controller. This mode is recommended for noisy systems.

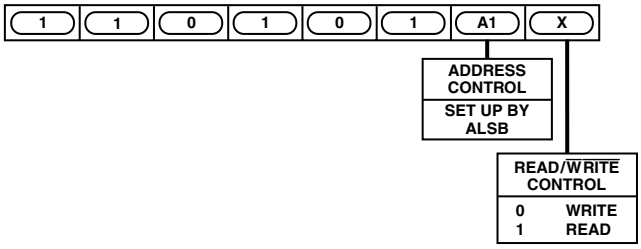


Figure 11. Slave Address

To control the various devices on the bus the following protocol must be followed. First the master initiates a data transfer by establishing a Start condition, defined by a high-to-low transition on SDA while SCL remains high. This indicates that an address/data stream will follow. All peripherals respond to the Start condition and shift the next eight bits (7-bit address + R/$\overline{W}$ bit). The bits are transferred from MSB down to LSB. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition. The idle condition is where the device monitors the SDA and SCL lines waiting for the Start condition and the correct transmitted address. The R/$\overline{W}$ bit determines the direction of the data.

A Logic "0" on the LSB of the first byte means that the master will write information to the peripheral. A Logic "1" on the LSB of the first byte means that the master will read information from the peripheral.

The ADV7196A acts as a standard slave device on the bus. The data on the SDA pin is 8 bits long supporting the 7-bit addresses plus the R/$\overline{W}$ bit. It interprets the first byte as the device address and the second byte as the starting subaddress. The subaddresses autoincrement allowing data to be written to or read from the starting subaddress. A data transfer is always terminated by a Stop condition. The user can also access any unique subaddress register on a one by one basis without having to update all the registers.

Stop and Start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, then these cause an immediate jump to the idle condition. During a given SCL high period the user should only issue one Start condition, one Stop condition or a single Stop condition followed by a single Start condition. If an invalid subaddress is issued by the user, the ADV7196A will not issue an acknowledge and will return to the idle condition. If in autoincrement mode, the user exceeds the highest subaddress then the following action will be taken:

1. In Read Mode, the highest subaddress register contents will continue to be output until the master device issues a no-acknowledge. This indicates the end of a read. A no-acknowledge condition is where the SDA line is not pulled low on the ninth pulse.
2. In Write Mode, the data for the invalid byte will be not be loaded into any subaddress register, a no-acknowledge will be issued by the ADV7196A and the part will return to the idle condition.

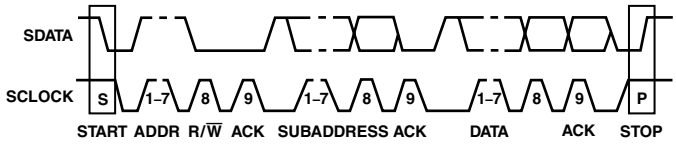


Figure 12. Bus Data Transfer

Figure 12 illustrates an example of data transfer for a read sequence and the Start and Stop conditions.

Figure 13 shows bus write and read sequences.

REGISTER ACCESSES

The MPU can write to or read from all of the registers of the ADV7196A except the Subaddress Registers, which are write-only registers. The Subaddress Register determines which register the next read or write operation accesses.

All communications with the part through the bus begin with an access to the Subaddress Register. A read/write operation is performed from/to the target address which then increments to the next address until a Stop command on the bus is performed.

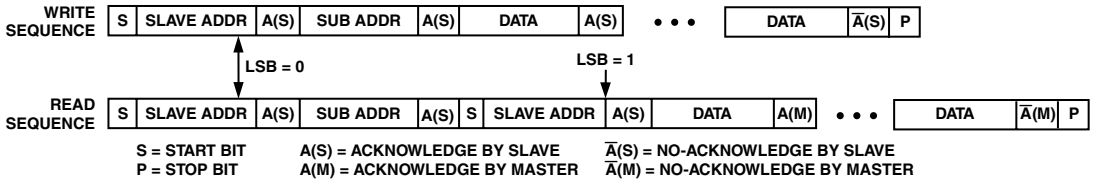


Figure 13. Write and Read Sequence

REGISTER PROGRAMMING

The following section describes the functionality of each register. All registers can be read from as well as written to unless otherwise stated.

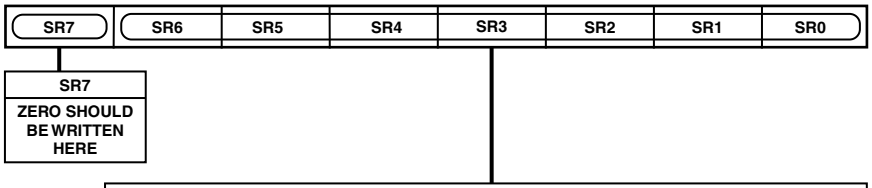
Subaddress Register (SR7–SR0)

The Communications Register is an eight bit write-only register. After the part has been accessed over the bus and a read/write operation is selected, the subaddress is set up. The Subaddress Register determines to/from which register the operation takes place.

Figure 14 shows the various operations under the control of the Subaddress Register. "0" should always be written to SR7.

Register Select (SR6–SR0)

These bits are set up to point to the required starting address.



ADV7196A SUBADDRESS REGISTER

ADDRESS	SR6	SR5	SR4	SR3	SR2	SR1	SR0	
00h	0	0	0	0	0	0	0	MODE REGISTER 0
01h	0	0	0	0	0	0	1	MODE REGISTER 1
02h	0	0	0	0	0	1	0	MODE REGISTER 2
03h	0	0	0	0	0	1	1	MODE REGISTER 3
04h	0	0	0	0	1	0	0	MODE REGISTER 4
05h	0	0	0	0	1	0	1	MODE REGISTER 5
06h	0	0	0	0	1	1	0	COLOR Y
07h	0	0	0	0	1	1	1	COLOR CR
08h	0	0	0	1	0	0	0	COLOR CB
09h	0	0	0	1	0	0	1	MODE REGISTER 6
0Ah	0	0	0	1	0	1	0	RESERVED
0Bh	0	0	0	1	0	1	1	RESERVED
0Ch	0	0	0	1	1	0	0	RESERVED
0Eh	0	0	0	1	1	1	0	RESERVED
0Fh	0	0	0	1	1	1	1	RESERVED
10h	0	0	1	0	0	0	0	FILTER GAIN
11h	0	0	1	0	0	0	1	CGMS DATA REGISTER 0
12h	0	0	1	0	0	1	0	CGMS DATA REGISTER 1
13h	0	0	1	0	0	1	1	CGMS DATA REGISTER 2
14h	0	0	1	0	1	0	0	GAMMA CORRECTION REGISTER 0
15h	0	0	1	0	1	0	1	GAMMA CORRECTION REGISTER 1
16h	0	0	1	0	1	1	0	GAMMA CORRECTION REGISTER 2
17h	0	0	1	0	1	1	1	GAMMA CORRECTION REGISTER 3
18h	0	0	1	1	0	0	0	GAMMA CORRECTION REGISTER 4
19h	0	0	1	1	0	0	1	GAMMA CORRECTION REGISTER 5
1Ah	0	0	1	1	0	1	0	GAMMA CORRECTION REGISTER 6
1Bh	0	0	1	1	0	1	1	GAMMA CORRECTION REGISTER 7
1Ch	0	0	1	1	1	0	0	GAMMA CORRECTION REGISTER 8
1Dh	0	0	1	1	1	0	1	GAMMA CORRECTION REGISTER 9
1Eh	0	0	1	1	1	1	0	GAMMA CORRECTION REGISTER 10
1Fh	0	0	1	1	1	1	1	GAMMA CORRECTION REGISTER 11
20h	0	1	0	0	0	0	0	GAMMA CORRECTION REGISTER 12
21h	0	1	0	0	0	0	1	GAMMA CORRECTION REGISTER 13
22h	0	1	0	0	0	1	0	ADAPTIVE FILTER GAIN 1
23h	0	1	0	0	0	1	1	ADAPTIVE FILTER GAIN 2
24h	0	1	0	0	1	0	0	ADAPTIVE FILTER GAIN 3
25h	0	1	0	0	1	0	1	ADAPTIVE FILTER THRESHOLD A
26h	0	1	0	0	1	1	0	ADAPTIVE FILTER THRESHOLD B
27h	0	1	0	0	1	1	1	ADAPTIVE FILTER THRESHOLD C

Figure 14. Subaddress Registers in Progressive Scan Mode

ADV7196A SUBADDRESS REGISTER

ADDRESS	SR6	SR5	SR4	SR3	SR2	SR1	SR0	
00h	0	0	0	0	0	0	0	MODE REGISTER 0
01h	0	0	0	0	0	0	1	MODE REGISTER 1
02h	0	0	0	0	0	1	0	MODE REGISTER 2
03h	0	0	0	0	0	1	1	MODE REGISTER 3
04h	0	0	0	0	1	0	0	MODE REGISTER 4
05h	0	0	0	0	1	0	1	MODE REGISTER 5
06h	0	0	0	0	1	1	0	COLOR Y
07h	0	0	0	0	1	1	1	COLOR CR
08h	0	0	0	1	0	0	0	COLOR CB

Figure 15. Subaddress Registers in HDTV Mode

PROGRESSIVE SCAN MODE

MODE REGISTER 0

MR0 (MR07–MR00)
(Address (SR4–SR0) = 00H)
Figure 16 shows the various operations under the control of Mode Register 0.

MR0 BIT DESCRIPTION

Output Standard Selection (MR00–MR01)
These bits are used to select the output levels for the ADV7196A.

If EIA-770.2 (MR01–00 = "00") is selected the output levels will be: 0 mV for blanking level, 700 mV for peak white for the Y channel, ±350 mV for Pr, Pb outputs and –300 mV for Sync. Sync insertion on the Pr, Pb channels is optional.

If EIA-770.1 (MR01–00 = "01") is selected the output levels will be: 0 mV for blanking level, 714 mV for peak white for the Y channel, ±350 mV for Pr, Pb outputs and –286 mV for Sync. Optional sync insertion on the Pr, Pb channels is not possible.

If Full I/P Range (MR01–00 = "10") is selected the output levels will be 0 mV for blanking level, 700 mV for peak white for the Y channel, ±350 mV for Pr, Pb outputs and –300 mV for Sync. Sync insertion on the Pr, Pb channels is optional. This mode is used for RS-170, RS-343A standard output compatibility. Refer to Appendix for output level plots.

Input Control Signals (MR02–MR03)
These control bits are used to select whether data is input with external horizontal, vertical and blanking sync signals or if the data is input with embedded EAV/SAV codes.

An Asynchronous timing mode is also available using TSYNC, $\overline{\text{SYNC}}$ and DV as input control signals. These control signals have to be programmed by the user.

Figure 17 shows an example of how to program the ADV7196A to accept a different high definition standard but SMPTE293M, SMPTE274M, SMPTE296M or ITU-R.BT1358 standard.

Input Standard (MR04)
Select between 525p progressive scan input or 625p progressive scan input.

Reserved (MR05)
A "0" must be written to this bit.

DV Polarity (MR06)
This control bit allows to select the polarity of the DV input control signal to be either active high or active low. This is in order to facilitate interfacing from I to P Converters which use an active low blanking signal output.

Macrovision (MR07)
To enable Macrovision this bit must be set to "1."

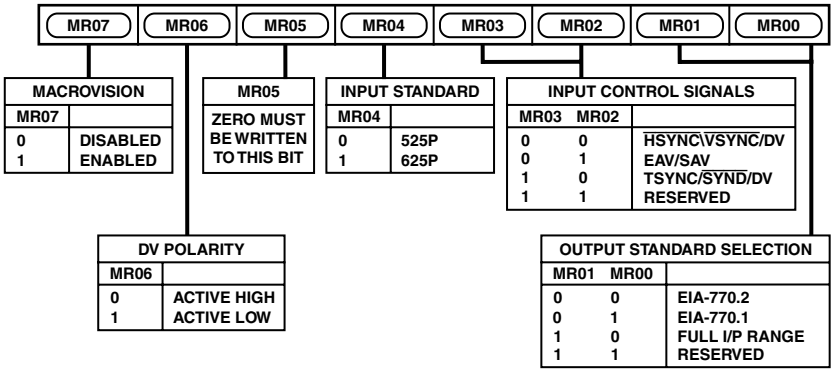


Figure 16. Mode Register 0

Table II must be followed when programming the control signals in Async Timing Mode.

Table II. Truth Table

$\overline{\text{SYNC}}$	TSYNC	DV	
1 –> 0	0	0 or 1	50% Point of Falling Edge of Tri-Level Horizontal Sync Signal, A
0	0 –> 1	0 or 1	25% Point of Rising Edge of Tri-Level Horizontal Sync Signal, B
0 –> 1	0 or 1	0	50% Point of Falling Edge of Tri-Level Horizontal Sync Signal, C
1	0 or 1	0 –> 1	50% Start of Active Video, D
1	0 or 1	1 –> 0	50% End of Active Video, E

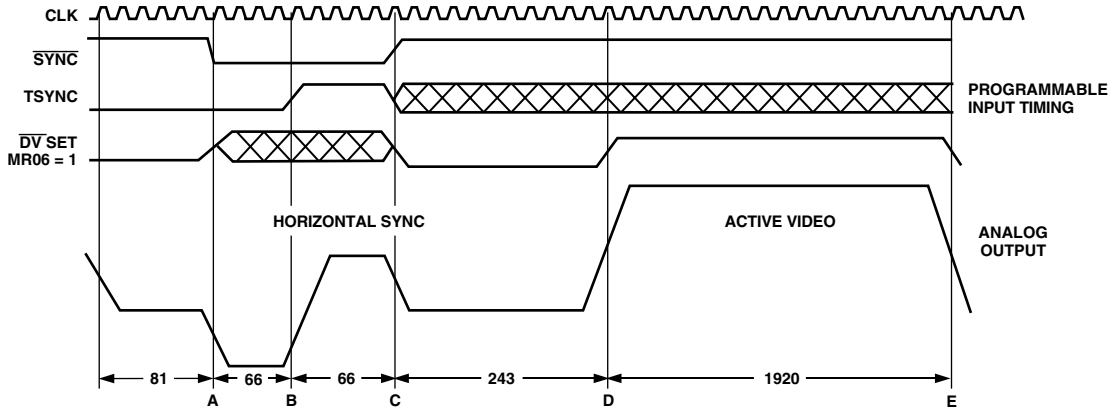


Figure 17. Async Timing Mode—Programming Input Control Signals for SMPTE295M Compatibility

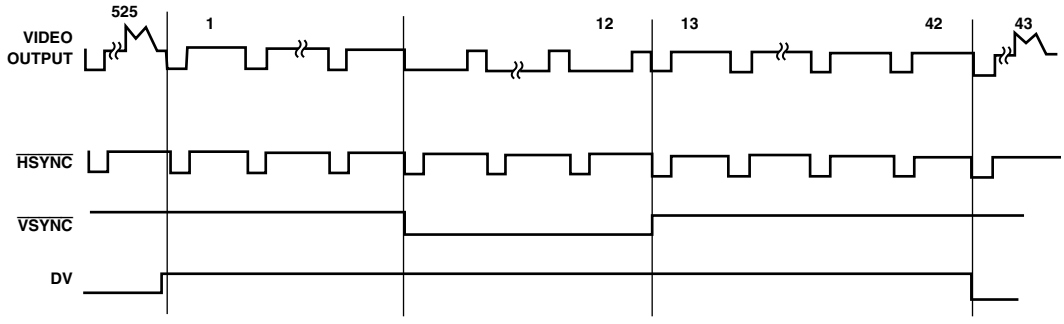


Figure 18. DV Input Control Signal in Relation to Video Output Signal

MODE REGISTER 1
MR1 (MR17–MR10)
(Address (SR4–SR0) = 01H)
Figure 20 shows the various operations under the control of Mode Register 1.

MR1 BIT DESCRIPTION
Pixel Data Enable (MR10)
When this bit is set to "0," the pixel data input to the ADV7196A is blanked such that a black screen is output from the DACs. When this bit is set to "1," pixel data is accepted at the input pins and the ADV7196A outputs the standard set in "Output Standard Selection" (MR01–00). This bit must be set to "1" to enable output of the test pattern signals.

Input Format (MR11)
It is possible to input data in 4:2:2 format or at 4:4:4 format at 27 MHz.

Test Pattern Enable (MR12)
Enables or disables the internal test pattern generator.

Test Pattern Hatch/Frame (MR13)
If this bit is set to "0," a cross-hatch test pattern is output from the ADV7196A (for example, in SMPTE293M 11 horizontal and 11 vertical white lines, four pixels wide are displayed against a black background). The cross-hatch test pattern can be used to test monitor convergence.

If this bit is set to "1," a uniform colored frame/field test pattern is output from the ADV7196A.

The color of the lines or the frame/field is by default white but can be programmed to be any color using the Color Y, Color Cr, Color Cb registers.

VBI Open (MR14)
This bit enables or disables the facility of VBI data insertion during the Vertical Blanking Interval.

For this purpose Lines 13 to 42 of each frame can be used for VBI when SMPTE293M standard is used, or Lines 6 to 43 when ITU-R.BT1358 standard is used.

Undershoot Limiter (MR15–MR16)
This control limits the Y signal to a programmable level in the active video region.

Available limit levels are –1.5 IRE, –6 IRE, –11 IRE.

Note that this facility is only available when Interpolation is enabled (MR36 = "1").

Sharpness Filter (MR17)
This control bit enables or disables the Sharpness Filter mode. This bit must be set to "1" for any values programmed into the Filter Gain 1 Register to take effect. It must also be set to "1" when Adaptive Filter mode is used.

Refer to Sharpness Filter control and Adaptive Filter control section.

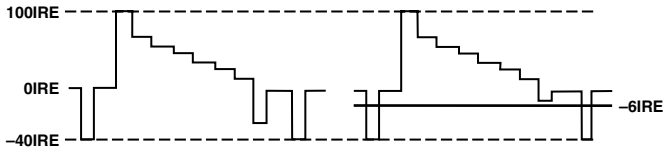


Figure 19. Undershoot Limiter, Programmed to –6 IRE

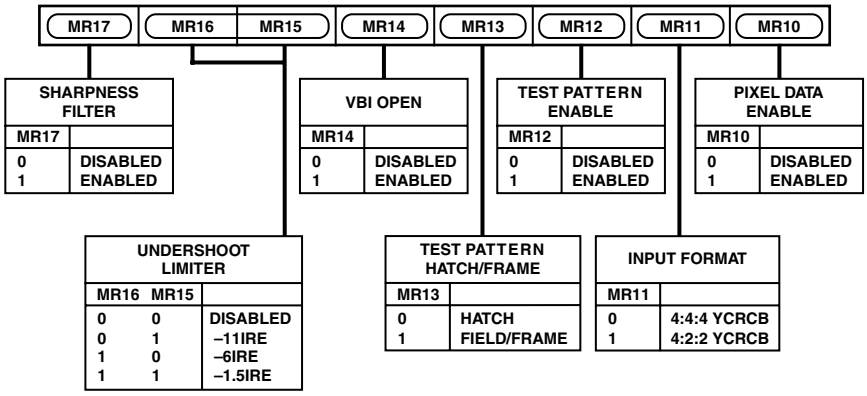


Figure 20. Mode Register 1

MODE REGISTER 2
MR1 (MR27–MR20)
(Address (SR4–SR0) = 02H)
Figure 22 shows the various operations under the control of Mode Register 2.

MR2 BIT DESCRIPTION
Y Delay (MR20–MR22)
This control bit delays the Y signal with respect to the falling edge of the horizontal sync signal by up to four pixel clock cycles. Figure 21 demonstrates this facility.

Color Delay (MR23–MR25)
This control allows delay of the color signals with respect to the falling edge of the horizontal sync signal by up to four pixel clock cycles. Figure 21 demonstrates this facility.

CGMS Enable (MR26)
When this bit is set to "1," CGMS data is inserted on Line 41 in 525p mode. The CGMS conforms: to CGMS-A EIA-J CPR1204-1, Transfer Method of Video ID information using vertical blanking interval (525p System), March 1998 and IEC61880, 1998, video systems (525/60)—video and accompanied data using the vertical blanking interval—analogue interface.

The CGMS data bits are programmed into the CGMS Data Registers 0–2. For more information refer to CGMS Data Registers section.

CGMS CRC (MR27)
This bit enables the automatic Cyclic Redundancy Check when CGMS is enabled.

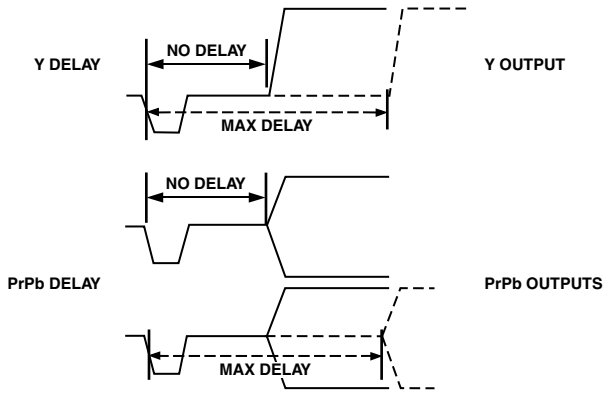


Figure 21. Y and Color Delay

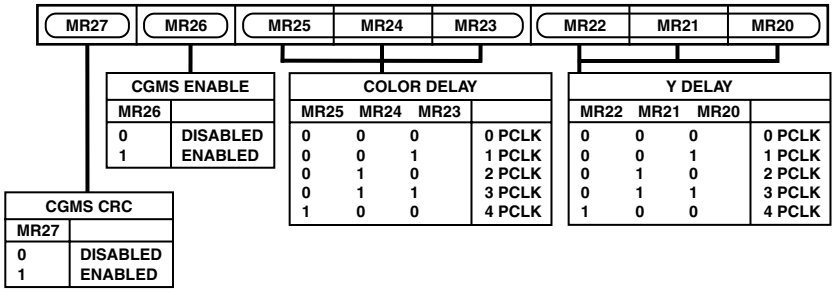


Figure 22. Mode Register 2

MODE REGISTER 3
MR3 (MR37–MR30)
(Address (SR4–SR0) = 03H)
Figure 23 shows the various operations under the control of Mode Register 3.

MR3 BIT DESCRIPTION
HDTV Enable (MR30)
When this bit is set to "1" the ADV7196A reverts to HDTV mode (refer to HDTV mode section). When set to "0" the ADV7196A is set up in Progressive Scan Mode (PS Mode).

Reserved (MR31–MR32)
A "0" must be written to these bits.

DAC A Control (MR33)
Setting this bit to "1" enables DAC A, otherwise this DAC is powered down.

DAC B Control (MR34)
Setting this bit to "1" enables DAC B, otherwise this DAC is powered down.

DAC C Control (MR35)
Setting this bit to "1" enables DAC C, otherwise this DAC is powered down.

Interpolation (MR36)
This bit enables the second stage interpolation filters. When this bit is enabled (MR36 = "1"). data is send at 54 MHz to the DAC output stage. After Reset it is recommended to toggle this bit. Before toggling this bit 3Ehex must be written to address 09hex to guarantee correct operations.

Reserved (MR37)
A zero must be written to this bit.

MODE REGISTER 4
MR4 (MR47–MR40)
(Address (SR4–SR0) = 04H)
Figure 24 shows the various operations under the control of Mode Register 4.

MR4 BIT DESCRIPTION
Timing Reset (MR40)
Toggling MR40 from low to high and low again resets the internal horizontal and vertical timing counters.

MODE REGISTER 5
MR5 (MR57–MR50)
(Address (SR4–SR0) = 05H)
Figure 25 shows the various operations under the control of Mode Register 5.

MR5 BIT DESCRIPTION
Reserved (MR50)
This bit is reserved for the revision code.

RGB Mode (MR51)
When RGB mode is enabled (MR51 = "1") the ADV7196A accepts unsigned binary RGB data at its input port. This control is also available in Async Timing Mode.

Sync on PrPb (MR52)
By default the color component output signals Pr, Pb do not contain any horizontal sync pulses. They can be inserted when MR52 = "1." This facility is only available when Output Standard Selection has been set to EIA-770.2 (MR01–00 = "00") or Full Input Range (MR01–00 = "10").

This control is not available in RGB mode.

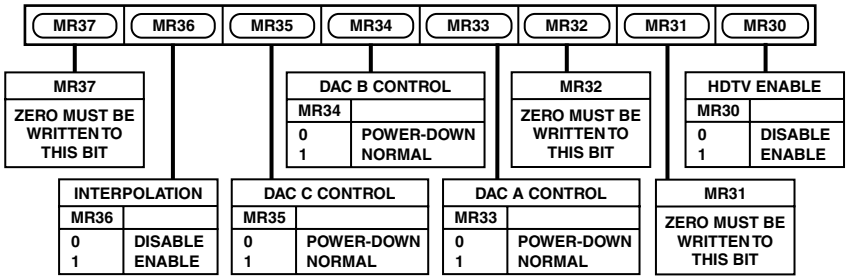


Figure 23. Mode Register 3

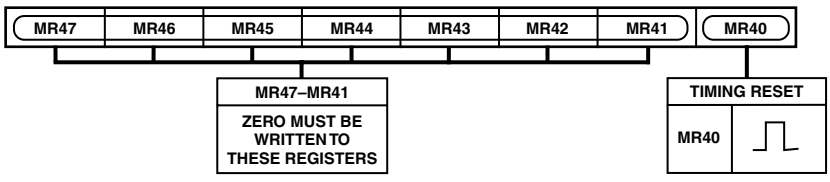


Figure 24. Model Register 4

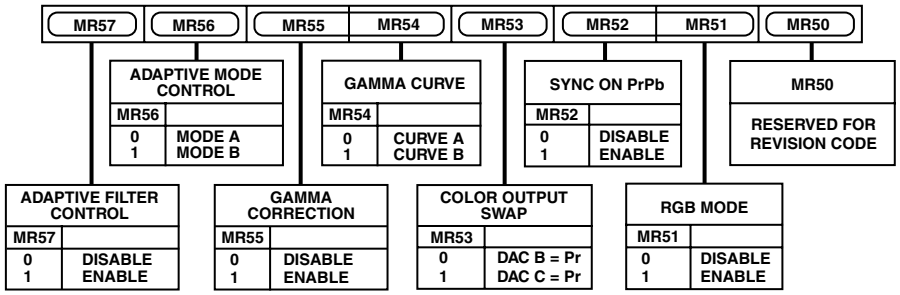


Figure 25. Mode Register 5

Color Output Swap (MR53)
By default DAC B is configured as the Pr output and DAC C as the Pb output. In setting this bit to "1" the DAC outputs can be swapped around so that DAC B outputs Pb and DAC C outputs Pr. Table III demonstrates this in more detail. This control is also available in RGB mode.

Table III. Relationship Between Color Input Pixel Port, MR53 and DAC B, DAC C Outputs

In 4:4:4 Input Mode

Color Data Input on Pins	MR53	Analog Output Signal
Cr9–0	0	DAC B
Cb/Cr9–0	0	DAC C
Cr9–0	1	DAC C
Cb/Cr9–0	1	DAC B

In 4:2:2 Input Mode

Color Data Input on Pins	MR53	Analog Output Signal
Cr9–0	0 or 1	Not Operational
Cb/Cr9–0	0	DAC C (Pb)
Cb/Cr9–0	1	DAC C (Pr)

Gamma Curve (MR54)
This bit selects which of the two programmable gamma curves is to be used. When setting MR54 to "0," the gamma correction curve selected is Curve A. Otherwise Curve B is selected. Each curve will have to be programmed by the user as explained in the Gamma Correction Registers section.

Gamma Correction (MR55)
To enable Gamma Correction and therefore activate the gamma curve programmed by the user, this bit must be set to "1." Otherwise the programmable Gamma Correction facility is bypassed. Programming of the gamma correction curves is explained in the Gamma Correction Registers section.

Adaptive Mode Control (MR56)
For this control to be effective, Adaptive Filter Control must be enabled (MR57 = "1") as well as the Sharpness Filter (MR17 = "1"). For filter plots refer to Sharpness Filter Control and Adaptive Filter Control section.

Adaptive Filter Control (MR57)
This bit enables the Adaptive Filter Control when set to "1." Sharpness Filter must be enabled as well (MR17 = "1"). The Adaptive Filter Controls is explained in more detail under Sharpness Filter Control and Adaptive Filter Control section.

COLOR Y
CY (CY7–CY0)
(Address (SR4–SR0) = 06H

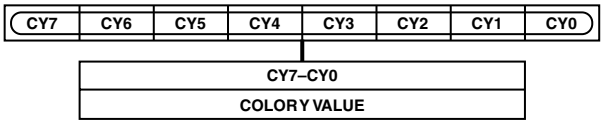


Figure 26. Color Y Register

COLOR CR
CCR (CCR7–CCR0)
(Address (SR4–SR0) = 07H

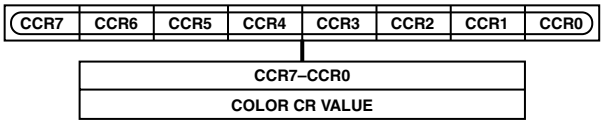


Figure 27. Color Cr Register

COLOR CB
CCB (CCB7–CCB0)
(Address (SR4–SR0) = 08H)

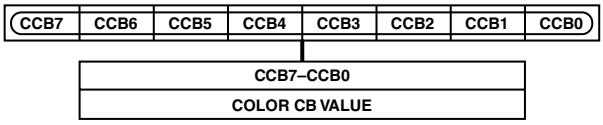


Figure 28. Color Cb Register

These three 8-bit-wide registers are used to program the output color of the internal test pattern generator, be it the lines of the cross-hatch pattern or the uniform field test pattern and are available in PS mode and HDTV mode.

The standard used for the values for Y and the color difference signals to obtain white, black and the saturated primary and complementary colors conforms to the ITU-R BT 601-4 standard.

The Table IV shows sample color values to be programmed into the color registers when Output Standard Selection is set to EIA-770.2 (MR01–00 = "00").

Table IV. Sample Color Values for EIA 770.2 Output Standard Selection

Sample Color	Color Y Value	Color Cr Value	Color Cb Value
White	235 (EB)	128 (80)	128 (80)
Black	16 (10)	128 (80)	128 (80)
Red	81 (51)	240 (F0)	90 (5A)
Green	145 (91)	34 (22)	54 (36)
Blue	41 (29)	110 (6E)	240 (F0)
Yellow	210 (D2)	146 (92)	16 (10)
Cyan	170 (AA)	16 (10)	166 (A6)
Magenta	106 (6A)	222 (DE)	202 (CA)

MODE REGISTER 6
MR6 (MR67–MR60)
(Address (SR4–SR0) = 09H)
Figure 29 shows the various operations under the control of Mode Register 6.

MR6 BIT DESCRIPTION
MR67–MR60
The value 3Ehex must be written to this register before the PLL is reset (reset MR36) to guarantee correct operation of the ADV7196A.

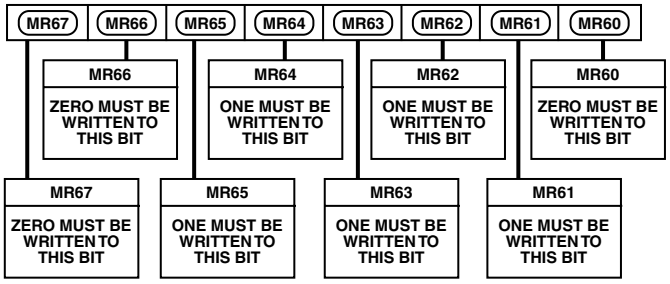


Figure 29. Mode Register 6

CGMS DATA REGISTERS 2–0
CGMS2 (CGMS27–CGMS20)
(Address (SR4–SR0) = 13H)
This 8-bit-wide register contains the last four CGMS data bits, (C16–C19) of the CGMS data stream.

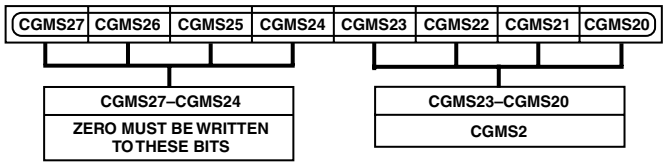


Figure 30. CGMS2 Data Register

CGMS1 (CGMS17–CGMS10)
(Address (SR4–SR0) = 12H)
This 8-bit-wide register contains (C8–C15) of the CGMS data stream.

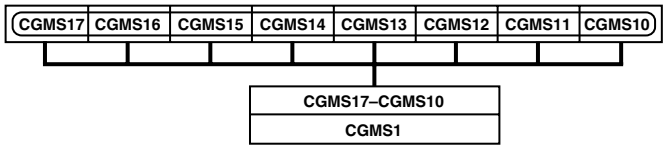


Figure 31. CGMS1 Data Register

CGMS0 (CGMS07–CGMS00)
(Address (SR4–SR0) = 11H)
This 8-bit-wide register contains the first eight CGMS data bits, (C0–C7) of the CGMS data stream.

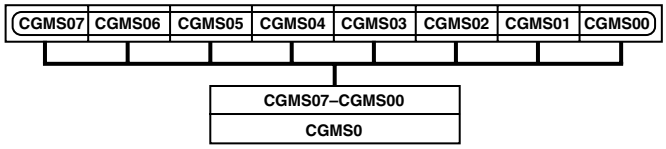


Figure 32. CGMS0 Data Register

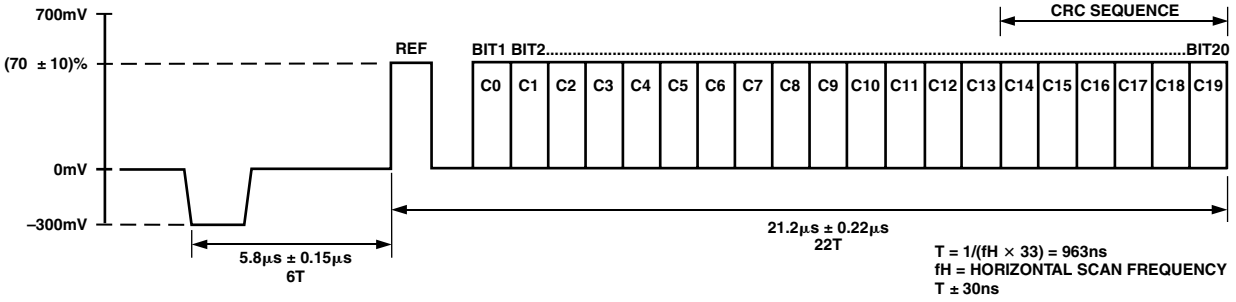
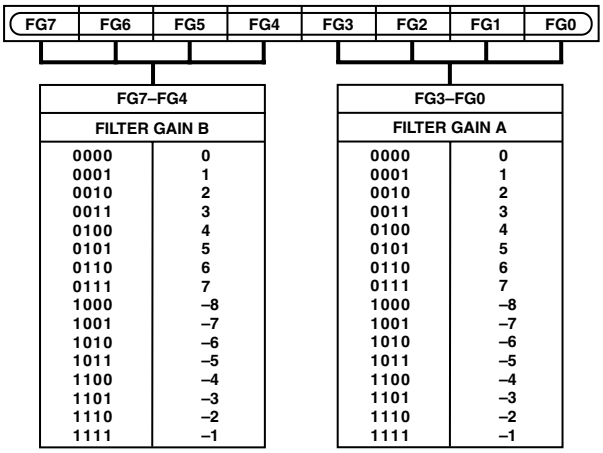


Figure 33. CGMS Waveform

FILTER GAIN
FG (FG7–FG0)
(Address (SR4–SR0) = 10H)
Figure 34 shows the various operations under the control of the Filter Gain register.



FG7–FG4	
FILTER GAIN B	
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	–8
1001	–7
1010	–6
1011	–5
1100	–4
1101	–3
1110	–2
1111	–1

FG3–FG0	
FILTER GAIN A	
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	–8
1001	–7
1010	–6
1011	–5
1100	–4
1101	–3
1110	–2
1111	–1

Figure 34. Filter Gain Register

FG BIT DESCRIPTION
Filter Gain A (FG3–FG0)
These bits are used to program the gain A value, which varies from response –8 to response +7 and are applied to Filter A.

Filter Gain B (FG4–FG7)
These bits are used to program the gain B value, which varies from response –8 to response +7 and are applied to Filter B.

Refer to Sharpness Filter Control and Adaptive Filter Control section for more detail.

GAMMA CORRECTION REGISTERS 0–13
(GAMMA CORRECTION 0–13)
(Address (SR5–SR0) = 14H–21H)
The Gamma Correction Registers are fourteen 8-bit-wide register. They are used to program the gamma correction Curves A and B.

Generally, gamma correction is applied to compensate for the nonlinear relationship between signal input and brightness level output (as perceived on the CRT). It can also be applied wherever nonlinear processing is used.

Gamma correction uses the function:

$$Signal_{OUT} = (Signal_{IN})\,\gamma$$

where γ = gamma power factor.

Gamma correction is performed on the luma data only.

The user has the choice to use two different curves, Curve A or Curve B. At any one time only one of these curves can be used.

The response of the curve is programmed at seven predefined locations. In changing the values at these locations the gamma curve can be modified. Between these points linear interpolation is used to generate intermediate values. Considering the curve to have a total length of 256 points, the seven locations are at: 32, 64, 96, 128, 160, 192, 224.

Location 0, 16, 240, and 255 are fixed and can not be changed.

For the length of 16 to 240 the gamma correction curve has to be calculated as below:

$$y = x^{\gamma}$$

where:

y = gamma corrected output.
x = linear input signal.
γ = gamma power factor.

To program the gamma correction registers, the seven values for y have to be calculated using the following formula:

$$y_n = [_{x(n-16)}/(240 - 16)]^{\gamma} \times (240) - 16) + 16$$

where:

$x_{(n-16)}$ = Value for x along x-axis at points:
n = 32, 64, 96, 128, 160, 192, or 224.
y_n = Value for y along the y-axis, which has to be written into the gamma correction register.

Example:

y_{32} = $[(16/22^{4)0}.5 \times 2\ 24] + 16 = 76$*
y_{64} = $[(48/22^{4)0}.5 \times 224] + 16 = 120$*
y_{96} = $[(80/22^{4)0}.5 \times 224] + 16 = 150$*
y_{128} = $[(112/22^{4)0}.5 \times 224] + 16 = 147$*

*Rounded to the nearest integer.

The above will result in a gamma curve shown below, assuming a ramp signal as an input.

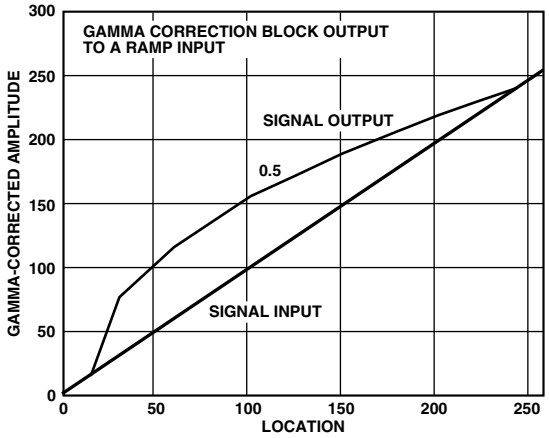


Figure 35. Signal Input (Ramp) and Signal Output for Gamma 0.5

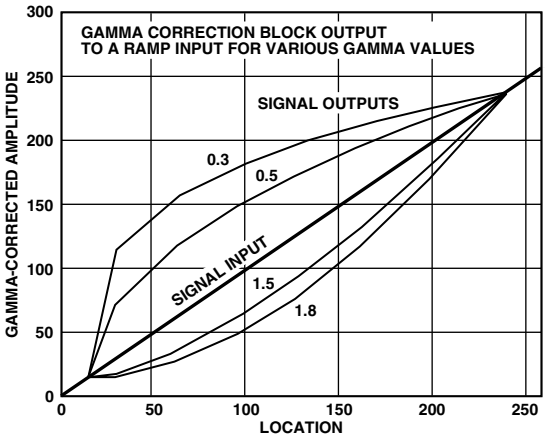


Figure 36. Signal Input (Ramp) and Selectable Gamma Output Curves

The gamma curves shown above are examples only, any user defined curve is acceptable in the range of 16–240.

SHARPNESS FILTER CONTROL AND ADAPTIVE FILTER CONTROL

There are three Filter modes available on the ADV7196A: one Sharpness Filter mode and two Adaptive Filter modes.

SHARPNESS FILTER MODE

To enhance or attenuate the Y signal in the frequency ranges shown in Figure 37, the following register settings must be used:

Sharpness Filter must be enabled (MR17 = "1") and Adaptive Filter Control must be disabled (MR57 = "0").

To select one of the 256 individual responses, the according gain values for each filter, which range from –8 to +7, must be programmed into the Filter Gain register.

ADAPTIVE FILTER MODE

The Adaptive Filter Threshold A, B, C registers, the Adaptive Filter Gain 1, 2, 3 registers and the Filter Gain register are used in Adaptive Filter mode. To activate the Adaptive Filter control, Sharpness Filter must be enabled (MR17 = "1") and Adaptive Filter Control must be enabled (MR57 = "1").

The derivative of the incoming signal is compared to the three programmable threshold values: Adaptive Filter Threshold A, B, C.

The edges can then be attenuated with the settings in Adaptive Filter Gain 1, 2, 3 registers and Filter Gain register.

According to the settings of the Adaptive Mode control (MR56), there are two Adaptive Filter Modes available:

1. Mode A: is used when Adaptive Filter Mode (MR56) is set to "0." In this case, Filter B (LPF) will be used in the adaptive filter block. Also, only the programmed values for Gain B in the Filter Gain, Adaptive Filter Gain 1, 2, 3 are applied when needed. The Gain A values are fixed and can not be changed.
2. Mode B: is used when Adaptive Filter Mode (MR56) is set to "1." In this mode a cascade of Filter A and Filter B is used. Both settings for Gain A and Gain B in the Filter Gain, Adaptive Filter Gain 1, 2, 3 become active when needed.

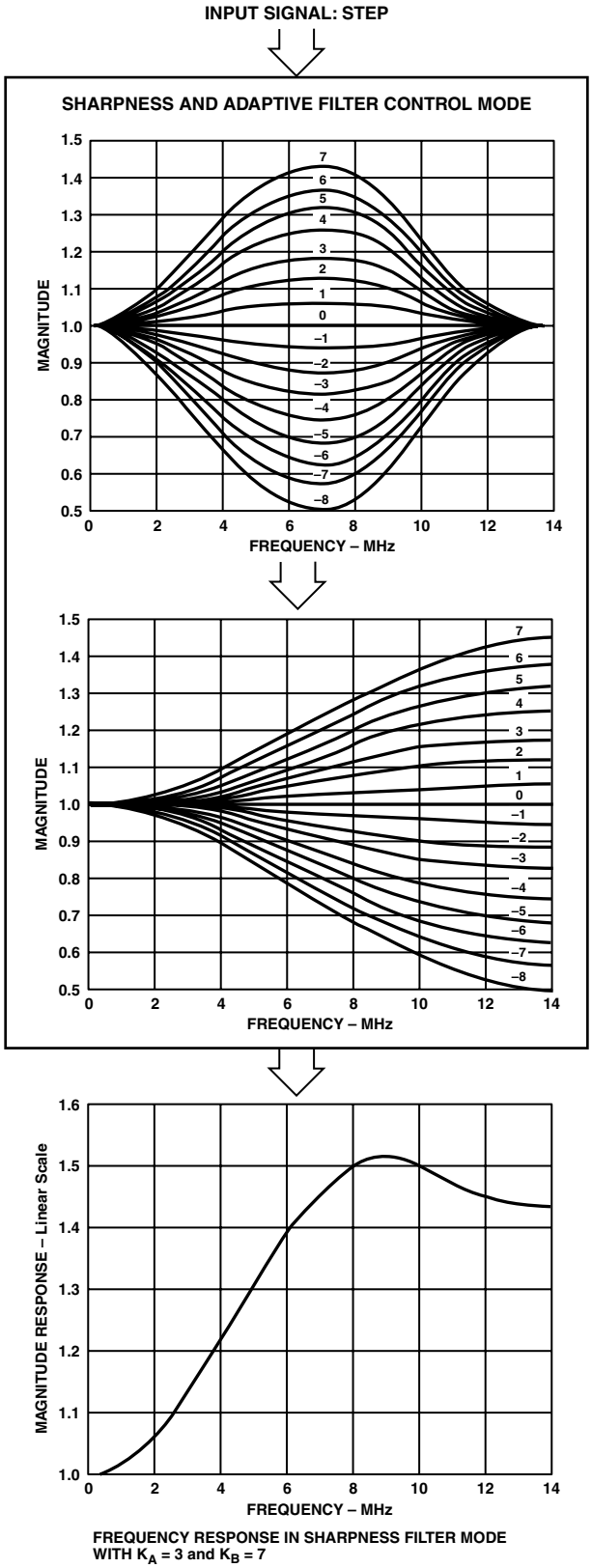


Figure 37. Sharpness and Adaptive Filter Control Mode

ADAPTIVE FILTER GAIN 1
AFG1 (AFG1)7–0
(Address (SR5–SR0) = 22H)
This 8-bit-wide register is used to program the gain applied to signals which lie above Adaptive Filter Threshold A but are smaller than Adaptive Filter Threshold B.

Gain A and Gain B values vary from –8 to +7. The individual responses are shown in the figures below.

Settings for (AFG1)3–0 have no effect unless Adaptive Mode Control is set to Mode B (MR56 = "1").

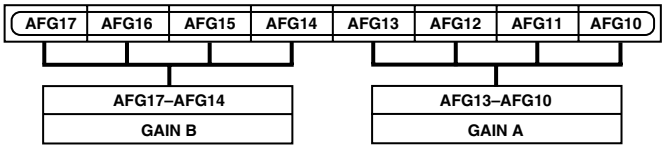


Figure 38. Adaptive Filter Gain 1 Register

ADAPTIVE FILTER GAIN 2
AFG2 (AFG2)7–0
(Address (SR5–SR0) = 23H)
This 8-bit-wide register is used to program the gain applied to signals which lie above Adaptive Filter Threshold B but are smaller than Adaptive Filter Threshold C.

Gain A and Gain B values vary from –8 to +7. The individual responses are shown in the figures below.

Settings for (AFG2)3–0 have no effect unless Adaptive Mode Control is set to Mode B (MR56 = "1").

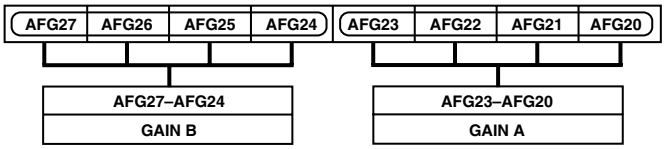


Figure 39. Adaptive Filter Gain 2 Register

ADAPTIVE FILTER GAIN 3
AFG3 (AFG3)7–0
(Address (SR5–SR0) = 24H)
This 8-bit-wide register is used to program the gain applied to signals which lie above Adaptive Filter Threshold C

Gain A and Gain B values vary from –8 to +7. The individual responses are shown in the figures below.

Settings for (AFG3)3–0 have no effect unless Adaptive Mode Control is set to Mode B (MR56 = "1").

The gain applied to signals which lie below Adaptive Threshold A are programmed in the Filter Gain register.

At any one time only one of the following registers is active: AFG1, AFG2, AFG3, FG. The gain values can be preprogrammed and become active whenever the threshold conditions for the according register is met. To program the Adaptive Filter Gain registers the source register settings are used as for the Filter Gain register.

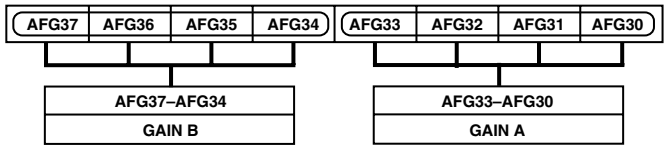


Figure 40. Adaptive Filter Gain 3 Register

ADAPTIVE FILTER THRESHOLD A
AFTA (AFTA)7–0
(Address (SR5–SR0) = 25H)
This 8-bit-wide register is used to program the threshold value for small edges. The recommended programmable threshold range is from 16–235, although any value in the range of 0–255 can be used.

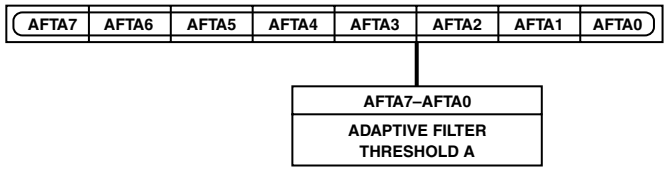


Figure 41. Adaptive Filter Threshold A Register

ADAPTIVE FILTER THRESHOLD B
AFTB (AFTB)7–0
(Address (SR5–SR0) = 26H)
This 8-bit-wide register is used to program the threshold value for medium edges and has priority over Adaptive Threshold A. The recommended programmable threshold range is from 16–235, although any value in the range of 0–255 can be used.

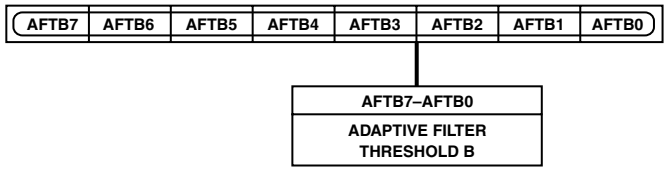


Figure 42. Adaptive Filter Threshold B Register

ADAPTIVE FILTER THRESHOLD C
AFTC (AFTC)7–0
(Address (SR5–SR0) = 27H)
This 8-bit-wide register is used to program the threshold value for large edges and has priority over Adaptive Threshold A and B. The recommended programmable threshold range is from 16–235, although any value in the range of 0–255 can be used.

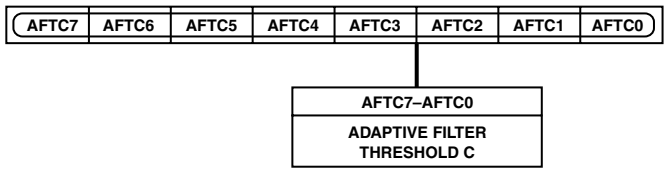


Figure 43. Adaptive Filter Threshold C Register

SHARPNESS FILTER AND ADAPTIVE FILTER APPLICATION EXAMPLES

Sharpness Filter Application

The sharpness filter can be used to enhance or attenuate the Y video output signal.

The following register settings were used to achieve the results shown in the figures below:

Input data was generated by an external signal source.

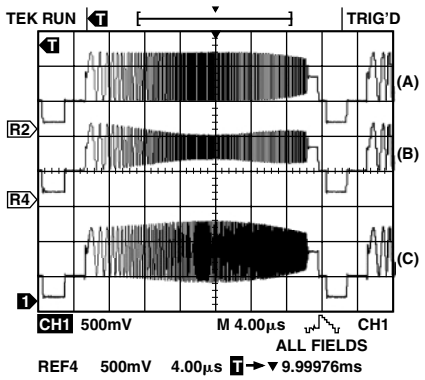
Table V.

Address		Register Setting	
00hex	Mode Register 0	40hex	
01hex	Mode Register 1	81hex	
02hex	Mode Register 2	00hex	
03hex	Mode Register 3	78hex	
04hex	Mode Register 4	00hex	
05hex	Mode Register 5	00hex	
09hex	Mode Register 6	3Ehex	
10hex	Filter Gain	00hex	(a)
10hex	Filter Gain	08hex	(b)
10hex	Filter Gain	04hex	(c)
10hex	Filter Gain	40hex	(d)
10hex	Filter Gain	80hex	(e)
10hex	Filter Gain	22hex	(f)

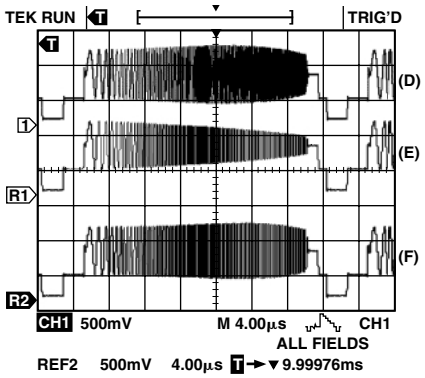
The effect of the sharpness filter can also be seen when using the internally generated cross hatch pattern**:**

Table VI.

Address		Register Setting
00hex	Mode Register 0	00hex
01hex	Mode Register 1	85hex
02hex	Mode Register 2	00hex
03hex	Mode Register 3	38hex
04hex	Mode Register 4	00hex
05hex	Mode Register 5	00hex
09hex	Mode Register 6	3Ehex



(a)



(b)

Figure 44. Sharpness Filter Control with Different Gain Settings for Filter Gain

In toggling MR17 (Sharpness Filter Enable/Disable) and setting the Filter Gain register value to 99hex it can be seen that the line contours of the cross hatch pattern change their sharpness.

Adaptive Filter Control Application

The figure below shows a typical signal to be processed by the Adaptive Filter Control block.

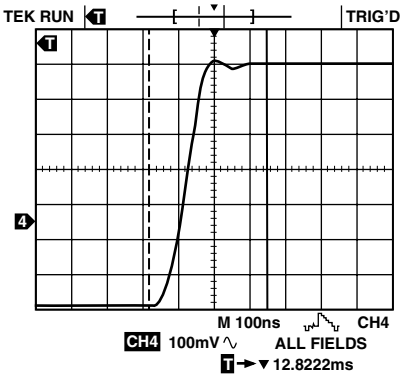


Figure 45. Input Signal to Adaptive Filter Control

The following register settings where used to obtain the results shown in the figure below, i.e., to remove the ringing on the Y signal:

Input data was generated by an external signal source.

Table VII.

Address		Register Setting
00hex	Mode Register 0	40hex
01hex	Mode Register 1	81hex
02hex	Mode Register 2	00hex
03hex	Mode Register 3	78hex
04hex	Mode Register 4	00hex
05hex	Mode Register 5	80hex
09hex	Mode Register 6	3Ehex
10hex	Filter Gain	00hex
22hex	Adaptive Filter Gain 1	AChex
23hex	Adaptive Filter Gain 2	9Ahex
24hex	Adaptive Filter Gain 3	88hex
25hex	Adaptive Filter Threshold A	28hex
26hex	Adaptive Filter Threshold B	3Fhex
27hex	Adaptive Filter Threshold C	64hex

The figure below shows the output signal when changing the Adaptive Filter mode to Mode B (MR56 = "1").

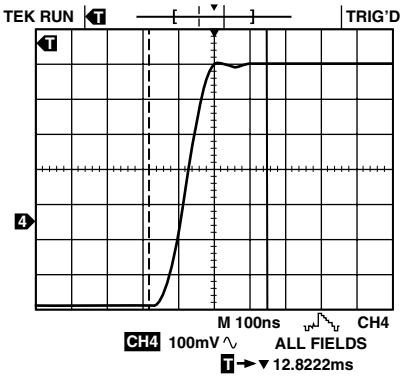


Figure 46. Output Signal from Adaptive Filter Control

The Adaptive Filter control can also be demonstrated using the internally generated crosshatch test pattern and toggling the Adaptive Filter Control bit (MR57) using the following register settings:

Table VIII.

Address		Register Setting
00hex	Mode Register 0	40hex
01hex	Mode Register 1	85hex
02hex	Mode Register 2	00hex
03hex	Mode Register 3	78hex
04hex	Mode Register 4	00hex
05hex	Mode Register 5	80hex
06hex	Color Y	6Chex
07hex	Color Cr	52hex
08hex	Color Cb	52hex
09hex	Mode Register 6	3Ehex
10hex	Filter Gain	00hex
22hex	Adaptive Filter Gain 1	AChex
23hex	Adaptive Filter Gain 2	9Ahex
24hex	Adaptive Filter Gain 3	88hex
25hex	Adaptive Filter Threshold A	28hex
26hex	Adaptive Filter Threshold B	3Fhex
27hex	Adaptive Filter Threshold C	64hex

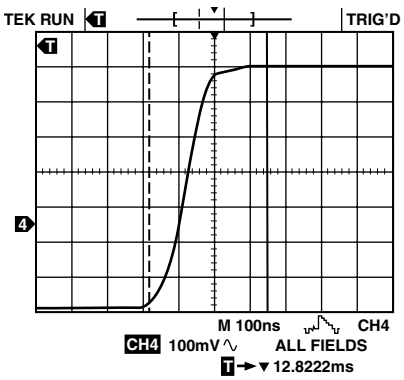


Figure 47. Output Signal from Adaptive Filter Control

HDTV MODE
MODE REGISTER 0
MR0 (MR07–MR00)
(Address (SR4–SR0) = 00H)
Figure 50 shows the various operations under the control of Mode Register 0.

HEXMR0 BIT DESCRIPTION
Output Standard Selection (MR00–MR01)
These bits are used to select the output levels from the ADV7196A.

If EIA 770.3 (MR01–00 = "00") is selected, the output levels will be: 0 mV for blanking level, 700 mV for peak white (Y channel), ±350 mV for Pr, Pb outputs and –300 mV for tri-level sync.

If Full Input Range (MR01–00 = "10") is selected, the output levels will be 700 mV for peak white for the Y channel, ±350 mV for Pr, Pb outputs and –300 mV for Sync. This mode is used for RS-170, RS-343A standard output compatibility.

Sync insertion on the Pr, Pb channels is optional.
For output levels, refer to the Appendix.

Input Control Signals (MR02–MR03)
These control bits are used to select whether data is input with external horizontal, vertical and blanking sync signals or if the data is input with embedded EAV/SAV code An Asynchronous timing mode is also available using TSYNC, $\overline{\text{SYNC}}$ and DV as input control signals. These timing control signals have to be programmed by the user.

Figure 48 shows an example of how to program the ADV7196A to accept a different high definition standard but SMPTE293M, SMPTE274M, SMPTE296M or ITU-R.BT1358 standard.

Reserved (MR04)
A "0" must be written to this bit.

Input Standard (MR05)
Select between 1080i or 720p input.

DV Polarity (MR06)
This control bit allows to select the polarity of the DV input control signal to be either active high or active low.

Reserved (MR07)
A "0" must be written to this bit.

Table IX. Truth Table

$\overline{\text{SYNC}}$	TSYNC	DV	
1 –> 0	0	0 or 1	50% Point of Falling Edge of Tri-Level Horizontal Signal, A
0	0 –> 1	0 or 1	25% Point of Rising Edge of Tri-Level Horizontal Signal, B
0 –> 1	0 or 1	0	50% Point of Falling Edge of Tri-Level Horizontal Signal, C
1	0 or 1	0 –> 1	50% Start of Active Video, D
1	0 or 1	1 –> 0	50% End of Active Video, E

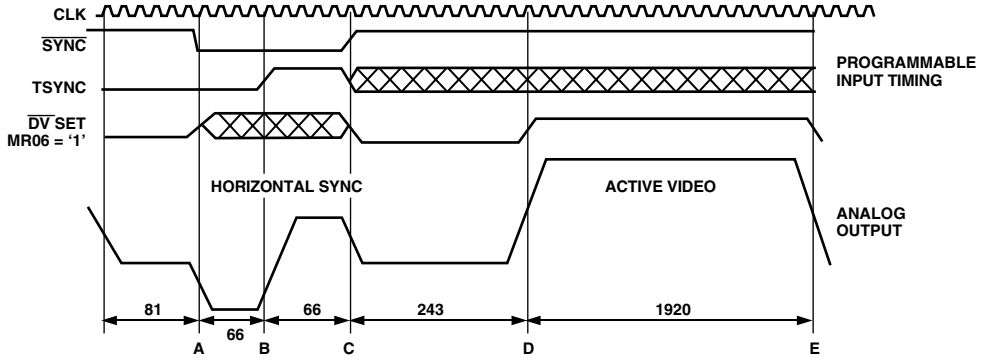


Figure 48. Async Timing Mode—Programming Input Control Signals for SMPTE295M Compatibility

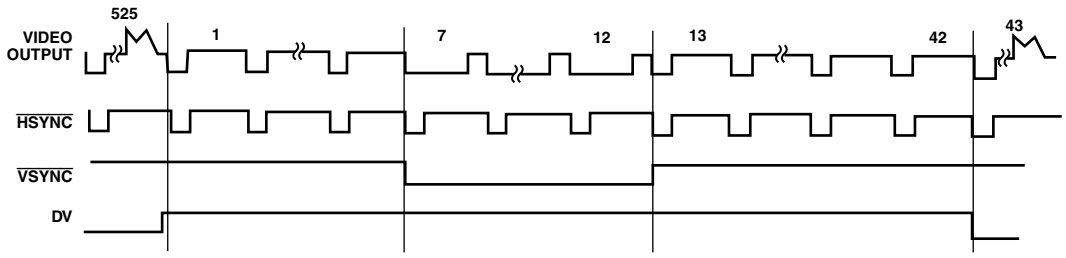


Figure 49. DV Input Control Signal in Relation to Video Output Signal

MODE REGISTER 1
MR1 (MR17–MR10)
(Address (SR4-SR0) = 01H)
Figure 51 shows the various operations under the control of Mode Register 1.

MR1 BIT DESCRIPTION
Pixel Data Enable (MR10)
When this bit is set to "0," the pixel data input to the ADV7196A is blanked such that a black screen is output from the DACs. When this bit is set to "1," pixel data is accepted at the input pins and the ADV7196A outputs to the standard set in "Output Standard Selection" (MR01–00). This bit also must be set to "1" to enable output pattern signals.

Input Format (MR11)
It is possible to input data in 4:2:2 format or in 4:4:4 HDTV format.

Test Pattern Enable (MR12)
Enables or disables the internal test pattern generator.

Test Pattern Hatch/Frame (MR13)
If this bit is set to "0," a cross-hatch test pattern is output from the ADV7196A. The cross-hatch test pattern can be used to test monitor convergence.

If this bit is set to "1," a uniform colored frame/field test pattern is output from the ADV7196A.

The color of the lines or the frame/field is by default white but can be programmed to be any color using the Color Y, Color Cr, Color Cb registers.

VBI Open (MR14)
This bit enables or disables the facility of VBI data insertion during the Vertical Blanking Interval.

For this purpose Lines 7–20 in 1080i and Lines 6–25 in 720p can be used for VBI data insertion.

Reserved (MR15–MR17)
A "0" must be written to these bits.

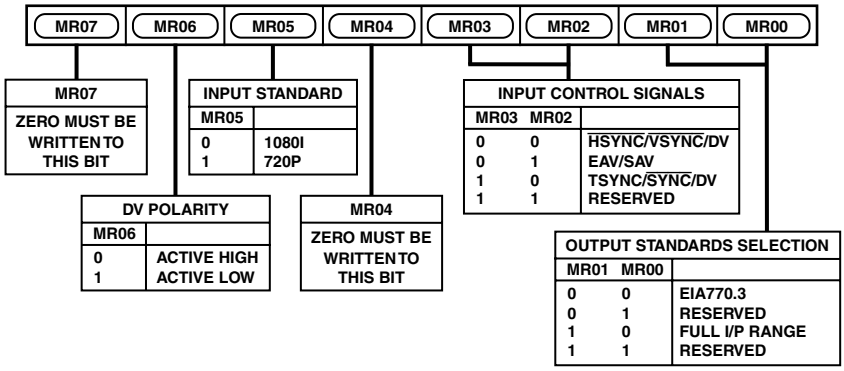


Figure 50. Mode Register 0

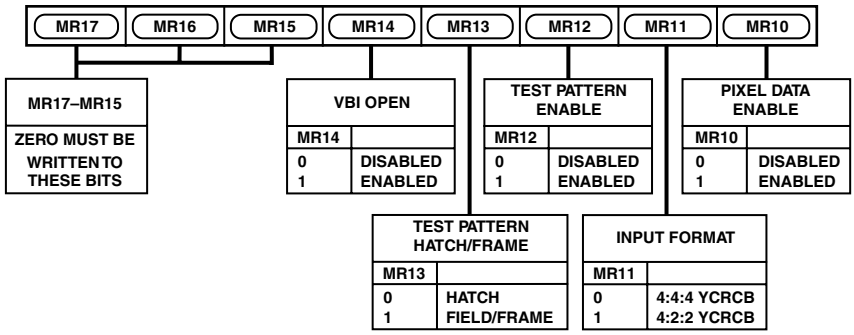


Figure 51. Mode Register 1

MODE REGISTER 2
MR1 (MR27–MR20)
(Address (SR4–SR0) = 02H)
Figure 53 shows the various operations under the control of Mode Register 2.

MR2 BIT DESCRIPTION
Y Delay (MR20–MR22)
With these bits it is possible to delay the Y signal with respect to the falling edge of the horizontal sync signal by up to four pixel clock cycles. Figure 52 demonstrates this facility.

Color Delay (MR23–MR25)
With theses bits it is possible to delay the color signals with respect to the falling edge of the horizontal sync signal by up to four pixel clock cycles. Figure 52 demonstrates this facility.

Reserved (MR26–MR27)
A "0" must be written to these bits.

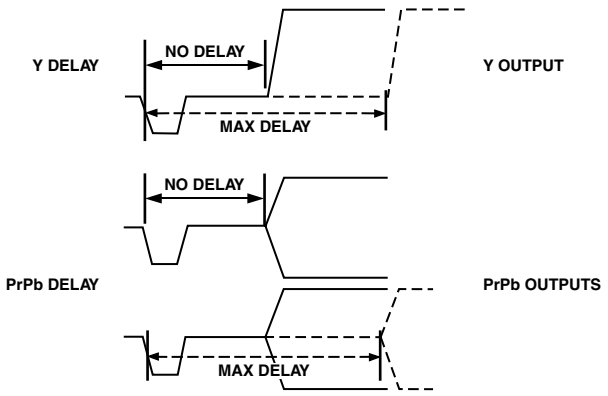


Figure 52. Y and Color Delay

MODE REGISTER 3
MR3 (MR37–MR30)
(Address (SR4-SR0) = 03H)
Figure 54 shows the various operations under the control of Mode Register 3.

MR3 BIT DESCRIPTION
HDTV Enable (MR30)
When this bit is set to "1" the ADV7196A reverts to HDTV mode. When set to "0" the ADV7196A reverts to Progressive Scan mode (PS mode).

Reserved (MR31–MR32)
A "0" must be written to these bits.

DAC A Control (MR33)
Setting this bit to "1" enables DAC A, otherwise this DAC is powered down.

DAC B Control (MR34)
Setting this bit to "1" enables DAC B, otherwise this DAC is powered down.

DAC C Control (MR35)
Setting this bit to "1" enables DAC C, otherwise this DAC is powered down.

Reserved (MR36–MR37)
A "0" must be written to these bits.

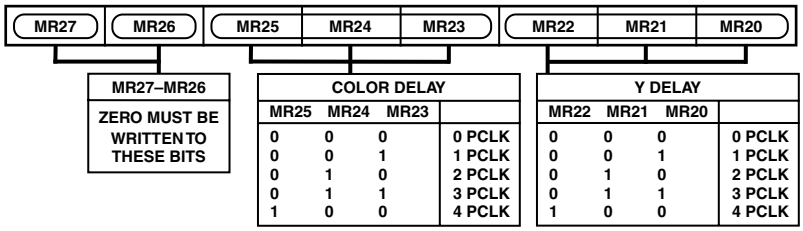


Figure 53. Mode Register 2

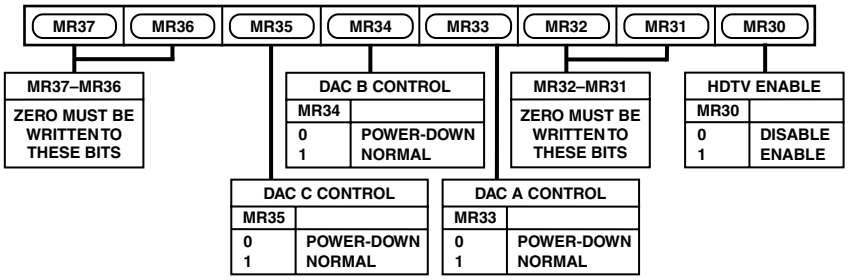


Figure 54. Mode Register 3

MODE REGISTER 4
MR4 (MR47–MR40)
(Address (SR4–SR0) = 04H)
Figure 55 shows the various operations under the control of Mode Register 4.

MR4 BIT DESCRIPTION
Timing Reset (MR40)
Toggling MR40 from low to high and low again resets the internal horizontal and vertical timing counters.

MODE REGISTER 5
MR5 (MR57–MR50)
(Address (SR4–SR0) = 05H)
Figure 56 shows the various operations under the control of Mode Register 5.

MR5 BIT DESCRIPTION
Reserved (MR50)
These bit is reserved for the revision code.

RGB Mode (MR51)
When RGB mode is enabled (MR51 = "1") the ADV7196A accepts unsigned binary RGB data at its input port. This control is also available in Async Timing Mode.

Sync on PrPb (MR52)
By default the color component output signals Pr, Pb do not contain any horizontal sync pulses. If required they can be inserted when MR52 = "1." This control is not available in RGB mode.

Color Output Swap (MR53)
By default DAC B is configured as the Pr output and DAC C as the Pb output. In setting this bit to "1" the DAC outputs can be swapped around so that DAC B outputs Pb and DAC C outputs Pr. Table X demonstrates this in more detail.

Reserved (MR54–MR57)
"0" must be written to these bits.

Table X. Relationship Between Input Pixel Port, MR53 and DAC B, DAC C Outputs

In 4:4:4 Input Mode

Color Data Input on Pins	MR53	Analog Output Signal
Cr9–0	0	DAC B
Cb/Cr9–0	0	DAC C
Cr9–0	1	DAC C
Cb/Cr9–0	1	DAC B

In 4:2:2 Input Mode

Color Data Input on Pins	MR53	Analog Output Signal
Cr9–0	0 or 1	Not Operational
Cb/Cr9–0	0	DAC C (Pb)
Cb/Cr9–0	1	DAC C (Pr)

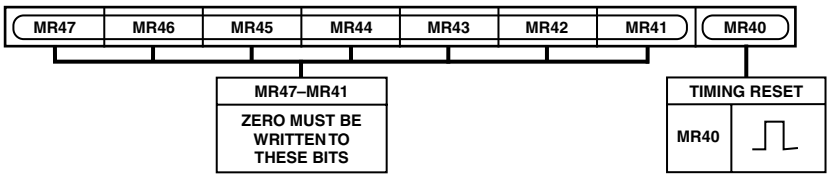


Figure 55. Mode Register 4

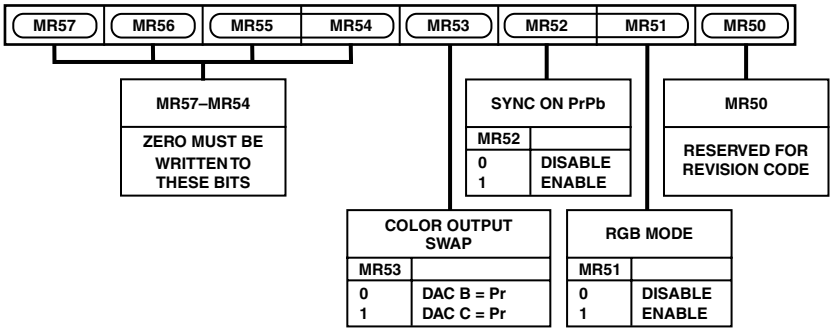


Figure 56. Mode Register 5

DAC TERMINATION AND LAYOUT CONSIDERATIONS

Voltage Reference

The ADV7196A contains an on-board voltage reference. The V_{REF} pin is normally terminated to V_{AA} through a 0.1 μF capacitor when the internal V_{REF} is used. Alternatively, the ADV7196A can be used with an external V_{REF} (AD589).

Resistor R_{SET} is connected between the R_{SET} pin and AGND and is used to control the full-scale output current and therefore the DAC voltage output levels. For full-scale output R_{SET} must have a value of 2470 Ω. R_{LOAD} has a value of 300 Ω. When an input range of 0–1023 is selected the value of R_{SET} must be 2820 Ω.

The ADV7196A has three analog outputs, corresponding to Y, Pr, Pb video signals. The DACs must be used with external buffer circuits in order to provide sufficient current to drive an output device. Suitable op amps are the AD8009, AD8002, AD8001, or AD8057.

To calculate the output full-scale current and voltage the following equations should be used:

$$V_{OUT} = I_{OUT} \times R_{LOAD}$$

$$I_{OUT} = [V_{REF} \times k]/R_{SET}$$

where:

k = 5.66 [for input ranges 64–940, 64–960, output standards EIA770.1–3]

k = 6.46 [for input ranges 0–1023, output standard RS–170/343A]

V_{REF} = 1.235 V

PC BOARD LAYOUT CONSIDERATIONS

The ADV7196A is optimally designed for lowest noise performance, both radiated and conducted noise. To complement the excellent noise performance of the ADV7196A, it is imperative that great care be given to the PC board layout.

The layout should be optimized for lowest noise on the ADV7196A power and ground lines. This can be achieved by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and AGND and V_{DD} and DGND pins should be kept as short as possible to minimized inductive ringing.

It is recommended that a four-layer printed circuit board is used. With power and ground planes separating the layer of the signal carrying traces of the components and solder side layer. Placement of components should consider to separate noisy circuits, such as crystal clocks, high-speed logic circuitry and analog circuitry.

There should be a separate analog ground plane (AGND) and a separate digital ground plane (GND).

Power planes should encompass a digital power plane (V_{DD}) and a analog power plane (V_{AA}). The analog power plane should contain the DACs and all associated circuitry, and the V_{REF} circuitry.

The digital power plane should contain all logic circuitry. The analog and digital power planes should be individually connected to the common power plane at one single point through a suitable filtering device, such as a ferrite bead.

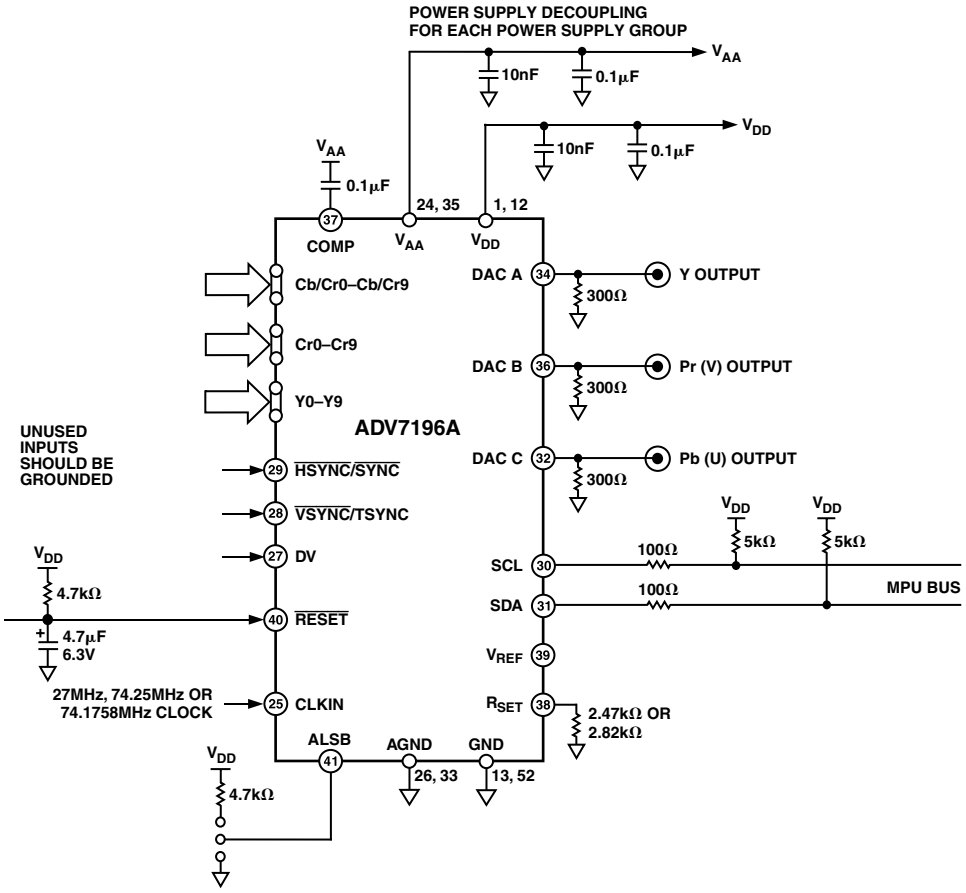


Figure 57. Circuit Layout

DAC output traces on a PCB should be treated as transmission lines. It is recommended that the DACs be placed as close as possible to the output connector, with the analog output traces being as short as possible (less than 3 inches). The DAC termination resistors should be placed as close as possible to the DAC outputs and should overlay the PCB's ground plane. As well as minimizing reflections, short analog output traces will reduce noise pickup due to neighboring digital circuitry.

Supply Decoupling
Noise on the analog power plane can be further reduced by the use of decoupling capacitors.

Optimum performance is achieved by the use of 0.1 µF ceramic capacitors. Each of group of V_{AA} or V_{DD} pins should be individually decoupled to ground. This should be done by placing the capacitors as close as possible to the device with the capacitor leads as short as possible, thus minimizing lead inductance.

Digital Signal Interconnect
The digital signal lines should be isolated as much as possible from the analog outputs and other analog circuitry. Digital signal lines should not overlay the analog power plane.

Due to the high clock rates used, long clock lines to the ADV7196A should be avoided to minimize noise pickup. Any active pull-up termination resistors for the digital inputs should be connected to the digital power plane and not the analog power plane.

Analog Signal Interconnect
The ADV7196A should be located as close as possible to the output connectors thus minimizing noise pickup and reflections due to impedance mismatch.

For optimum performance, the analog outputs should each have a source termination resistance to ground of 75 Ω. This termination resistance should be as close as possible to the ADV7196A to minimize reflections.

Any unused inputs should be tied to ground.

Video Output Buffer and Optional Output Filter
Output buffering is necessary in order to drive output devices, such as progressive scan or HDTV monitors.

Analog Devices produces a range of suitable op amps for this application. Suitable op amps would be the AD8009, AD8002, AD8001, or AD8057. More information on line driver buffering circuits is given in the relevant op amp data sheets.

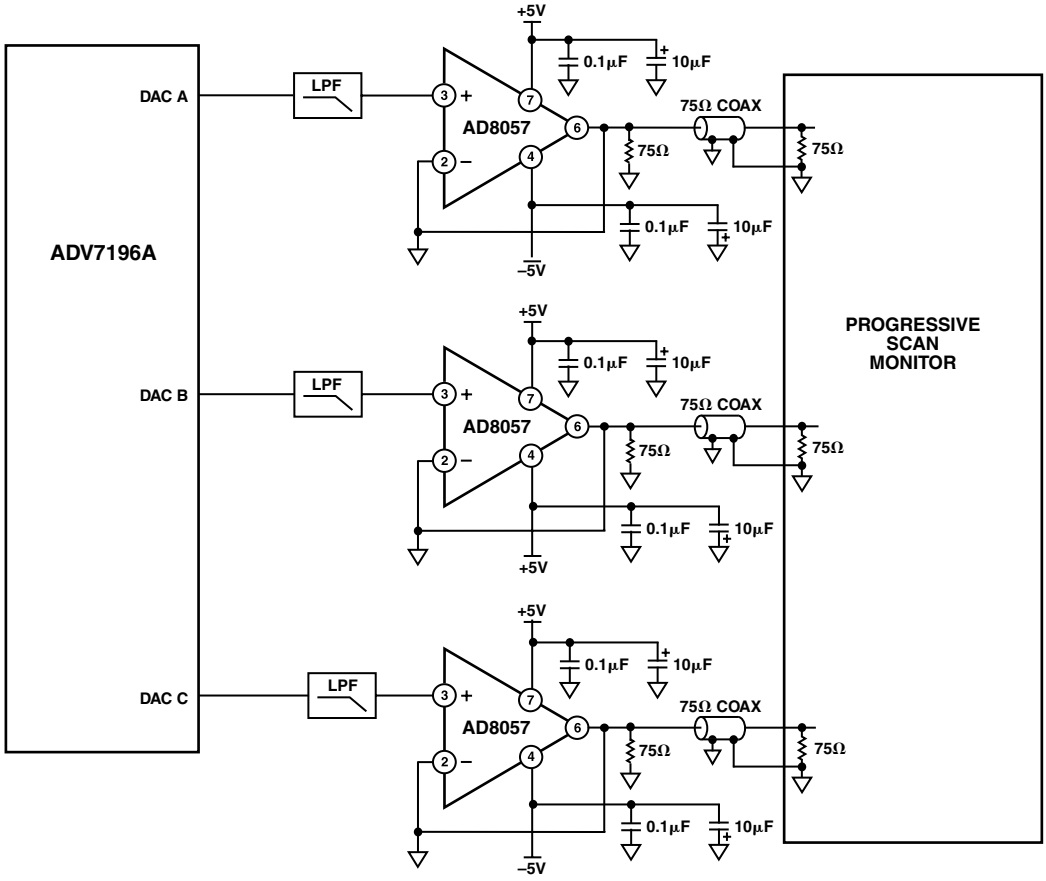


Figure 58. Output Buffer and Optional Filter

An optional analog reconstruction LPF might be required as an antialias filter if the ADV7196A is connected to a device that requires this filtering.

The Eval ADV7196A/7EB evaluation board uses the ML6426 Microlinear IC, which provides buffering and low-pass filtering for progressive scan applications.

The Eval ADV7196A/7EB Rev B and Rev C evaluation board uses the AD8057 as a buffer and a 6th order LPF.

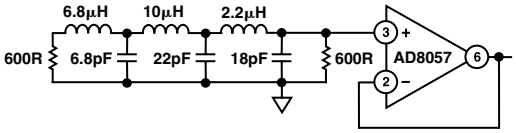


Figure 59. Example for Output Filter: PS Mode/ 2x Oversampling

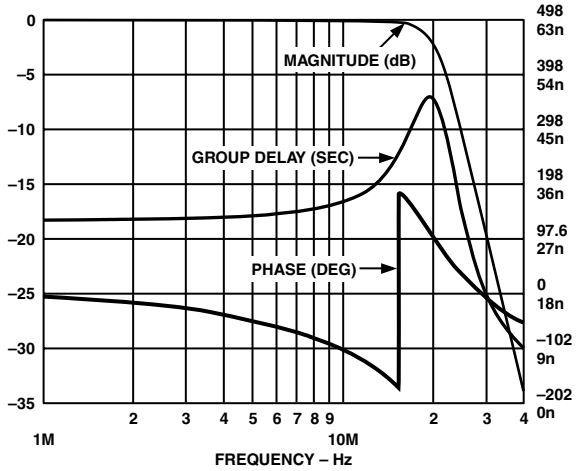


Figure 60. Frequency Response for Filter Current in Above Figure

REGISTER SETTINGS

Table XI. Register Settings on Power-Up

Address		Register Setting
00hex	Mode Register 0	00hex
01hex	Mode Register 1	00hex
02hex	Mode Register 2	00hex
03hex	Mode Register 3	38hex
04hex	Mode Register 4	00hex
05hex	Mode Register 5	00hex
06hex	Color Y	A0hex
07hex	Color CR	80hex
08hex	Color Cb	80hex
09hex	Mode Register 6	00hex
10hex	Filter Gain	00hex
22hex	Adaptive Filter Gain 1	AChex
23hex	Adaptive Filter Gain 2	9Ahex
24hex	Adaptive Filter Gain 3	88hex
25hex	Adaptive Filter Threshold A	28hex
26hex	Adaptive Filter Threshold B	3Fhex
27hex	Adaptive Filter Threshold C	64hex

Table XII. Internal Colorbars (Hatch), Progressive Scan Mode

Address		Register Setting
00hex	Mode Register 0	00hex
01hex	Mode Register 1	05hex
02hex	Mode Register 2	00hex
03hex	Mode Register 3	38hex
04hex	Mode Register 4	00hex
05hex	Mode Register 5	00hex
06hex	Color Y	xxhex
07hex	Color CR	xxhex
08hex	Color Cb	xxhex
09hex	Mode Register 6	3Ehex

Table XIII. Internal Colorbars (Field), HDTV Scan Mode

Address		Register Setting
00hex	Mode Register 0	00hex
01hex	Mode Register 1	0Dhex
02hex	Mode Register 2	00hex
03hex	Mode Register 3	39hex
04hex	Mode Register 4	00hex
05hex	Mode Register 5	00hex
06hex	Color Y	xxhex
07hex	Color CR	xxhex
08hex	Color Cb	xxhex

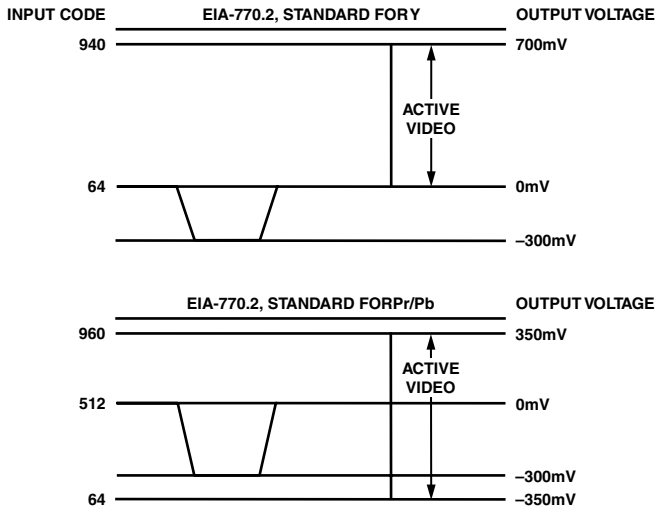


Figure 61. EIA-770.2 Standard Output Signals (525p)

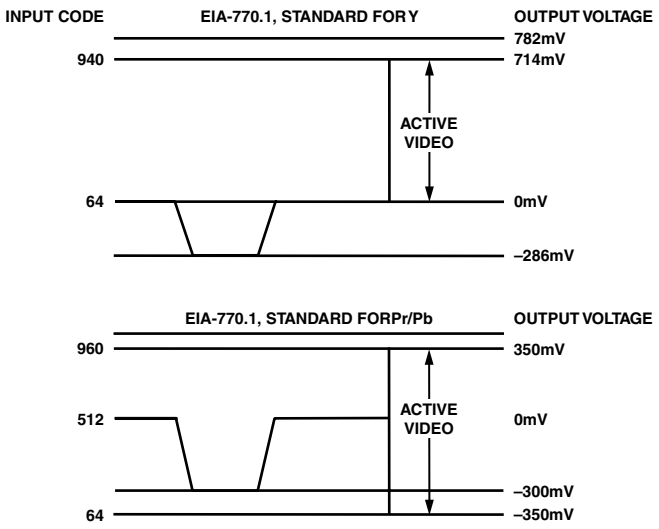


Figure 62. EIA-770.1 Standard Output Signals (525p)

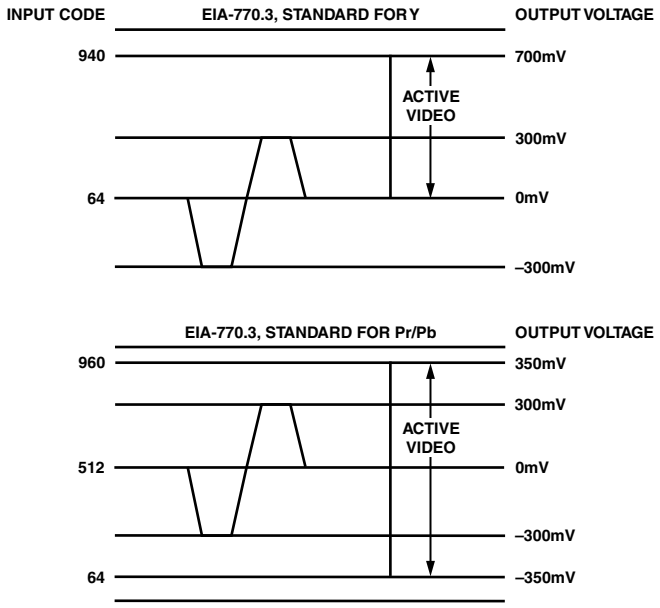


Figure 63. EIA-770.3 Standard Output Signals (1080i, 720p)

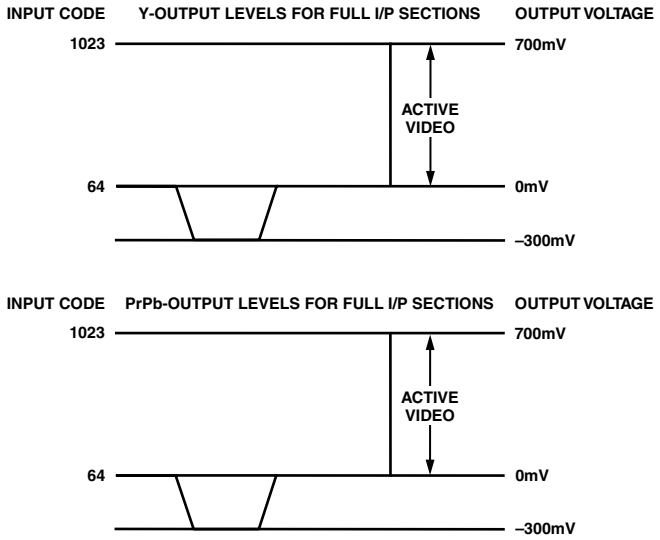


Figure 64. Output Levels for Full I/P Selection

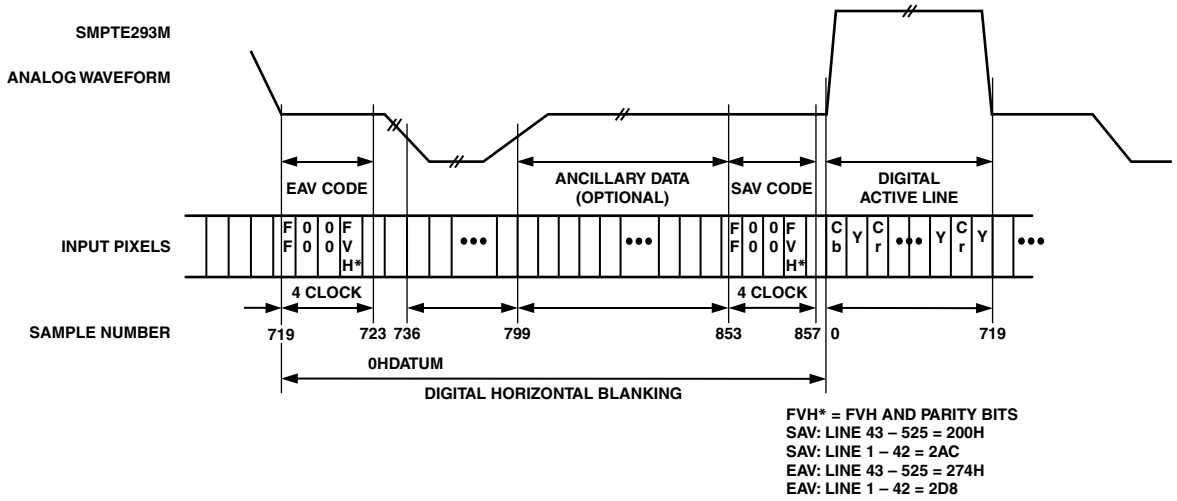


Figure 65. EAV/SAV Input Data Timing Diagram—SMPTE293M

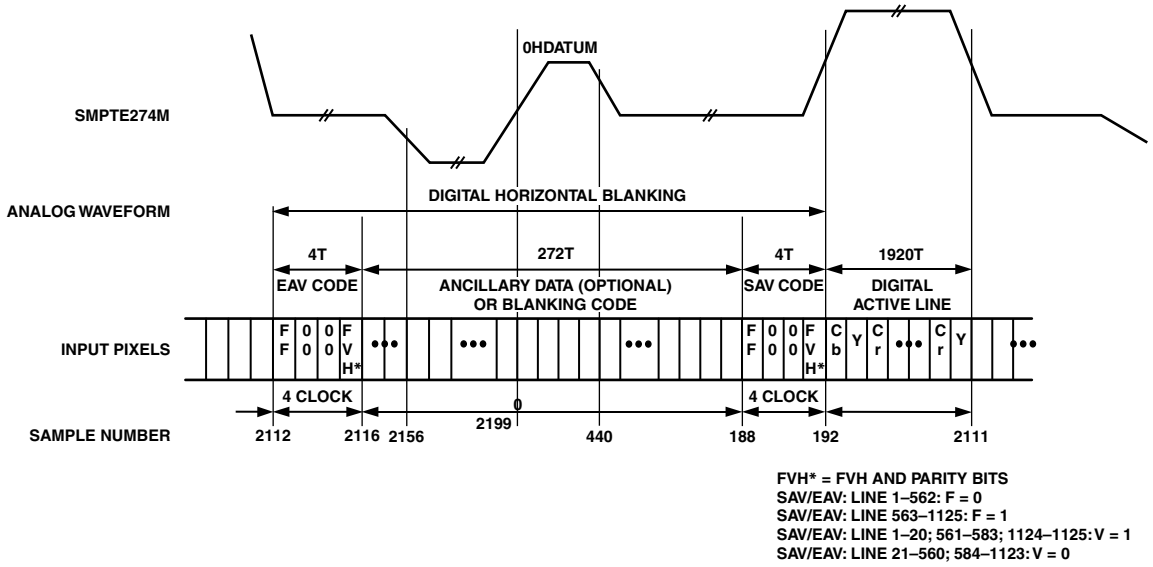


Figure 66. EAV/SAV Input Data Timing Diagram—SMPTE274M

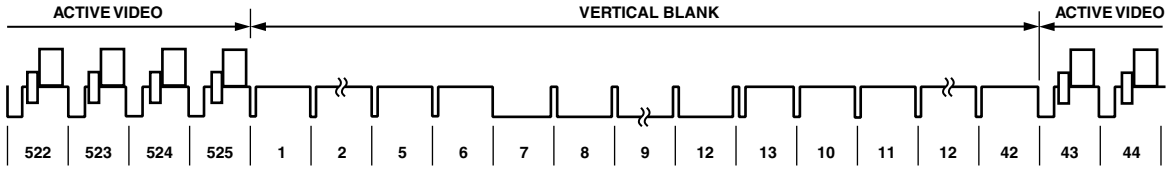


Figure 67. SMPTE293M (525p)

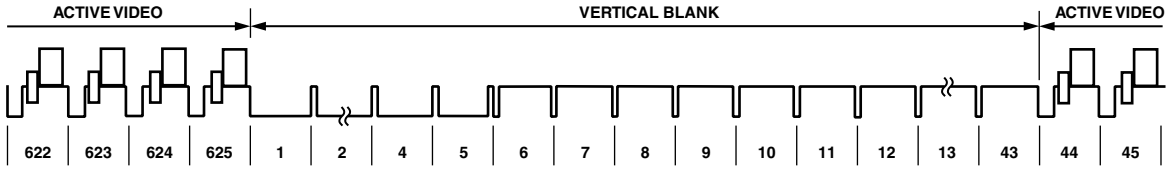


Figure 68. ITU-R. BT1358 (625p)

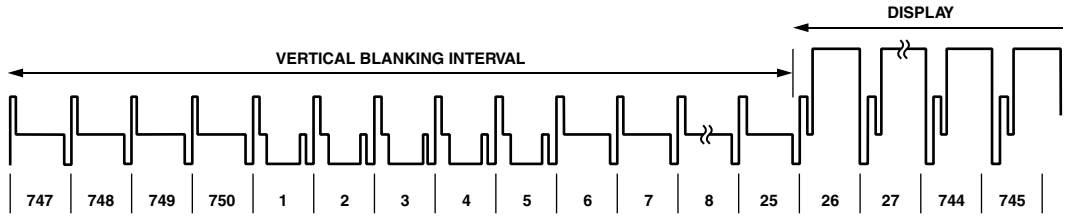


Figure 69. SMPTE296M (720p)

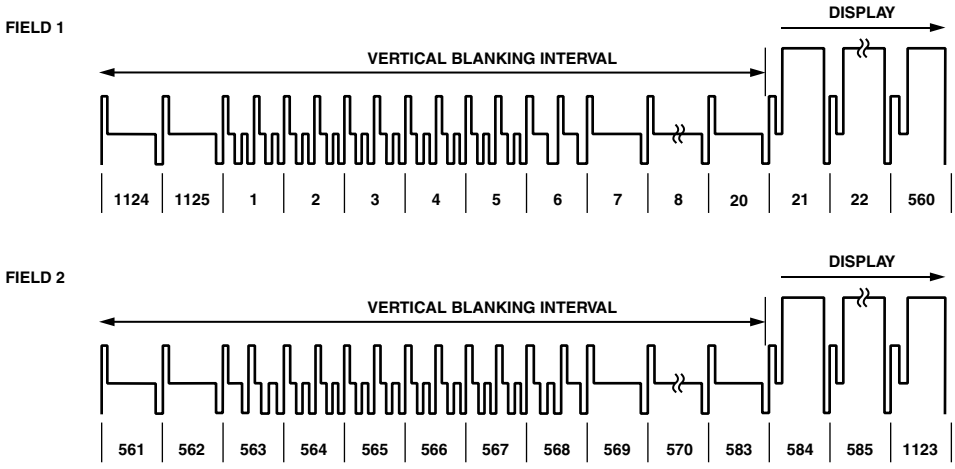
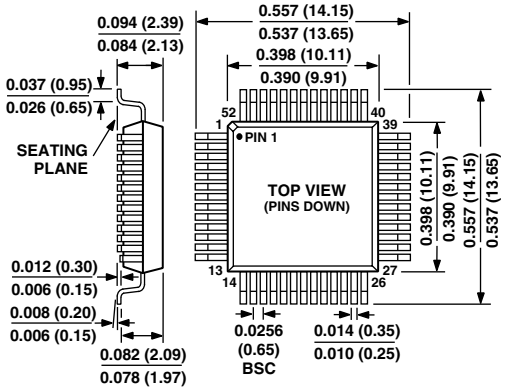


Figure 70. SMPT274M (1080i)

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

52-Lead Plastic Quad Flatpack (MQFP)
(S-52)



C02154–1.5–4/01(0)

PRINTED IN U.S.A.