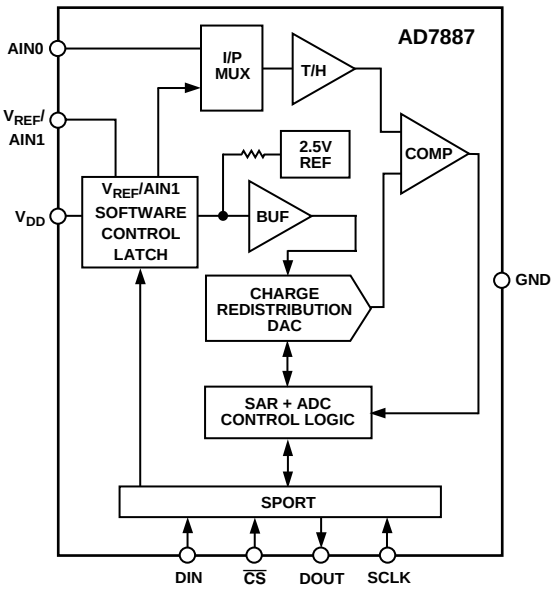
+2.7 V to +5.25 V, Micropower, 2-Channel, 125 kSPS, 12-Bit ADC in 8-Lead μSOIC

AD7887

FEATURES
Specified for V_{DD} of +2.7 V to +5.25 V
Flexible Power/Throughput Rate Management
Shutdown Mode: 1 μA Max
One/Two Single-Ended Inputs
Serial Interface: SPI™/QSPI™/MICROWIRE™/DSP Compatible
8-Lead Narrow SOIC and μSOIC Packages

APPLICATIONS
Battery-Powered Systems (Personal Digital Assistants, Medical Instruments, Mobile Communications)
Instrumentation and Control Systems
High Speed Modems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7887 is a high speed, low power, 12-bit ADC that operates from a single +2.7 V to +5.25 V power supply. The AD7887 is capable of 125 kSPS throughput rate. The input track-and-hold acquires a signal in 500 ns and features a single-ended sampling scheme. The output coding for the AD7887 is straight binary and the part is capable of converting full power signals up to 2.5 MHz.

The AD7887 can be configured for either dual or single channel operation, via the on-chip Control Register. There is a default single-channel mode that allows the AD7887 to be operated as a read-only ADC. In single-channel operation, there is one analog input (AIN0) with the V_{REF}/AIN1 pin assuming its V_{REF} function. This V_{REF} pin allows the user access to the part's internal +2.5 V reference, or the V_{REF} pin can be overdriven by an external reference to provide the reference voltage for the part. This external reference voltage has a range of +2.5 V to V_{DD}. The analog input range on AIN0 is 0 to $+V_{REF}$.

In dual-channel operation, the V_{REF}/AIN1 pin assumes its AIN1 function, providing a second analog input channel. In this case, the reference voltage for the part is provided via the V_{DD} pin. As a result, the input voltage range on both the AIN0 and AIN1 inputs is 0 to V_{DD}.

CMOS construction ensures low power dissipation of typically 2 mW for normal operation and 3 μW in power-down mode. The part is available in an 8-lead, 0.15-inch-wide narrow body SOIC and an 8-lead μSOIC package.

PRODUCT HIGHLIGHTS

1. Smallest 12-bit dual/single-channel ADC; 8-lead μSOIC package.
2. Lowest power 12-bit dual/single-channel ADC.
3. Flexible power management options including automatic power-down after conversion.
4. Read-Only ADC capability.
5. Analog input range from 0 V to V_{REF}.
6. Versatile serial I/O port (SPI/QSPI/MICROWIRE/DSP compatible).

SPI and QSPI are trademarks of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corporation.

REV. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

AD7887–SPECIFICATIONS[1] (V_{DD} = +2.7 V to +5.25 V, V_{REF} = +2.5 V External/Internal Reference unless otherwise noted, f_{SCLK} = 2 MHz; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	A Version[1]	B Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE				
Signal to Noise + Distortion Ratio[2, 3] (SNR)	71	71	dB typ	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 125 kSPS
Total Harmonic Distortion[2] (THD)	–80	–80	dB typ	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 125 kSPS
Peak Harmonic or Spurious Noise[2]	–80	–80	dB typ	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 125 kSPS
Intermodulation Distortion[2] (IMD)				
Second Order Terms	–80	–80	dB typ	fa = 9.983 kHz, fb = 10.05 kHz, f_{SAMPLE} = 125 kSPS
Third Order Terms	–80	–80	dB typ	fa = 9.983 kHz, fb = 10.05 kHz, f_{SAMPLE} = 125 kSPS
Channel-to-Channel Isolation[2]	–80	–80	dB typ	f_{IN} = 25 kHz
Full Power Bandwidth	2.5	2.5	MHz typ	@ 3 dB
DC ACCURACY				Any Channel
Resolution	12	12	Bits	
Integral Nonlinearity[2]	±2	±1	LSB max	
Differential Nonlinearity[2]	±2	±1	LSB max	Guaranteed No Missing Codes to 11 Bits (A Grade)
Offset Error[2]	±3	±3	LSB max	V_{DD} = 5 V, Dual-Channel Mode
	±4	±4	LSB max	V_{DD} = 3 V, Dual-Channel Mode
	±6	±6	LSB typ	Single-Channel Mode
Offset Error Match[2]	0.5	0.5	LSB max	
Gain Error[2]	±2	±2	LSB max	Dual-Channel Mode
	±1	±1	LSB max	Single-Channel Mode, External Reference
	±6	±6	LSB typ	Single-Channel Mode, Internal Reference
Gain Error Match[2]	2	2	LSB max	
ANALOG INPUT				
Input Voltage Ranges	0 to V_{REF}	0 to V_{REF}	Volts	
Leakage Current	±5	±5	µA max	
Input Capacitance	20	20	pF typ	
REFERENCE INPUT/OUTPUT				
REF_{IN} Input Voltage Range	2.5/V_{DD}	2.5/V_{DD}	V min/max	Functional from 1.2 V
Input Impedance	10	10	kΩ typ	Very High Impedance If Internal Reference Disabled
REF_{OUT} Output Voltage	2.45/2.55	2.45/2.55	V min/max	
REF_{OUT} Tempco	±50	±50	ppm/°C typ	
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	V_{DD} = +4.75 V to +5.25 V
	2.1	2.1	V min	V_{DD} = +2.7 V to +3.6 V
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = +2.7 V to +5.25 V
Input Current, I_{IN}	±1	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[4]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}				I_{SOURCE} = 200 µA
	V_{DD} – 0.5	V_{DD} – 0.5	V min	V_{DD} = +2.7 V to +5.25 V
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±1	±1	µA max	
Floating-State Output Capacitance[5]	10	10	pF max	
Output Coding	Straight (Natural) Binary			
CONVERSION RATE				
Throughput Time	16	16	SCLK Cycles	Conversion Time + Acquisition Time 125 kSPS with 2 MHz Clock
Track/Hold Acquisition Time[2]	1.5	1.5	SCLK Cycles	
Conversion Time	14.5	14.5	SCLK Cycles	7.25 µs (2 MHz Clock)

Parameter	A Version[1]	B Version[1]	Units	Test Conditions/Comments
POWER REQUIREMENTS				
V_{DD}	+2.7/+5.25	+2.7/+5.25	V min/max	
I_{DD}				
Normal Mode[5] (Mode 2)				
Static	700	700	µA max	
Operational (f_{SAMPLE} = 125 kSPS)	850	850	µA typ	Internal Reference Enabled
	700	700	µA typ	Internal Reference Disabled
Using Standby Mode (Mode 4)	450	450	µA typ	f_{SAMPLE} = 50 kSPS
Using Shutdown Mode (Modes 1, 3)	120	120	µA typ	f_{SAMPLE} = 10 kSPS
	12	12	µA typ	f_{SAMPLE} = 1 kSPS
Standby Mode[6]	210	210	µA max	V_{DD} = +2.7 V to +5.25 V
Shutdown Mode[6]	1	1	µA max	V_{DD} = +2.7 V to +3.6 V
	2	2	µA max	V_{DD} = +4.75 V to +5.25 V
Normal Mode Power Dissipation	3.5	3.5	mW max	V_{DD} = +5 V
	2.1	2.1	mW max	V_{DD} = +3 V
Shutdown Power Dissipation	5	5	µW max	V_{DD} = +5 V
	3	3	µW max	V_{DD} = +3 V
Standby Power Dissipation	1.05	1.05	mW max	V_{DD} = +5 V
	630	630	µW max	V_{DD} = +3 V

NOTES
[1]Temperature ranges as follows: A, B Versions: –40°C to +125°C.
[2]See Terminology.
[3]SNR calculation includes distortion and noise components.
[4]Sample tested @ +25°C to ensure compliance.
[5]All digital inputs @ GND except $\overline{CS}$ @ V_{DD}. No load on the digital outputs. Analog inputs @ GND.
[6]SCLK @ GND when SCLK off. All digital inputs @ GND except for $\overline{CS}$ @ V_{DD}. No load on the digital outputs. Analog inputs @ GND.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND ..... –0.3 V to +7 V
Analog Input Voltage to AGND ..... –0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to AGND ..... –0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to AGND .... –0.3 V to V_{DD} + 0.3 V
REF_{IN}/REF_{OUT} to AGND ..... –0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[2] ..... ±10 mA
Operating Temperature Range
  Commercial
    A, B Versions ..... –40°C to +125°C
  Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
SOIC, µSOIC Package, Power Dissipation ..... 450 mW
  θ_{JA} Thermal Impedance ..... 157°C/W (SOIC)
    ..... 205.9°C/W (µSOIC)
  θ_{JC} Thermal Impedance ..... 56°C/W (SOIC)
    ..... 43.74°C/W (µSOIC)
  Lead Temperature, Soldering
    Vapor Phase (60 sec) ..... +215°C
    Infrared (15 sec) ..... +220°C
ESD ..... 4.5 kV

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latch-up.

ORDERING GUIDE

Model	Linearity Error (LSB)[1]	Package Options[2]	Branding
AD7887AR	±2	SO-8	AD7887AR
AD7887ARM	±2	RM-8	C5A
AD7887BR	±1	SO-8	AD7887BR
EVAL-AD7887CB[3]	Evaluation Board		
EVAL-CONTROL BOARD[4]	Controller Board		

NOTES
[1]Linearity error here refers to integral linearity error.
[2]SO = SOIC; RM = µSOIC.
[3]This can be used as a stand-alone evaluation board or in conjunction with the EVAL-CONTROL BOARD for evaluation/demonstration purposes.
[4]This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.

TIMING SPECIFICATIONS[1]

Parameter	Limit at T_{MIN}, T_{MAX} (A, B Versions) +4.75 V to +5.25 V	+2.7 V to +3.6 V	Units	Description
f_{SCLK}[2]	2	2	MHz max	
$t_{CONVERT}$	14.5 t_{SCLK}	14.5 t_{SCLK}		
t_{ACQ}	1.5 t_{SCLK}	1.5 t_{SCLK}		Throughput Time = $t_{CONVERT}$ + t_{ACQ} = 16 t_{SCLK}
t_1	10	10	ns min	$\overline{CS}$ to SCLK Setup Time
t_2[3]	30	60	ns max	Delay from $\overline{CS}$ Until DOUT Three-State Disabled
t_3[3]	75	100	ns max	Data Access Time after SCLK Falling Edge
t_4	20	20	ns min	Data Setup Time Prior to SCLK Rising Edge
t_5	20	20	ns min	Data Valid to SCLK Hold Time
t_6	0.4 t_{SCLK}	0.4 t_{SCLK}	ns min	SCLK High Pulsewidth
t_7	0.4 t_{SCLK}	0.4 t_{SCLK}	ns min	SCLK Low Pulsewidth
t_8[4]	80	80	ns max	$\overline{CS}$ Rising Edge to DOUT High Impedance
t_9	5	5	µs typ	Power-Up Time from Shutdown

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 volts.

[2]Mark/Space ratio for the SCLK input is 40/60 to 60/40.

[3]Measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.8 V or 2.0 V.

[4]t_8 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_8, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

Specifications subject to change without notice.

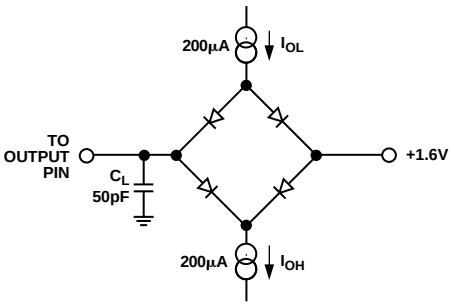
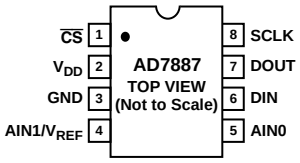


Figure 1. Load Circuit for Digital Output Timing Specifications

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Pin Mnemonic	Function
1	$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7887 and also frames the serial data transfer. When the AD7887 operates in its default mode, the $\overline{CS}$ pin also acts as the shutdown pin such that with the $\overline{CS}$ pin high, the AD7887 is in its power-down mode.
2	V_{DD}	Power Supply Input. The V_{DD} range for the AD7887 is from +2.7 V to +5.25 V. When the AD7887 is configured for two-channel operation, this pin also provides the reference source for the part.
3	GND	Ground Pin. This pin is the ground reference point for all circuitry on the AD7887. In systems with separate AGND and DGND planes, these planes should be tied together as close as possible to this GND pin. Where this is not possible, this GND pin should connect to the AGND plane.
4	AIN1/V_{REF}	Analog Input 1/Voltage Reference Input. In single-channel mode, this pin becomes the reference input/output. In this case, the user can either access the internal +2.5 V reference or overdrive the internal reference with the voltage applied to this pin. The reference voltage range for an externally-applied reference is +1.2 V to V_{DD}. In two-channel mode, this pin provides the second analog input channel AIN1. The input voltage range on AIN1 is 0 to V_{DD}.
5	AIN0	Analog Input 0. In single-channel mode, this is the analog input and the input voltage range is 0 to V_{REF}. In dual-channel mode, it has an analog input range of 0 to V_{DD}.
6	DIN	Data In. Logic Input. Data to be written to the AD7887's Control Register is provided on this input and is clocked into the register on the rising edge of SCLK (see Control Register section). The AD7887 can be operated as a single-channel read-only ADC by tying the DIN line permanently to GND.
7	DOUT	Data Out. Logic Output. The conversion result from the AD7887 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream consists of four leading zeros followed by the 12 bits of conversion data, which is provided MSB first.
8	SCLK	Serial Clock. Logic Input. SCLK provides the serial clock for accessing data from the part and writing serial data to the Control Register. This clock input is also used as the clock source for the AD7887's conversion process.

TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1/2 LSB below the first code transition, and full scale, a point 1/2 LSB above the last code transition.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
This is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, i.e., AGND + 0.5 LSB.

Offset Error Match
This is the difference in Offset Error between any two channels.

Gain Error
This is the deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal (i.e., V_{REF} – 1.5 LSB) after the offset error has been adjusted out.

Gain Error Match
This is the difference in Gain Error between any two channels.

Track/Hold Acquisition Time
The track/hold amplifier returns into track mode at the end of conversion. Track/Hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion.

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$Signal\ to\ (Noise + Distortion) = (6.02\ N + 1.76)\ dB$$

Thus for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7887, it is defined as:

$$THD\ (dB) = 20 \log \frac{\sqrt{V_2^{\ 2} + V_3^{\ 2} + V_4^{\ 2} + V_5^{\ 2} + V_6^{\ 2}}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7887 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves, while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

Channel-to-Channel Isolation
Channel-to-channel isolation is a measure of the level of crosstalk between channels. It is measured by applying a full-scale 25 kHz sine wave signal to the nonselected input channel and determining how much that signal is attenuated in the selected channel. The figure given is the worst case across both channels for the AD7887.

PSR (Power Supply Rejection)
Variations in power supply will affect the full-scale transition, but not the converter's linearity. Power Supply Rejection is the maximum change in the full-scale transition point due to a change in power-supply voltage from the nominal value.

CONTROL REGISTER

The Control Register on the AD7887 is an 8-bit, write-only register. Data is loaded from the DIN pin of the AD7887 on the rising edge of SCLK. The data is transferred on the DIN line at the same time as the conversion result is read from the part. This requires 16 serial clocks for every data transfer. Only the information provided on the first eight rising clock edges (after $\overline{CS}$ falling edge) is loaded to the Control Register. MSB denotes the first bit in the data stream. The bit functions are outlined in Table I. The contents of the Control Register on power up is all zeros.

Table I. Control Register

MSB

DONTC	ZERO	REF	SIN/DUAL	CH	ZERO	PM1	PM0

Bit	Mnemonic	Comment
7	DONTC	Don't Care. The value written to this bit of the Control Register is a don't care, i.e., it doesn't matter if the bit is 0 or 1.
6	ZERO	A zero must be written to this bit to ensure correct operation of the AD7887.
5	REF	Reference Bit. With a 0 in this bit, the on-chip reference is enabled. With a 1 in this bit, the on-chip reference is disabled.
4	SIN/DUAL	Single/Dual Bit. This bit determines whether the AD7887 operates in single-channel or dual-channel mode. A 0 in this bit selects single-channel operation and the AIN1/V_{REF} pin assumes its V_{REF} function. A 1 in this bit selects dual-channel mode and the reference voltage for the ADC is internally connected to V_{DD} and the AIN1/V_{REF} pin assumes its AIN1 function as the second analog input channel. To obtain best performance from the AD7887, the internal reference should be disabled when operating in the dual channel mode, i.e., REF = 1.
3	CH	Channel Bit. When the part is selected for dual-channel mode, this bit determines which channel will be converted for the next conversion. A 0 in this bit selects the AIN0 input while a 1 in this bit selects the AIN1 input. In single-channel mode, this bit should always be 0.
2	ZERO	A zero must be written to this bit to ensure correct operation of the AD7887.
1, 0	PM1, PM0	Power Management Bits. These two bits decode the mode of operation of the AD7887 as described below.

Table II. Power Management Options

PM1	PM0	Mode
0	0	**Mode 1**. In this mode, the AD7887 enters shutdown if the $\overline{CS}$ input is 1 and is in full power mode when $\overline{CS}$ is 0. Thus the part comes out of shutdown on the falling edge of $\overline{CS}$ and enters shutdown on the rising edge of $\overline{CS}$.
0	1	**Mode 2**. In this mode, the AD7887 is always fully powered up, regardless of the status of any of the logic inputs.
1	0	**Mode 3**. In this mode, the AD7887 automatically enters shutdown mode at the end of each conversion, regardless of the state of $\overline{CS}$.
1	1	**Mode 4**. In this standby mode, portions of the AD7887 are powered down but the on-chip reference voltage remains powered up. This mode is similar to Mode 3, but allows the part to power up much faster. The REF bit should be 0 to ensure the on-chip reference is enabled.

PERFORMANCE CURVES

Figure 2 shows a typical FFT plot for the AD7887 at 125 kHz sample rate and 10 kHz input frequency.

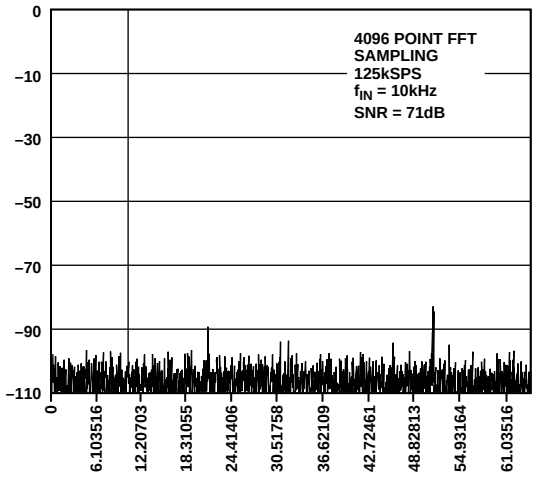


Figure 2. Dynamic Performance

Figure 3 shows the SNR vs. Frequency for a 5 V supply with a 5 V external reference.

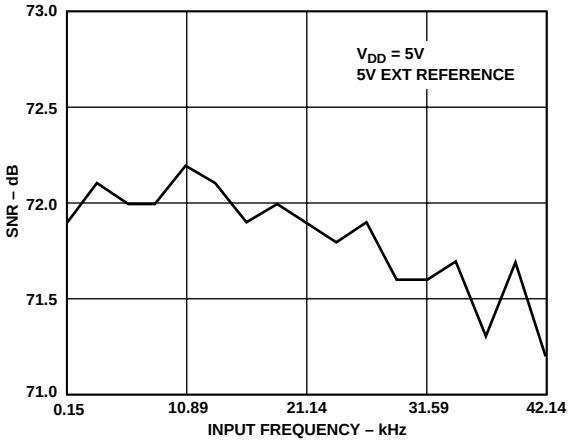


Figure 3. SNR vs. Input Frequency

Figure 4 shows the power supply rejection ratio versus frequency for the part. The power supply rejection ratio is defined as the ratio of the power in the ADC output at frequency f to the power of a full-scale sine wave applied to the ADC of frequency f_S:

$$PSRR\ (dB) = 10 \log (Pf/Pfs)$$

Pf = Power at frequency f in ADC output, *Pfs* = power at frequency f_S in ADC full-scale input. Here a 100 mV peak-to-peak sine wave is coupled onto the V_{DD} supply. Both the +2.7 V and +5.5 V supply performances are shown.

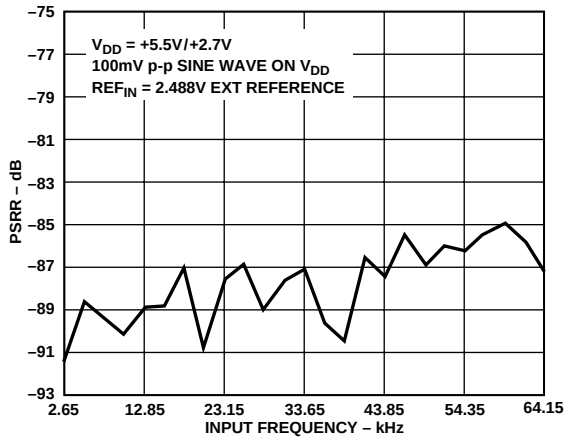


Figure 4. PSRR vs. Frequency

CIRCUIT INFORMATION

The AD7887 is a fast, low power, 12-bit, single supply, single-channel/dual-channel A/D converter. The part can be operated from a +3 V (+2.7 V to +3.6 V) supply or from a +5 V (+4.75 V to +5.25 V) supply. When operated from either a +5 V or +3 V supply, the AD7887 is capable of throughput rates of 125 kSPS when provided with a 2 MHz clock.

The AD7887 provides the user with an on-chip track/hold, A/D converter, reference and serial interface housed in an 8-lead package. The serial clock input accesses data from the part and also provides the clock source for the successive approximation A/D converter. The part can be configured for single-channel or dual-channel operation. When configured as a single-channel part, the analog input range is 0 to V_{REF} (where the externally-applied V_{REF} can be between +1.2 V and V_{DD}). When the AD7887 is configured for two input channels, the input range is determined by internal connections to be 0 to V_{DD}.

If single-channel operation is required, the AD7887 can be operated in a read-only mode by tying the DIN line permanently to GND. For applications where the user wants to change the mode of operation or wants to operate the AD7887 as a dual-channel A/D converter, the DIN line can be used to clock data into the part's control register.

CONVERTER OPERATION

The AD7887 is a successive approximation analog-to-digital converter based around a charge redistribution DAC. Figures 5 and 6 show simplified schematics of the ADC. Figure 5 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in position A, the comparator is held in a balanced condition and the sampling capacitor acquires the signal on AIN.

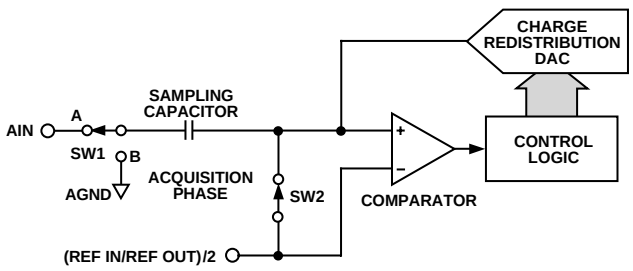


Figure 5. ADC Acquisition Phase

When the ADC starts a conversion (see Figure 6), SW2 will open and SW1 will move to Position B causing the comparator to become unbalanced. The control logic and the charge redistribution DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced the conversion is complete. The control logic generates the ADC output code. Figure 7 shows the ADC transfer function.

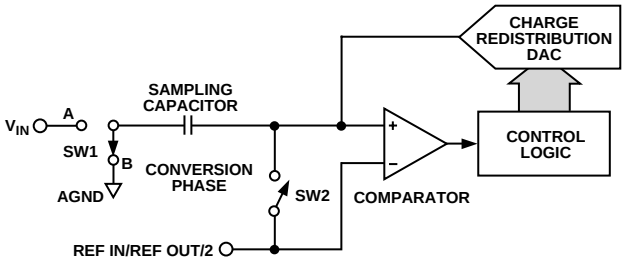


Figure 6. ADC Conversion Phase

ADC TRANSFER FUNCTION

The output coding of the AD7887 is straight binary. The designed code transitions occur at successive integer LSB values (i.e., 1 LSB, 2 LSBs, etc.). The LSB size is = V_{REF}/4096. The ideal transfer characteristic for the AD7887 is shown in Figure 7.

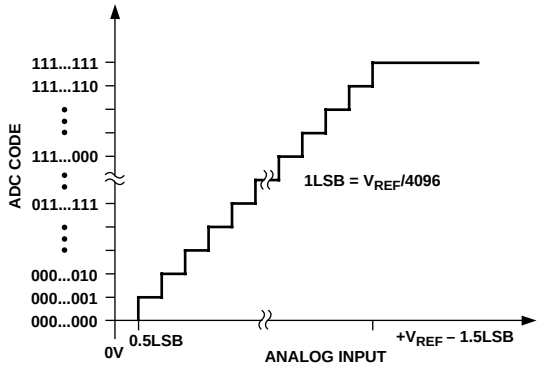


Figure 7. Transfer Characteristic

TYPICAL CONNECTION DIAGRAM

Figure 8 shows a typical connection diagram for the AD7887. The GND pin is connected to the analog ground plane of the system. The part is in dual-channel mode so V_{REF} is internally connected to a well decoupled V_{DD} pin to provide an analog input range of 0 V to V_{DD}. The conversion result is output in a 16-bit word with four leading zeros followed by the MSB of the 12-bit result. For applications where power consumption is of concern, the automatic power-down at the end of conversion should be used to improve power performance. See Modes of Operation section of the data sheet.

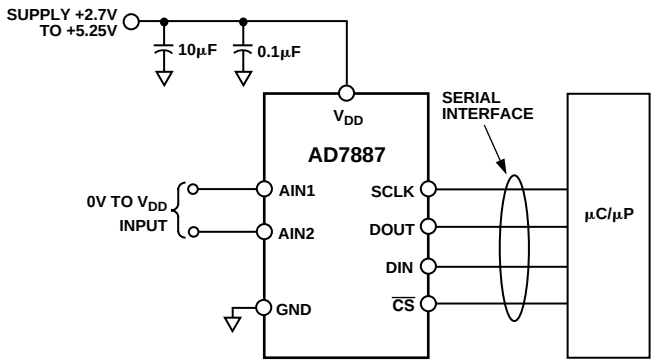


Figure 8. Typical Connection Diagram

Analog Input

Figure 9 shows an equivalent circuit of the analog input structure of the AD7887. The two diodes D1 and D2 provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 200 mV. This will cause these diodes to become forward biased and start conducting current into the substrate. 20 mA is the maximum current these diodes can conduct without causing irreversible damage to the part. However, it is worth noting that a small amount of current (1 mA) being conducted into the substrate due to an overvoltage on an unselected channel can cause inaccurate conversions on a selected channel. The capacitor C1 in Figure 9 is typically about 4 pF and can primarily be attributed to pin capacitance. The resistor R1 is a lumped component made up of the on resistance of a multiplexer and a switch. This resistor is typically about 100 Ω. The capacitor C2 is the ADC sampling capacitor and typically has a capacitance of 20 pF.

Note: The analog input capacitance seen when in track mode is typically 38 pF while in hold mode it is typically 4 pF.

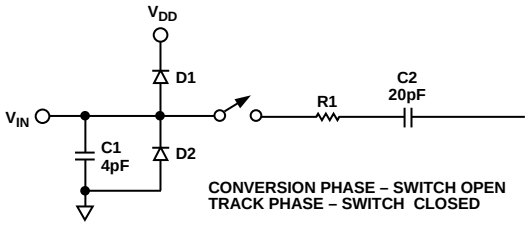


Figure 9. Equivalent Analog Input Circuit

For ac applications, removing high frequency components from the analog input signal is recommended by use of an RC low-pass filter on the relevant analog input pin. In applications where harmonic distortion and signal to noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances will significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the op amp will be a function of the particular application.

When no amplifier is used to drive the analog input the source impedance should be limited to low values. The maximum source impedance will depend on the amount of total harmonic distortion (THD) that can be tolerated. The THD will increase

as the source impedance increases and performance will degrade. Figure 10 shows a graph of the total harmonic distortion versus analog input signal frequency for different source impedances.

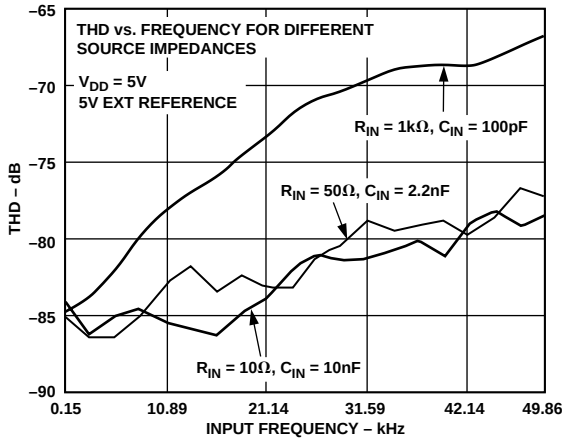


Figure 10. THD vs. Analog Input Frequency

On-Chip Reference

The AD7887 has an on-chip 2.5 V reference. This reference can be enabled or disabled by clearing or setting the REF bit in the control register respectively. If the on-chip reference is to be used externally in a system then it must be buffered before it is applied elsewhere. If an external reference is applied to the device, then the internal reference is automatically overdriven. However, it is advised to disable the internal reference by setting the REF bit in the control register when an external reference is applied in order to obtain optimum performance from the device. When the internal reference is disabled, SW1 in Figure 11 will open and the input impedance seen at the AIN1/V_{REF} pin is the input impedance of the reference buffer, which is in the region of gigaohms. When the internal reference is enabled the input impedance seen at the pin is typically 10 kΩ. When the AD7887 is operated in two-channel mode, the reference is taken from V_{DD} internally and not from the on-chip 2.5 V reference.

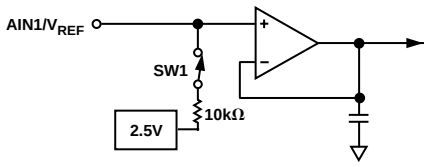


Figure 11. On-Chip Reference Circuitry

POWER-DOWN OPTIONS

The AD7887 provides flexible power management to allow the user to achieve the best power performance for a given throughput rate.

The power management options are selected by programming the power management bits (i.e., PM1 and PM0) in the control register. Table II summarizes the available options. When the power management bits are programmed for either of the auto power-down modes, the part will enter power-down mode on the 16th rising SCLK edge after the falling edge of $\overline{CS}$. The first falling SCLK edge after the $\overline{CS}$ falling edge will cause the part to power up again. When the AD7887 is in Mode 1, i.e., PM1 = PM0 = 0, the part will enter shutdown on the rising edge of $\overline{CS}$ and power up from shutdown on the falling edge of $\overline{CS}$. If $\overline{CS}$ is brought high during the conversion in this mode, the part will immediately enter shutdown.

Power-Up Times

The AD7887 has an approximate 1 µs power-up time when powering up from standby or when using an external reference. When V_{DD} is first connected the AD7887 will power up in Mode 1, i.e., PM1 = PM0 = 0. The part is put into shutdown on the rising edge of $\overline{CS}$ in this mode. A subsequent power-up from shutdown will take approximately 5 µs. The AD7887 wake-up time is very short in the autostandby mode so it is possible to wake-up the part and carry out a valid conversion in the same read/write operation.

POWER VS. THROUGHPUT RATE

By operating the AD7887 in autoshutdown, autostandby mode or Mode 1, the average power consumption of the AD7887 decreases at lower throughput rates. Figure 12 shows how, as the throughput rate is reduced, the device remains in its power-down state longer and the average power consumption over time drops accordingly.

For example if the AD7887 is operated in a continuous sampling mode with a throughput rate of 10 kSPS and a SCLK of 2 MHz (V_{DD} = 5 V), and if PM1 = 1 and PM0 = 0, i.e., the device is in autoshutdown mode, and the on-chip reference is used, the power consumption is calculated as follows. The power dissipation during normal operation is 3.5 mW (V_{DD} = 5 V). If the power-up time is 5 µs, and the remaining conversion plus acquisition time is 15.5 t_{SCLK}, i.e., approximately 7.75 µs, (see Figure 15a), the AD7887 can be said to dissipate 3.5 mW for 12.75 µs during each conversion cycle. If the throughput rate is 10 kSPS, the cycle time is 100 µs and the average power dissipated during each cycle is (12.75/100) × (3.5 mW) = 446.25 µW. If V_{DD} = 3 V, SCLK = 2 MHz and the device is again in autoshutdown mode using the on-chip reference, then the power dissipation during normal operation is 2.1 mW. The AD7887 can now be said to dissipate 2.1 mW for 12.75 µs during each conversion cycle. With a throughput rate of 10 kSPS, the average power dissipated during each cycle is (12.75/100) × (2.1 mW) = 267.75 µW. Figure 12 shows the Power vs. Throughput Rate for automatic shutdown with both 5 V and 3 V supplies.

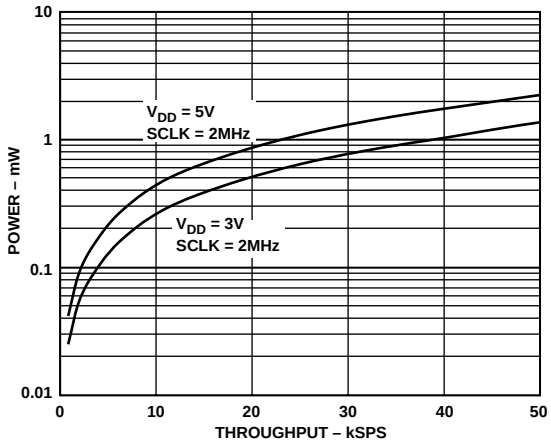


Figure 12. Power vs. Throughput

MODES OF OPERATION

The AD7887 has a number of different modes of operation. These are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/throughput rate ratio for differing application requirements. The modes of operation are controlled by the PM1 and PM0 bits of the Control Register as previously outlined. For read-only operation of the AD7887, the default mode of all 0s in the Control Register can be set up by tying the DIN line permanently low.

Mode 1 (PM1 = 0, PM0 = 0)

This mode allows the user to control the powering down of the part via the $\overline{CS}$ pin. Whenever $\overline{CS}$ is low, the AD7887 is fully powered up; whenever $\overline{CS}$ is high, the AD7887 is in full shutdown. When $\overline{CS}$ goes from high to low, all on-chip circuitry starts to power up. It takes approximately, 5 µs for the AD7887 internal circuitry to be fully powered up. As a result, a conversion (or sample-and-hold acquisition) should not be initiated during this 5 µs.

Figure 13 shows a general diagram of the operation of the AD7887 in this mode. The input signal is sampled on the second rising edge of SCLK following the $\overline{CS}$ falling edge. The user should ensure that 5 µs elapses between the falling edge of $\overline{CS}$ and the second rising edge of SCLK. In microcontroller applications, this is readily achievable by driving the $\overline{CS}$ input from one of the port lines and ensuring that the serial data read (from the microcontrollers serial port) is not initiated for 5 µs. In DSP applications, where the $\overline{CS}$ is generally derived from the serial frame synchronization line, it is usually not possible to separate the $\overline{CS}$ falling edge and second SCLK rising edge by up to 5 µs without affecting the speed of the rest of the serial clock. Therefore, the user will need to write to the Control Register to exit this mode and (by writing PM1 = 0 and PM0 = 1) put the part into Mode 2, i.e., normal mode. A second conversion will then need to be initiated when the part is powered-up to get a conversion result. The write operation which takes place in conjunction with this second conversion can put the part back into Mode 1 and the part will go into power-down mode when $\overline{CS}$ returns high.

Mode 2 (PM1 = 0, PM0 = 1)

In this mode of operation, the AD7887 remains fully powered up regardless of the status of the $\overline{CS}$ line. It is intended for fastest throughput rate performance as the user does not have to worry about the 5 µs power-up time previously mentioned. Figure 14 shows the general diagram of the operation of the AD7887 in this mode.

The data presented to the AD7887 on the DIN line during the first eight clock cycles of the data transfer are loaded to the Control Register. To continue to operate in this mode, the user must ensure that PM1 is loaded with 0 and PM0 is loaded with 1 on every data transfer.

The falling edge of $\overline{CS}$ initiates the sequence and the input signal is sampled on the second rising edge of the SCLK input. Sixteen serial clock cycles are required to complete the conversion and access the conversion result. Once a data transfer is complete ($\overline{CS}$ has returned high), another conversion can be initiated immediately by bringing $\overline{CS}$ low again.

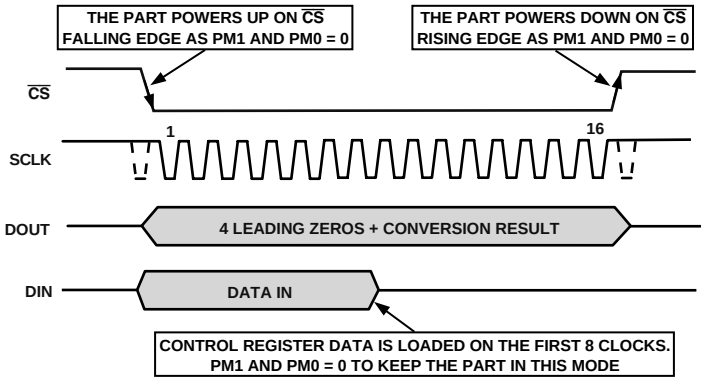


Figure 13. Mode 1 Operation

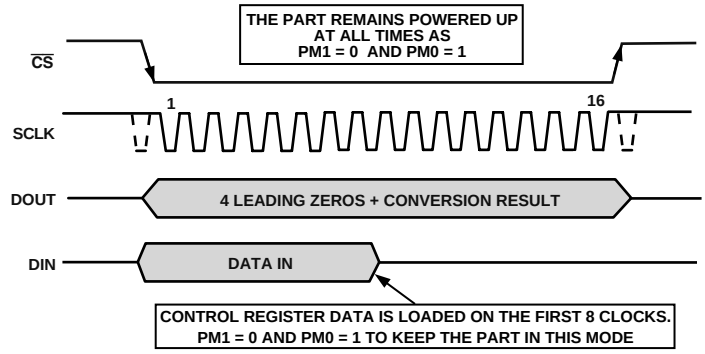


Figure 14. Mode 2 Operation

Mode 3 (PM1 = 1, PM0 = 0)

In this mode, the AD7887 automatically enters its full shutdown mode at the end of every conversion. It is similar to Mode 1 except that the status of $\overline{CS}$ does not have any effect on the power-down status of the AD7887.

Figure 15a shows the general diagram of the operation of the AD7887 in this mode. On the first falling SCLK edge after $\overline{CS}$ goes low, all on-chip circuitry starts to power up. It takes approximately, 5 µs for the AD7887 internal circuitry to be fully powered up. As a result, a conversion (or sample-and-hold acquisition) should not be initiated during this 5 µs. The input signal is sampled on the second rising edge of SCLK following the $\overline{CS}$ falling edge. The user should ensure that 5 µs elapses between the first falling edge of $\overline{SCLK}$ and the second rising edge of SCLK after the $\overline{CS}$ falling edge as shown in Figure 15a. In microcontroller applications (or with a slow serial clock) this is readily achievable by driving the $\overline{CS}$ input from one of the port lines and ensuring that the serial data read (from the microcontroller's serial port) is not initiated for 5 µs. However, for higher speed serial clocks it will not be possible to have a 5 µs delay between powering up and the first rising edge of the SCLK. Therefore, the user will need to write to the Control Register to exit this mode and (by writing PM1 = 0 and PM0 = 1) put the part into Mode 2. A second conversion will then need to be initiated when the part is powered up to get a conversion result, as shown in Figure 15b. The write operation that takes place in conjunction with this second conversion can put the part back into Mode 3 and the part will go into power-down mode when the conversion sequence ends.

Mode 4 (PM1 = 1, PM0 = 1)

In this mode, the AD7887 automatically enters a standby (or sleep) mode at the end of every conversion. In this standby mode, all on-chip circuitry, apart from the on-chip reference, is powered down. This mode is similar to Mode 3 but in this case, the power-up time is much shorter as the on-chip reference remains powered up at all times.

Figure 16 shows the general diagram of the operation of the AD7887 in this mode. On the first falling SCLK edge after $\overline{CS}$ goes low, the AD7887 comes out of standby. The AD7887 wake-up time is very short in this mode so it is possible to wake-up the part and carry out a valid conversion in the same read/write operation. The input signal is sampled on the second rising edge of SCLK following the $\overline{CS}$ falling edge. At the end of conversion (last rising edge of SCLK) the part automatically enters its standby mode.

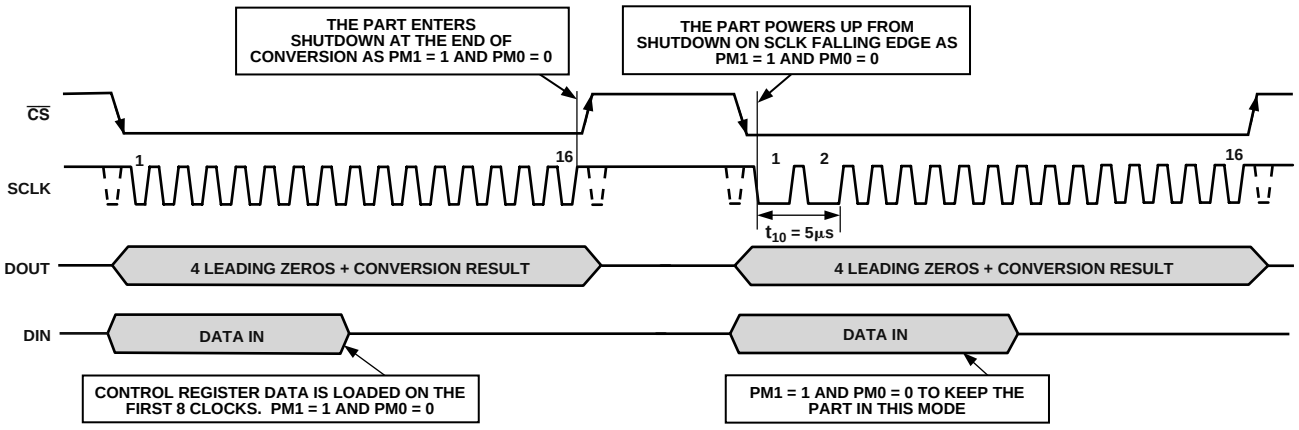


Figure 15a. Mode 3 Operation

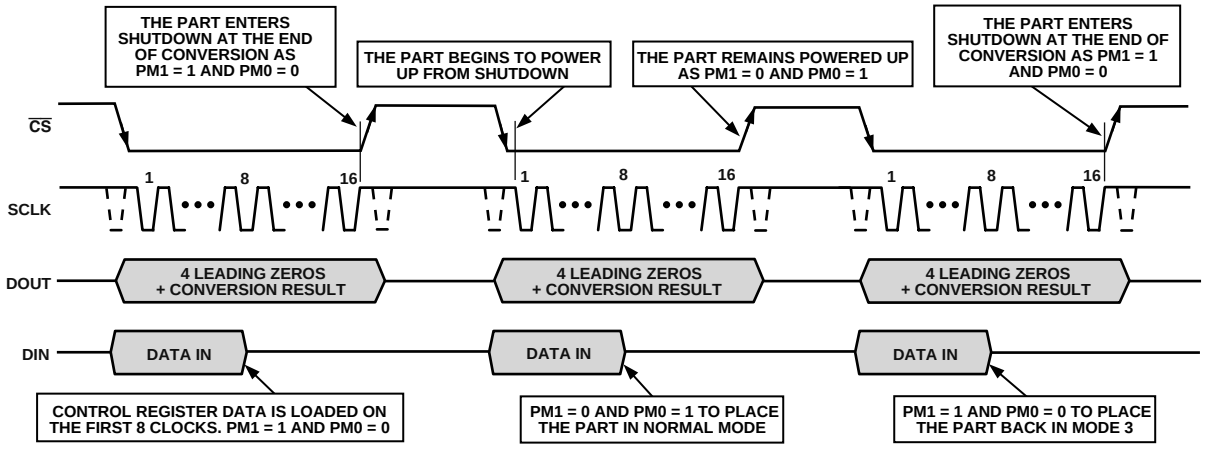


Figure 15b. Mode 3 Operation

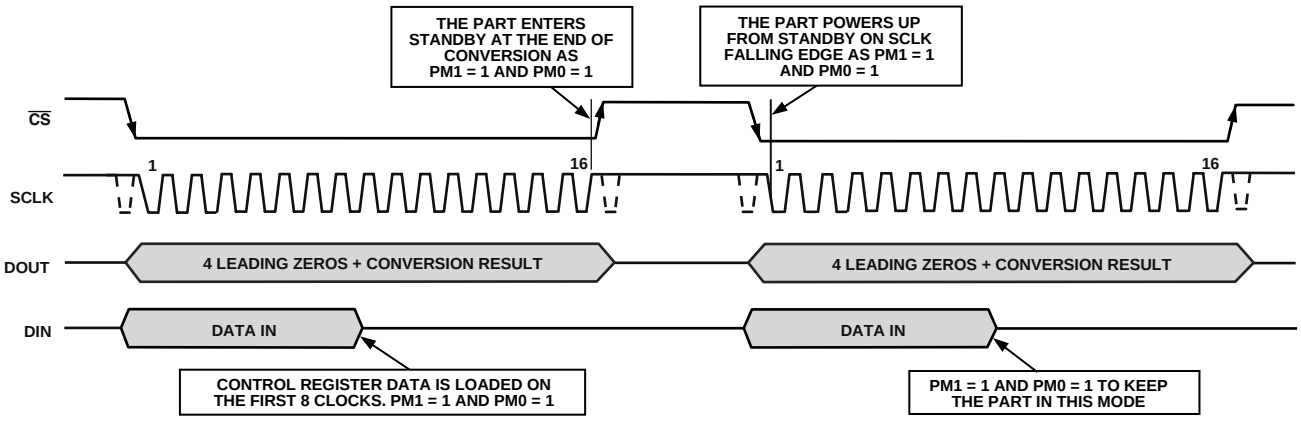


Figure 16. Mode 4 Operation

SERIAL INTERFACE

Figure 17 shows the detailed timing diagrams for serial interfacing to the AD7887. The serial clock provides the conversion clock and also controls the transfer of information to and from the AD7887 during conversion.

$\overline{CS}$ initiates the data transfer and conversion process. For some modes, the falling edge of $\overline{CS}$ wakes up the part. In all cases, it gates the serial clock to the AD7887 and puts the on-chip track/hold into track mode. The input signal is sampled on the second rising edge of the SCLK input after the falling edge of $\overline{CS}$. Thus, the first one and one-half clock cycles after the falling edge of $\overline{CS}$ are when the acquisition of the input signal takes place. This time is denoted as the acquisition time (t_{ACQ}). In modes where the falling edge of $\overline{CS}$ wakes up the part, the acquisition time must allow for the wake-up time of 5 μs. The on-chip track/hold goes from track mode to hold mode on the second rising edge of SCLK and a conversion is also initiated on this edge. The conversion process takes a further fourteen and one-half SCLK cycles to complete. The rising edge of $\overline{CS}$ will put the bus back into three-state. If $\overline{CS}$ is left low a new conversion will be initiated.

In dual-channel operation, the input channel that is sampled is the one that was selected in the previous write to the Control Register. Thus, in dual-channel operation the user must write ahead the channel for conversion. In other words, the user must write the channel address for the next conversion while the present conversion is in progress.

Writing of information to the Control Register takes place on the first eight rising edges of SCLK in a data transfer. The Control Register is always written to when a data transfer takes place. However, the AD7887 can be operated in a read-only mode by tying DIN low, thereby loading all 0s to the Control Register every time. When operating the AD7887 in write/read mode, the user must be careful to always set up the correct information on the DIN line when reading data from the part.

Sixteen serial clock cycles are required to perform the conversion process and to access data from the AD7887. In applications where the first serial clock edge, following $\overline{CS}$ going low, is a falling edge, this edge clocks out the first leading zero. Thus, the first rising clock edge on the SCLK clock has the first leading zero provided. In applications where the first serial clock edge, following $\overline{CS}$ going low, is a rising edge, the first leading zero may not be set up in time for the processor to read it correctly. However, subsequent bits are clocked out on the falling edge of SCLK so that they are provided to the processor on the following rising edge. Thus, the second leading zero is clocked out on the falling edge subsequent to the first rising edge. The final bit in the data transfer is valid on the sixteenth rising edge, having being clocked out on the previous falling edge.

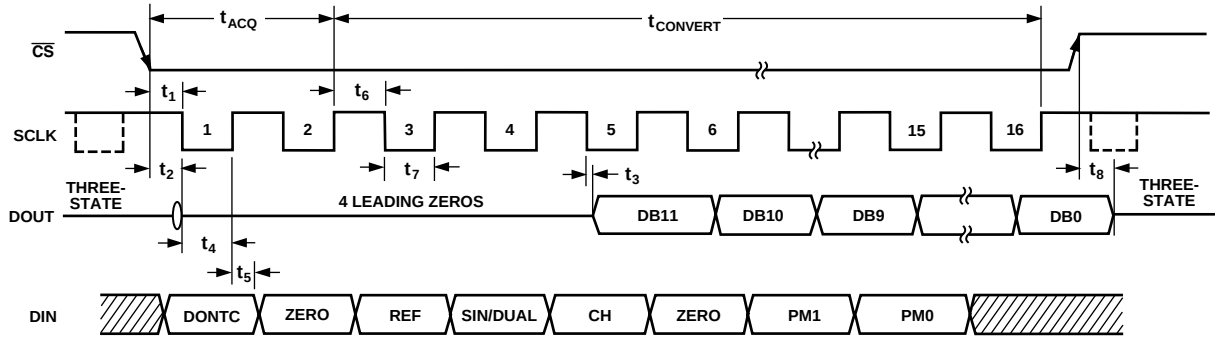


Figure 17. Serial Interface Timing Diagram

MICROPROCESSOR INTERFACING

The serial interface on the AD7887 allows the part to be directly connected to a range of many different microprocessors. This section explains how to interface the AD7887 with some of the more common microcontroller and DSP serial interface protocols.

AD7887 to TMS320C5x

The serial interface on the TMS320C5x uses a continuous serial clock and frame synchronization signals to synchronize the data transfer operations with peripheral devices like the AD7887. The $\overline{CS}$ input allows easy interfacing with an inverter between the serial clock of the TMS320C5x and the AD7887 being the only glue logic required. The serial port of the TMS320C5x is set up to operate in burst mode with internal CLKX (TX serial clock) and FSX (TX frame sync). The serial port control register (SPC) must have the following setup: FO = 0, FSM = 1, MCM = 1 and TXM = 1. The connection diagram is shown in Figure 18.

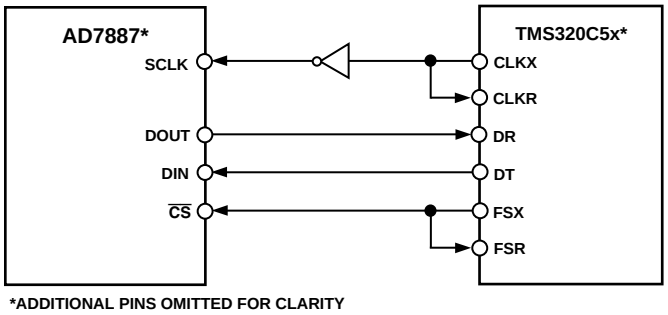


Figure 18. Interfacing to the TMS320C5x

AD7887 to ADSP-21xx

The ADSP-21xx family of DSPs are easily interfaced to the AD7887 with an inverter between the serial clock of the ADSP-21xx and the AD7887. This is the only glue logic required. The SPORT control register should be set up as follows:

TFSW = RFSW = 1, Alternate Framing
INVRFS = INVTFS = 1, Active Low Frame Signal
DTYPE = 00, Right Justify Data
SLEN = 1111, 16-Bit Data Words
ISCLK = 1, Internal Serial Clock
TFSR = RFSR = 1, Frame Every Word
IRFS = 0
ITFS = 1

The connection diagram is shown in Figure 19. The ADSP-21xx has the TFS and RFS of the SPORT tied together, with TFS set as an output and RFS set as an input. The DSP operates in Alternate Framing Mode and the SPORT control register is set up as described. The Frame synchronization signal generated on the TFS is tied to $\overline{CS}$ and as with all signal processing applications equidistant sampling is necessary. In this example however, the timer interrupt is used to control the sampling rate of the ADC and under certain conditions, equidistant sampling may not be achieved.

The Timer registers etc., are loaded with a value that will provide an interrupt at the required sample interval. When an interrupt is received, a value is transmitted with TFS/DT (ADC control word). The TFS is used to control the RFS and hence the reading of data. The frequency of the serial clock is set in the SCLKDIV register. When the instruction to transmit with TFS is given (i.e., AX0 = TX0), the state of the SCLK is checked. The DSP will wait until the SCLK has gone High, Low and High before transmission will start. If the timer and SCLK values are chosen such that the instruction to transmit occurs on or near the rising edge of SCLK, the data may be transmitted or it may wait until the next clock edge.

For example, the ADSP-2111 has a master clock frequency of 16 MHz. If the SCLKDIV register is loaded with the value 3 then a SCLK of 2 MHz is obtained, and 8 master clock periods will elapse for every 1 SCLK period. If the timer registers are loaded with the value 803, then 100.5 SCLKs will occur between interrupts and subsequently between transmit instructions. This situation will result in nonequidistant sampling as the transmit instruction is occurring on an SCLK edge. If the number of SCLKs between interrupts is a whole integer number of N, equidistant sampling will be implemented by the DSP.

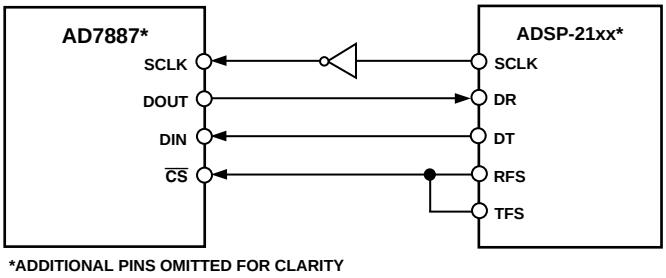


Figure 19. Interfacing to the ADSP-21xx

AD7887 to DSP56xxx

The connection diagram in Figure 20 shows how the AD7887 can be connected to the SSI (Synchronous Serial Interface) of the DSP56xxx family of DSPs from Motorola. The SSI is operated in Synchronous Mode (SYN bit in CRB = 1) with internally generated 1-bit clock period frame sync for both TX and RX (Bits FSL1 =1 and FSL0 =0 in CRB). Set the word length to 16 by setting bits WL1 = 1 and WL0 = 0 in CRA. An inverter is also necessary between the SCLK from the DSP56xxx and the SCLK pin of the AD7887 as shown in Figure 20.

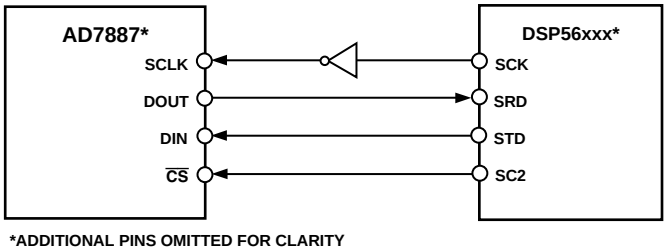


Figure 20. Interfacing to the DSP56xxx

AD7887 to MC68HC11

The Serial Peripheral Interface (SPI) on the MC68HC11 is configured for Master Mode (MSTR = 1), Clock Polarity Bit (CPOL) = 1 and the Clock Phase Bit (CPHA) = 1. The SPI is configured by writing to the SPI Control Register (SPCR)—see 68HC11 user manual. The serial transfer will take place as two 8-bit operations. A connection diagram is shown in Figure 21.

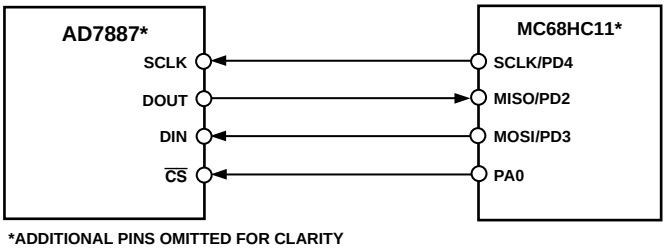


Figure 21. Interfacing to the MC68HC11

AD7887 to 8051

It is possible to implement a serial interface using the data ports on the 8051. This allows a full duplex serial transfer to be implemented. The technique involves "bit-banging" an I/O port (e.g., P1.0) to generate a serial clock and using two other I/O ports (e.g., P1.1 and P1.2) to shift data in and out—see Figure 22.

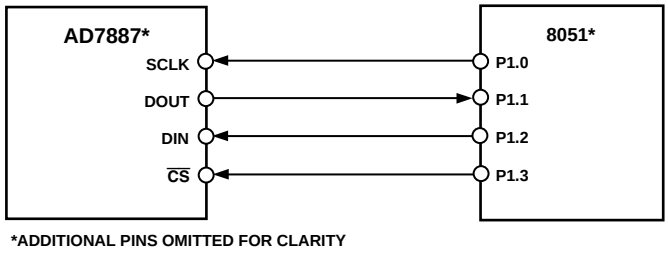


Figure 22. Interfacing to the 8051 Using I/O Ports

AD7887 to PIC16C6x/7x

The PIC16C6x Synchronous Serial Port (SSP) is configured as an SPI Master with the Clock Polarity Bit = 1. This is done by writing to the Synchronous Serial Port Control Register (SSPCON). See user *PIC16/17 Microcontroller User Manual*. Figure 23 shows the hardware connections needed to interface to the PIC16C6x/7x. In this example I/O port RA1 is being used to pulse $\overline{CS}$. This microcontroller only transfers eight bits of data during each serial transfer operation. Therefore two consecutive read/write operations are needed.

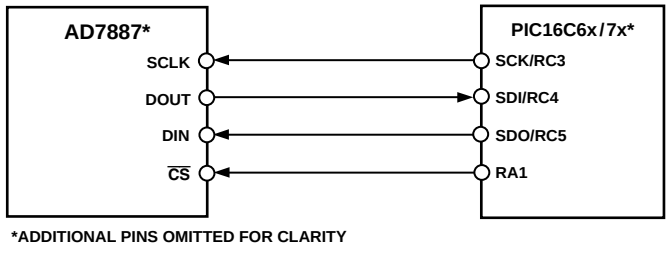


Figure 23. Interfacing to the PIC16C6x/7x

APPLICATION HINTS

Grounding and Layout

The AD7887 has very good immunity to noise on the power supplies as can be seen in Figure 4. However, care should still be taken with regard to grounding and layout.

The printed circuit board that houses the AD7887 should be designed so the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. A minimum etch technique is generally best for ground planes as it gives the best shielding. Digital and analog ground planes should be joined in only one place, as close as possible to the GND pin of the AD7887. If the AD7887 is in a system where multiple devices require AGND-to-DGND connections, the connection should still be made at one point only, a star ground point, which should be established as close as possible to the AD7887.

Avoid running digital lines under the device as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7887 to avoid noise coupling. The power supply lines to the AD7887 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never be run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feedthrough through the board. A microstrip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes while signals are placed on the solder side.

Good decoupling is also important. All analog supplies should be decoupled with 10 μF tantalum in parallel with 0.1 μF capacitors to AGND. To achieve the best from these decoupling components, they must be placed as close as possible to the device, ideally right up against the device.

Evaluating the AD7887 Performance

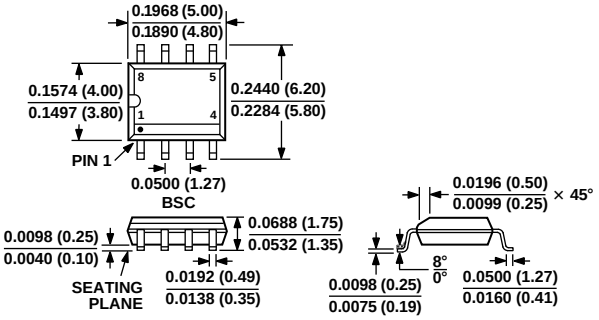
The recommended layout for the AD7887 is outlined in the evaluation board for the AD7887. The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from the PC via the EVAL-CONTROL BOARD. The EVAL-CONTROL BOARD can be used in conjunction with the AD7887 Evaluation board, as well as many other Analog Devices evaluation boards ending in the CB designator, to demonstrate/evaluate the ac and dc performance of the AD7887.

The software allows the user to perform ac (fast Fourier transform) and dc (histogram of codes) tests on the AD7887.

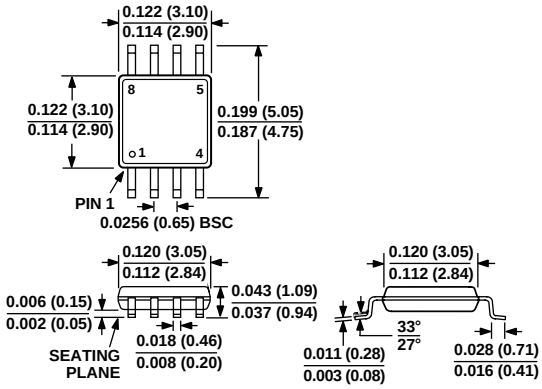
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead Narrow Body (SOIC)
(SO-8)



8-Lead μSOIC
(RM-8)



C3477b–2–9/99

PRINTED IN U.S.A.