14-Bit, 105 MSPS/125 MSPS, 1.8 V Analog-to-Digital Converter

AD9246

FEATURES

1.8 V analog supply operation
1.8 V to 3.3 V output supply
SNR = 71.7 dBc (72.7 dBFS) to 70 MHz input
SFDR = 85 dBc to 70 MHz input
Low power: 395 mW @ 125 MSPS
Differential input with 650 MHz bandwidth
On-chip voltage reference and sample-and-hold amplifier
DNL = ±0.5 LSB
Flexible analog input: 1 V p-p to 2 V p-p range
Offset binary, Gray code, or twos complement data format
Clock duty cycle stabilizer
Data output clock
Serial port control
- **Built-in selectable digital test pattern generation**
- **Programmable clock and data alignment**

APPLICATIONS

Ultrasound equipment
IF sampling in communications receivers
- **IS-95, CDMA-One, IMT-2000**

Battery-powered instruments
Hand-held scopemeters
Low cost digital oscilloscopes

GENERAL DESCRIPTION

The AD9246 is a monolithic, single 1.8 V supply, 14-bit, 105 MSPS/ 125 MSPS analog-to-digital converter (ADC), featuring a high performance sample-and-hold amplifier (SHA) and on-chip voltage reference. The product uses a multistage differential pipeline architecture with output error correction logic to provide 14-bit accuracy at 125 MSPS data rates and guarantees no missing codes over the full operating temperature range.

The wide bandwidth, truly differential SHA allows a variety of user-selectable input ranges and offsets, including single-ended applications. It is suitable for multiplexed systems that switch full-scale voltage levels in successive channels and for sampling single-channel inputs at frequencies well beyond the Nyquist rate. Combined with power and cost savings over previously available ADCs, the AD9246 is suitable for applications in communications, imaging, and medical ultrasound.

A differential clock input controls all internal conversion cycles. A duty cycle stabilizer (DCS) compensates for wide variations in the clock duty cycle while maintaining excellent overall ADC performance.

FUNCTIONAL BLOCK DIAGRAM

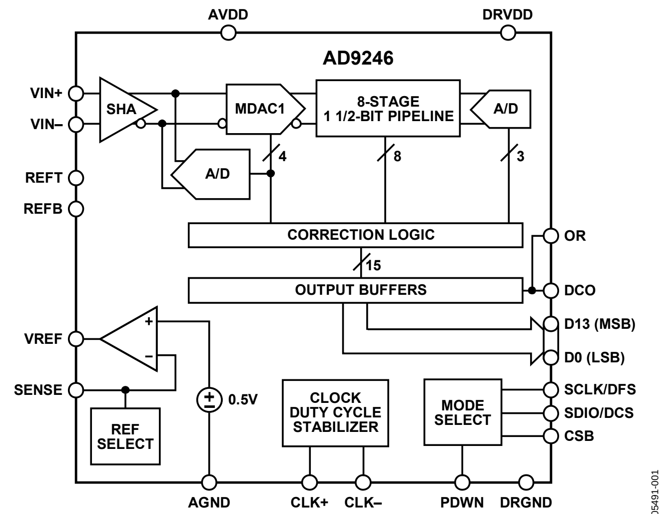

Figure 1.

The digital output data is presented in offset binary, Gray code, or twos complement formats. A data output clock (DCO) is provided to ensure proper latch timing with receiving logic.

The AD9246 is available in a 48-lead LFCSP and is specified over the industrial temperature range (–40°C to +85°C).

PRODUCT HIGHLIGHTS

1. The AD9246 operates from a single 1.8 V power supply and features a separate digital output driver supply to accommodate 1.8 V to 3.3 V logic families.
2. The patented SHA input maintains excellent performance for input frequencies up to 225 MHz.
3. The clock DCS maintains overall ADC performance over a wide range of clock pulse widths.
4. A standard serial port interface supports various product features and functions, such as data formatting (offset binary, twos complement, or Gray coding), enabling the clock DCS, power-down, and voltage reference mode.
5. The AD9246 is pin compatible with the AD9233, allowing a simple migration from 12 bits to 14 bits.

Rev. 0

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REVISION HISTORY

4/06—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

AVDD = 1.8 V; DRVDD = 2.5 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = −1.0 dBFS, DCS enabled, unless otherwise noted.

Table 1.

Parameter	Temp	AD9246BCPZ-105 Min	AD9246BCPZ-105 Typ	AD9246BCPZ-105 Max	AD9246BCPZ-125 Min	AD9246BCPZ-125 Typ	AD9246BCPZ-125 Max	Unit
RESOLUTION	Full	14			14			Bits
ACCURACY								
No Missing Codes	Full		Guaranteed			Guaranteed		
Offset Error	Full		±0.3	±0.8		±0.3	±0.8	% FSR
Gain Error	Full		±0.6	±5.0		±0.6	±4.2	% FSR
Differential Nonlinearity (DNL)[1]	Full			±1.0			±1.0	LSB
	25°C		±0.4			±0.4		LSB
Integral Nonlinearity (INL)[1]	Full			±5.0			±5.0	LSB
	25°C		±1.3			±1.5		LSB
TEMPERATURE DRIFT								
Offset Error	Full		±15			±15		ppm/°C
Gain Error	Full		±95			±95		ppm/°C
INTERNAL VOLTAGE REFERENCE								
Output Voltage Error (1 V Mode)	Full		±5	±35		±5	±35	mV
Load Regulation @ 1.0 mA	Full		7			7		mV
INPUT REFERRED NOISE								
VREF = 1.0 V	25°C		1.3			1.3		LSB rms
ANALOG INPUT								
Input Span, VREF = 1.0 V	Full		2			2		V p-p
Input Capacitance[2]	Full		8			8		pF
REFERENCE INPUT RESISTANCE	Full		6			6		kΩ
POWER SUPPLIES								
Supply Voltage								
AVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD	Full	1.7	2.5	3.6	1.7	2.5	3.6	V
Supply Current								
IAVDD[1]	Full		178			220		mA
IDRVDD[1](1.8 V)	Full		9			11		mA
IDRVDD[1] (3.3 V)	Full		16			19		mA
POWER CONSUMPTION								
DC Input	Full		320	350		395	425	mW
Sine Wave Input[1] (DRVDD = 1.8 V)	Full		337			415		mW
Sine Wave Input[1] (DRVDD = 3.3 V)	Full		373			458		mW
Standby Power[3]	Full		40			40		mW
Power-Down Power	Full		1.8			1.8		mW

[1] Measured with a low input frequency, full-scale sine wave, with approximately 5 pF loading on each output bit.
[2] Input capacitance refers to the effective capacitance between one differential input pin and AGND. Refer to Figure 4 for the equivalent analog input structure.
[3] Standby power is measured with a dc input, the CLK pin inactive (set to AVDD or AGND).

AC SPECIFICATIONS

AVDD = 1.8 V; DRVDD = 2.5 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = −1.0 dBFS, DCS enabled, unless otherwise noted.

Table 2.

Parameter[1]	Temp	AD9246BCPZ-105 Min	AD9246BCPZ-105 Typ	AD9246BCPZ-105 Max	AD9246BCPZ-125 Min	AD9246BCPZ-125 Typ	AD9246BCPZ-125 Max	Unit
SIGNAL-TO-NOISE-RATIO (SNR)								
f_{IN} = 2.4 MHz	25°C		71.9			71.9		dBc
f_{IN} = 70 MHz	25°C		71.9			71.7		dBc
	Full			69.5			69.5	dBc
f_{IN} = 100 MHz	25°C		71.6			71.6		dBc
f_{IN} = 170 MHz	25°C		70.9			70.8		dBc
SIGNAL-TO-NOISE AND DISTORTION (SINAD)								
f_{IN} = 2.4 MHz	25°C		71.1			71.1		dBc
f_{IN} = 70 MHz	25°C		70.8			70.6		dBc
	Full			68.5			68.5	dBc
f_{IN} = 100 MHz	25°C		70.6			70.6		dBc
f_{IN} = 170 MHz	25°C		69.9			69.8		dBc
EFFECTIVE NUMBER OF BITS (ENOB)								
f_{IN} = 2.4 MHz	25°C		11.7			11.7		Bits
f_{IN} = 70 MHz	25°C		11.6			11.6		Bits
f_{IN} = 100 MHz	25°C		11.6			11.6		Bits
f_{IN} = 170 MHz	25°C		11.5			11.5		Bits
WORST SECOND OR THIRD HARMONIC								
f_{IN} = 2.4 MHz	25°C		90			90		dBc
f_{IN} = 70 MHz	25°C		85			85		dBc
	Full			73			73	dBc
f_{IN} = 100 MHz	25°C		85			85		dBc
f_{IN} = 170 MHz	25°C		83.5			83		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)								
f_{IN} = 2.4 MHz	25°C		90			90		dBc
f_{IN} = 70 MHz	25°C		85			85		dBc
	Full			73			73	dBc
f_{IN} = 100 MHz	25°C		85			85		dBc
f_{IN} = 170 MHz	25°C		83.5			83		dBc
WORST OTHER (HARMONIC OR SPUR)								
f_{IN} = 2.4 MHz	25°C		90			90		dBc
f_{IN} = 70 MHz	25°C		90			90		dBc
	Full			80			80	dBc
f_{IN} = 100 MHz	25°C		90			90		dBc
f_{IN} = 170 MHz	25°C		90			90		dBc
TWO-TONE SFDR								
f_{IN} = 29 MHz (−7 dBFS), 32 MHz (−7 dBFS)	25°C		87			85		dBc
f_{IN} = 169 MHz (−7 dBFS), 172 MHz (−7 dBFS)	25°C		83			84		dBc
ANALOG INPUT BANDWIDTH	25°C		650			650		MHz

[1] See AN-835, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V; DRVDD = 2.5 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = −1.0 dBFS, DCS enabled, unless otherwise noted.

Table 3.

Parameter	Temp	AD9246BCPZ-105/125 Min	Typ	Max	Unit
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance			CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		1.2		V
Differential Input Voltage	Full	0.2		6	V p-p
Input Voltage Range	Full	AVDD − 0.3		AVDD + 1.6	V
Input Common-Mode Range	Full	1.1		AVDD	V
High Level Input Voltage	Full	1.2		3.6	V
Low Level Input Voltage	Full	0		0.8	V
High Level Input Current	Full	−10		+10	μA
Low Level Input Current	Full	−10		+10	μA
Input Resistance	Full	8	10	12	kΩ
Input Capacitance	Full		4		pF
LOGIC INPUTS (SCLK/DFS, OEB, PWDN)					
High Level Input Voltage	Full	1.2		3.6	V
Low Level Input Voltage	Full	0		0.8	V
High Level Input Current	Full	−50		−75	μA
Low Level Input Current	Full	−10		+10	μA
Input Resistance	Full		30		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUTS (CSB)					
High Level Input Voltage	Full	1.2		3.6	V
Low Level Input Voltage	Full	0		0.8	V
High Level Input Current	Full	−10		+10	μA
Low Level Input Current	Full	+40		+135	μA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUTS (SDIO/DCS)					
High Level Input Voltage	Full	1.2		DRVDD + 0.3	V
Low Level Input Voltage	Full	0		0.8	V
High Level Input Current	Full	−10		+10	μA
Low Level Input Current	Full	+40		+130	μA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF
DIGITAL OUTPUTS					
DRVDD = 3.3 V					
High Level Output Voltage (I_{OH} = 50 μA)	Full	3.29			V
High Level Output Voltage (I_{OH} = 0.5 mA)	Full	3.25			V
Low Level Output Voltage (I_{OL} = 1.6 mA)	Full			0.2	V
Low Level Output Voltage (I_{OL} = 50 μA)	Full			0.05	V
DRVDD = 1.8 V					
High Level Output Voltage (I_{OH} = 50 μA)	Full	1.79			V
High Level Output Voltage (I_{OH} = 0.5 mA)	Full	1.75			V
Low Level Output Voltage (I_{OL} = 1.6 mA)	Full			0.2	V
Low Level Output Voltage (I_{OL} = 50 μA)	Full			0.05	V

SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 2.5 V, unless otherwise noted.

Table 4.

Parameter[1]	Temp	AD9246BCPZ-105 Min	AD9246BCPZ-105 Typ	AD9246BCPZ-105 Max	AD9246BCPZ-125 Min	AD9246BCPZ-125 Typ	AD9246BCPZ-125 Max	Unit
CLOCK INPUT PARAMETERS								
Conversion Rate, DCS Enabled	Full	20		105	20		125	MSPS
Conversion Rate, DCS Disabled	Full	10		105	10		125	MSPS
CLK Period	Full	9.5			8			ns
CLK Pulse Width High, DCS Enabled	Full	2.85	4.75	6.65	2.4	4	5.6	ns
CLK Pulse Width High, DCS Disabled	Full	4.28	4.75	5.23	3.6	4	4.4	ns
DATA OUTPUT PARAMETERS								
Data Propagation Delay (t_{PD})[2]	Full	3.1	3.9	4.8	3.1	3.9	4.8	ns
DCO Propagation Delay (t_{DCO})	Full		4.4			4.4		ns
Setup Time (t_S)	Full	3.4	4.3		2.6	3.5		ns
Hold Time (t_H)	Full	4.4	5.3		3.7	4.5		ns
Pipeline Delay (Latency)	Full		12			12		cycles
Aperture Delay (t_A)	Full		0.8			0.8		ns
Aperture Uncertainty (Jitter, t_J)	Full		0.1			0.1		ps rms
Wake-Up Time[3]	Full		350			350		μs
OUT-OF-RANGE RECOVERY TIME	Full		2			3		cycles
SERIAL PORT INTERFACE[4]								
SCLK Period (t_{CLK})	Full	40			40			ns
SCLK Pulse Width High Time (t_{HI})	Full	16			16			ns
SCLK Pulse Width Low Time (t_{LO})	Full	16			16			ns
SDIO to SCLK Setup Time (t_{DS})	Full	5			5			ns
SDIO to SCLK Hold Time (t_{DH})	Full	2			2			ns
CSB to SCLK Setup Time (t_S)	Full	5			5			ns
CSB to SCLK Hold Time (t_H)	Full	2			2			ns

[1] See AN-835, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.
[2] Output propagation delay is measured from CLK 50% transition to DATA 50% transition, with 5 pF load.
[3] Wake-up time is dependant on the value of the decoupling capacitors, values shown with 0.1 μF capacitor across REFT and REFB.
[4] See Figure 73 and the Serial Port Interface (SPI) section.

TIMING DIAGRAM

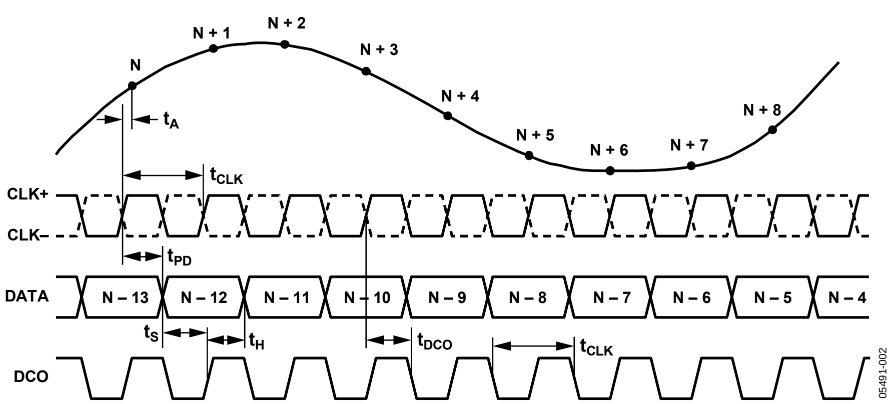

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
ELECTRICAL	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to DGND	−0.3 V to +3.9 V
AGND to DGND	−0.3 V to +0.3 V
AVDD to DRVDD	−3.9 V to +2.0 V
D0 through D13 to DGND	−0.3 V to DRVDD + 0.3 V
DCO to DGND	−0.3 V to DRVDD + 0.3 V
OR to DGND	−0.3 V to DRVDD + 0.3 V
CLK+ to AGND	−0.3 V to +3.9 V
CLK− to AGND	−0.3 V to +3.9 V
VIN+ to AGND	−0.3 V to AVDD + 0.2 V
VIN− to AGND	−0.3 V to AVDD + 0.2 V
VREF to AGND	−0.3 V to AVDD + 0.2 V
SENSE to AGND	−0.3 V to AVDD + 0.2 V
REFT to AGND	−0.3 V to AVDD + 0.2 V
REFB to AGND	−0.3 V to AVDD + 0.2 V
SDIO/DCS to DGND	−0.3 V to DRVDD + 0.3 V
PDWN to AGND	−0.3 V to +3.9 V
CSB to AGND	−0.3 V to +3.9 V
SCLK/DFS to AGND	−0.3 V to +3.9 V
OEB to AGND	−0.3 V to +3.9 V
ENVIRONMENTAL	
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering 10 Sec)	+300°C
Junction Temperature	+150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

The exposed paddle must be soldered to the ground plane for the LFCSP package. Soldering the exposed paddle to the customer board, increases the reliability of the solder joints, maximizing the thermal capability of the package.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
48-lead LFCSP (CP-48-3)	26.4	2.4	°C/W

Typical θ_{JA} and θ_{JC} are specified for a 4-layer board in still air. Airflow increases heat dissipation effectively reducing θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, and through holes, ground, and power planes, reduces the θ_{JA}.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

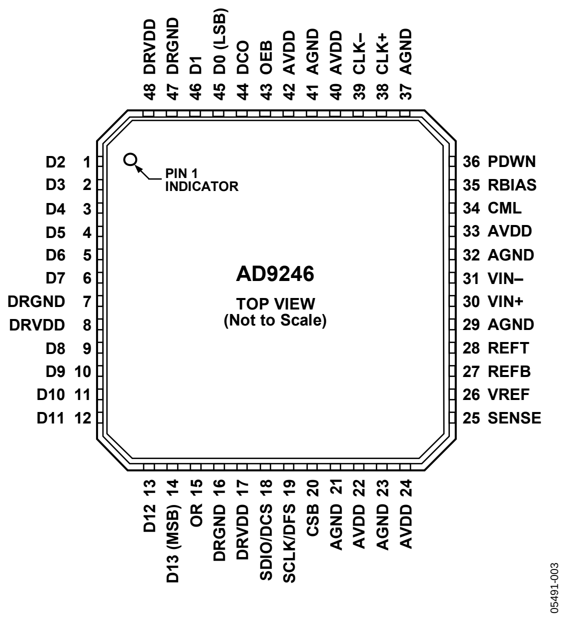

Figure 3. Pin Configuration

Table 7. Pin Function Description

Pin No.	Mnemonic	Description
0, 21, 23, 29, 32, 37, 41	AGND	Analog Ground. (Pin 0 is the exposed thermal pad on the bottom of the package.)
1 to 6, 9 to 14, 45, 46	D0 (LSB) to D13 (MSB)	Data Output Bits.
7, 16, 47	DRGND	Digital Output Ground.
8, 17, 48	DRVDD	Digital Output Driver Supply (1.8 V to 3.3 V).
15	OR	Out-of-Range Indicator.
18	SDIO/DCS	Serial Port Interface (SPI)® Data Input/Output (Serial Port Mode); Duty Cycle Stabilizer Select (External Pin Mode). See Table 10.
19	SCLK/DFS	Serial Port Interface Clock (Serial Port Mode); Data Format Select Pin (External Pin Mode).
20	CSB	Serial Port Interface Chip Select (Active Low). See Table 10.
22, 24, 33, 40, 42	AVDD	Analog Power Supply.
25	SENSE	Reference Mode Selection. See Table 9.
26	VREF	Voltage Reference Input/Output.
27	REFB	Differential Reference (–).
28	REFT	Differential Reference (+).
30	VIN+	Analog Input Pin (+).
31	VIN–	Analog Input Pin (–).
34	CML	Common-Mode Level Bias Output.
35	RBIAS	External Bias Resister Connection. A 10 kΩ resistor must be connected between this pin and analog ground (AGND).
36	PDWN	Power-Down Function Select.
38	CLK+	Clock Input (+).
39	CLK–	Clock Input (–).
43	OEB	Output Enable (Active Low).
44	DCO	Data Clock Output.

EQUIVALENT CIRCUITS

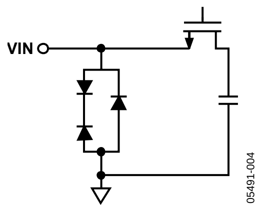

Figure 4. Equivalent Analog Input Circuit

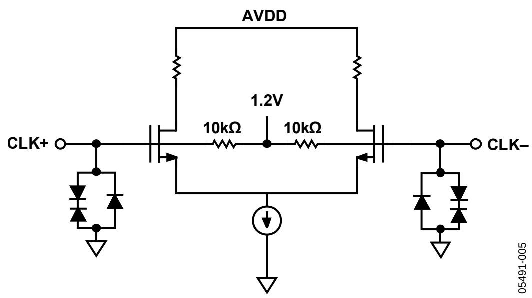

Figure 5. Equivalent Clock Input Circuit

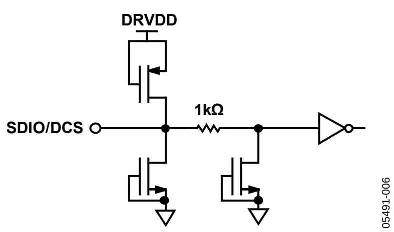

Figure 6. Equivalent SDIO/DCS Input Circuit

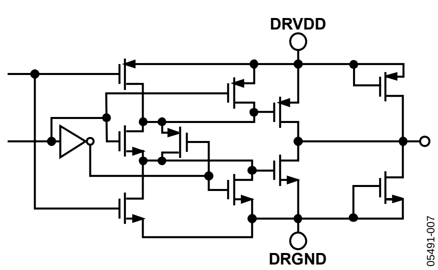

Figure 7. Equivalent Digital Output Circuit

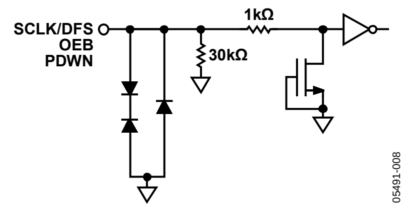

Figure 8. Equivalent SCLK/DFS, OEB, PDWN Input Circuit

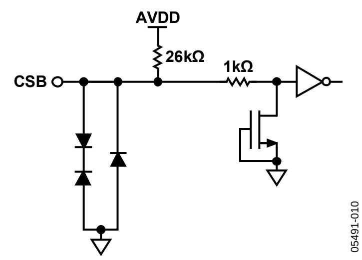

Figure 9. Equivalent CSB Input Circuit

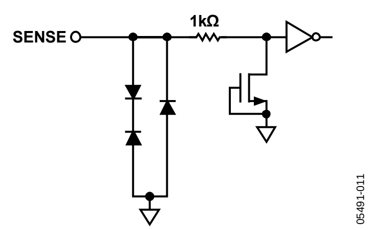

Figure 10. Equivalent Sense Circuit

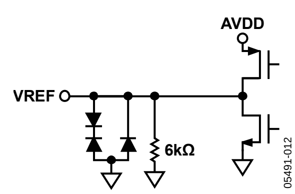

Figure 11. Equivalent VREF Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 1.8 V; DRVDD = 2.5 V; maximum sample rate, DCS enabled, 1 V internal reference; 2 V p-p differential input; AIN = −1.0 dBFS; 64k sample; T_A = 25°C, unless otherwise noted.

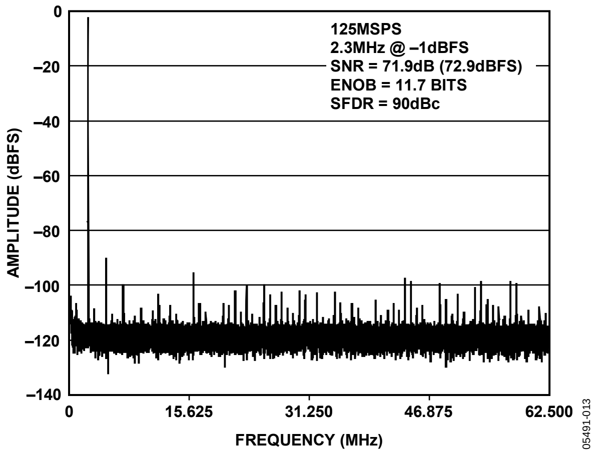

Figure 12. AD9246-125 Single-Tone FFT with f_{IN} = 2.3 MHz

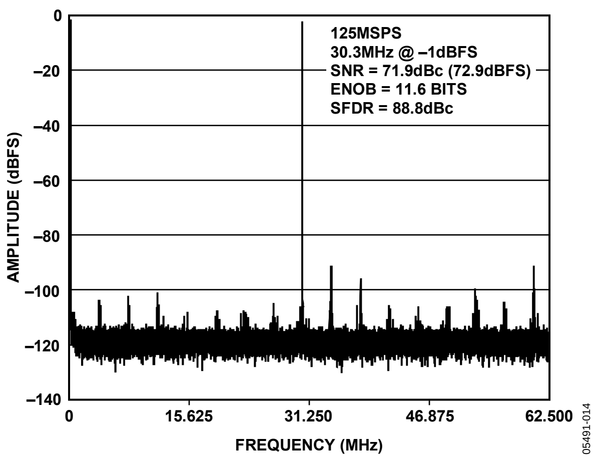

Figure 13. AD9246-125 Single-Tone FFT with f_{IN} = 30.3 MHz

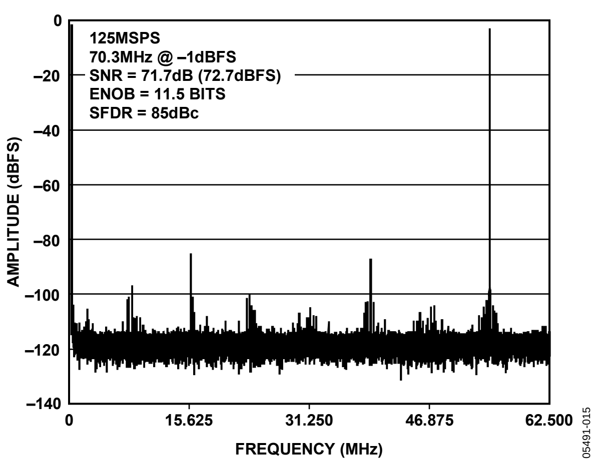

Figure 14. AD9246-125 Single-Tone FFT with f_{IN} = 70.3 MHz

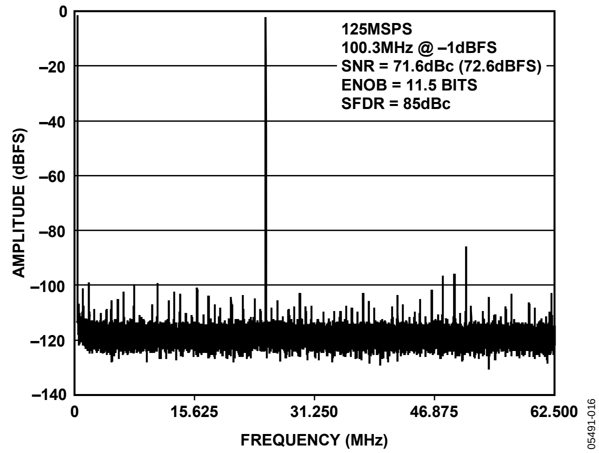

Figure 15. AD9246-125 Single-Tone FFT with f_{IN} = 100.3 MHz

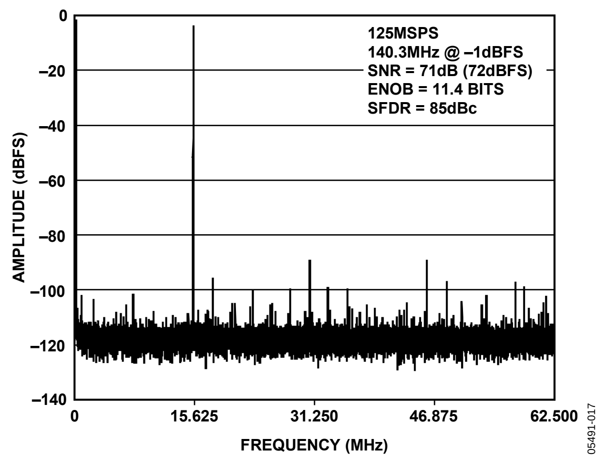

Figure 16. AD9246-125 Single-Tone FFT with f_{IN} = 140.3 MHz

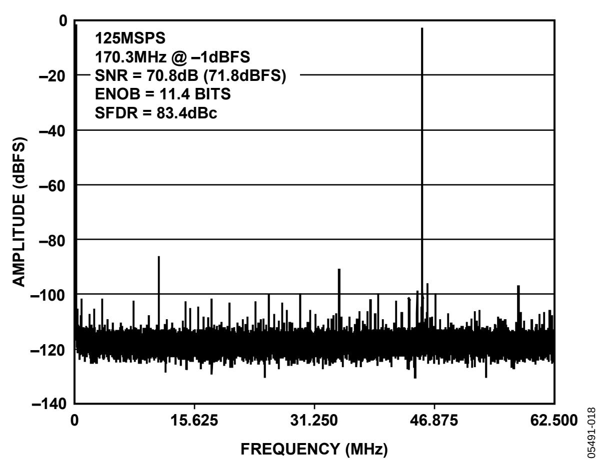

Figure 17. AD9246-125 Single-Tone FFT with f_{IN} = 170.3 MHz

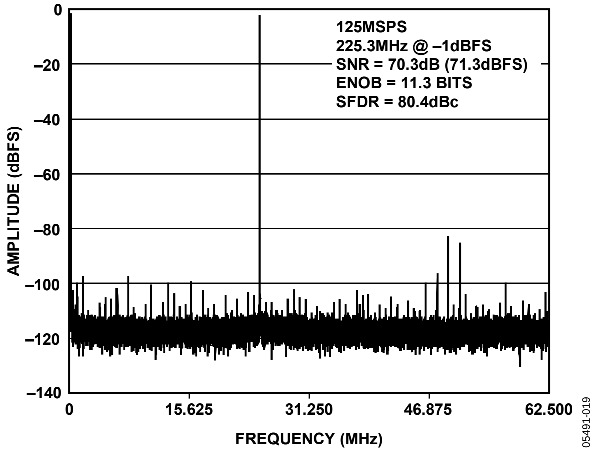

Figure 18. AD9246-125 Single-Tone FFT with f_{IN} = 225.3 MHz

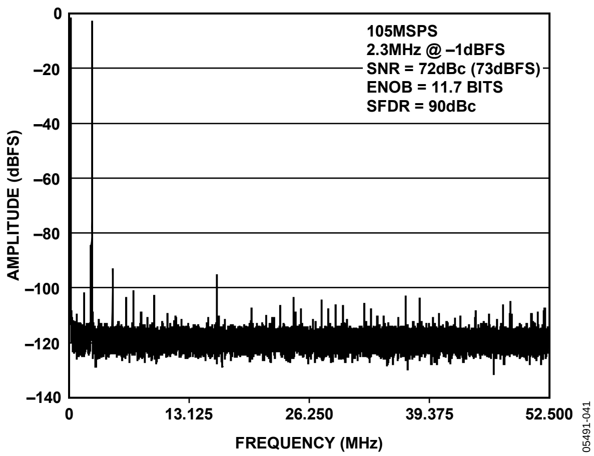

Figure 19. AD9246-105 Single-Tone FFT with f_{IN} = 2.3 MHz

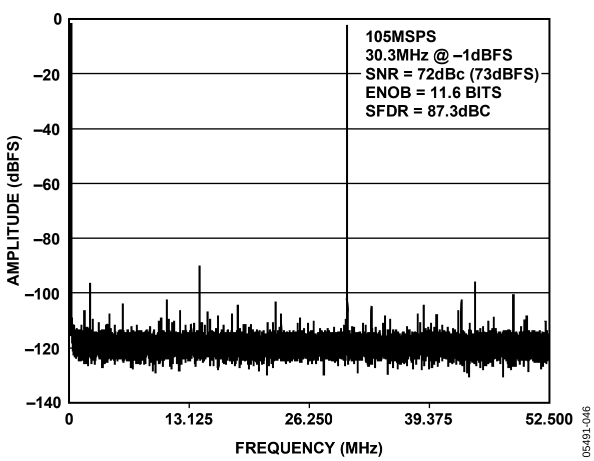

Figure 20. AD9246-105 Single-Tone FFT with f_{IN} = 30.3 MHz

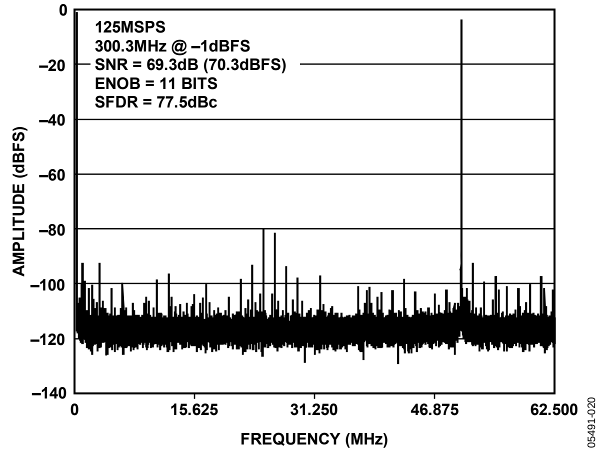

Figure 21. AD9246-125 Single-Tone FFT with f_{IN} = 300.3 MHz

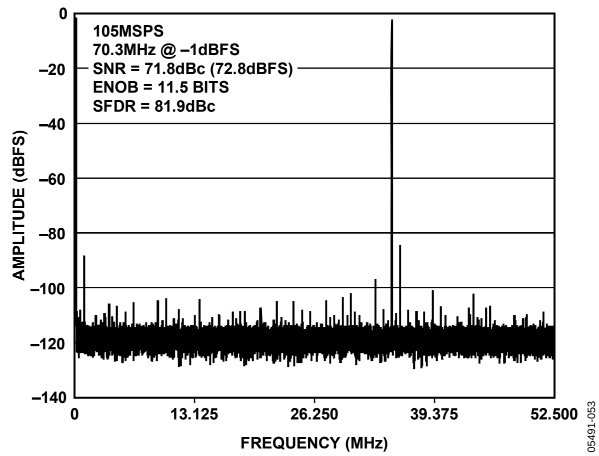

Figure 22. AD9246-105 Single-Tone FFT with f_{IN} = 70.3 MHz

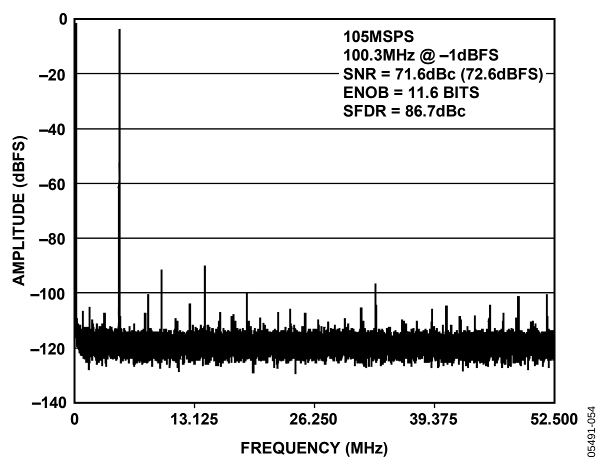

Figure 23. AD9246-105 Single-Tone FFT with f_{IN} = 100.3 MHz

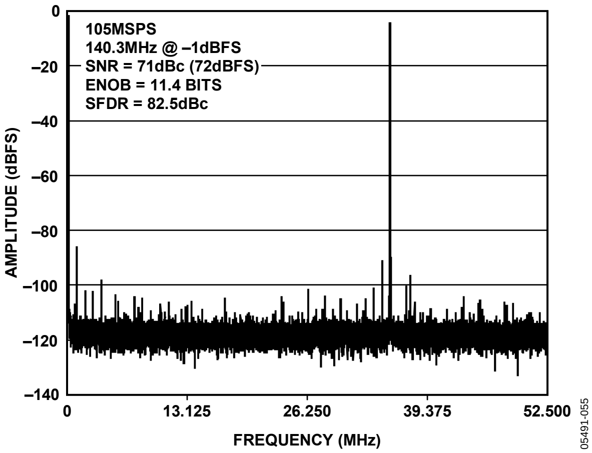

Figure 24. AD9246-105 Single-Tone FFT with f_{IN} = 140. 3 MHz

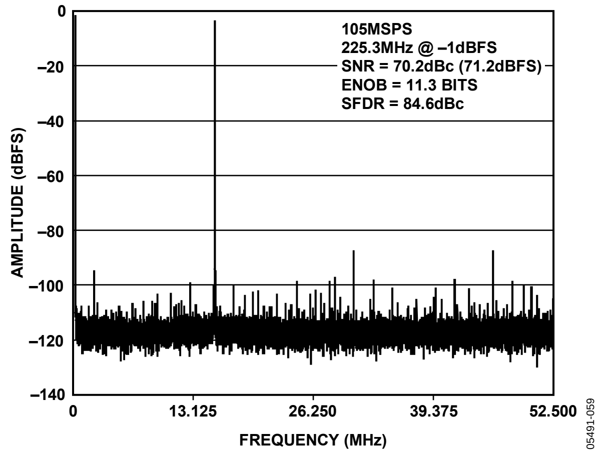

Figure 27. AD9246-105 Single-Tone FFT with F_{IN} = 225.3 MHz

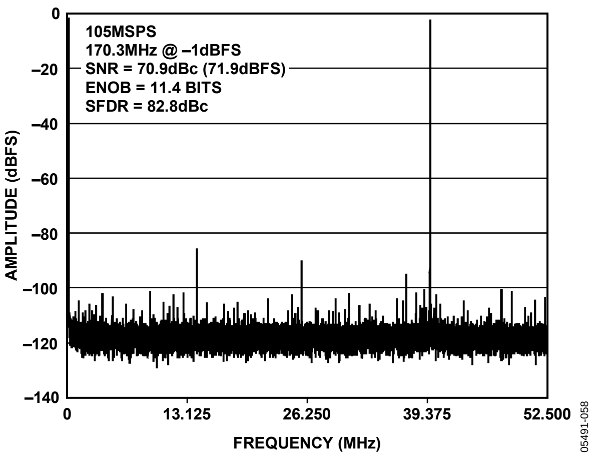

Figure 25. AD9246-105 Single-Tone FFT with f_{IN} = 170.3 MHz

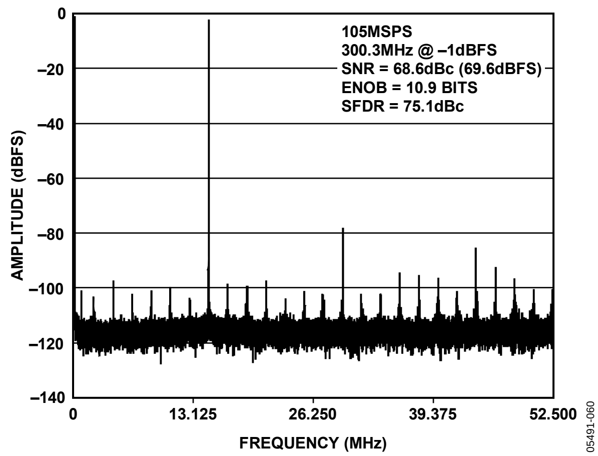

Figure 28. AD9246-105 Single-Tone FFT with f_{IN} = 300.3 MHz

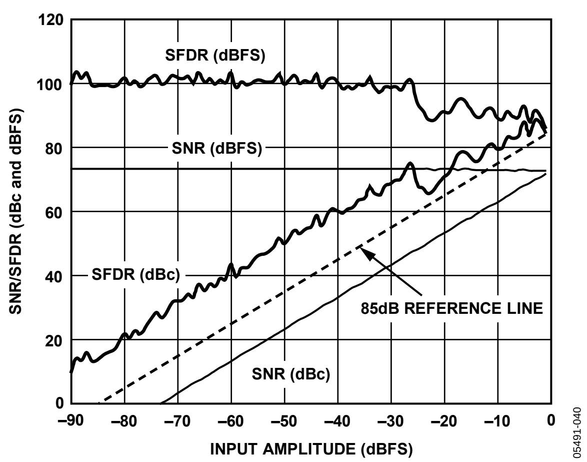

Figure 26. AD9246-125 Single-Tone SNR/SFDR vs. Input Amplitude (AIN) with f_{IN} = 2.4 MHz

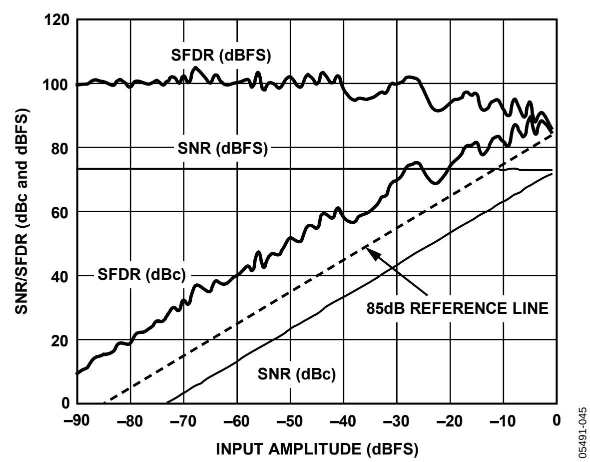

Figure 29. AD9246-105 Single-Tone SNR/SFDR vs. Input Amplitude (AIN) with f_{IN} = 2.4 MHz

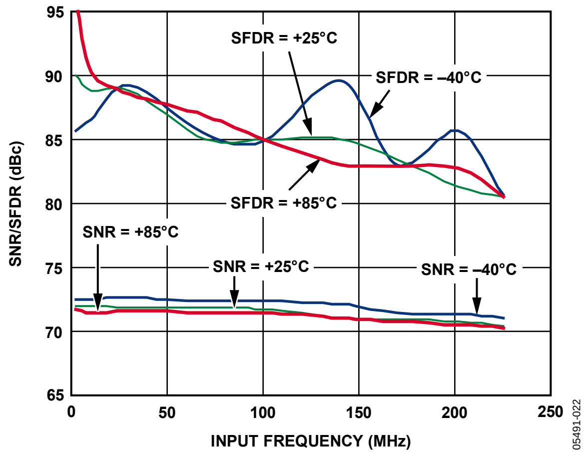

Figure 30. AD9246-125 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) and Temperature with 2 V p-p Full Scale

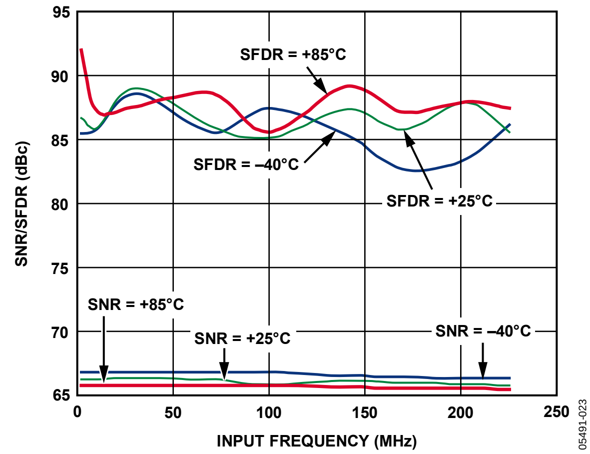

Figure 33. AD9246-125 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) and Temperature with 1 V p-p Full Scale

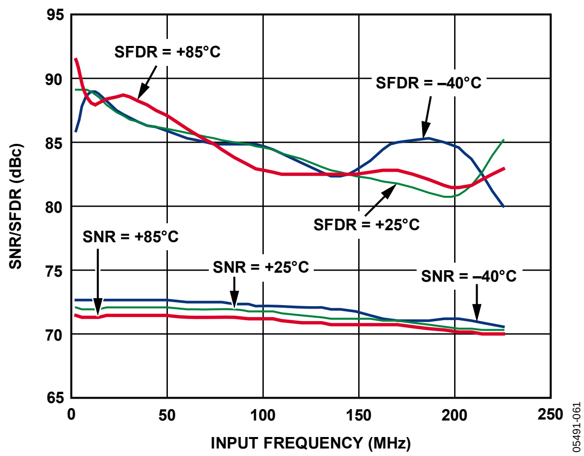

Figure 31. AD9246-105 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) and Temperature with 2 V p-p Full Scale

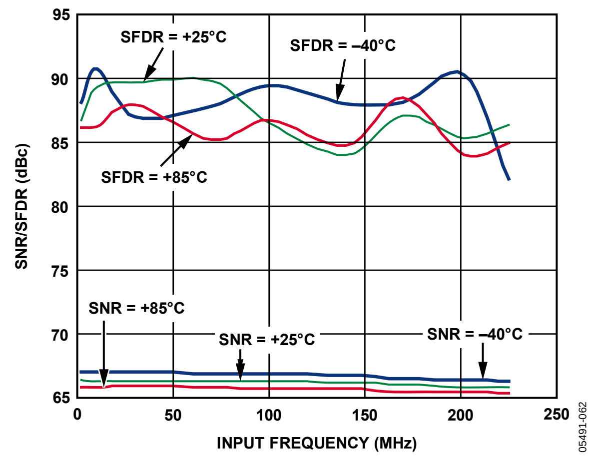

Figure 34. AD9246-105 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) and Temperature with 1 V p-p Full Scale

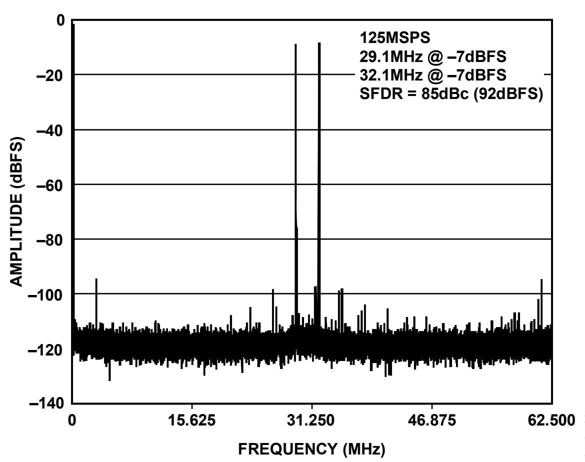

Figure 32. AD9246-125 Two-Tone FFT with f_{IN1} = 29.1 MHz, f_{IN2} = 32.1 MHz

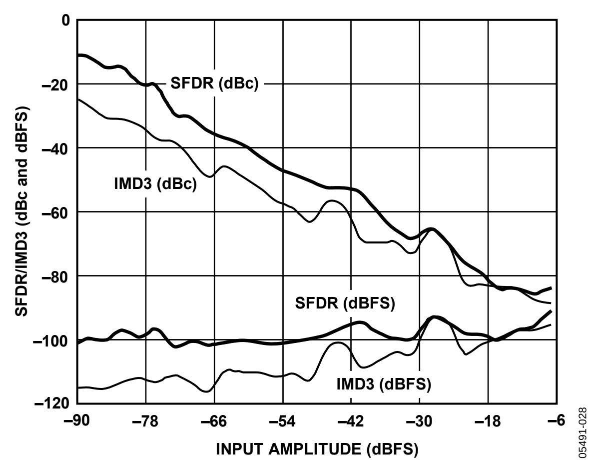

Figure 35. AD9246-125 Two-Tone SFDR/IMD vs. Input Amplitude (AIN) with f_{IN1} = 29.1 MHz, f_{IN2} = 32.1 MHz

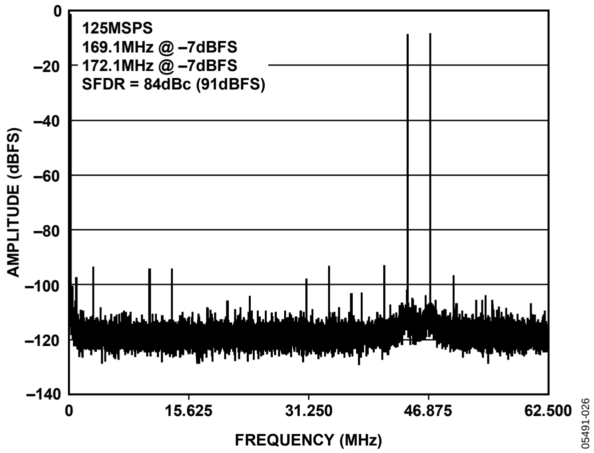

Figure 36. AD9246-125 Two-Tone FFT with f_{IN1} = 169.1 MHz, f_{IN2} = 172.1 MHz

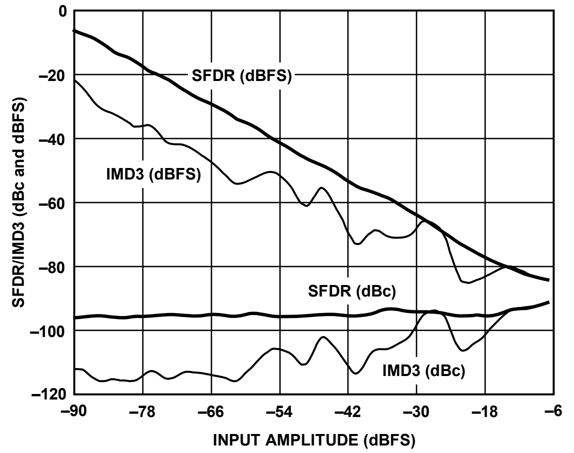

Figure 39. AD9246-125 Two-Tone SFDR/IMD vs. Input Amplitude (AIN) with f_{IN1} = 169.1 MHz, f_{IN2} = 172.11 MHz

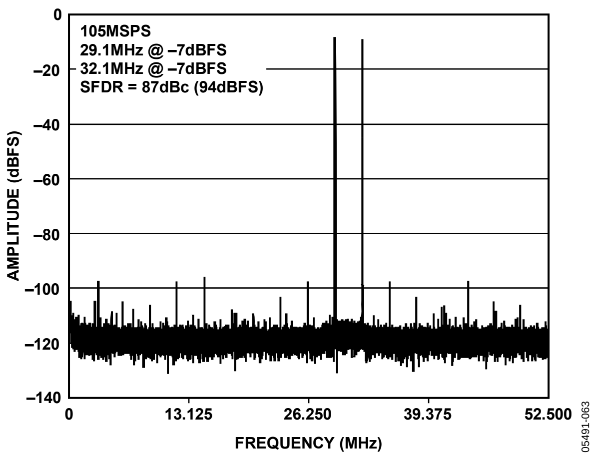

Figure 37. AD9246-105 Two-Tone FFT with f_{IN1} = 29.1 MHz, f_{IN2} = 32.1 MHz

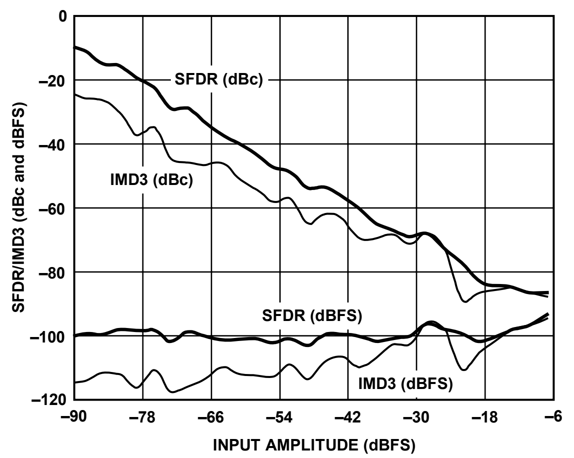

Figure 40. AD9246-105 Two-Tone SFDR/IMD vs. Input Amplitude (AIN) with f_{IN1} = 29.1 MHz, f_{IN2} = 32.1 MHz

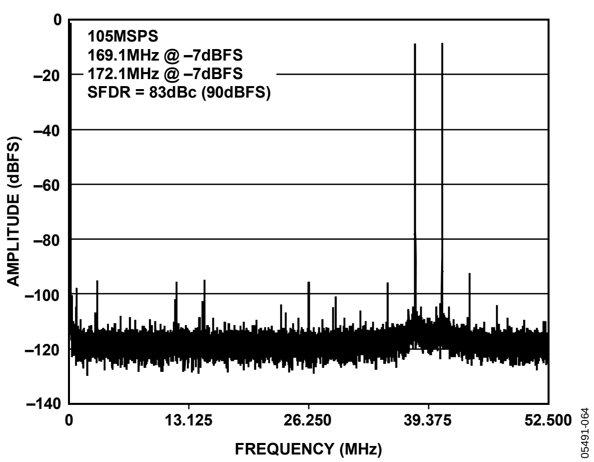

Figure 38. AD9246-105 Two-Tone FFT with f_{IN1} = 169.1 MHz, f_{IN2} = 172.1 MHz

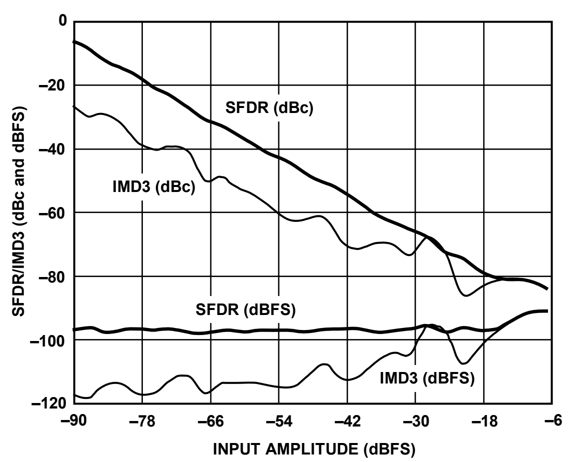

Figure 41. AD9246-105 Two-Tone SFDR/IMD vs. Input Amplitude (AIN) with f_{IN1} = 169.1 MHz, f_{IN2} = 172.1 MHz

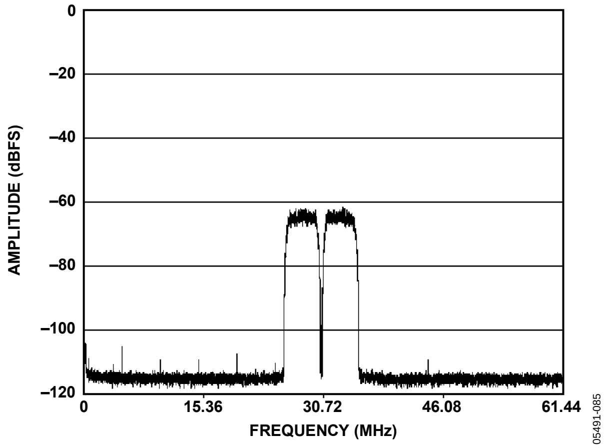

Figure 42. AD9246-125 Two 64k WCDMA Carriers with f_{IN} = 215.04 MHz, f_S = 122.88 MSPS

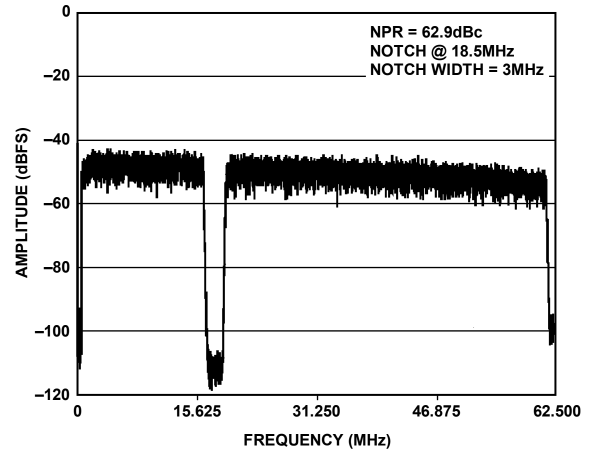

Figure 45. AD9246 Noise Power Ratio (NPR)

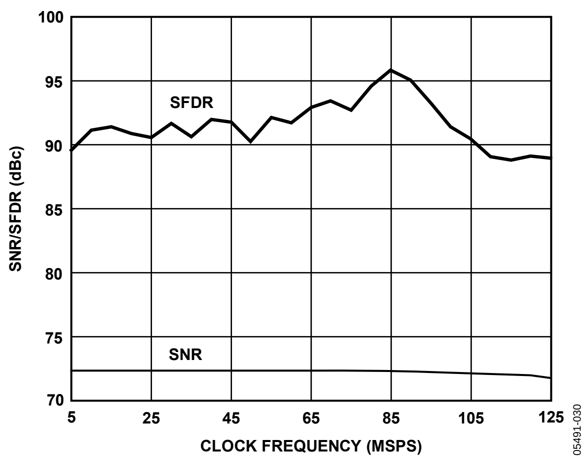

Figure 43. AD9246-125 Single-Tone SNR/SFDR vs. Clock Frequency (f_S) with f_{IN} = 2.4 MHz

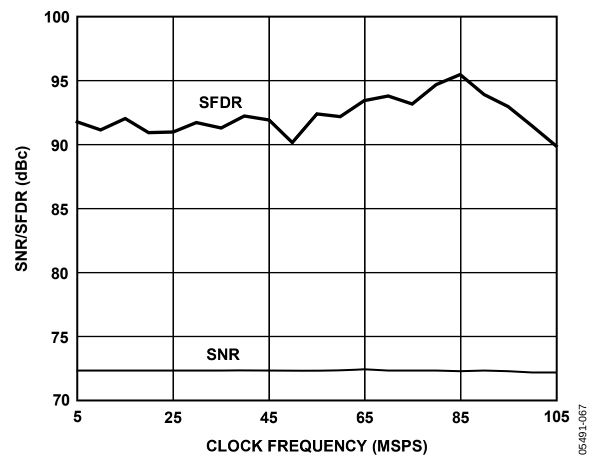

Figure 46. AD9246-105 Single-Tone SNR/SFDR vs. Clock Frequency (f_S) with f_{IN} = 2.4 MHz

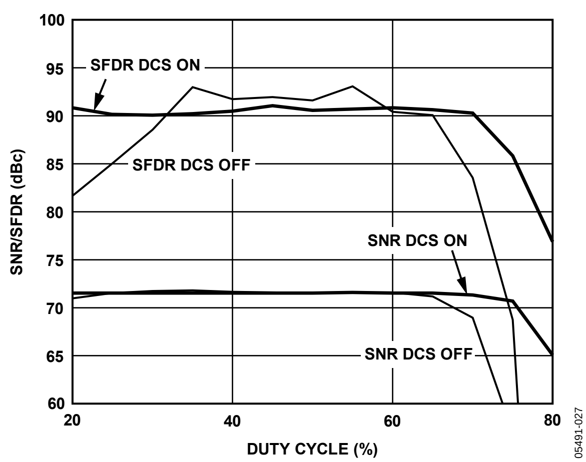

Figure 44. AD9246 SNR/SFDR vs. Duty Cycle with f_{IN} = 10.3 MHz

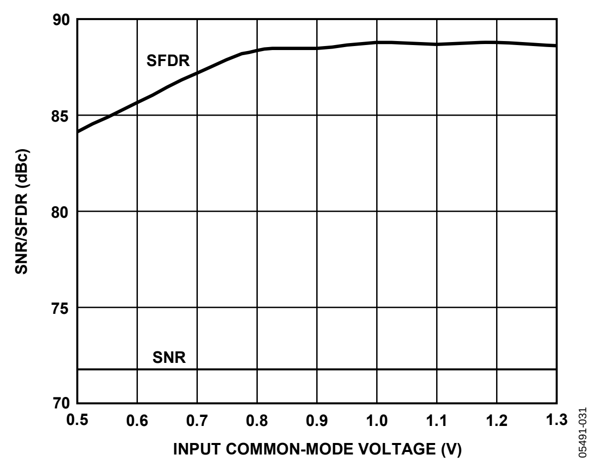

Figure 47. AD9246 SNR/SFDR vs. Input Common Mode (VCM) with f_{IN} = 30 MHz

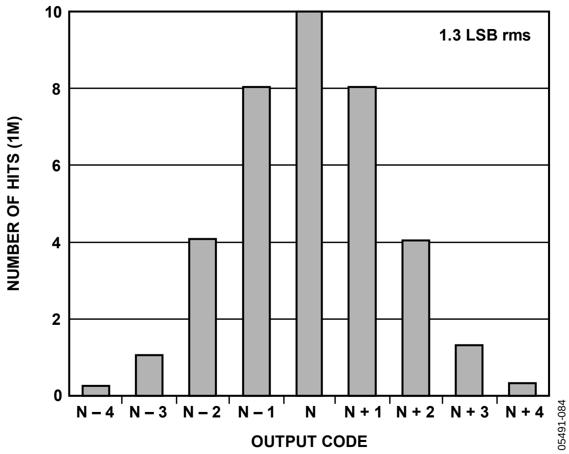

Figure 48. AD9246 Grounded Input Histogram

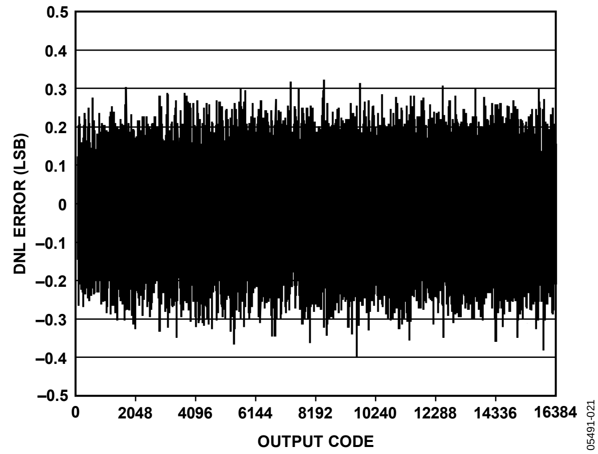

Figure 51. AD9246 DNL with f_{IN} = 10.3 MHz

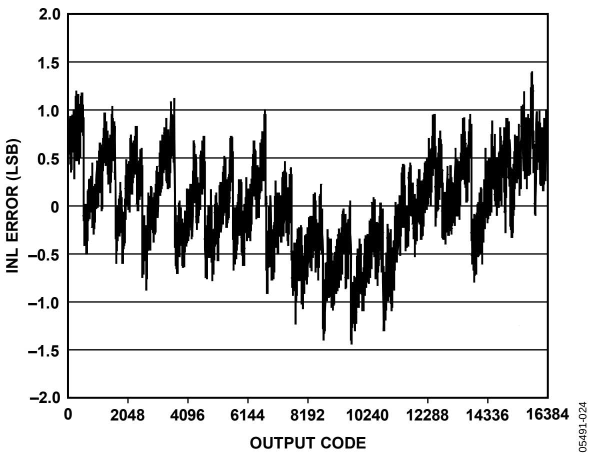

Figure 49. AD9246-125 INL with f_{IN} = 10.3 MHz

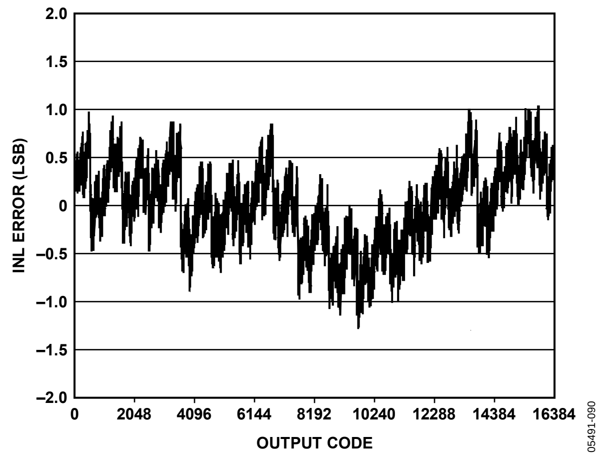

Figure 52. AD9246-105 INL with f_{IN} = 10.3 MHz

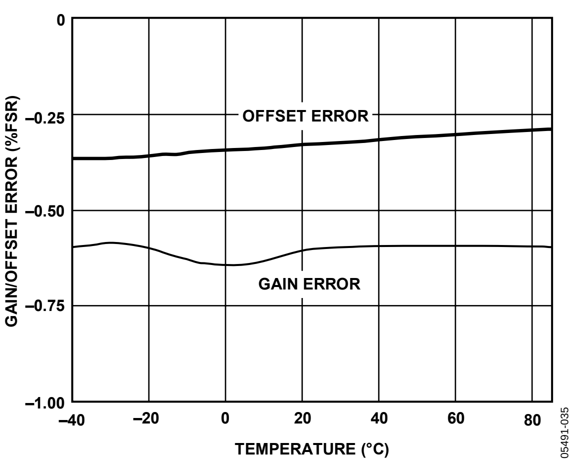

Figure 50. AD9246 Gain and Offset vs. Temperature

THEORY OF OPERATION

The AD9246 architecture consists of a front-end sample and hold amplifier (SHA) followed by a pipelined switched capacitor ADC. The quantized outputs from each stage are combined into a final 14-bit result in the digital correction logic. The pipeline architecture permits the first stage to operate on a new input sample, while the remaining stages operate on preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched capacitor DAC and interstage residue amplifier (MDAC). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage contains a differential SHA that can be ac- or dc-coupled in differential or single-ended modes. The output staging block aligns the data, carries out the error correction, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing adjustment of the output voltage swing. During power down, the output buffers go into a high impedance state.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9246 is a differential switched capacitor SHA that has been designed for optimum performance while processing a differential input signal.

The clock signal alternately switches the SHA between sample mode and hold mode (see Figure 53). When the SHA is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor in series with each input can help reduce the peak transient current required from the output stage of the driving source.

A shunt capacitor can be placed across the inputs to provide dynamic charging currents. This passive network creates a low-pass filter at the ADC input; therefore, the precise values are dependant upon the application.

In IF undersampling applications, any shunt capacitors should be reduced. In combination with the driving source impedance, these capacitors would limit the input bandwidth. See the AN-742 application note, the AN-827 Application Note, and the *Analog Dialogue* article, "Transformer-Coupled Front-End for Wideband A/D Converters" for more information.

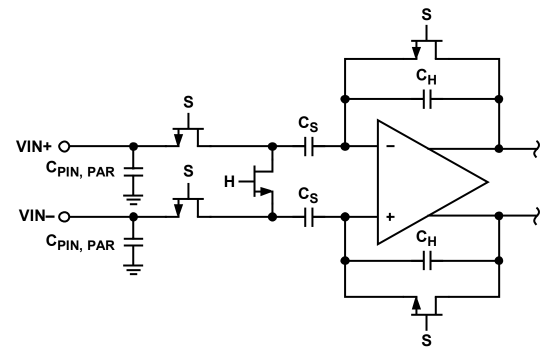

Figure 53. Switched-Capacitor SHA Input

For best dynamic performance, the source impedances driving VIN+ and VIN− should match such that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC.

An internal differential reference buffer creates two reference voltages used to define the input span of the ADC core. The span of the ADC core is set by the buffer to be 2 × VREF. The reference voltages are not available to the user. Two bypass points, REFT and REFB, are brought out for decoupling to reduce the noise contributed by the internal reference buffer. It is recommended that REFT be decoupled to REFB by a 0.1 μF capacitor, as described in the Layout Considerations section.

Input Common Mode

The analog inputs of the AD9246 are not internally dc-biased. In ac-coupled applications, the user must provide this bias externally. Setting the device such that $V_{CM} = 0.55 \times$ AVDD is recommended for optimum performance, however the device functions over a wider range with reasonable performance (see Figure 47). An on-board common-mode voltage reference is included in the design and is available from the CML pin. Optimum performance is achieved when the common-mode voltage of the analog input is set by the CML pin voltage (typically 0.55 × AVDD). The CML pin must be decoupled to ground by a 0.1 μF capacitor, as described in the Layout Considerations section.

Differential Input Configurations

Optimum performance is achieved by driving the AD9246 in a differential input configuration. For baseband applications, the AD8138 differential driver provides excellent performance and a flexible interface to the ADC. The output common-mode voltage of the AD8138 is easily set with the CML pin of the AD9246 (see Figure 54), and the driver can be configured in a Sallen-Key filter topology to provide band limiting of the input signal.

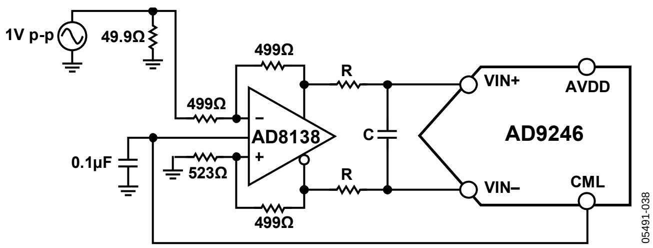

Figure 54. Differential Input Configuration Using the AD8138

For baseband applications where SNR is a key parameter, differential transformer coupling is the recommended input configuration. An example is shown in Figure 55. The CML voltage can be connected to the center tap of the secondary winding of the transformer to bias the analog input.

The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few MHz, and excessive signal power can cause core saturation, which leads to distortion.

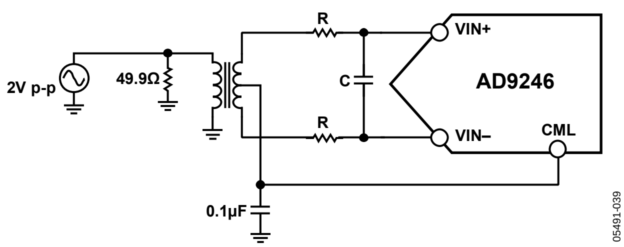

Figure 55. Differential Transformer-Coupled Configuration

At input frequencies in the second Nyquist zone and above, the noise performance of most amplifiers is not adequate to achieve the true SNR performance of the AD9246. For applications where SNR is a key parameter, transformer coupling is the recommended input. For applications where SFDR is a key parameter, differential double balun coupling is the recommended input configuration. An example is shown in Figure 57.

As an alternative to using a transformer-coupled input at frequencies in the second Nyquist zone, the AD8352 differential driver can be used. An example is shown in Figure 58.

In any configuration, the value of the shunt capacitor, C, is dependent on the input frequency and source impedance and may need to be reduced or removed. Table 8 displays recommended values to set the RC network. However, these values are dependant on the input signal and should only be used as a starting guide.

Table 8. RC Network Recommended Values

Frequency Range (MHz)	R Series (Ω)	C Differential (pF)
0 to 70	33	15
70 to 200	33	5
200 to 300	15	5
>300	15	Open

Single-Ended Input Configuration

Although not recommended, it is possible to operate the AD9246 in a single-ended input configuration, as long as the input voltage swing is within the AVDD supply. Single-ended operation can provide adequate performance in cost-sensitive applications.

In this configuration, SFDR and distortion performance degrade due to the large input common-mode swing. If the source impedances on each input are matched, there should be little effect on SNR performance. Figure 56 details a typical single-ended input configuration.

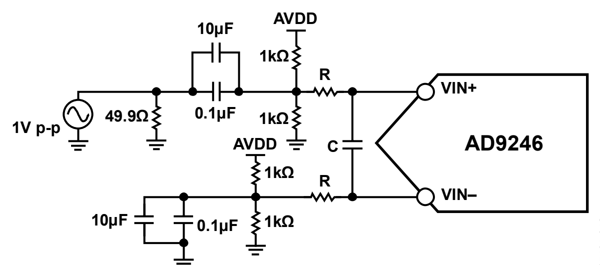

Figure 56. Single-Ended Input Configuration

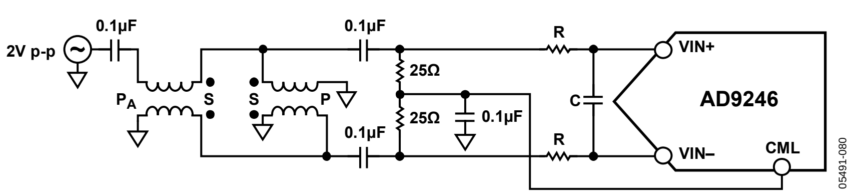

Figure 57. Differential Double Balun Input Configuration

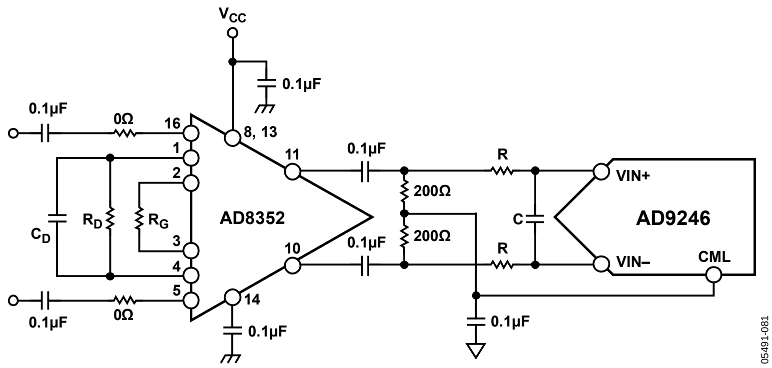

Figure 58. Differential Input Configuration Using the AD8352

Table 9. Reference Configuration Summary

Selected Mode	SENSE Voltage	Resulting VREF (V)	Resulting Differential Span (V p-p)
External Reference	AVDD	N/A	2 × External Reference
Internal Fixed Reference	VREF	0.5	1.0
Programmable Reference	0.2 V to VREF	$0.5 \times \left(1 + \frac{R2}{R1}\right)$ (See Figure 60)	2 × VREF
Internal Fixed Reference	AGND to 0.2 V	1.0	2.0

VOLTAGE REFERENCE

A stable and accurate voltage reference is built into the AD9246. The input range is adjustable by varying the reference voltage applied to the AD9246, using either the internal reference or an externally applied reference voltage. The input span of the ADC tracks reference voltage changes linearly. The various reference modes are summarized in the following sections. The Reference Decoupling section describes the best practices and requirements for PCB layout of the reference.

Internal Reference Connection

A comparator within the AD9246 detects the potential at the SENSE pin and configures the reference into four possible states, as summarized in Table 9. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 59), setting VREF to 1 V.

Connecting the SENSE pin to VREF switches the reference amplifier input to the SENSE pin, completing the loop and providing a 0.5 V reference output. If a resistor divider is connected external to the chip as shown in Figure 60, the switch sets to the SENSE pin. This puts the reference amplifier in a noninverting mode with the VREF output defined as

$$VREF = 0.5\left(1 + \frac{R2}{R1}\right)$$

If the SENSE pin is connected to AVDD, the reference amplifier is disabled, and an external reference voltage can be applied to the VREF pin (see the External Reference Operation section).

The input range of the ADC always equals twice the voltage at the reference pin for either an internal or an external reference.

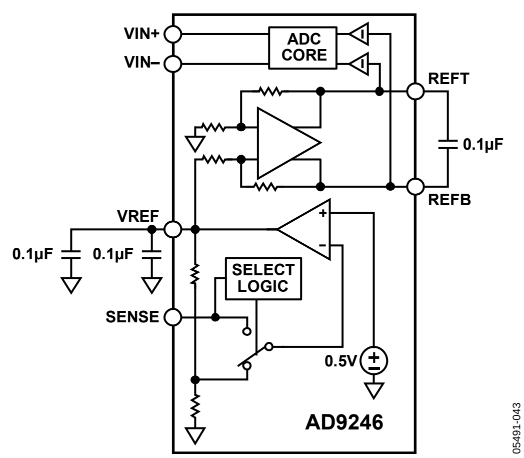

Figure 59. Internal Reference Configuration

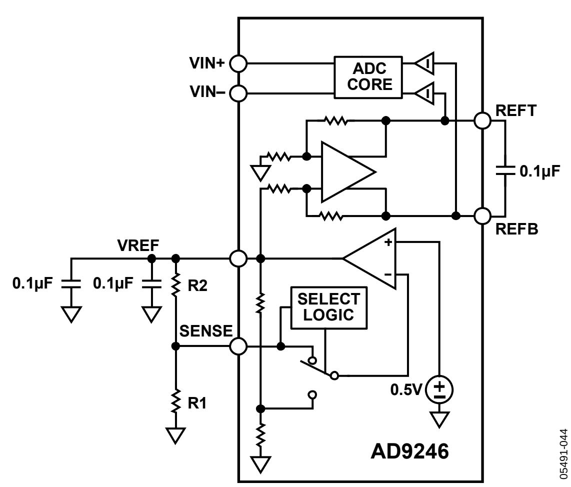

Figure 60. Programmable Reference Configuration

If the internal reference of the AD9246 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 61 depicts how the internal reference voltage is affected by loading.

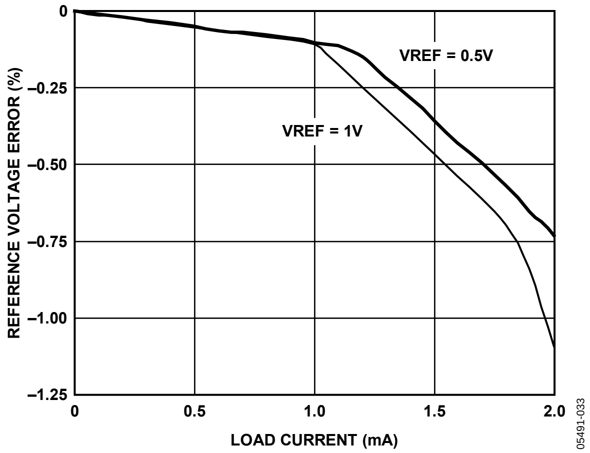

Figure 61. VREF Accuracy vs. Load

External Reference Operation

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or improve thermal drift characteristics. Figure 62 shows the typical drift characteristics of the internal reference in both 1 V and 0.5 V modes.

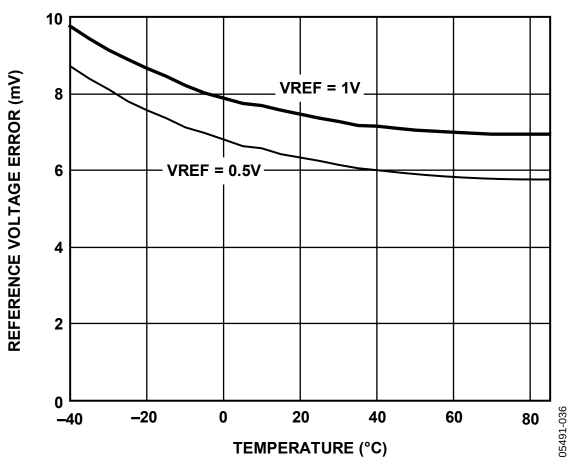

Figure 62. Typical VREF Drift

When the SENSE pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference. An internal resistor divider loads the external reference with an equivalent 6 kΩ load (see Figure 11). In addition, an internal buffer generates the positive and negative full-scale references for the ADC core. Therefore, the external reference must be limited to a maximum of 1 V.

CLOCK INPUT CONSIDERATIONS

For optimum performance, the AD9246 sample clock inputs (CLK+ and CLK−) should be clocked with a differential signal. The signal is typically ac-coupled into the CLK+ pin and the CLK− pin via a transformer or capacitors. These pins are biased internally (See Figure 5) and require no external bias.

Clock Input Options

The AD9246 has a very flexible clock input structure. The clock input can be a CMOS, LVDS, LVPECL, or sine wave signal. Regardless of the type of signal used, the jitter of the clock source is of the most concern, as described in the Jitter section.

Figure 63 shows one preferred method for clocking the AD9246. A low jitter clock source is converted from single-ended to a differential signal using an RF transformer. The back-to-back Schottky diodes across the transformer secondary limit clock excursions into the AD9246 to approximately 0.8 V p-p differential. This helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9246 while preserving the fast rise and fall times of the signal, which are critical to a low jitter performance.

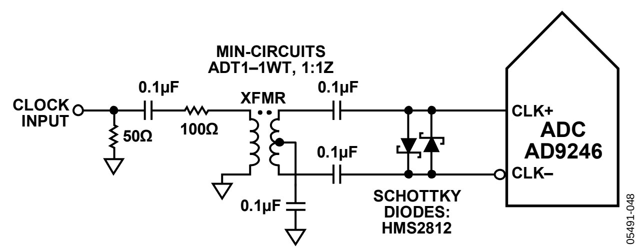

Figure 63. Transformer Coupled Differential Clock

If a low jitter clock source is not available, another option is to ac-couple a differential PECL signal to the sample clock input pins as shown in Figure 64. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515 family of clock drivers offers excellent jitter performance.

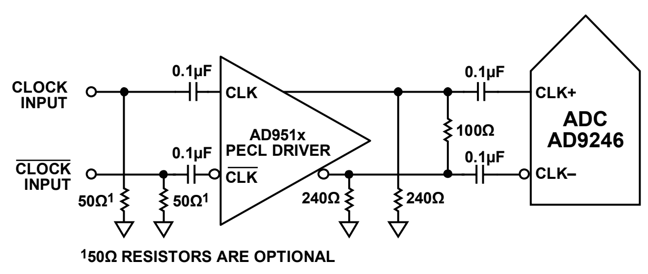

Figure 64. Differential PECL Sample Clock

A third option is to ac-couple a differential LVDS signal to the sample clock input pins as shown in Figure 65. The AD9510/ AD9511/AD9512/AD9513/AD9514/AD9515 family of clock drivers offers excellent jitter performance.

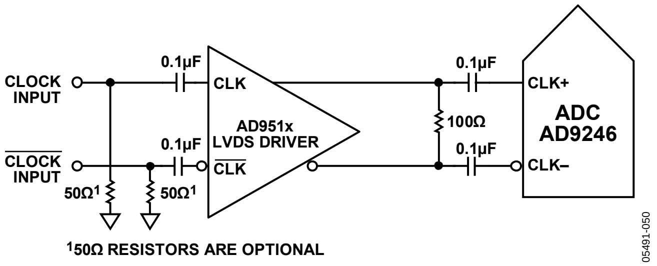

Figure 65. Differential LVDS Sample Clock

In some applications, it is acceptable to drive the sample clock inputs with a single-ended CMOS signal. In such applications, directly drive CLK+ from a CMOS gate, while bypassing the CLK– pin to ground using a 0.1 μF capacitor in parallel with a 39 kΩ resistor (see Figure 66). CLK+ may be directly driven from a CMOS gate. This input is designed to withstand input voltages up to 3.6 V, making the selection of the drive logic voltage very flexible. When driving CLK+ with a 1.8 V CMOS signal, biasing the CLK– pin with a 0.1 μF capacitor in parallel with a 39 kΩ resistor (see Figure 66) is required. The 39 kΩ resistor is not required when driving CLK+ with a 3.3 V CMOS signal (see Figure 67).

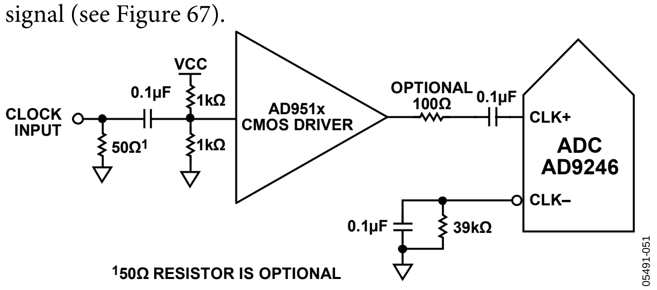

Figure 66. Single-Ended 1.8 V CMOS Sample Clock

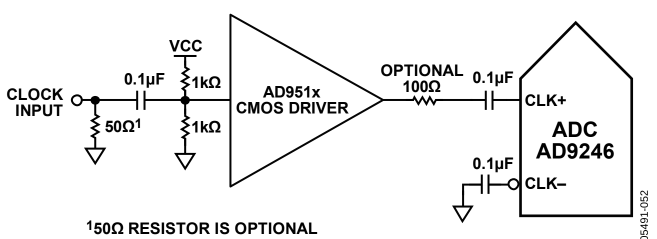

Figure 67. Single-Ended 3.3 V CMOS Sample Clock

Clock Duty Cycle

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals. As a result, these ADCs may be sensitive to clock duty cycle. Commonly, a ±5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The AD9246 contains a duty cycle stabilizer (DCS) that retimes the nonsampling, or falling edge, providing an internal clock signal with a nominal 50% duty cycle. This allows a wide range of clock input duty cycles without affecting the performance of the AD9246. Noise and distortion performance are nearly flat for a wide range of duty cycles when the DCS is on, as shown in Figure 44.

Jitter in the rising edge of the input is still of paramount concern and is not reduced by the internal stabilization circuit. The duty cycle control loop does not function for clock rates less than 20 MHz nominally. The loop has a time constant associated with it that needs to be considered in applications where the clock rate can change dynamically. This requires a wait time of 1.5 μs to 5 μs after a dynamic clock frequency increase (or decrease) before the DCS loop is relocked to the input signal. During the time period the loop is not locked, the DCS loop is bypassed, and the internal device timing is dependant on the duty cycle of the input clock signal. In such an application, it may be appropriate to disable the duty cycle stabilizer. In all other applications, enabling the DCS circuit is recommended to maximize ac performance.

The DCS can be enabled or disabled by setting the SDIO/DCS pin when operating in the external pin mode (see Table 10), or via the SPI as described in the Table 13.

Table 10. Mode Selection (External Pin Mode)

Voltage at Pin	SCLK/DFS	SDIO/DCS
AGND	Binary (default)	DCS disabled
AVDD	Twos complement	DCS enabled (default)

JITTER CONSIDERATIONS

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_{INPUT}) due to jitter (t_J) is calculated as follows:

$$SNR = -20 \log (2\pi \times f_{INPUT} \times t_J)$$

In the equation, the rms aperture jitter represents the root mean square of all jitter sources, which include the clock input, analog input signal, and ADC aperture jitter specification. IF undersampling applications are particularly sensitive to jitter, as illustrated in Figure 68.

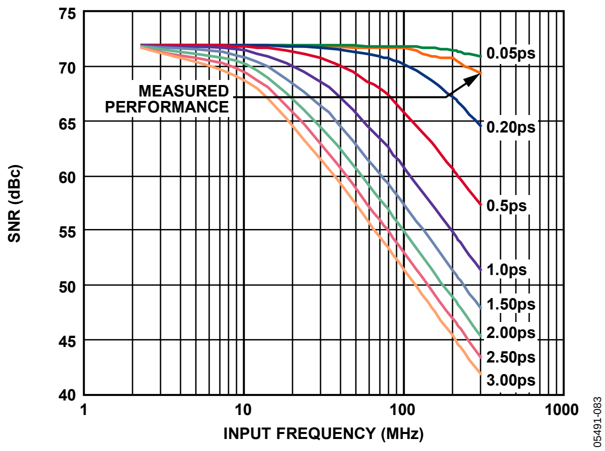

Figure 68. SNR vs. Input Frequency and Jitter

Treat the clock input as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9246. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. The power supplies should also not be shared with analog input circuits, such as buffers, to avoid the clock modulating onto the input signal or vice versa. Low jitter, crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it should be retimed by the original clock at the last step.

Refer to the AN-501 Application Note and the AN-756 Application Note for more in-depth information about jitter performance as it relates to ADCs.

POWER DISSIPATION AND STANDBY MODE

As shown in Figure 69 and Figure 70, the power dissipated by the AD9246 is proportional to its sample rate. The digital power dissipation is determined primarily by the strength of the digital drivers and the load on each output bit. The maximum DRVDD current (I_{DRVDD}) can be calculated as:

$$I_{DRVDD} = V_{DRVDD} \times C_{LOAD} \times \frac{f_{CLK}}{2} \times N$$

where *N* is the number of output bits, 14 in the case of the AD9246.

This maximum current occurs when every output bit switches on every clock cycle, that is, a full-scale square wave at the Nyquist frequency, $f_{CLK}/2$. In practice, the DRVDD current is established by the average number of output bits switching, which is determined by the sample rate and the characteristics of the analog input signal. Reducing the capacitive load presented to the output drivers can minimize digital power consumption. The data in Figure 69 and Figure 70 was taken under the same operating conditions as the data for the Typical Performance Characteristics section with a 5 pF load on each output driver.

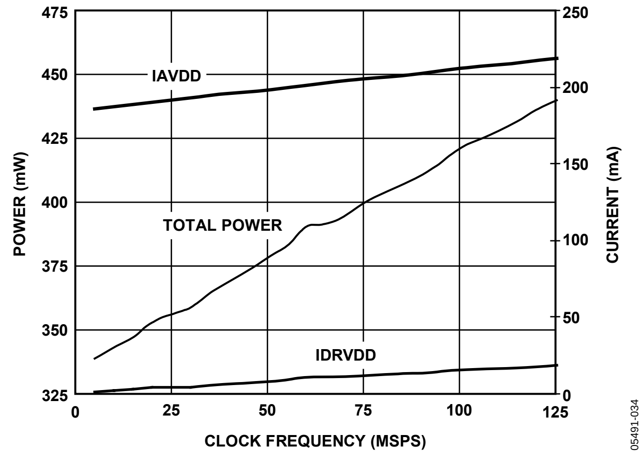

Figure 69. AD9246-125 Power and Current vs. Clock Frequency f_{IN} = 30 MHz

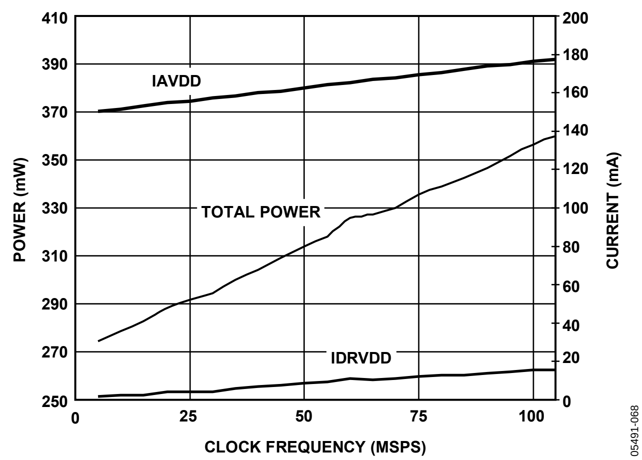

Figure 70. AD9246-105 Power and Current vs. Clock Frequency f_{IN} = 30 MHz

Power-Down Mode

By asserting the PDWN pin high, the AD9246 is placed in power-down mode. In this state, the ADC typically dissipates 1.8 mW. During power-down, the output drivers are placed in a high impedance state. Reasserting the PDWN pin low returns the AD9246 to its normal operational mode. This pin is both 1.8 V and 3.3 V tolerant.

Low power dissipation in power-down mode is achieved by shutting down the reference, reference buffer, biasing networks, and clock. The decoupling capacitors on REFT and REFB are discharged when entering power-down mode and then must be recharged when returning to normal operation. As a result, the wake-up time is related to the time spent in power-down mode; and shorter power-down cycles result in proportionally shorter wake-up times. With the recommended 0.1 μF decoupling capacitors on REFT and REFB, it takes approximately 0.25 ms to fully discharge the reference buffer decoupling capacitors and 0.35 ms to restore full operation.

Standby Mode

When using the SPI port interface, the user can place the ADC in power-down or standby modes. Standby mode allows the user to keep the internal reference circuitry powered when faster wake-up times are required. See the Memory Map section for more details.

DIGITAL OUTPUTS

The AD9246 output drivers can be configured to interface with 1.8 V to 3.3 V logic families by matching DRVDD to the digital supply of the interfaced logic. The output drivers are sized to provide sufficient output current to drive a wide variety of logic families. However, large drive currents tend to cause current glitches on the supplies that may affect converter performance. Applications requiring the ADC to drive large capacitive loads or large fan-outs may require external buffers or latches.

The output data format can be selected for either offset binary or twos complement by setting the SCLK/DFS pin when operating in the external pin mode (see Table 10). As detailed in the Analog Devices user manual titled *Interfacing to High Speed ADCs via SPI*, the data format can be selected for either offset binary, twos complement, or Gray code when using the SPI control.

Out-of-Range (OR) Condition

An out-of-range condition exists when the analog input voltage is beyond the input range of the ADC. OR is a digital output that is updated along with the data output corresponding to the particular sampled input voltage. Thus, OR has the same pipeline latency as the digital data.

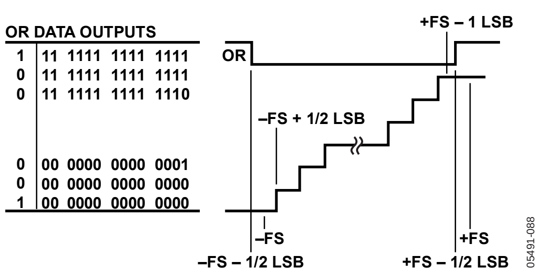

Figure 71. OR Relation to Input Voltage and Output Data

OR is low when the analog input voltage is within the analog input range and high when the analog input voltage exceeds the input range as shown in Figure 71.

OR will remain high until the analog input returns to within the input range and another conversion is completed. By logically AND'ing the OR bit with the MSB and its complement, overrange high or underrange low conditions can be detected. Table 11 is a truth table for the overrange/underrange circuit in Figure 72, which uses NAND gates.

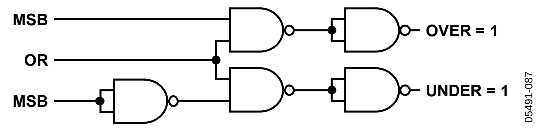

Figure 72. Overrange/Underrange Logic

Table 11. Overrange/Underrange Truth Table

OR	MSB	Analog Input Is:
0	0	Within Range
0	1	Within Range
1	0	Underrange
1	1	Overrange

Digital Output Enable Function (OEB)

The AD9246 has three-state ability. If the OEB pin is low, the output data drivers are enabled. If the OEB pin is high, the output data drivers are placed in a high impedance state. This is not intended for rapid access to the data bus.

Note that OEB is referenced to the digital supplies (DRVDD) and should not exceed that supply voltage.

TIMING

The AD9246 provides latched data outputs with a pipeline delay of twelve clock cycles. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the clock signal.

The length of the output data lines and the loads placed on them should be minimized to reduce transients within the AD9246. These transients can degrade the dynamic performance of the converter. The AD9246 also provides data clock output (DCO) intended for capturing the data in an external register. The data outputs are valid on the rising edge of DCO. See Figure 2 for a graphical timing description.

The lowest typical conversion rate of the AD9246 is 10 MSPS. At clock rates below 10 MSPS, dynamic performance can degrade.

Table 12. Output Data Format

Input (V)	Condition (V)	Binary Output Mode	Twos Complement Mode	Gray Code Mode (SPI accessible)	OR
VIN+ – VIN–	< –VREF – 0.5 LSB	00 0000 0000 0000	10 0000 0000 0000	11 0000 0000 0000	1
VIN+ – VIN–	= –VREF	00 0000 0000 0000	10 0000 0000 0000	11 0000 0000 0000	0
VIN+ – VIN–	= 0	10 0000 0000 0000	00 0000 0000 0000	00 0000 0000 0000	0
VIN+ – VIN–	= +VREF – 1.0 LSB	11 1111 1111 1111	01 1111 1111 1111	10 0000 0000 0000	0
VIN+ – VIN–	> +VREF – 0.5 LSB	11 1111 1111 1111	01 1111 1111 1111	10 0000 0000 0000	1

SERIAL PORT INTERFACE (SPI)

The AD9246 serial port interface (SPI) allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. This provides the user added flexibility and customization depending on the application. Addresses are accessed via the serial port and may be written to or read from via the port. Memory is organized into bytes that are further divided into fields, as documented in the Memory Map section. For detailed operational information, see the *Interfacing to High Speed ADCs via SPI* user manual.

CONFIGURATION USING THE SPI

As summarized in Table 13, three pins define the SPI of this ADC. The SCLK/DFS pin synchronizes the read and write data presented to the ADC. The SDIO/DCS dual purpose pin allows data to be sent and read from the internal ADC memory map registers. The CSB pin is an active low control that enables or disables the read and write cycles.

Table 13. Serial Port Interface Pins

Pin Name	Function
SCLK/DFS	SCLK (Serial Clock) is the serial shift clock in. SCLK synchronizes serial interface reads and writes.
SDIO/DCS	SDIO (Serial Data Input/Output) is a dual purpose pin. The typical role for this pin is an input and output depending on the instruction being sent and the relative position in the timing frame.
CSB	CSB (Chip Select Bar) is an active low control that gates the read and write cycles.

The falling edge of the CSB in conjunction with the rising edge of the SCLK determines the start of the framing. Figure 73 and Table 14 provide an example of the serial timing and its definitions.

Other modes involving the CSB are available. The CSB can be held low indefinitely to permanently enable the device (this is called streaming). The CSB can stall high between bytes to allow for additional external timing. When CSB is tied high, SPI functions are placed in a high impedance mode. This mode turns on any SPI pin secondary functions.

During an instruction phase, a 16-bit instruction is transmitted. Data follows the instruction phase and the length is determined by the W0 bit and the W1 bit. All data is composed of 8-bit words. The first bit of each individual byte of serial data indicates whether a read or write command is issued. This allows the serial data input/output (SDIO) pin to change direction from an input to an output.

In addition to word length, the instruction phase determines if the serial frame is a read or write operation, allowing the serial port to be used to both program the chip as well as read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the serial data input/output (SDIO) pin to change direction from an input to an output at the appropriate point in the serial frame.

Data may be sent in MSB- or in LSB-first mode. MSB first is default on power up and may be changed via the configuration register. For more information, see the *Interfacing to High Speed ADCs via SPI* user manual.

Table 14. SPI Timing Diagram Specifications

Name	Description
t_{DS}	Setup time between data and rising edge of SCLK
t_{DH}	Hold time between data and rising edge of SCLK
t_{CLK}	Period of the clock
t_S	Setup time between CSB and SCLK
t_H	Hold time between CSB and SCLK
t_{HI}	Minimum period that SCLK should be in a logic high state
t_{LO}	Minimum period that SCLK should be in a logic low state

HARDWARE INTERFACE

The pins described in Table 13 comprise the physical interface between the user's programming device and the serial port of the AD9246. The SCLK and CSB pins function as inputs when using the SPI interface. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI interface is flexible enough to be controlled by either PROM or PIC microcontrollers. This provides the user with the ability to use an alternate method to program the ADC. One method is described in detail in the AN-812 Application Note.

When the SPI interface is not used, some pins serve a dual function. When strapped to AVDD or ground during device power on, the pins are associated with a specific function.

CONFIGURATION WITHOUT THE SPI

In applications that do not interface to the SPI control registers, the SDIO/DCS and SCLK/DFS pins serve as stand alone CMOS-compatible control pins. When the device is powered up, it is assumed that the user intends to use the pins as static control lines for the output data format and duty cycle stabilizer (see Table 10). In this mode, the CSB chip select should be connected to AVDD, which will disable the serial port interface. For more information, see the *Interfacing to High Speed ADCs via SPI* user manual.

MEMORY MAP

READING THE MEMORY MAP TABLE

Each row in the memory map table has eight address locations. The memory map is roughly divided into three sections: Chip Configuration Registers map (Address 0x00 to Address 0x02), Device Index and Transfer Registers map (Address 0xFF), and ADC Functions map (Address 0x08 to Address 0x18).

The memory map register in Table 15 displays the register address number in hexadecimal in the first column. The last column displays the default value for each hexadecimal address. The Bit 7 (MSB) column is the start of the default hexadecimal value given. For example, Hexadecimal Address 0x14, output_phase has a hexadecimal default value of 0x00. This means Bit 3 = 0, Bit 2 = 0, Bit 1 = 1, and Bit 0 = 1 or 0011 in binary. This setting is the default output clock or DCO phase adjust option. The default value adjusts the DCO phase 90 degrees relative to the nominal DCO edge and 180 degrees relative to the data edge. For more information on this function, consult the *Interfacing to High Speed ADCs via SPI* user manual.

Open Locations

Locations marked as open are currently not supported for this device. When required, these locations should be written with 0s. Writing to these locations is required only when part of an address location is open (for example, Address 0x14). If the entire address location is open (Address 0x13), then the address location does not need to be written.

Default Values

Coming out of reset, critical registers are loaded with default values. The default values for the registers are provided in Table 15.

Logic Levels

An explanation of two registers follows:

- "Bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit."
- "Clear a bit" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit."

SPI-Accessible Features

A list of features accessible via the SPI and a brief description of what the user can do with these features follows. These features are described in detail in the *Interfacing to High Speed ADCs via SPI* user manual.

- Modes: Set either power-down or standby mode.
- Clock: Access the DCS via the SPI.
- Offset: Digitally adjust the converter offset.
- Test I/O: Set test modes to have known data on output bits.
- Output Mode: Setup outputs, vary the strength of the output drivers.
- Output Phase: Set the output clock polarity.
- VREF: Set the reference voltage.

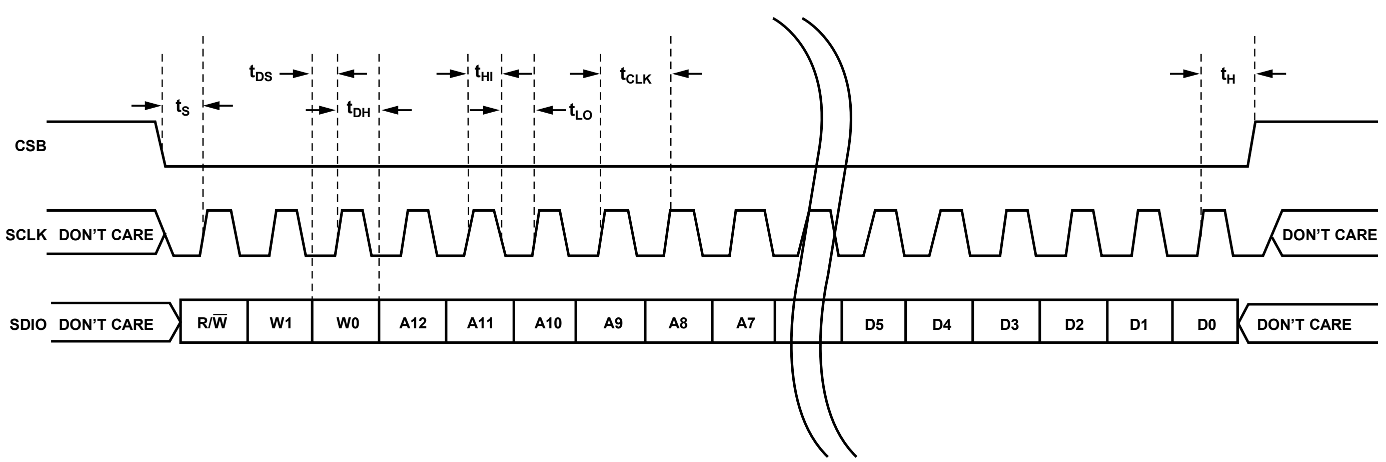

Figure 73. Serial Port Interface Timing Diagram

Table 15. Memory Map Register

Addr. (Hex)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/ Comments
Chip Configuration Registers											
00	chip_port_config	Open	LSB first	Soft reset	Open	Open	Soft reset	LSB first	Open	0x18	The nibbles should be mirrored so that LSB- or MSB-first mode registers correctly regardless of shift mode.
01	chip_id	8-bit Chip ID Bits 7:0 (AD9246 = 0x00), (default)								Read only	Default is unique chip ID, different for each device.
02	chip_grade	Open	Open	Open	Open	Child ID 0 = 125 MSPS, 1 = 105 MSPS	Open	Open	Open	Read only	Child ID used to differentiate speed grades.
Device Index and Transfer Registers											
FF	device_update	Open	Open	Open	Open	Open	Open	Open	SW transfer	0x00	Synchronously transfers data from the master shift register to the slave.
Global ADC Functions											
08	modes	Open	Open	PDWN 0—Full 1—Standby	Open	Open	Internal power-down mode 000—normal (power-up) 001—full power-down 010—standby 011—normal (power-up) Note: External PDWN pin overrides this setting.			0x00	Determines various generic modes of chip operation. See Power Dissipation and Standby Mode and SPI-Accessible Features sections.
09	clock	Open	Open	Open	Open	Open	Open	Open	Duty cycle stabilizer 0—disabled 1—enabled	0x01	See Clock Duty Cycle and SPI-Accessible Features sections.

Addr. (Hex)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/ Comments
Flexible ADC Functions											
10	offset			**Digital Offset Adjust<5:0>** 011111 011110 011101 … 000010 000001 000000 111111 111110 111101 ... 100001 100000			**Offset in LSBs** +31 +30 +29 +2 +1 0 1 −2 −3 −31 −32			0x00	Adjustable for offset inherent in the converter. See SPI-Accessible Features section.
0D	test_io			PN23 0 = normal 1 = reset	PN9 0 = normal 1 = reset		Global Output Test Options 0—off 1—midscale short 2—+FS short 3—−FS short 4—checker board output 5—PN 23 sequence 6—PN 9 7—one/zero word toggle			0x00	See the *Interfacing to High Speed ADCs via SPI* user manual.
14	output_mode	Output Driver Configuration 00 for DRVDD = 2.5 V to 3.3 V 10 for DRVDD = 1.8 V		Open	Output Disable 1—disabled 0—enabled[1]	Open	Output Data Invert 1 = invert	Data Format Select 00—offset binary (default) 01—twos complement		0x00	Configures the outputs and the format of the data.
16	output_phase	Output Clock Polarity 1 = inverted 0 = normal	Open	Open	Open	Open	Open	Open	Open	0x00	See SPI-Accessible Features section.
18	VREF	Internal Reference Resistor Divider 00—VREF = 1.25 V 01—VREF = 1.5 V 10—VREF = 1.75 V 11—VREF = 2.00 V		Open	Open	Open	Open	Open	Open	0xC0	See SPI-Accessible Features section.

[1] External Output Enable (OEB) pin must be high.

LAYOUT CONSIDERATIONS

POWER AND GROUND RECOMMENDATIONS

When connecting power to the AD9246, it is recommended that two separate supplies be used: one for analog (AVDD, 1.8 V nominal) and one for digital (DRVDD, 1.8 V to 3.3 V nominal). If only a single 1.8 V supply is available, then it is routed to AVDD first, then tapped off and isolated with a ferrite bead or filter choke with decoupling capacitors proceeding connection to DRVDD. The user can employ several different decoupling capacitors to cover both high and low frequencies. These should be located close to the point of entry at the PC board level and close to the parts with minimal trace length.

A single PC board ground plane is sufficient when using the AD9246. With proper decoupling and smart parti-tioning analog, digital, and clock sections of the PC board, optimum performance is easily achieved.

Exposed Paddle Thermal Heat Slug Recommendations

It is required that the exposed paddle on the underside of the ADC is connected to analog ground (AGND) to achieve the best electrical and thermal performance of the AD9246. An exposed, continuous copper plane on the PCB should mate to the AD9246 exposed paddle, Pin 0. The copper plane should have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. These vias should be solder filled or plugged.

To maximize the coverage and adhesion between the ADC and PCB, partition the continuous plane by overlaying a silkscreen on the PCB into several uniform sections. This provides several tie points between the two during the reflow process. Using one continuous plane with no partitions only guarantees one tie point between the ADC and PCB. See Figure 74 for a PCB layout example. For detailed information on packaging and the PCB layout of chip scale packages, see AN-772, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package* application note.

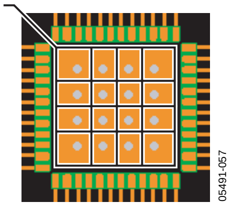

Figure 74. Typical PCB Layout

CML

The CML pin should be decoupled to ground with a 0.1 μF capacitor, as shown in Figure 55.

RBIAS

The AD9246 requires the user to place a 10 kΩ resistor between the RBIAS pin and ground. This resister sets the master current reference of the ADC core and should have at least a 1% tolerance.

REFERENCE DECOUPLING

The VREF pin should be externally decoupled to ground with a low ESR 1.0 μF capacitor in parallel with a 0.1 μF ceramic low ESR capacitor. In all reference configurations, REFT and REFB are bypass points provided for reducing the noise contributed by the internal reference buffer. It is recommended to place an external 0.1 μF ceramic capacitor across REFT/REFB. While it is not required to place this 0.1 μF capacitor, the SNR performance will degrade by approximately 0.1 dB without it. All reference decoupling capacitors should be placed as close to the ADC as possible with minimal trace lengths.

EVALUATION BOARD

The AD9246 evaluation board provides all of the support circuitry required to operate the ADC in its various modes and configurations. The converter can be driven differentially through a double balun configuration (default) or through the AD8352 differential driver. The ADC can also be driven in a single-ended fashion. Separate power pins are provided to isolate the DUT from the AD8352 drive circuitry. Each input configuration can be selected by proper connection of various components (see Figure 76 to Figure 86). Figure 75 shows the typical bench characterization setup used to evaluate the ac performance of the AD9246.

It is critical that the signal sources used for the analog input and clock have very low phase noise (<1 ps rms jitter) to realize the optimum performance of the converter. Proper filtering of the analog input signal to remove harmonics and lower the integrated or broadband noise at the input is also necessary to achieve the specified noise performance.

See Figure 76 to Figure 80 for the complete schematics and layout diagrams that demonstrate the routing and grounding techniques that should be applied at the system level.

POWER SUPPLIES

This evaluation board comes with a wall-mountable switching power supply that provides a 6 V, 2 A maximum output. Simply connect the supply to the rated 100 V ac to 240 V ac wall outlet at 47 Hz to 63 Hz. The other end is a 2.1 mm inner diameter jack that connects to the PCB at P500. Once on the PC board, the 6 V supply is fused and conditioned before connecting to five low dropout linear regulators that supply the proper bias to each of the various sections on the board.

When operating the evaluation board in a nondefault condition, L501, L503, L504, L508, and L509 can be removed to disconnect the switching power supply. This enables the user to individually bias each section of the board. Use P501 to connect a different supply for each section. At least one 1.8 V supply is needed with a 1 A current capability for AVDD_DUT and DRVDD_DUT; however, it is recommended that separate supplies be used for analog and digital. To operate the evaluation board using the AD8352 option, a separate 5.0 V supply (AMP_VDD) with a 1 A current capability is needed. To operate the evaluation board using the alternate SPI options, a separate 3.3 V analog supply is needed, in addition to the other supplies. The 3.3 V supply (AVDD_3.3V) should have a 1 A current capability as well. Solder jumpers J501, J502, and J505 allow the user to combine these supplies. See Figure 80 for more details.

INPUT SIGNALS

When connecting the clock and analog source, use clean signal generators with low phase noise, such as Rohde & Schwarz SMHU or Agilent HP8644 signal generators or the equivalent. Use one meter long, shielded, RG-58, 50 Ω coaxial cable for making connections to the evaluation board. Enter the desired frequency and amplitude for the ADC. Typically, most ADI evaluation boards can accept a ~2.8 V p-p or 13 dBm sine wave input for the clock. When connecting the analog input source, it is recommended to use a multipole, narrow-band, band-pass filter with 50 Ω terminations. ADI uses TTE®, Allen Avionics, and K&L® types of band-pass filters. Connect the filter directly to the evaluation board, if possible.

OUTPUT SIGNALS

The parallel CMOS outputs interface directly with the Analog Devices' standard single-channel FIFO data capture board (HSC-ADC-EVALB-SC). For more information on the FIFO boards and their optional settings, visit www.analog.com/FIFO.

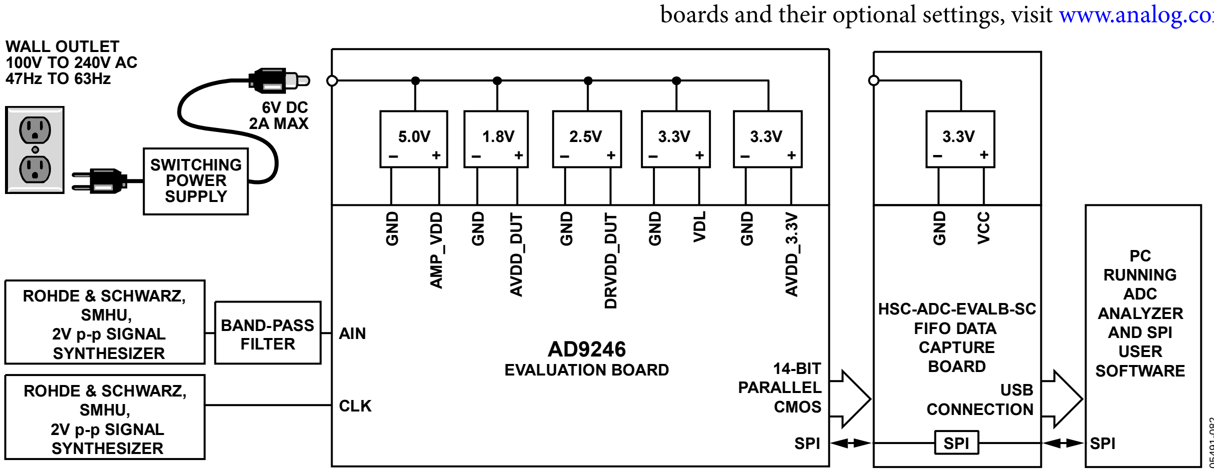

Figure 75. Evaluation Board Connection

DEFAULT OPERATION AND JUMPER SELECTION SETTINGS

The following is a list of the default and optional settings or modes allowed on the AD9246 Rev. A evaluation board.

POWER

Connect the switching power supply that is supplied in the evaluation kit between a rated 100 V ac to 240 V ac wall outlet at 47 Hz to 63 Hz and P500.

VIN

The evaluation board is set up for a double balun configuration analog input with optimum 50 Ω impedance matching out to 70 MHz. For more bandwidth response, the differential capacitor across the analog inputs can be changed or removed (see Table 8). The common mode of the analog inputs is developed from the center tap of the transformer via the CML pin of the ADC. See the Analog Input Considerations section.

VREF

VREF is set to 1.0 V by tying the SENSE pin to ground via JP507 (Pin 1 and Pin 2). This causes the ADC to operate in 2.0 V p-p full-scale range. A separate external reference option is also included on the evaluation board. Simply connect JP507 between Pin 2 and Pin 3, connect JP501, and provide an external reference at E500. Proper use of the VREF options is detailed in the Voltage Reference section.

RBIAS

RBIAS, requires a 10 kΩ resistor (R503) to ground and is used to set the ADC core bias current.

CLOCK

The default clock input circuitry is derived from a simple transformer-coupled circuit using a high bandwidth 1:1 impedance ratio transformer (T503) that adds a very low amount of jitter to the clock path. The clock input is 50 Ω terminated and ac-coupled to handle single-ended sine wave inputs. The transformer converts the single-ended input to a differential signal that is clipped before entering the ADC clock inputs.

PDWN

To enable the power-down feature, connect JP506, shorting the PDWN pin to AVDD.

CSB

The CSB pin is internally pulled-up, setting the chip into external pin mode, to ignore the SDIO and SCLK information. To connect the control of the CSB pin to the SPI circuitry on the evaluation board, connect JP1 Pin 1 and Pin 2. To set the chip into serial pin mode, to enable the SPI information on the SDIO and SCLK pins, tie JP1 low (connect Pin 2 and Pin 3) in the always enabled mode.

SCLK/DFS

If the SPI port is in external pin mode, the SCLK/DFS pin sets the data format of the outputs. If the pin is left floating, the pin is internally pulled down, setting the default condition to binary. Connecting JP2 Pin 2 and Pin 3 sets the format to twos complement. If the SPI port is in serial pin mode, connecting JP2 Pin 1 and Pin 2 connects the SCLK pin to the on board SPI circuitry. See the Serial Port Interface (SPI) section for more details.

SDIO/DCS

If the SPI port is in external pin mode, the SDIO/DCS pin acts to set the duty cycle stabilizer. If the pin is left floating, the pin is internally pulled up, setting the default condition to DCS enabled. To disable the DCS, connect JP3 Pin 2 and Pin 3. If the SPI port is in serial pin mode, connecting JP3 Pin 1 and Pin 2 connects the SDIO pin to the on-board SPI circuitry. See the Serial Port Interface (SPI) section for more details.

ALTERNATIVE CLOCK CONFIGURATIONS

A differential LVPECL clock can also be used to clock the ADC input using the AD9515 (U500). When using this drive option, the components listed in Table 16 need to be populated. Consult the AD9515 data sheet for further information.

To configure the analog input to drive the AD9515 instead of the default transformer option, the following components need to be added, removed, and/or changed.

1. Remove R507, R508, C532, and C533 in the default clock path.
2. Populate R505 with a 0 Ω resistors and C531 in the default clock path.
3. Populate R511, R512, R513, R515-R524, U500, R580, R582, R583, R584, C536, C537, and R586.

If using an oscillator, two oscillator footprint options are also available (OSC500) to check the performance of the ADC. JP508 provides the user flexibility in using the enable pin, which is common on most oscillators. Populate OSC500, R575, R587, and R588 to use this option.

ALTERNATIVE ANALOG INPUT DRIVE CONFIGURATION

This section provides a brief description of the alternative analog input drive configuration using the AD8352. When using this particular drive option, some components need to be populated as listed in Table 16. For more details on the AD8352 differential driver, including how it works and its optional pin settings, consult the AD8352 data sheet.

To configure the analog input to drive the AD8352 instead of the default transformer option, the following components need to be added, removed and/or changed.

1. Remove C1 and C2 in the default analog input path.
2. Populate R3 and R4 with 200 Ω resistors in the analog input path.
3. Populate the optional amplifier input path with all components, except R594, R595, and C502. Note that to terminate the input path, only one of these components, (R9, R592, or R590 and R591) should be populated.
4. Populate C529 with a 5 pF capacitor in the analog input path.

Currently, R561 and R562 are populated with 0 Ω resistors to allow signal connection. This area allows the user to design a filter if additional requirements are necessary.

SCHEMATICS

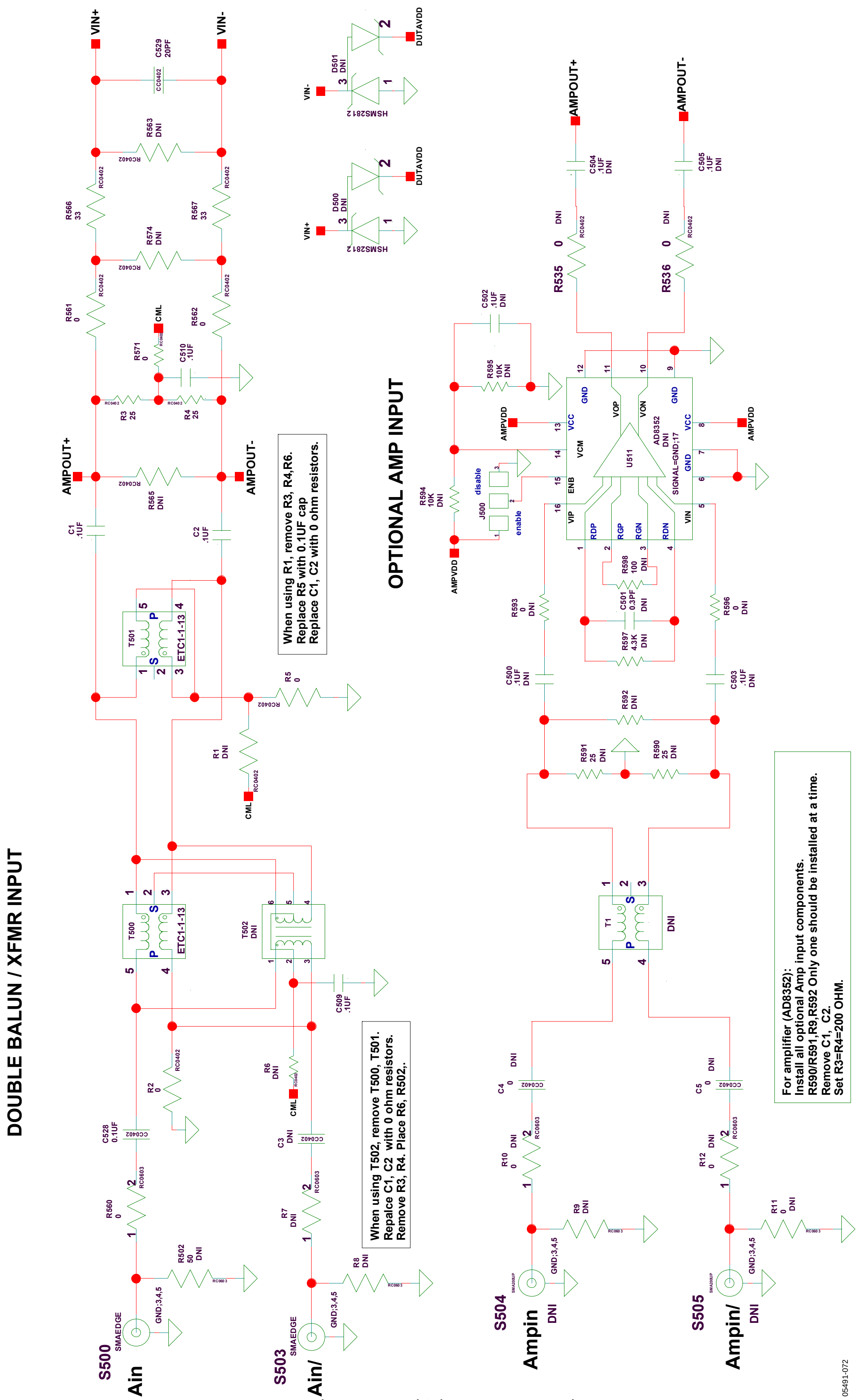

Figure 76. Evaluation Board Schematic, DUT Analog Inputs

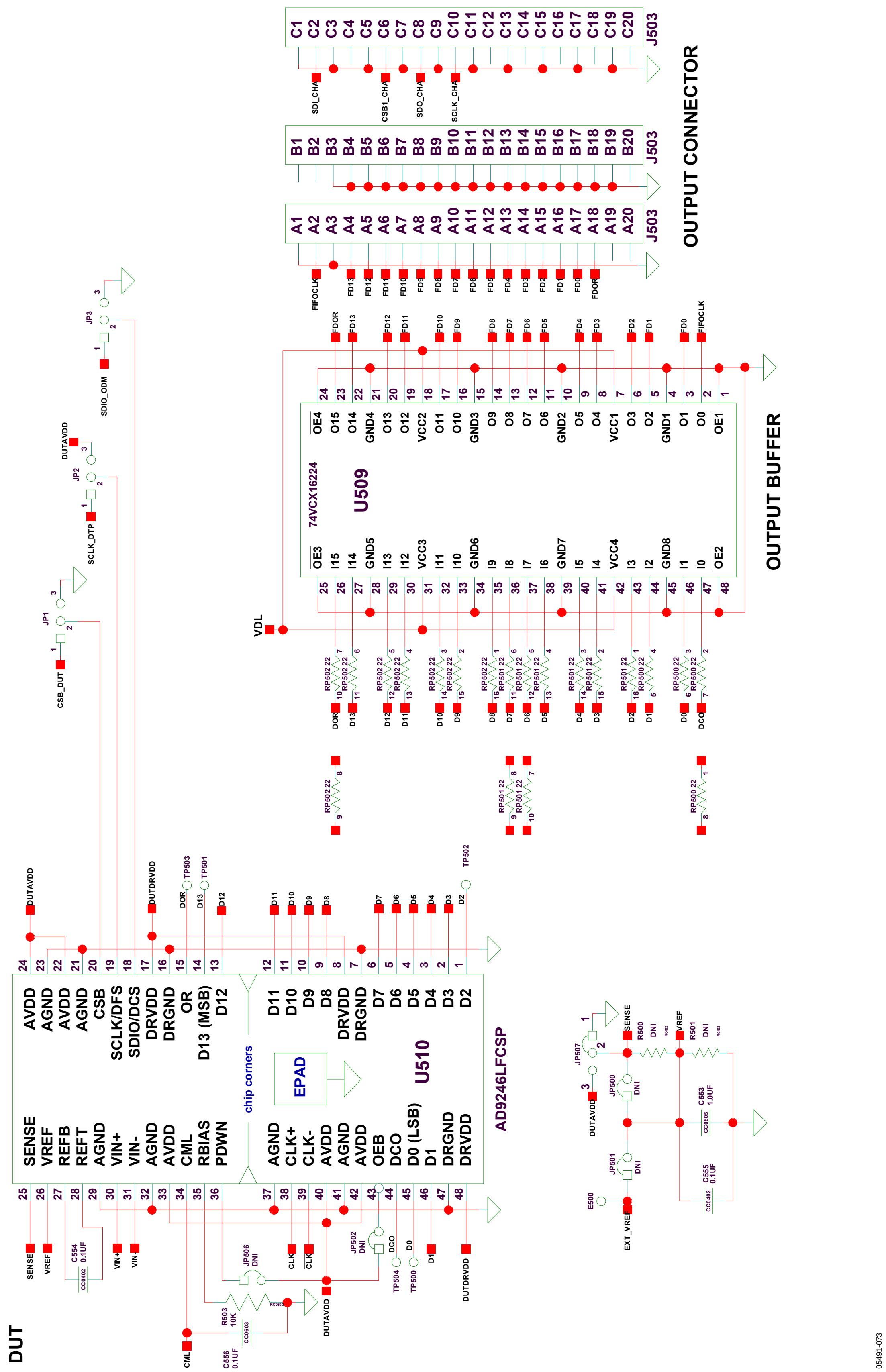

Figure 77. Evaluation Board Schematic, DUT, VREF, and Digital Output Interface

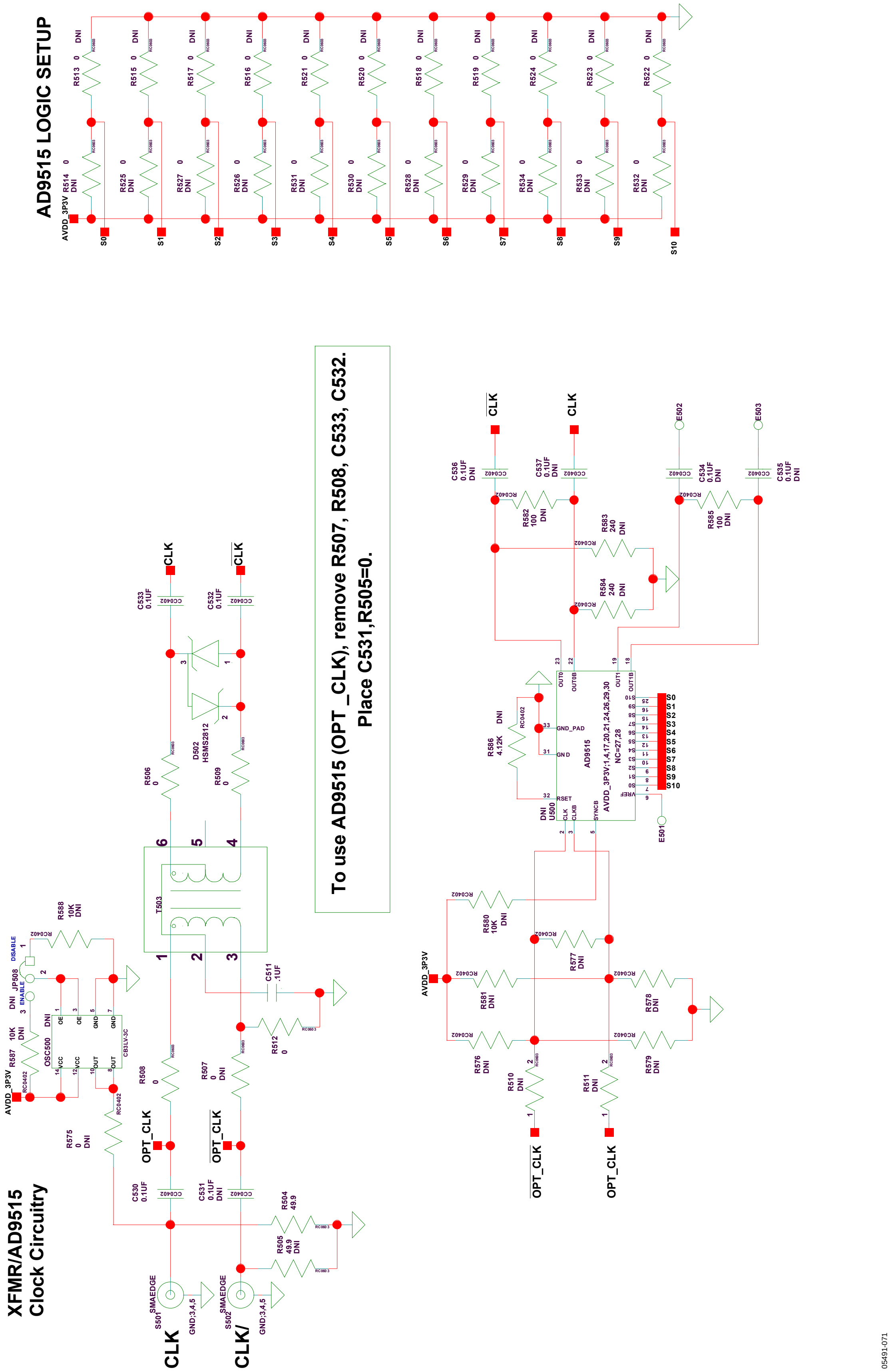

Figure 78. Evaluation Board Schematic, DUT Clock Input

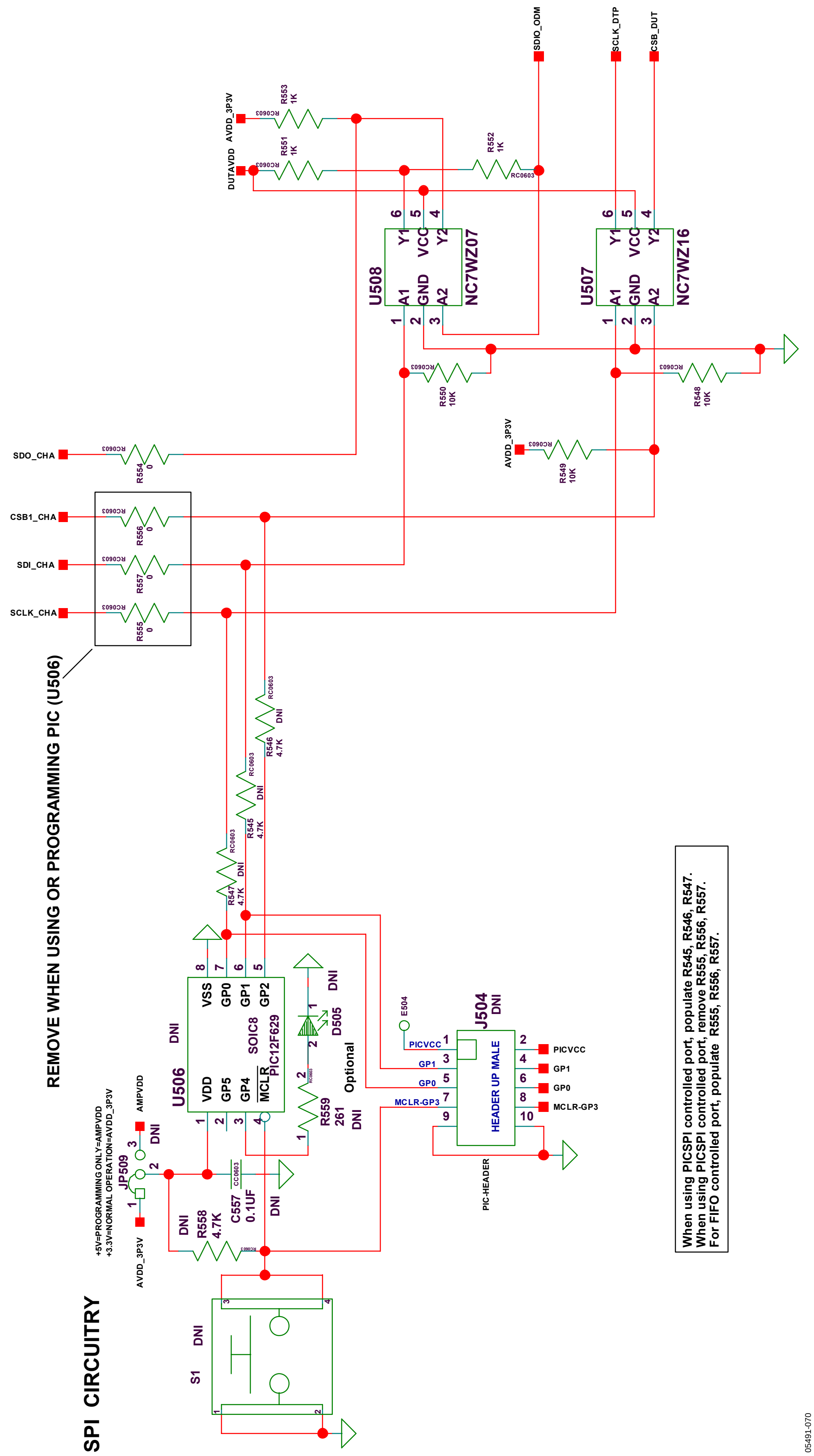

Figure 79. Evaluation Board Schematic, SPI Circuitry

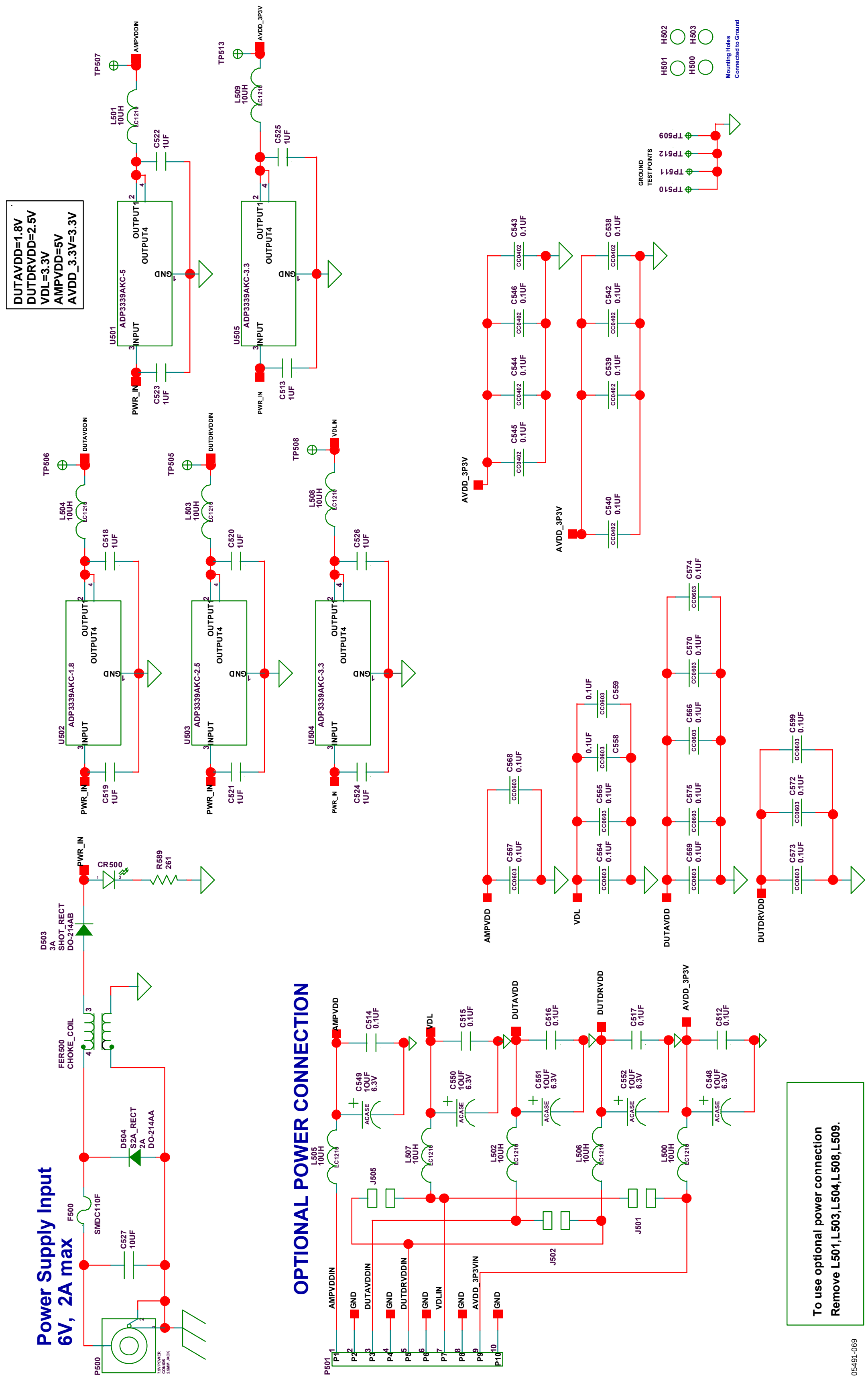

Figure 80. Evaluation Board Schematic, Power Supply Inputs

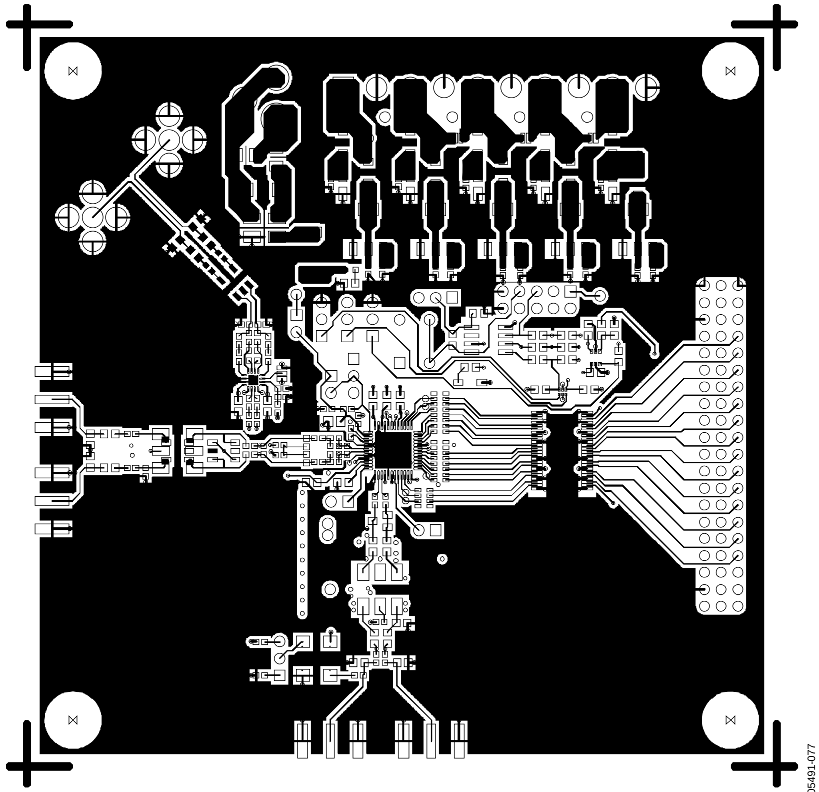

Figure 81. Evaluation Board Layout, Primary Side

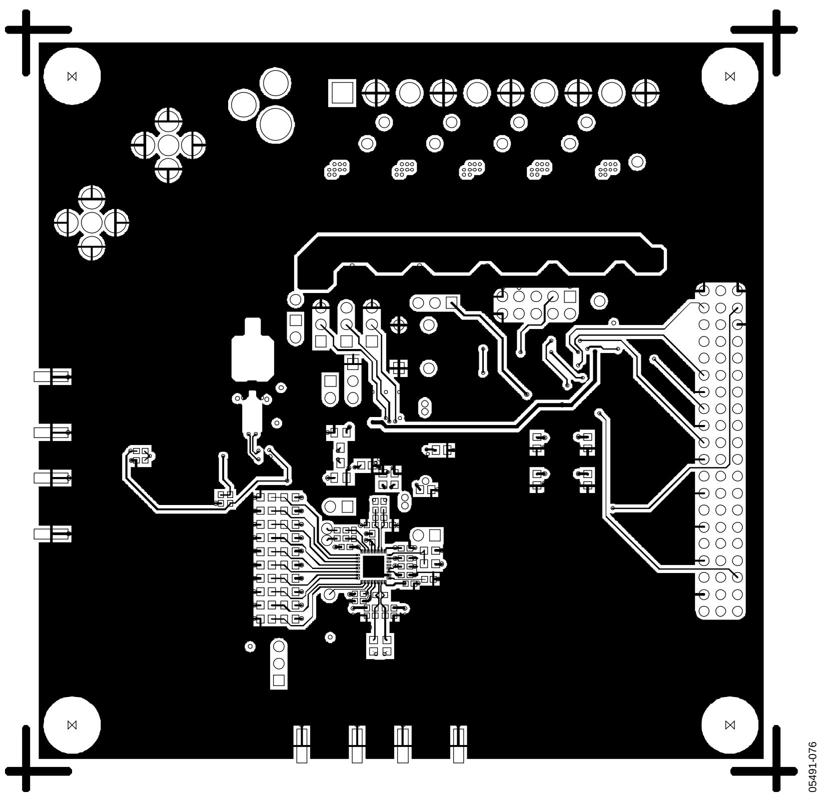

Figure 82. Evaluation Board Layout, Secondary Side (Mirrored Image)

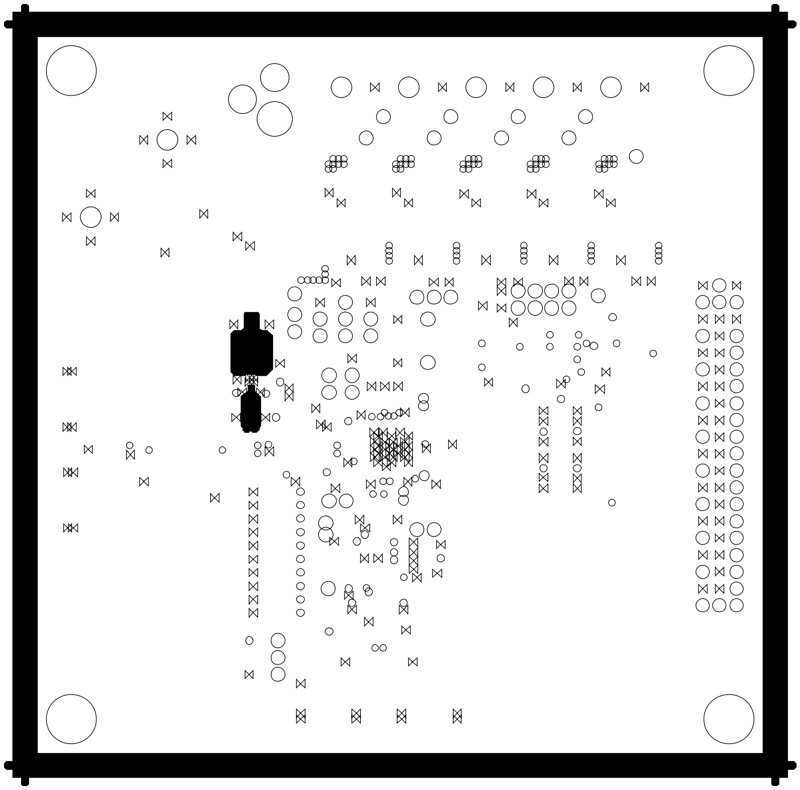

Figure 83. Evaluation Board Layout, Ground Plane

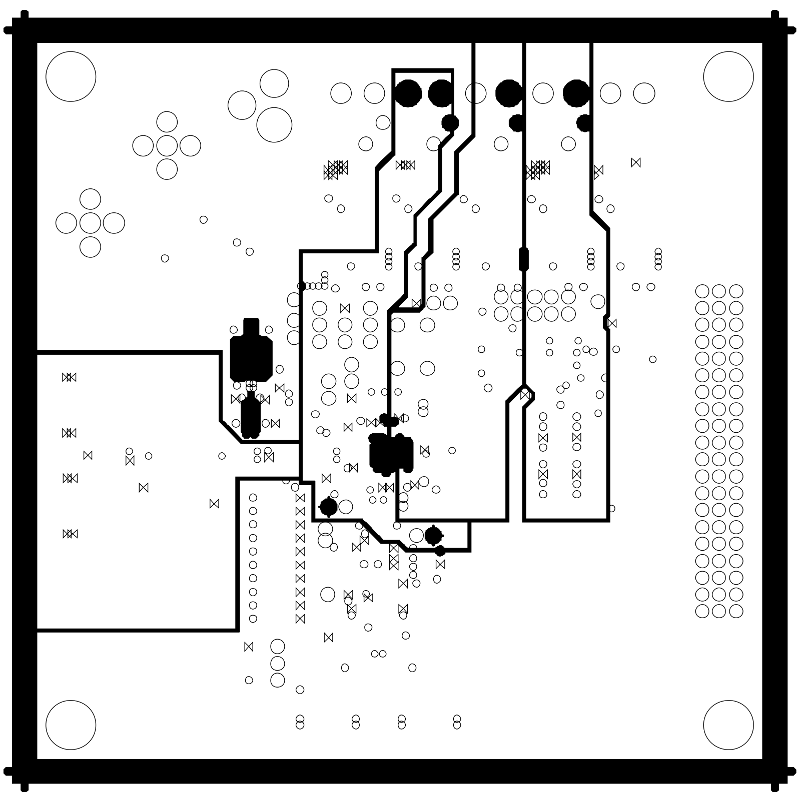

Figure 84. Evaluation Board Layout, Power Plane

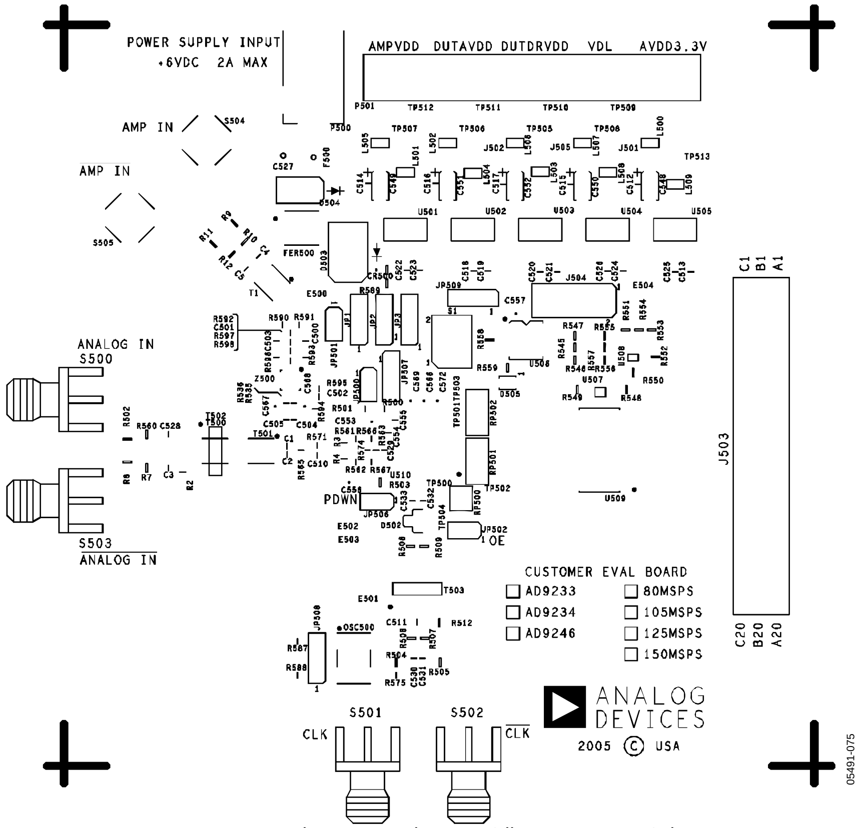

Figure 85. Evaluation Board Layout, Silkscreen Primary Side

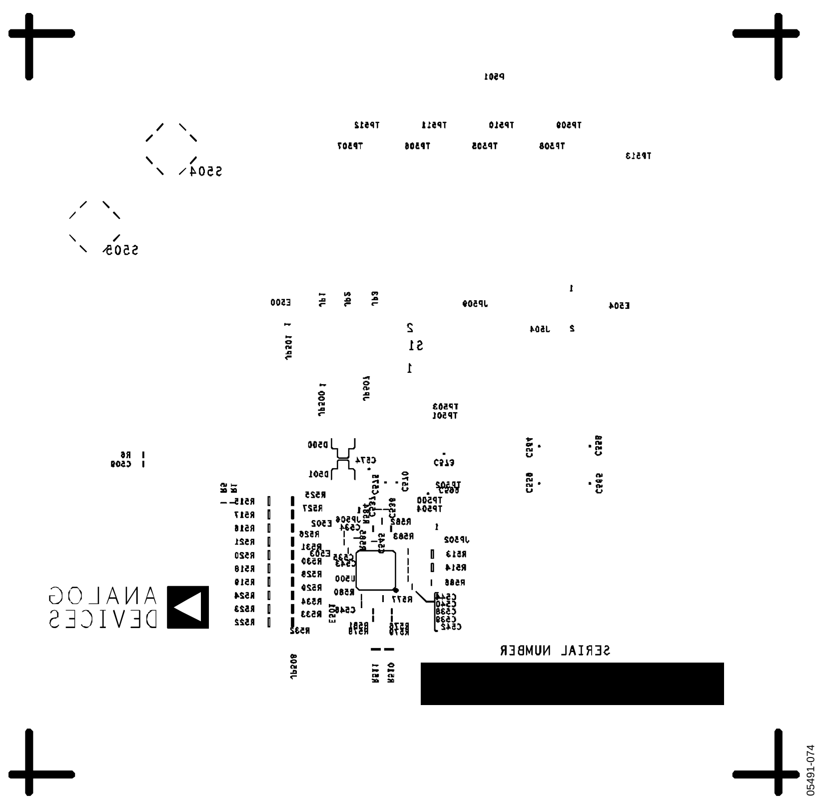

Figure 86. Evaluation Board Layout, Silkscreen Secondary Side (Mirrored Image)

BILL OF MATERIALS

Table 16. Evaluation Board Bill of Materials (BOM)

Item	Qty.	Omit (DNP)	Reference Designator	Device	Package	Description	Supplier/Part Number
1	1		AD9246CE_REVA	PCB		PCB	ADI
2	24		C1, C2, C509, C510, C511, C512, C514, C515, C516, C517, C528, C530, C532, C533, C538, C539, C540, C542, C543, C544, C545, C546, C554, C555	Capacitor	0402	0.1 µF	
		12	C3, C500, C502, C503, C504, C505, C531, C534, C535, C536, C537, C557				
3		1	C501	Capacitor	0402	0.3 pF	
4		2	C4, C5	Resistor	0402	0 Ω	
5	10		C513, C518, C519, C520, C521, C522, C523, C524, C525, C526	Capacitor	0402	1.0 µF	
6	1		C527	Capacitor	1206	10 µF	
7	1		C529	Capacitor	0402	20 pF	
8	5		C548, C549, C550, C551, C552	Capacitor	ACASE	10 µF	
9	1		C553	Capacitor	0805	1.0 µF	
10	15		C556, C558, C559, C564, C565, C566, C567, C568, C569, C570, C572, C573, C574, C575, C599	Capacitor	0603	0.1 µF	
11	1		CR500	LED	0603	green	Panasonic LNJ314G8TRA
12	1		D502	Diode	SOT-23	30 V, 20 mA, dual Schottky	HSMS2812
		2	D500, D501				
13	1		D503	Diode	DO-214AB	3 A, 30 V, SMC	Micro Commercial Group SK33MSCT
14	1		D504	Diode	DO-214AA	2 A, 50 V, SMC	Micro Commercial Group S2A
15		1	D505	LED	LN1461C	AMB	Amber LED
16	1		F500	Fuse	1210	6.0 V, 2.2 A trip current resettable fuse	Tyco, Raychem NANOSMDC110F-2
17	1		FER500	Choke	2020		Murata DLW5BSN191SQ2
18		1	J500	Jumper		Solder jumper	
19		3	J501, J502, J505	Jumper		Solder jumper	
20	1		J503	Connector	120 pin	Male header	Samtec TSW-140-08-G-T-RA
21		1	J504	Connector	10 pin	Male, 2 × 5	Samtec
22	3		JP1, JP2, JP3	Jumper	3 pin	Male, straight	Samtec TSW-103-07-G-S
23	4		JP500, JP501, JP502, JP506	Jumper	2 pin	Male, straight	Samtec TSW-102-07-G-S
24	1		JP507	Jumper	3-pin jumper	Male, straight	Samtec TSW-103-07-G-S
		2	JP508, JP509				
25	10		L500, L501, L502, L503, L504, L505, L506, L507, L508, L509	Ferrite Bead	3.2 × 2.5 × 1.6 mm		Digikey P9811CT-ND
26		1	OSC500	Oscillator	SMT	125 MHz or 105 MHz	CTS Reeves CB3LV-3C
27	1		P500	Connector	PJ-102A	DC power jack	Digikey CP-102A-ND
28		1	P501	Connector	10 pin	Male, straight	PTMICRO10

Item	Qty.	Omit (DNP)	Reference Designator	Device	Package	Description	Supplier/Part Number
29		6	R1, R6, R563, R565, R574, R577	Resistor	0402	DNI	
30	5		R2, R5, R561, R562, R571	Resistor	0402	0 Ω	
		6	R10, R11, R12, R535, R536, R575				
31	2		R3, R4	Resistor	0402	25 Ω	
32		6	R7, R8, R9, R502, R510, R511	Resistor	0603	DNI	
33		6	R500, R501, R576, R578, R579, R581	Resistor	0402	DNI	
34	4		R503, R548, R549, R550	Resistor	0603	10 kΩ	
35	1		R504	Resistor	0603	49.9 Ω	
		1	R505				
36	9		R506, R508, R509, R512, R554, R555, R556, R557, R560	Resistor	0603	0 Ω	
		23	R507, R514, R513, R515, R516, R517, R518, R519, R520, R521, R522, R523, R524, R525, R526, R527, R528, R529, R530, R531, R532, R533, R534,				
37		4	R545, R546, R547, R558	Resistor	0603	4.7 kΩ	
38	3		R551, R552, R553	Resistor	0603	1 kΩ	
39		1	R559	Resistor	0603	261 Ω	
40	2		R566, R567	Resistor	0402	33 Ω	
41		3	R582, R585, R598	Resistor	0402	100 Ω	
42		2	R583, R584	Resistor	0402	240 Ω	
43		1	R586	Resistor	0402	4.12 kΩ	
44		3	R580, R587, R588	Resistor	0402	10 kΩ	
45		1	R559	Resistor	0603	261 Ω	
46		2	R590, R591	Resistor	0402	25 Ω	
47		1	R592	Resistor	0402	DNI	
48		2	R593, R596	Resistor	0402	0 Ω	
49		2	R594, R595	Resistor	0402	10 kΩ	
50		1	R597	Resistor	0402	4.3 kΩ	
51	1		RP500	Resistor	RCA74204	22 Ω	
52	2		RP501, RP502	Resistor	RCA74208	22 Ω	
53		1	S1	Switch		Momentary (normally open)	Panasonic EVQ-PLDA15
54	2		S500, S501	Connector	SMAEDGE	SMA edge right angle	
		2	S502, S503				
55		2	S504, S505	Connector	SMA200UP	SMA RF 5-pin upright	
56	2		T500, T501	Transformer	SM-22		M/A-Com ETC1-1-13
		1	T1				
57	1		T503	Transformer	CD542		Mini-Circuits ADT1-1WT
		1	T502				
58		1	U500	IC	32-pin LFCSP	Clock distribution	ADI AD9515BCPZ
59	1		U501	IC	SOT-223	Voltage regulator	ADI ADP3339AKCZ-5
60	1		U502	IC	SOT-223	Voltage regulator	ADI ADP3339AKCZ-1.8
61	1		U503	IC	SOT-223	Voltage regulator	ADI ADP3339AKCZ-2.5

Item	Qty.	Omit (DNP)	Reference Designator	Device	Package	Description	Supplier/Part Number
62	2		U504, U505	IC	SOT-223	Voltage regulator	ADI ADP3339AKCZ-3.3
63		1	U506	IC	8-pin SOIC	8-bit microcontroller	Microchip PIC12F629
64	1		U507	IC	SC70	Dual buffer	Fairchild NC7WZ16
65	1		U508	IC	SC70	Dual buffer	Fairchild NC7WZ07
66	1		U509	IC	48-pin TSSOP	Buffer/line driver	Fairchild 74VCX162244
67	1		U510	DUT (AD9246)	48-pin LFCSP	ADC	ADI AD9246BCPZ
68		1	U511 (or Z500)	IC	16-pin LFCSP	Differential amplifier	ADI AD8352ACPZ
Total	127	108					

OUTLINE DIMENSIONS

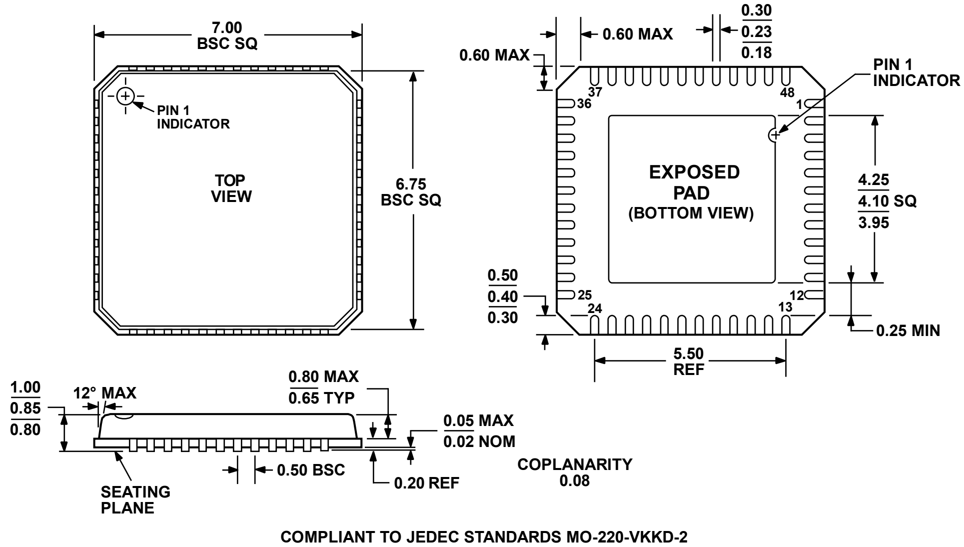

Figure 87. 48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
7 mm × 7 mm Body, Very Thin Quad (CP-48-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9246BCPZ-125[1, 2]	–40°C to +85°C	48-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-48-3
AD9246BCPZRL7–125[1, 2]	–40°C to +85°C	48-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-48-3
AD9246BCPZ-105[1, 2]	–40°C to +85°C	48-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-48-3
AD9246BCPZRL7–105[1, 2]	–40°C to +85°C	48-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-48-3
AD9246-125EB		Evaluation Board	
AD9246-105EB		Evaluation Board	

[1] Z = Pb-free part.
[2] It is required that the exposed paddle be soldered to the AGND plane to achieve the best electrical and thermal performance.

NOTES